VLBA Correlator Memo No. 64

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National Radio Astronomy Observatory

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To: VLBA Correlator Memo Series

From: John Benson, Ray Escoffier

Subject: On-line Computers for the FX Correlator

1.0 Summary

In this memo, we discuss the on-line computer requirements of the VLBA 'FX' Correlator. The computer hardware choices (and options) are presented, and the software tasks are listed. The computer configuration that accompanies the FX architecture is similar to that of the 'delay lagged' correlator that was the previous VLBA correlator design (VLBA Correlator Memo 41). The FX architecture relieves its attendant computers of some significant and costly tasks : 1) the post-correlation FFT's are not required, and 2) the model calculations are totally station dependant. No high speed baseline calculations are required (in particular, phase subtractions).

2.0 Computer Hardware Standards.

The VLBA project has adopted the following general computer hardware and software standards :

* 32-bit minis : DEC family of VAX computers, operating under VMS.

* 16/32-bit micros : Motorola MC68000 series processors, VMEbus systems, VERSAdos Real-Time Operating System.

The correlator will use both classes of processors in its on-line system. In addition, the correlator will require 8-bit microprocessors. We have not chosen the particular 8-bit processor yet.

The correlator software will be written in C and Fortran-77. We will use C for the control software and interface systems, and Fortran-77 for the algorithms that require heavy calculational power (correlator model, calibration and corrections, fringe fitting). The 8-bit micros may be programmed in assembly language.

3.0 The Correlator Computer Configuration.

The correlator computer configuration is shown in figure 1. There are three main components in the on-line system :

* the Correlator Control Computer sets up the correlator configuration and acts as an interface between the various elements of the system,

* the Station Model Processor controls and monitors the station electronics,

* the Backend Processor corrects, calibrates and archives the correlator output.

3.1 The Correlator Control Computer (CCC)

The CCC will be chosen from the DEC VAX family. It will probably be a VAX 8200,or less likely, a MicroVAX II. The CCC will be equipped with terminals having high resolution graphics and a DECnet connection into Array Operation Center VAX. We will require a disk drive and a low speed tape drive to support the operating system. A second, larger disk will be necessary to support the global fringe fitting of the clock calibrator sources. We may share additional peripherials with the AOC VAX. No array processors are required for the CCC. The CCC is not required to make time critical responses to external interrupts. These will occur in the SMP and Backend Processors.

The Correlator Control Computer is responsible for the following tasks :

* organizing the processing schedules. The CCC downloads observing logs from the VLBA database and organizes the correlator operational schedule. Processing scans are initialized, and model setup parameters are passed to the Station Model Processor (SMP). The correlator control program will create control files (text) that are accessible to direct examination and editting.

* communication with the correlator operators. The operator-correlator interface is supported on the CCC. The human operator will control the correlator by means of a control language with an optional menu driven screen display and an on-line help system. We will support the display of correlator monitor data thru graphics systems.

* communication with the Data Playback Systems (DPS). The CCC will communicate with the DPS's thru the DPS control interface. The CCC will be able to address all DPS's and individual DPS's with global and specific commands.

* communication with the VLBA database. The CCC must have ready access to the VLBA database system. The CCC will down-load information from the VLBA database that is necessary for setting up correlator configurations and schedules. The CCC will in turn upload processing logs into the VLBA database. The CCC will also use the VLBA database to generate the gain tables for the archive writer.

* supports correlator diagnostics. The CCC will support routine monitoring and display of the correlator performance during processing, and will allow the operator to query specific monitor points in the system, on-line.

* fringe fit clock calibrator source. The VLBA must routinely observe selected sources in order to measure time offsets and drifts in the station hydrogen maser frequency standards. The CCC will receive cal. source visibility data from the COP's (section 3.3.1). The data will have been averaged to 8 or fewer frequency channels, and to 10 second integrations. The AIPS global fringe fitting algorithm will run in the CCC (with no array processor). Timing tests have shown that fringe fitting 10 minutes of 14 station data takes about 10 minutes of real time on a VAX 11/780.

* create archive tables. Using data from the VLBA database, the CCC creates the archive tables that contain gain and calibration information, on-line flagging data and the interferometer model parameters.

3.2 The Station Model Processor (SMP)

The SMP will consist of a Motorola 68020 processor with a MC68881 floating point co-processor, DMA controller 68440, and two RS-232 serial I/O ports. The SMP will be a commerically availiable VMEmodule.

SMP tasks :

* calculation of the interferometric models. The SMP receives scan initializations from the CCC, and calculates the station based delays and four derivatives at 60 to 1200 second intervals. The model will calculate the wave front arrival time at the earth center, and at each antenna. An atmospheric model is included (probably a modified secant z). The model parameters will be transfered at 60 to 1200 second intervals to the lobe rotator phase generator, the delay buffer address generator and the fractional sample correction generator.

3.3 The Backend Processor

The correlator backend processors perform two basic logical operations : data correction and calibration, and creation of the archive database. In the earlier VLBA correlator design, these two operations were in separate hardware systems.

The proposed FX architecture relieves us of three computer intensive tasks that were required in the 'fringe processor' system that accompained the 'delay lagged' correlator (VLBA Correl. Memo 41) :

* station doppler shift tracking (now accomplished in the correlator lobe rotators),

* transforming delay lags to frequency channels (the FX output is already in the frequency domain),

* fractional-bit-shift corrections (this will be done in the FX hardware).

As yet, the backend computer hardware configuration has not been determined. The requirements that will drive our selection are :

* large I/O bandwidths (as great as 4 Mbytes/sec),

* networking and communication with the CCC and the VLBA database system,

* high speed archive writing (4 Mbytes/sec max).

The chief difficulty in specifying the backend processor hardware is that sometimes it will require an uncomfortably very high I/O capacity. We expect the data rates through the backend processor to break down in approximately this fashion :

3.9 Mbyte/sec,	2 %	of VLBA scheduled observing time
1.6 Mbyte/sec,	8 %	"
0.8 Mbyte/sec,	10 %	"
0.4 Mbyte/sec,	80 %	"

We are considering two different solutions to the hardware dilemma : 1. We may run a number of moderate speed processors in parallel (the COPs, section 3.3.1). These processors would be Motorola 68020 VME-bus systems. We will require at least four such systems to handle the data corrections and calibration. The four parallel processors would be followed a single processor that writes the archive data set. 2. The raw correlator output may be written directly onto large, fast disks. A single, slower conventional computer will read the disk data, correct and calibrate the visibilities, and write the archive data set. During 10 % of the array observing time, the correlator-backend processor data rates will exceed 1.6 Mbyte/sec, and the slower backend processor will not be able to keep up with the correlator dump rate. The correlator would operate until the buffer disks are filled (about 45 minutes for a 10 Gbyte capacity disk at 4 Mbytes/sec). The disks would then drained through the backend machine at about 500 kbytes/sec, one eighth of the maximum correlator ouput rate. The correlator would not need to sit idle while the disk data are being processed, however. Smaller experiments could be correlated and buffered, and later archived as the correlator schedule permits.

3.3.1 The Correlator Output Processers (COP)

The hardware accumulators will be dumped into the Correlator Output Processor memory via DMA transfer. The COP(s) may be four MC68020 processors with floating point co-processors, DMA controllers, and low speed ports connecting to the CCC Unibus.

The COP tasks are :

* to retrieve the auto- and cross-correlation data from the hardware accumulators,

* create 4 byte floating point words,

* normalize the cross-correlation data by using the zero lag autocorrelation channels, apply two-level and four-level quantization corrections,

* apply various frequency channel averaging options,

* pass clock calibrator source visibility data into the CCC for global fringe fitting,

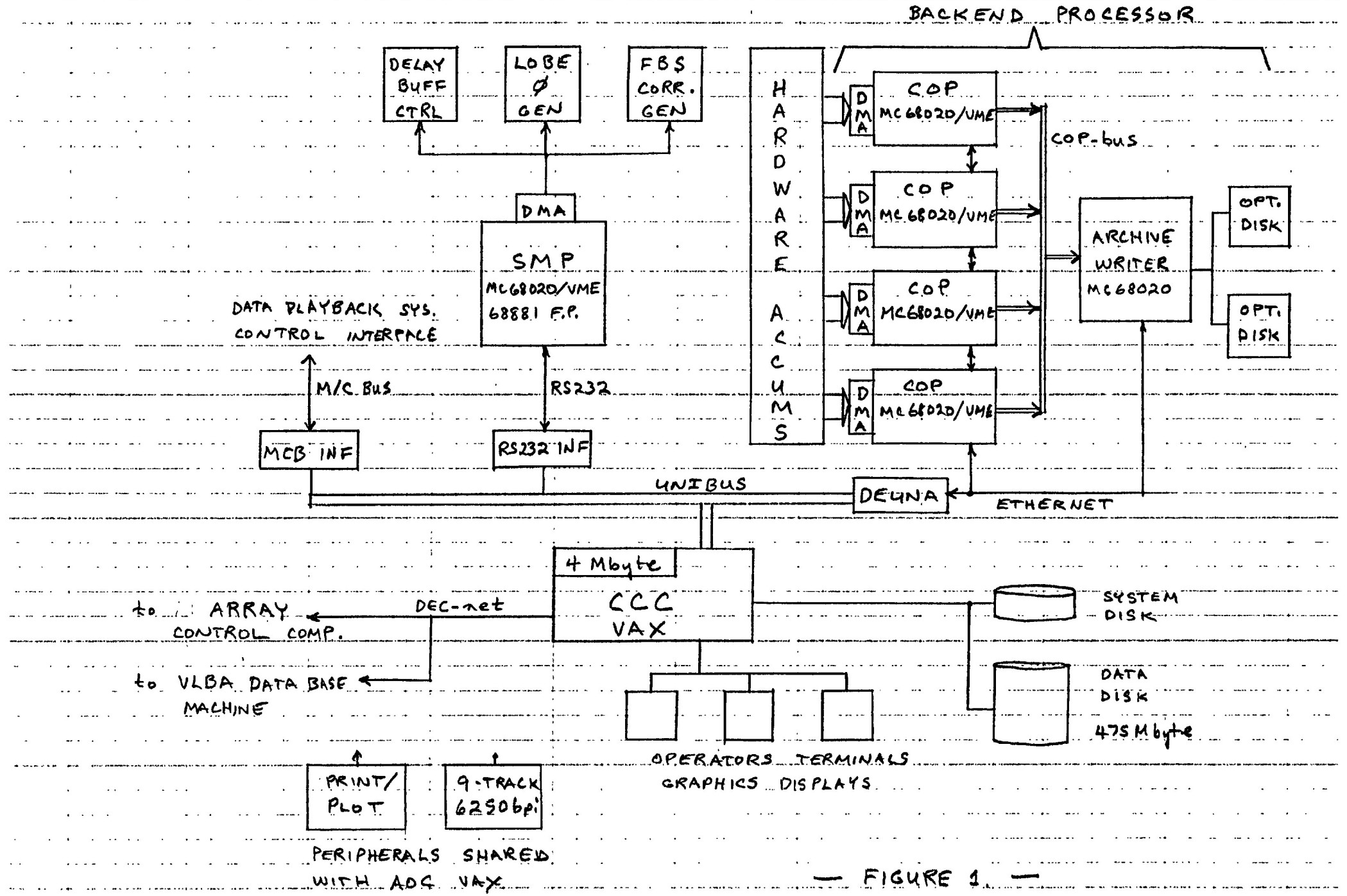
* pass the visibility and autocorrelation data into the archive writer.

3.3.2 The Archive Writer

The archived data will be written on an as yet unspecified media. Currently, the contending choices are : conventional 6250 bpi 9 track tapes, optical disks, or one of the emerging technology high density tape systems. The archive media must be a safe long term storage media (at least 10 years) and allow error recovery encoding.

The optical disks present certain advantages. They hold 2 Gbytes per disk as opposed to < 0.18 Gbytes per 9 track tape. If the optical disks may be used in a random access mode, VLBA observations that are being correlated simultaneously can be archived directly into separate disk files. A random access archive writer will also allow the FITS formatted calibration tables to be written after an observation is completely processed.

The logical contents of the archive database is listed in Appendix B, VLBA Correlator Memo 41. The archive data format will follow the uv-FITs format of the distribution tape as closely as possible.


BACKEND PROCESSOR
DELAY BUFF CTRL
LOBE Ø GEN
FBS CORR. GEN
HARDWARE ACCUMS
DMA
COP MC68020/VME
COP-bus
ARCHIVE WRITER MC68020
OPT. DISK
OPT. DISK
DMA
SMP MC68020/VME 68881 F.P.
DATA PLAYBACK SYS. CONTROL INTERFACE
M/C Bus
RS232
MCB INF
RS232 INF
UNIBUS
DELUNA
ETHERNET
4 Mbyte
CCC VAX
DEC-net
to ARRAY CONTROL COMP.
to VLBA DATA BASE MACHINE
SYSTEM DISK
DATA DISK
475 Mbyte
OPERATORS TERMINALS
GRAPHICS DISPLAYS
PRINT/ PLOT
9-TRACK 6250bpi
PERIPHERALS SHARED WITH ADC VAX

— FIGURE 1 —