VLBA Correlator Memo No. 86

VLBA Correlator Cost Estimate

by Ray Escoffier

June 15, 1987

I) Introduction

This memo gives a preliminary cost estimate for the VLBA FX correlator. The cost estimate presented is based on an estimated chip count of the custom designed hardware and our best estimates of the off-the-shelf items we plan to use. The correlator is in the early stages of design at this time and we think that a simple estimated chip count multiplied by an average chip overhead cost is a reasonably accurate method of cost estimation. A gross cost of $15 per chip was assumed for an average integrated circuit which should account for the chip purchase price, the mounting, wiring, power, cooling, expenses like NRE costs of PC card layout, breadboards, etc. As a justification for this approach, we can cite the VLA correlator experience in which the total VLA correlator charge accounts expenditures ($915,000) divided by the final VLA correlator chip count (85,000 IC's) gives $10.76 as the average chip overhead. A $15 figure is used here in consideration of inflation, the higher integration level of the VLBA correlator, and the desire to get a pessimistic figure to offset the probable underestimation of the chip count made due to the early stage of the design.

Two appendices are included in the memo. Appendix I presents a series of drawings and brief explanations that are the basis of the hardware chip count used in the estimate. Appendix II presents a comparison lag correlator design and associated cost estimate. This lag correlator design and cost estimate were presented at the February FX correlator workshop held in Charlottesville this year and this seems to be a good opportunity to get it into the written VLBA record. A few minor changes have been made to bring this design up to date.

Information in this memo on both the FX correlator design and attendant cost estimate differ from the design and cost estimate given at the Feb. FX workshop in so much as our thinking concerning the design has changed. The biggest change in the FX design since the Feb. FX workshop is our intention to use a gate array with on-board RAM storage for both the FFT butterfly and cross-multiply functions. This change results in a higher gate array cost but a lower system chip count.

One item in the cost estimate needs pointing out at this point. The proposed gate array integrated circuits are counted twice in the cost estimate. They appear in the hardware chip count and enter the cost total at $15 per chip. They appear separately in the final cost estimate at their estimated purchase cost of $67 per chip plus NRE charge. Double counting these high purchase price chips was done since $15 is a reasonable (pessimistic) chip overhead for these large chips over and above the purchase price.

II) Cost Estimate

Hardware Chip Count:

Delay System	3,600
FFT System	3,360
Cross multiplier System	8,560
Miscellaneous (1)	5,000
	21,000

Computer System:

VME system (2)	$ 55,000
Micro-VAX system (3)	100,000
Archive tape units (4)	20,000
Distribution tape units (5)	42,000
	$217,000

Cost Estimate:

Hardware ($15/IC)	$315,000
Gate array NRE (6)	95,000
Gate array chips (6)	200,000
Computer system	217,000
Test Equipment (7)	50,000
	$877,000

(1) Control logic, FFT control, delay model generator, fringe model generator, pulsar gate generator, accumulator/ALU, and filter.

(2) based on 2 VME backplanes, 4 20 Mhz CPU cards, development system, and associated hardware and software.

(3) based on Micro-Vax II system plus associated hardware and software.

(4) based on 4 Exabyte EXB-8200 8MM recorders plus Winchester disc buffer.

(5) based on two STC model 1968/1963 tape units (if streaming tape recorders are deemed acceptable for the distribution tape application, two Cipher model 990 GCR tape units could be substituted here for a cost saving of about $25,000).

(6) based on a quote from LSI Logic Corp. for their LSA-1502 gate array.

(7) PAL/PROM programmer, PAL assembler, oscilloscope, logic analyzer.

Appendix I

This appendix presents a brief review of the FX correlator design and the use of this design in obtaining the cost estimate above. Circuit descriptions will not be given in fine detail but with sufficient information to allow review of the cost estimate procedure. Later memos will cover the proposed system design and performance in much greater detail.

Figure 1 gives the block diagram of the VLBA FX correlator. Up to 160 channels drive the correlator input from the DPS system (up to 8 channels each from up to 20 antennas). Each channel is provided with a programmable delay line, fringe rotated, windowed, and Fourier transformed in the station electronics. At the FFT output, a fractional sample time error correction (FSTC) is applied and the resulting station electronics outputs drive the cross-multiplier/accumulator arrays. The cross-multiplier/ accumulator arrays produce and integrate the cross- and auto-spectra. Long term accumulation and normalization is done in the accumulator/ALU.

The correlator computer system includes the back-end CPU which writes archive tapes, the calibrator fringe processor that does occasional fringe searches and model checking, the distribution tape translator which writes a distribution tape from the archive tape, the system controller and the Correlator Control Computer. Four VME 20-Mhz processors are planned for the correlator computer in addition to a Micro-Vax for the CCC.

Figure 2 gives a sketch of the station delay system. A delay range of about 2 msec (for a 32 Mhz sample rate) is provided to each output of the DPS. One 16K x 4 static RAM each for the sign, magnitude and validity bits provides this delay. Data input into a RAM requires serial to parallel conversion while parallel to serial conversion is required at the RAM output to accommodate the 4-bit wide RAM I/O structure. These conversion stages are shown as implemented in PALs in Figure 2. A system wide address bus is used for writing data into the RAM's and a RAM address from a delay model generator produces the RAM read addresses. The stay time in the RAM's establishes the delay.

Figures 3, 4, and 5 give an outline of the FFT card. This card will do the fringe rotation, windowing, Fourier transformation, the fractional sample error correction, and provides drive into the cross-multipliers. Figure 3 shows the whole card in block form. Four FFT chains per card are now planned with no intermediate RAM storage between butterfly chips (the required RAM storage being on board the butterfly chips themselves). The first and last butterfly chips require an external RAM address bus, the first to do the point scramble and the last to get the proper sequence of points into the cross-multipliers. Intermediate FFT butterfly stages use address generators on board the gate array chips. Figure 4 shows in more detail the station based fringe rotator. An 8-bit bit slice of a number controlled oscillator (NCO) will be included on board each butterfly chip and by connecting 5 such bit slices together a 40-bit NCO is created that can be used as a two coefficient Taylor series implementation of a station fringe tracker. A 40-bit fringe phase exists in the top register of this NCO and a 40-bit fringe rate in the register below the adder stage. The fringe rate coefficient is added to the fringe phase at the 32-Mhz clock rate. This fringe tracker is capable of tracking the station fringe phase

to the required accuracy for about 4.0-msec. Two additional secondary storage registers are provided in the gate array that will be loaded with updated phases and rates from the fringe model generator. After a set interval, the new coefficients are clocked into the active registers and a new tracking cycle starts. The actual fringe rotation is done in look-up table ROM's. These ROMs have pre-calculated multiplication tables of all four possible sample values multiplied by all possible 256 8-bit fringe phasors.

Figure 5 shows the fractional sample error correction in more detail. This circuit uses the bit slice NCO's in the gate array chips to produce a phase ramp from a fractional sample error coefficient. Again look-up table ROM's do the actual work. The twiddle factors going to the final FFT butterfly stage are rotated by the NCO generated phases effectively rotating the final spectral point by the desired value (see VLBA correlator memo 72).

Figure 6 shows the currently planned design for the cross-multiplier card. The RAM storage available on the gate array chip is used as the short term accumulator memory. The complex multiplier required by the FFT butterfly function is used as the cross-multiplier and the accumulation function uses a butterfly adder stage doing floating point additions. The short term accumulation is performed in complex floating point arithmetic with 15-bit real and imaginary mantissa fields with a common 6-bit exponent (15, 15, 6). The onboard RAM in the gate array chip is large enough to allow secondary storage of integrated results for readout into the long term integrator.

In all cases IC count estimates are made for each card and these figures were used in the overall cost estimate.

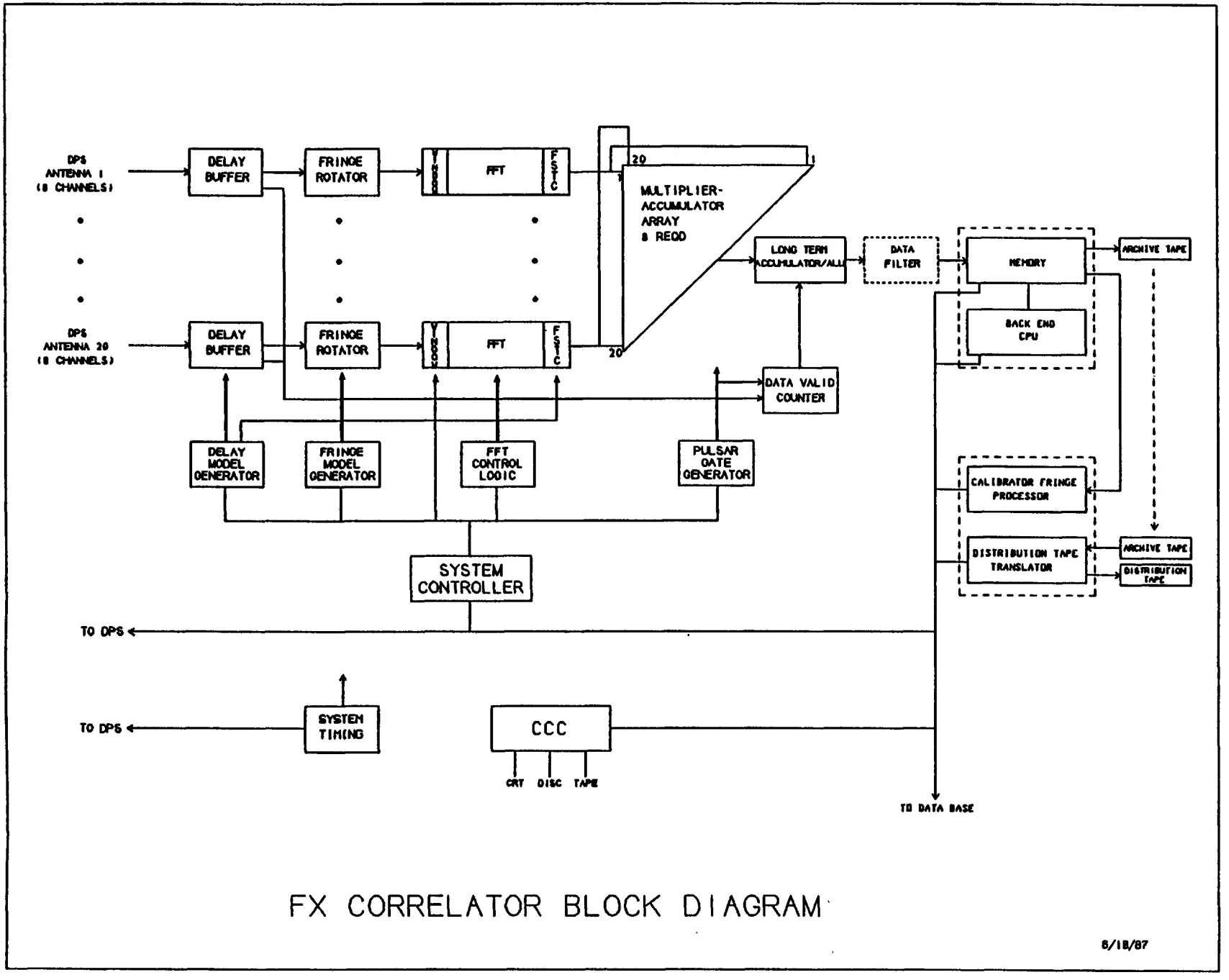

DPS ANTENNA 1 (8 CHANNELS)
DELAY BUFFER
FRINGE ROTATOR
FFT
20
1
MULTIPLIER-ACCUMULATOR ARRAY 8 REQD
DPS ANTENNA 20 (8 CHANNELS)
DELAY BUFFER
FRINGE ROTATOR
FFT
20
1
LONG TERM ACCUMULATOR/ALL
DATA FILTER
MEMORY
ARCHIVE TAPE
BACK END CPU
DATA VALID COUNTER
DELAY MODEL GENERATOR
FRINGE MODEL GENERATOR
FFT CONTROL LOGIC
PULSAR GATE GENERATOR
CALIBRATOR FRINGE PROCESSOR
DISTRIBUTION TAPE TRANSLATOR
ARCHIVE TAPE
DISTRIBUTION TAPE
SYSTEM CONTROLLER
TO DPS
TO DPS
SYSTEM TIMING
CCC
CRT
DISC
TAPE
TO DATA BASE
FX CORRELATOR BLOCK DIAGRAM
8/18/87

FIGURE 1

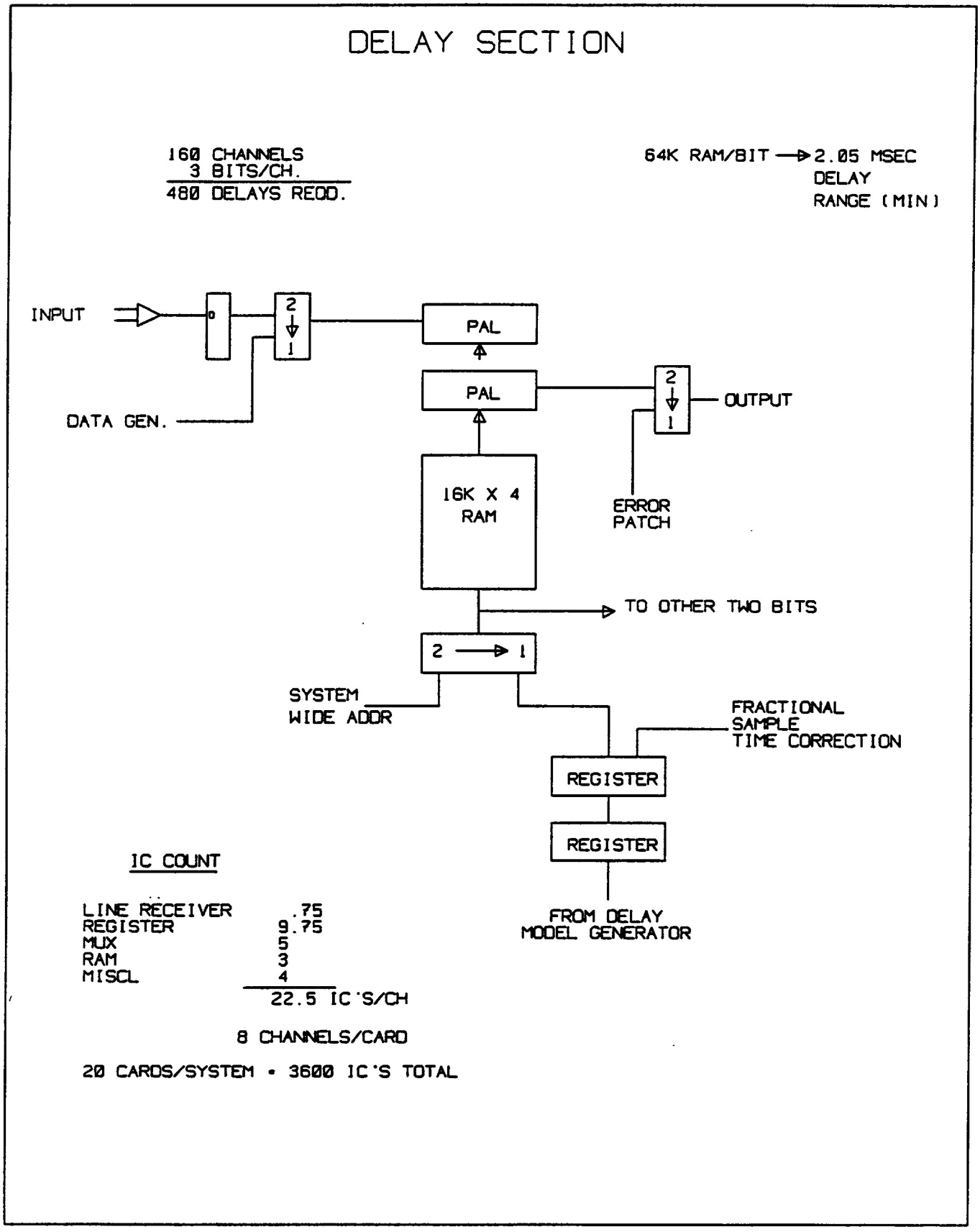

DELAY SECTION
160 CHANNELS
3 BITS/CH.
480 DELAYS REQD.
64K RAM/BIT → 2.05 MSEC
DELAY
RANGE (MIN)
INPUT
2
1
PAL
PAL
2
1
OUTPUT
DATA GEN.
16K X 4
RAM
ERROR
PATCH
TO OTHER TWO BITS
2 → 1
SYSTEM
WIDE ADDR
FRACTIONAL
SAMPLE
TIME CORRECTION
REGISTER
REGISTER
FROM DELAY
MODEL GENERATOR
IC COUNT
LINE RECEIVER .75
REGISTER 9.75
MUX 5
RAM 3
MISCL 4
22.5 IC'S/CH
8 CHANNELS/CARD
20 CARDS/SYSTEM • 3600 IC'S TOTAL

FIGURE 2

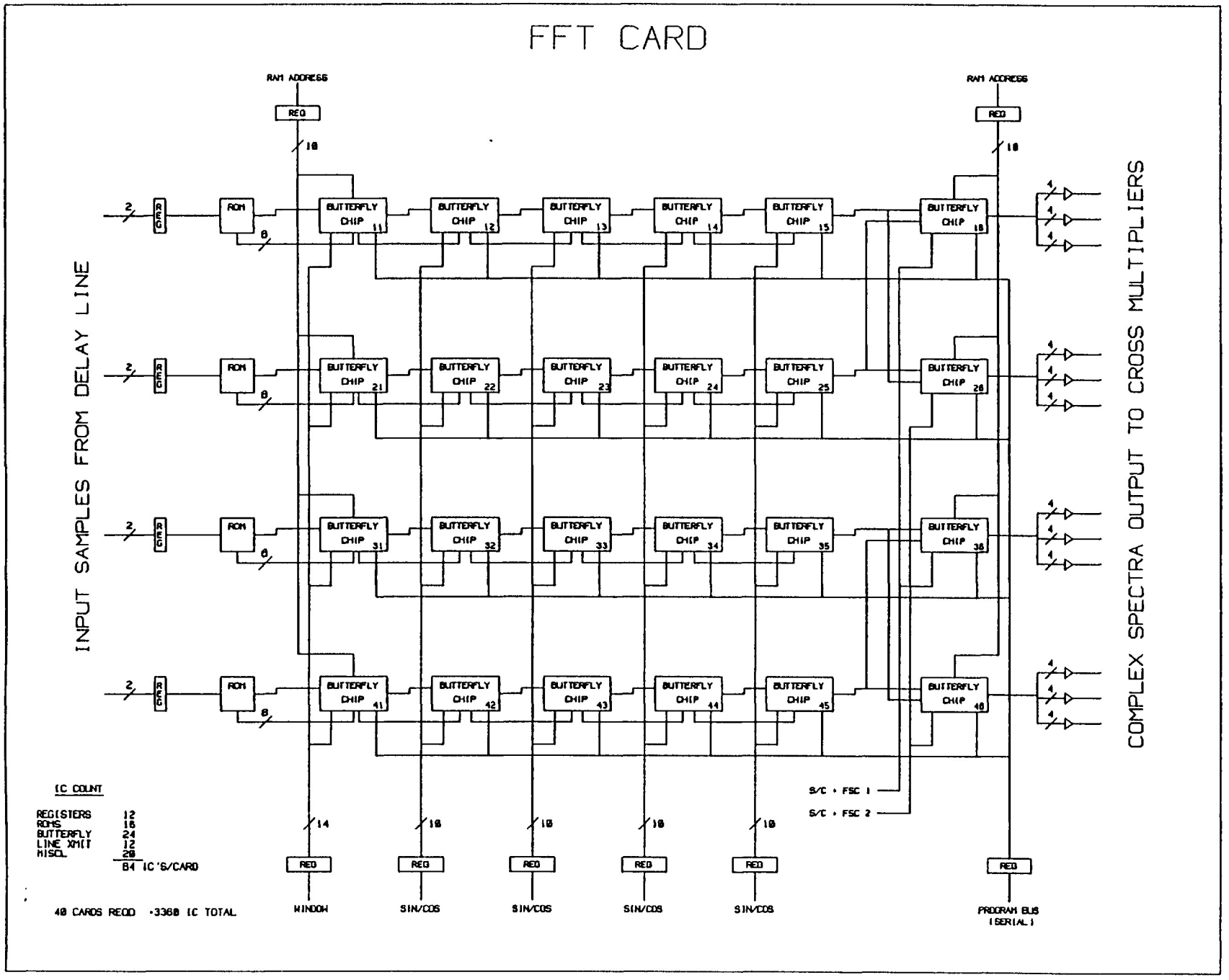

FFT CARD
RAM ADDRESS
REG
18
INPUT SAMPLES FROM DELAY LINE
2
ROM
8
BUTTERFLY CHIP 11
BUTTERFLY CHIP 12
BUTTERFLY CHIP 13
BUTTERFLY CHIP 14
BUTTERFLY CHIP 15
BUTTERFLY CHIP 16
BUTTERFLY CHIP 21
BUTTERFLY CHIP 22
BUTTERFLY CHIP 23
BUTTERFLY CHIP 24
BUTTERFLY CHIP 25
BUTTERFLY CHIP 26
BUTTERFLY CHIP 31
BUTTERFLY CHIP 32
BUTTERFLY CHIP 33
BUTTERFLY CHIP 34
BUTTERFLY CHIP 35
BUTTERFLY CHIP 36
BUTTERFLY CHIP 41
BUTTERFLY CHIP 42
BUTTERFLY CHIP 43
BUTTERFLY CHIP 44
BUTTERFLY CHIP 45
BUTTERFLY CHIP 46
4
COMPLEX SPECTRA OUTPUT TO CROSS MULTIPLIERS
S/C + FSC 1
S/C + FSC 2
IC COUNT
REGISTERS 12
ROMS 16
BUTTERFLY 24
LINE XMIT 12
MISCL 20
84 IC'S/CARD
40 CARDS REQD •3360 IC TOTAL
14
16
WINDOW
SIN/COS
PROGRAM BUS (SERIAL)

FIGURE 3

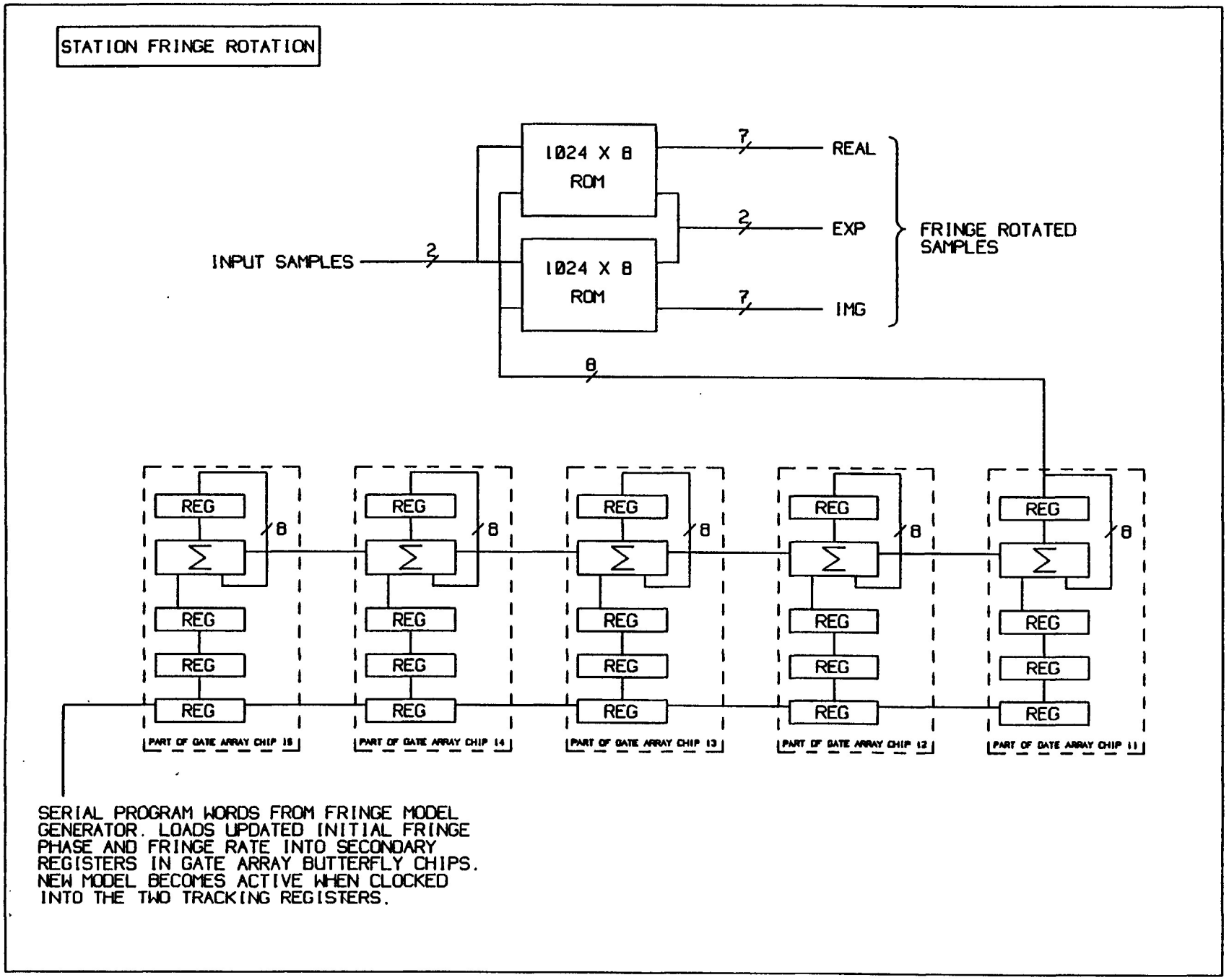

STATION FRINGE ROTATION
1024 X 8 ROM
1024 X 8 ROM
INPUT SAMPLES
2
7
REAL
2
EXP
7
IMG
FRINGE ROTATED SAMPLES
8
REG
Σ
8
PART OF GATE ARRAY CHIP 15
PART OF GATE ARRAY CHIP 14
PART OF GATE ARRAY CHIP 13
PART OF GATE ARRAY CHIP 12
PART OF GATE ARRAY CHIP 11
SERIAL PROGRAM WORDS FROM FRINGE MODEL GENERATOR. LOADS UPDATED INITIAL FRINGE PHASE AND FRINGE RATE INTO SECONDARY REGISTERS IN GATE ARRAY BUTTERFLY CHIPS. NEW MODEL BECOMES ACTIVE WHEN CLOCKED INTO THE TWO TRACKING REGISTERS.

FIGURE 4

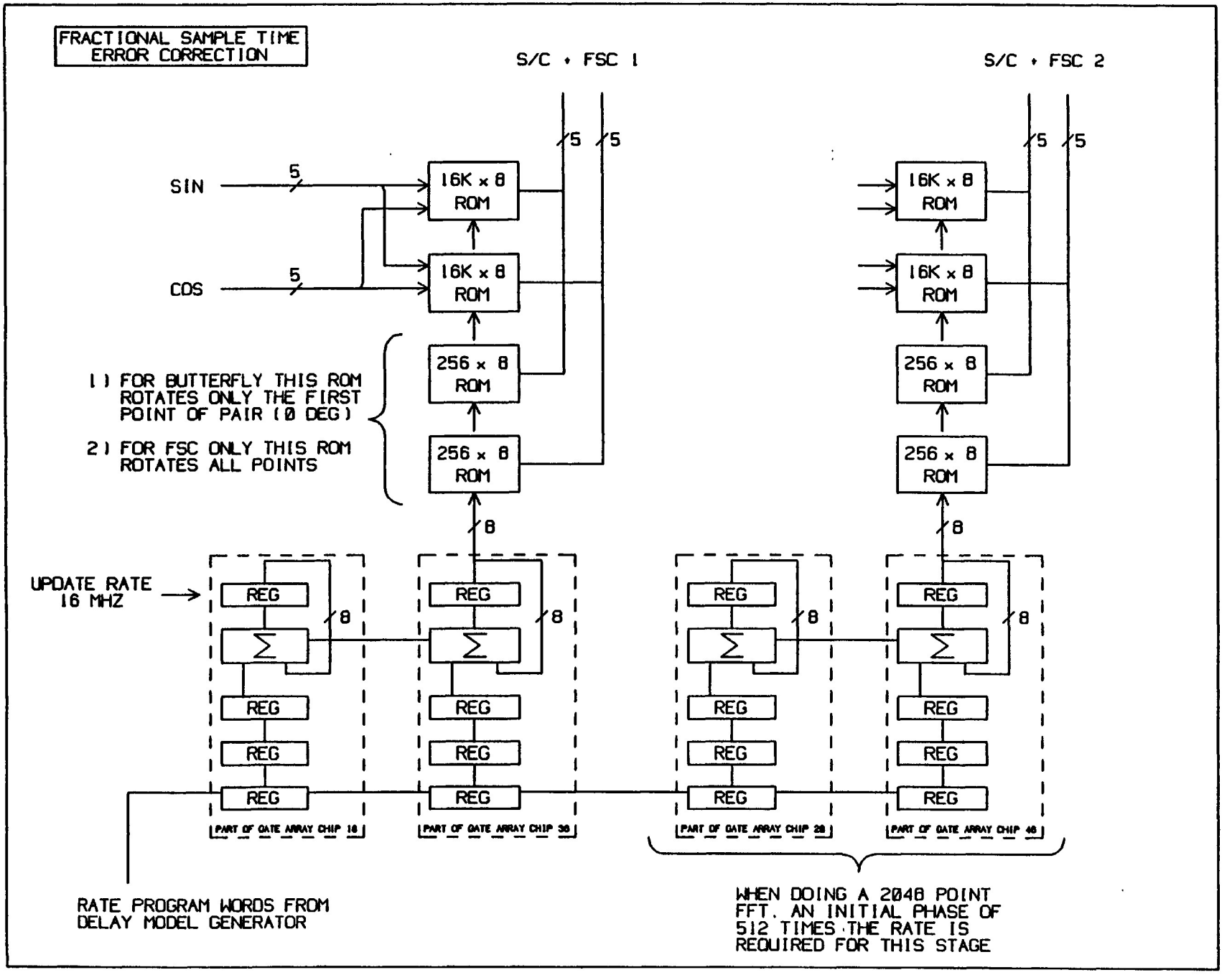

FRACTIONAL SAMPLE TIME ERROR CORRECTION
S/C + FSC 1
S/C + FSC 2
SIN
COS
5
16K x 8 ROM
256 x 8 ROM
1) FOR BUTTERFLY THIS ROM ROTATES ONLY THE FIRST POINT OF PAIR (0 DEG)
2) FOR FSC ONLY THIS ROM ROTATES ALL POINTS
8
UPDATE RATE 16 MHZ
REG
Σ
PART OF GATE ARRAY CHIP 1B
PART OF GATE ARRAY CHIP 3B
PART OF GATE ARRAY CHIP 2B
PART OF GATE ARRAY CHIP 4B
RATE PROGRAM WORDS FROM DELAY MODEL GENERATOR
WHEN DOING A 2048 POINT FFT, AN INITIAL PHASE OF 512 TIMES THE RATE IS REQUIRED FOR THIS STAGE

FIGURE 5

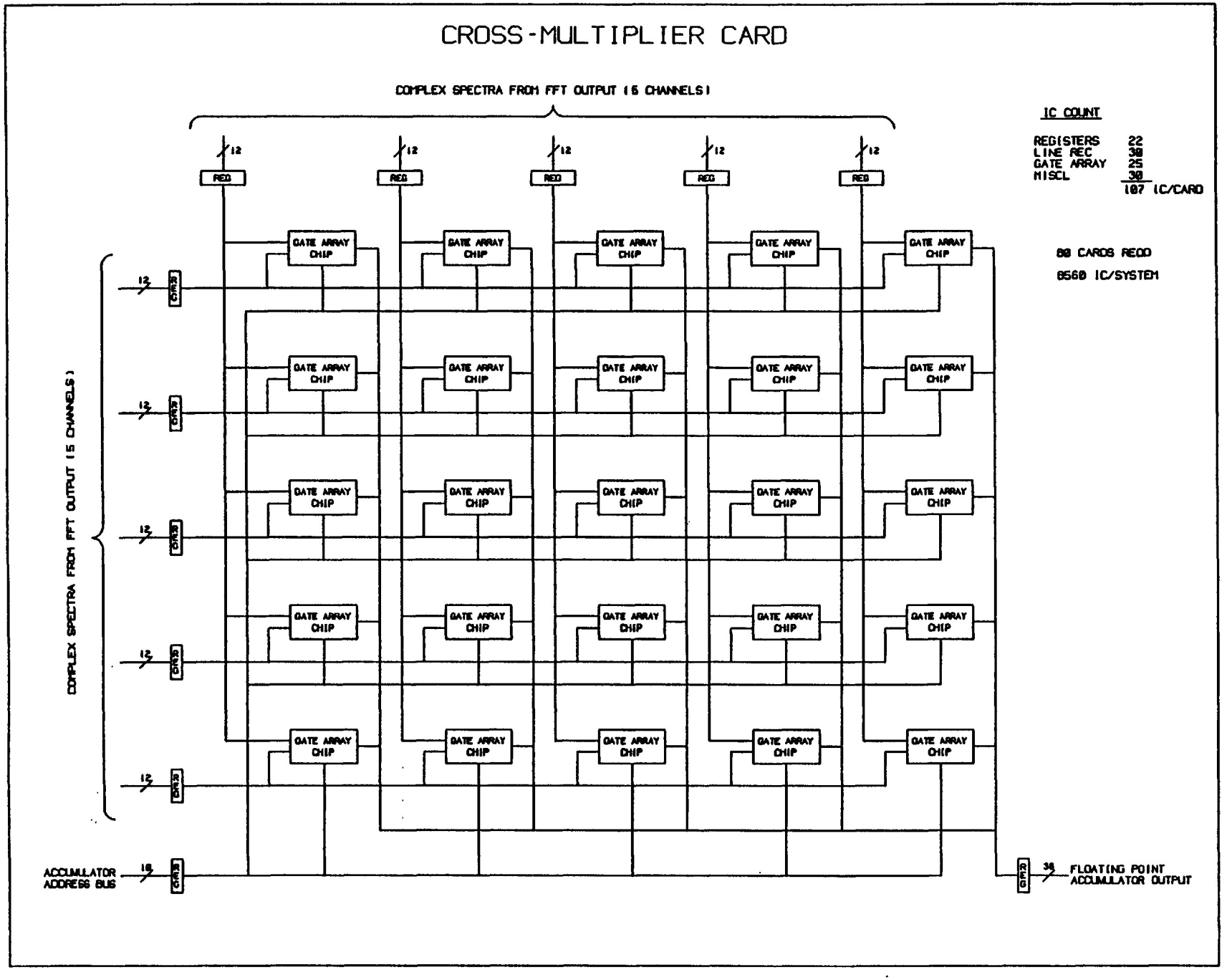

CROSS-MULTIPLIER CARD
COMPLEX SPECTRA FROM FFT OUTPUT (5 CHANNELS)
IC COUNT
REGISTERS 22
LINE REC 30
GATE ARRAY 25
MISCL 30
107 IC/CARD
60 CARDS REQD
8560 IC/SYSTEM
REG
GATE ARRAY CHIP
COMPLEX SPECTRA FROM FFT OUTPUT (5 CHANNELS)
ACCUMULATOR ADDRESS BUS
FLOATING POINT ACCUMULATOR OUTPUT

FIGURE 6

Appendix II

This appendix will describe a VLBA correlator using a lag design. This design was made for comparison with the FX concept while NRAO was studying the best way to make the VLBA correlator since it was felt that the CalTech work in defining a lag correlator for the VLBA needed updating to take advantage of advances in technology since that effort ended. The design was based on a gate array chip developed by A. Bos of the Netherlands Foundation for Radio Astronomy (NFRA). This chip contains a 16-lag correlator with short term integrators and seems a good way to make the VLBI correlator, being similar to the chip proposed by CalTech in their VLBA correlator study and described in VLBA memo 41, "Architectural Design for the VLBA Correlator", of April 1985. Both a brief block diagram description of this design and a cost estimate are given for this design in this appendix.

Figure 7 gives a block diagram of the lag correlator design. Much of this design is similar to that given for the FX correlator. The two main differences from the FX block diagram are the cross-multiplier array and the driver stage.

Figure 8 describes the delay section and is identical to Figure 2, the FX correlator delay system.

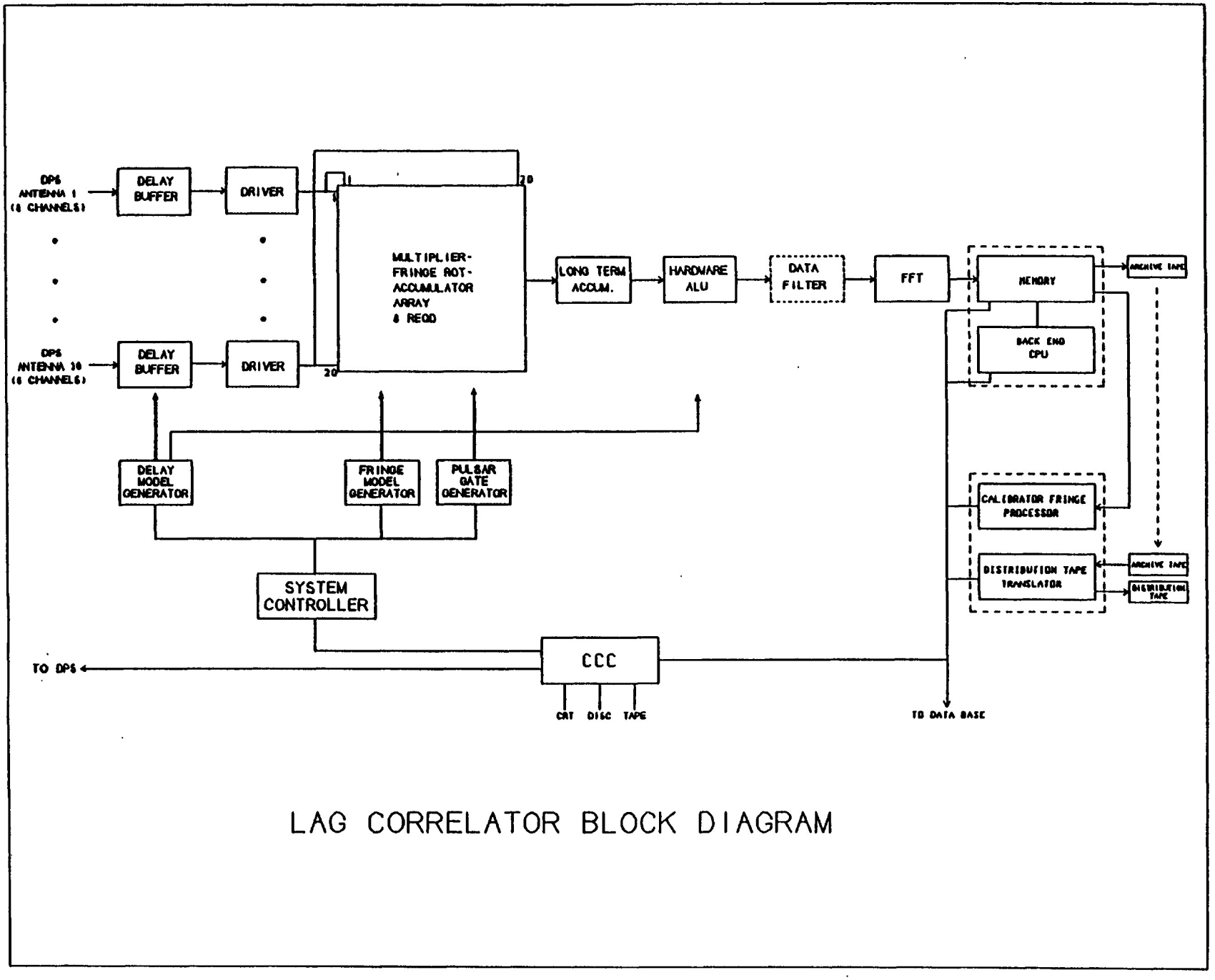
The driver system is shown in Figure 9 in block diagram form which illustrates the multiplexers used to do the switching required to support all of the operating modes required of the correlator. The driver contains logic to drive the multiplexed data signal into the cross-multipliers.

Figures 10, 11 and 12 detail the cross-multiplier and the use of the NFRA gate array chip. Figure 10 shows a possible configuration of a cross-multiplier array of 10-antennas by 10-antennas, made up of four PC cards each of which are implemented using a 5 by 5 NFRA chip array. The 5 by 5 card would have 25 NFRA chips and baseline fringe rotators as depicted at the bottom of Figure 10. Figure 11 shows in more detail the NFRA chip and a proposed fringe rotator gate array chip which would do the baseline fringe phase generation economically. Figure 12 gives the complete cross-multiplier structure and how this structure is rearranged to accommodate the 10 station, 15 station, or 20 station operation modes. In brief, Figure 12 shows how to rearrange the 5 antenna by 5 antenna PC cards of Figure 10 (one square in any of the three configurations of Figure 12) to optimize the system for the number of active antennas. In each case, the cross-multipliers required for one of the eight channels is shown.

Figure 13 illustrates the long term integrator for this lag correlator design. This figure is equally applicable to the FX correlator.

In the lag correlator after accumulation the Fourier transform must be done and Figure 14 shows the FFT requirements.

A cost estimate was made for this lag design and is presented below. The basis for this cost estimate is the same as for the FX design, i.e., doing a careful chip count estimate and assuming an average per chip overhead cost of $15.



LAG CORRELATOR BLOCK DIAGRAM

FIGURE 7

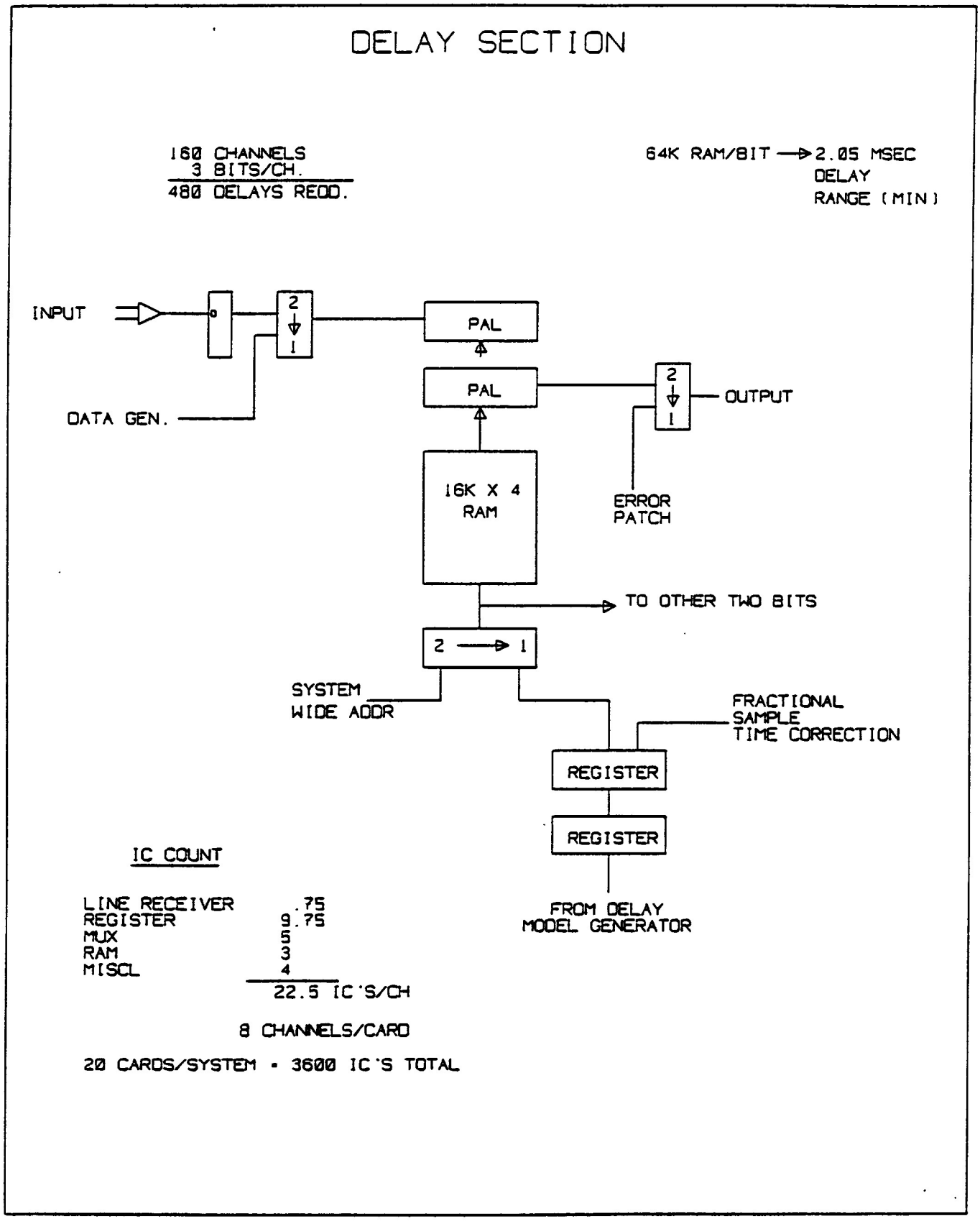

DELAY SECTION
160 CHANNELS
3 BITS/CH.
480 DELAYS REQD.
64K RAM/BIT → 2.05 MSEC
DELAY
RANGE (MIN)
INPUT
2
1
PAL
PAL
2
1
OUTPUT
DATA GEN.
16K X 4
RAM
ERROR
PATCH
TO OTHER TWO BITS
2 → 1
SYSTEM
WIDE ADDR
FRACTIONAL
SAMPLE
TIME CORRECTION
REGISTER
REGISTER
FROM DELAY
MODEL GENERATOR
IC COUNT
LINE RECEIVER .75
REGISTER 9.75
MUX 5
RAM 3
MISCL 4
22.5 IC'S/CH
8 CHANNELS/CARD
20 CARDS/SYSTEM = 3600 IC'S TOTAL

FIGURE 8

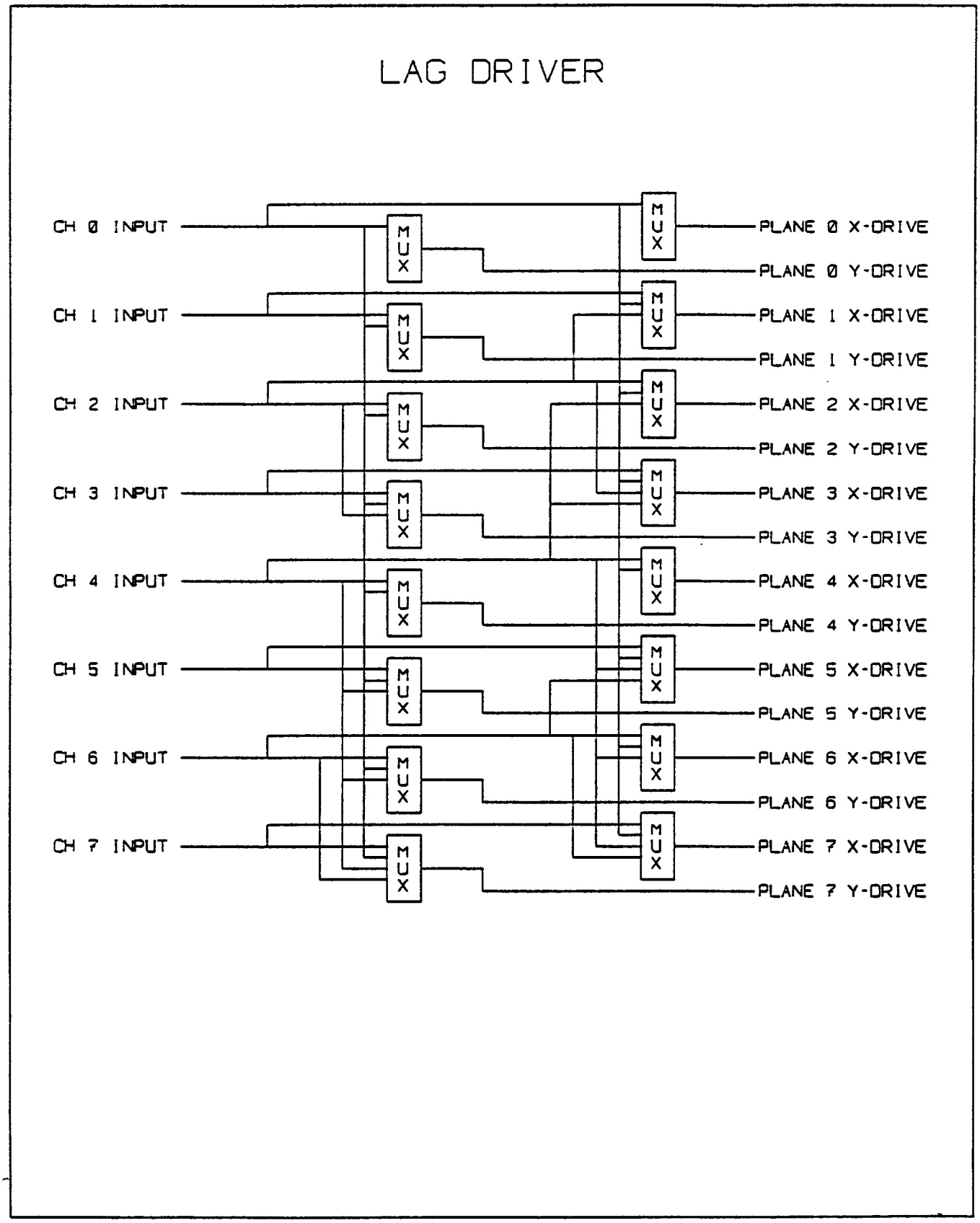
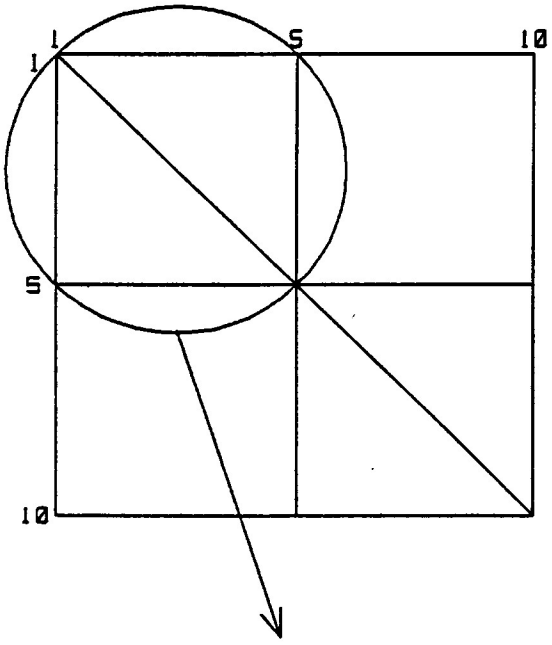

LAG DRIVER
CH 0 INPUT
CH 1 INPUT
CH 2 INPUT
CH 3 INPUT
CH 4 INPUT
CH 5 INPUT
CH 6 INPUT
CH 7 INPUT
MUX
PLANE 0 X-DRIVE
PLANE 0 Y-DRIVE
PLANE 1 X-DRIVE
PLANE 1 Y-DRIVE
PLANE 2 X-DRIVE
PLANE 2 Y-DRIVE
PLANE 3 X-DRIVE
PLANE 3 Y-DRIVE
PLANE 4 X-DRIVE
PLANE 4 Y-DRIVE
PLANE 5 X-DRIVE
PLANE 5 Y-DRIVE
PLANE 6 X-DRIVE
PLANE 6 Y-DRIVE
PLANE 7 X-DRIVE
PLANE 7 Y-DRIVE

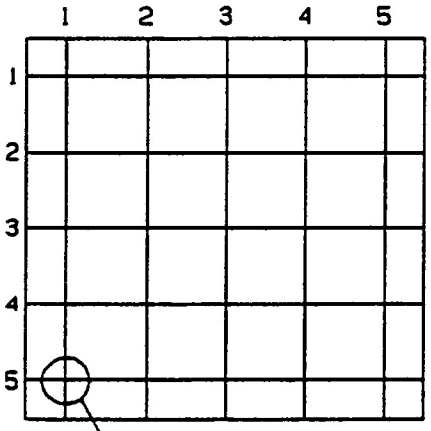
FIGURE 9

CROSS MULTIPLIER ARRAY FOR LAG CORRELATOR

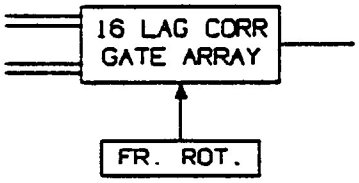


ARRAY OF CROSS MULTIPLIERS

16 REAL LAGS. 16 REAL LEADS. AND 16 AUTO CORRELATOR LAGS FOR 10 ANTENNA ARRAY.



CROSS MULTIPLIER CARD



GATE ARRAY MULTIPLIER CHIP AND FRINGE ROT. CHIP

FIGURE 10

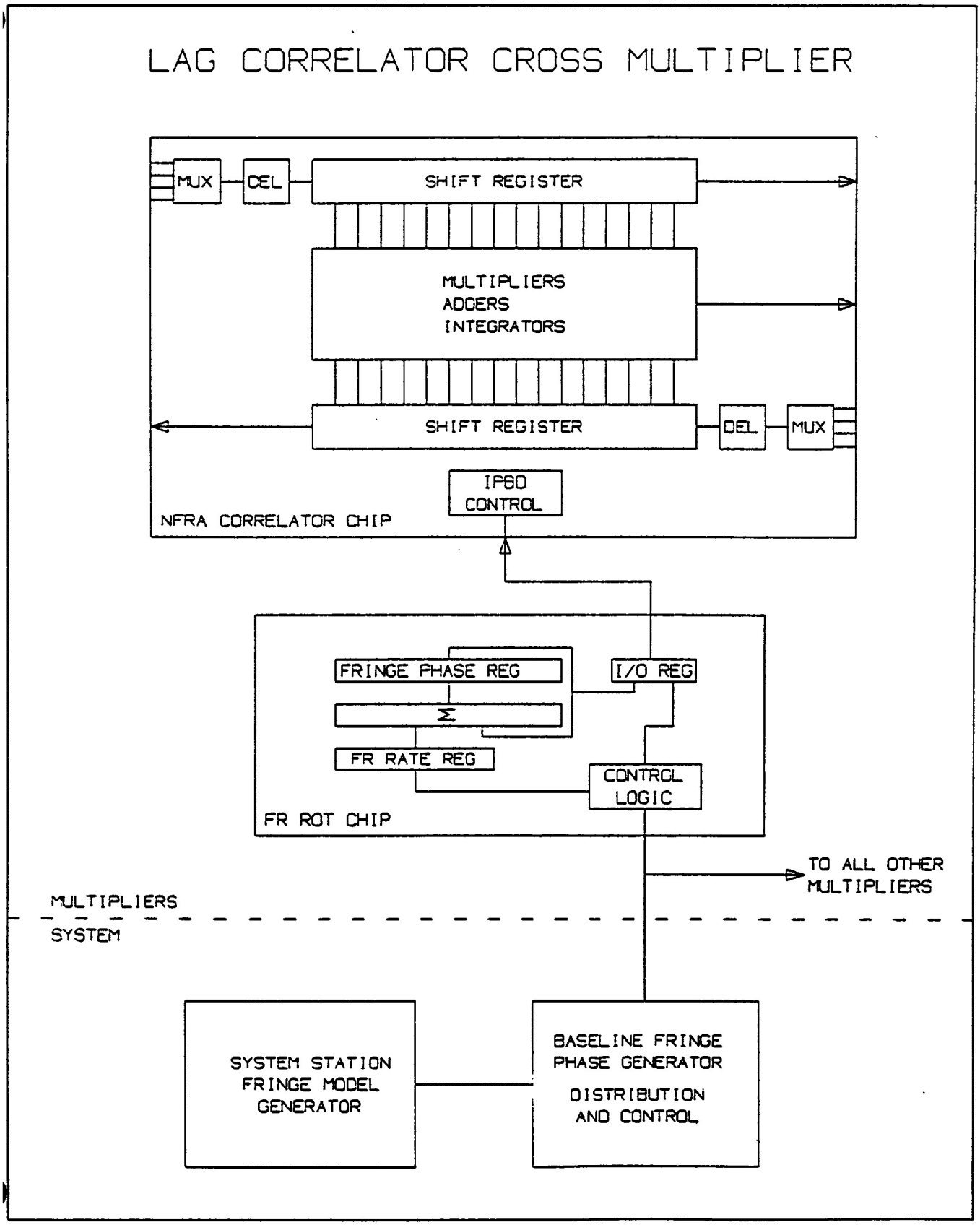

LAG CORRELATOR CROSS MULTIPLIER
MUX
DEL
SHIFT REGISTER
MULTIPLIERS
ADDERS
INTEGRATORS
SHIFT REGISTER
DEL
MUX
IPBD
CONTROL
NFRA CORRELATOR CHIP
FRINGE PHASE REG
I/O REG
Σ
FR RATE REG
CONTROL
LOGIC
FR ROT CHIP
TO ALL OTHER
MULTIPLIERS
MULTIPLIERS
SYSTEM
SYSTEM STATION
FRINGE MODEL
GENERATOR
BASELINE FRINGE
PHASE GENERATOR
DISTRIBUTION
AND CONTROL

FIGURE 11

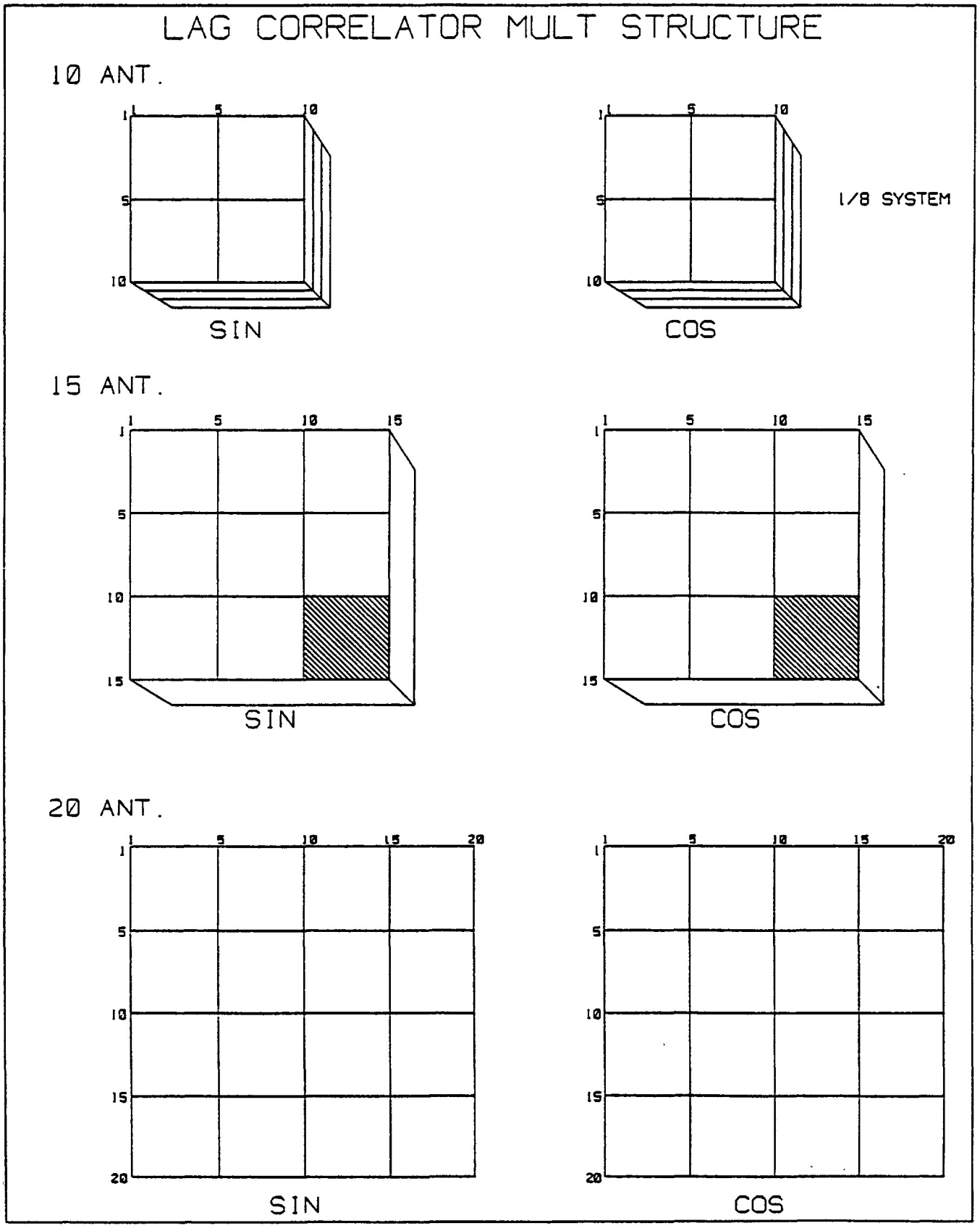

LAG CORRELATOR MULT STRUCTURE
10 ANT.
1
5
10
SIN
COS
1/8 SYSTEM
15 ANT.
15
SIN
COS
20 ANT.
20
SIN
COS

FIGURE 12

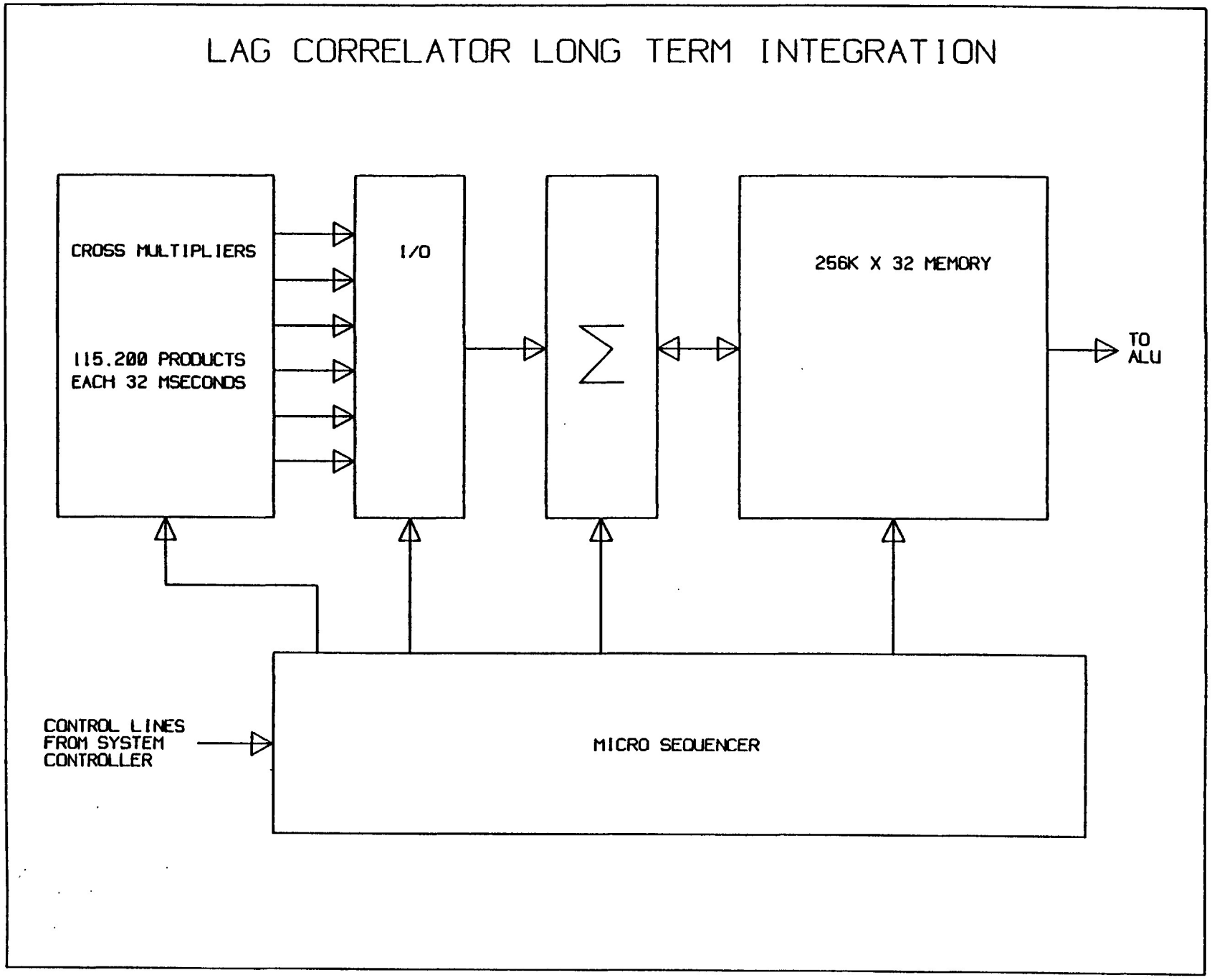

LAG CORRELATOR LONG TERM INTEGRATION
CROSS MULTIPLIERS
115.200 PRODUCTS
EACH 32 MSECONDS
I/O
256K X 32 MEMORY
TO
ALU
CONTROL LINES
FROM SYSTEM
CONTROLLER
MICRO SEQUENCER

FIGURE 13

LAG CORRELATOR FFT REQUIRMENTS

MODE	NUMBER FFT's	FFT LENGTH	NUMBER OF BUTTERFLYS
10 ANT 1 CHANNEL	55	1024 POINT	281,600
10 ANT 8 CHANNEL	440	128 POINT	197,120
15 ANT 1 CHANNEL	120	512 POINT	276,480
15 ANT 8 CHANNEL	960	64 POINT	184,320
20 ANT 1 CHANNEL	210	256 POINT	215,040
20 ANT 8 CHANNEL	1680	32 POINT	134,400

WORSE CASE:

281 600 BUTTERFLYS IN 200 MSECONDS
0.7 MICROSECONDS PER BUTTERFLY

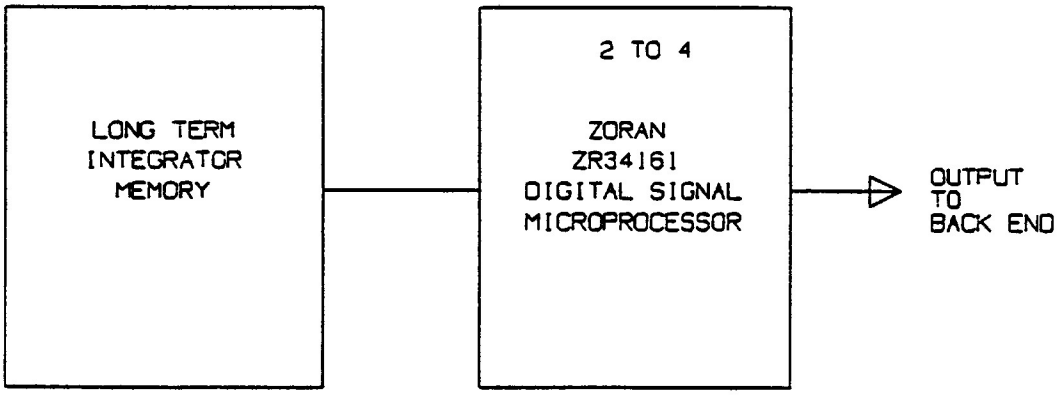


FIGURE 14

Cost Estimate:

Hardware Chip Count:

Delay System		3,600
Driver System		5,000
Cross multiplier System		16,400
Miscellaneous (8)		5,000
	TOTAL	30,000

Computer System:

Back end system	$ 55,000
Micro-VAX system	100,000
Archive tape units	20,000
Distribution tape unit	42,000
	$217,000

Cost Estimate:

Hardware ($15/IC)	$ 450,000
NFRA Gate array NRE (9)	35,000
NFRA Gate array chips (9)	360,000
Fringe rot. gate array NRE (10)	30,000
Fringe rot. gate array chips (10)	108,000
Computer system	217,000
Test Equipment	50,000
	$1,250,000

(8) Control logic, delay model generator, fringe model generator, pulsar gate generator, long term accumulator, hardware ALU, and filter.

(9) Based on discussions with NFRA. NRE charge includes the NRAO pro-rated share of the NFRA chip development cost.

(10) Estimate for cost of small gate array chip ($15/IC).