VLBA Correlator Memo No. 89

(870929)

AN OVERVIEW OF THE VLBA CORRELATOR

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1.0 INTRODUCTION

This memo will present an overview of the VLBA correlator. The hardware will be presented from the block diagram level and the performance will be presented in the form of a brief specification. Figure 1 illustrates the rack layout of the system as it exists at this stage of design and Figure 2 gives a block diagram of the correlator.

2.0 BLOCK DIAGRAM

The following paragraphs describe the block diagram of the FX correlator depicted in figure 2.

2.1 THE PLAYBACK INTERFACE

The playback interface logic is the interface between the Data Playback System (DPS) and the correlator. The functions provided by this system of the correlator include receiving raw track data and clocks from the DPS playback drives, synchronizing the recovered track data to a system clock, extracting time and other inserted information from the playback data, providing the playback units with speed control information, delaying the playback data, performing track to channel conversion on the data, and driving the delayed channel data into the FFT system. A data multiplexer at the input of the playback interface logic of each station is required to support spare playback drive switching.

2.2 THE FFT SYSTEM

The FFT system contains 160 FFT engines that will perform Fourier transforms on input samples. Samples are taken into an FFT engine at 32-Msamp per second. The pipelined FFT chain performs the equivalent of a 2048-point transform in 2048 clock periods or 64-microseconds. Window tapering, fringe rotation, and fractional sample error correction also occur in the FFT system. Calculations in the FFT system are performed in complex floating point arithmetic.

2.3 THE CROSS MULTIPLIERS

The cross multipliers will perform all of the cross and auto multiplications required on the spectra output by the FFT system. Multiplication and short term accumulation is performed in complex floating point arithmetic.

FX CORRELATOR

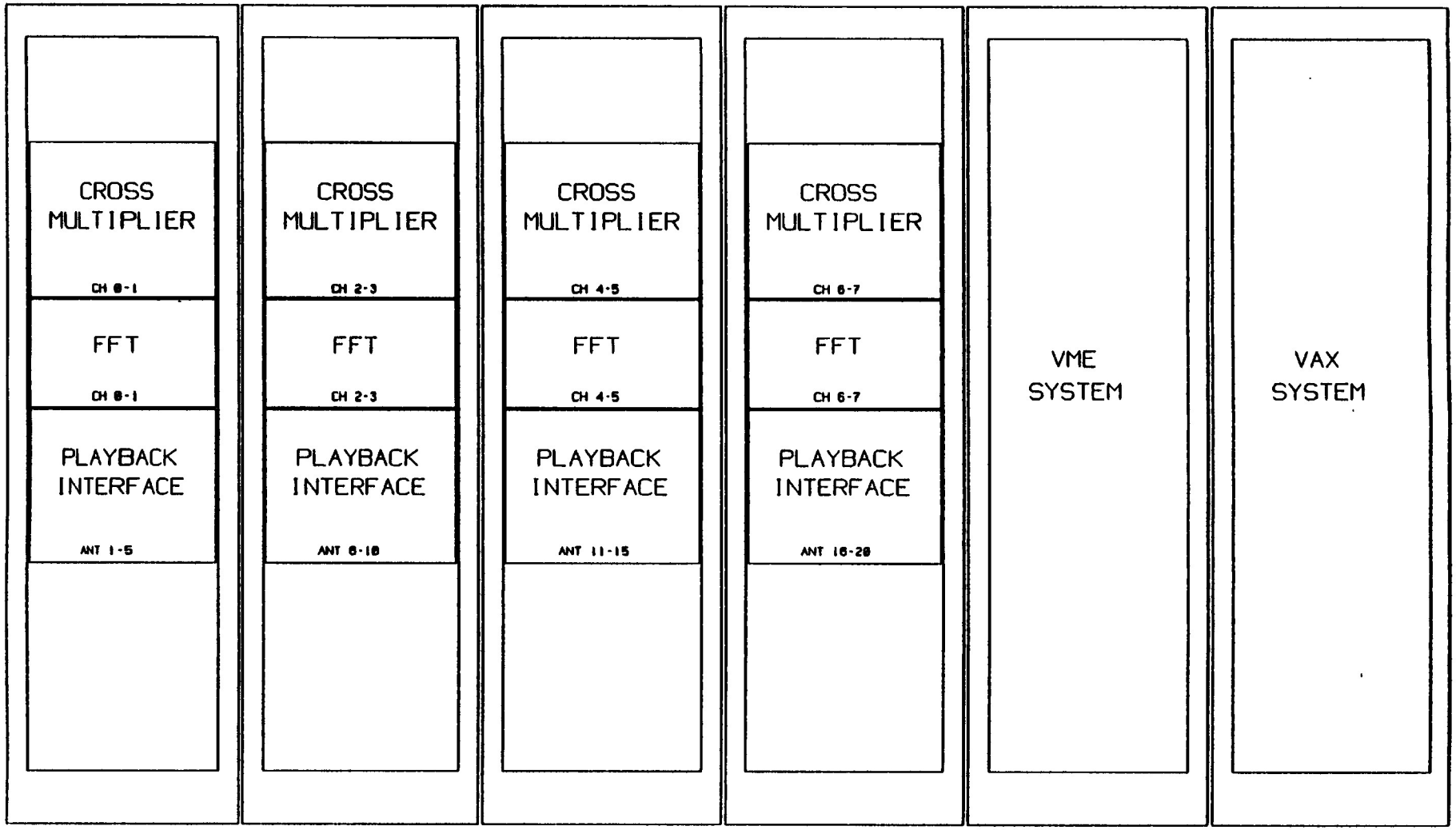

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Figure 1

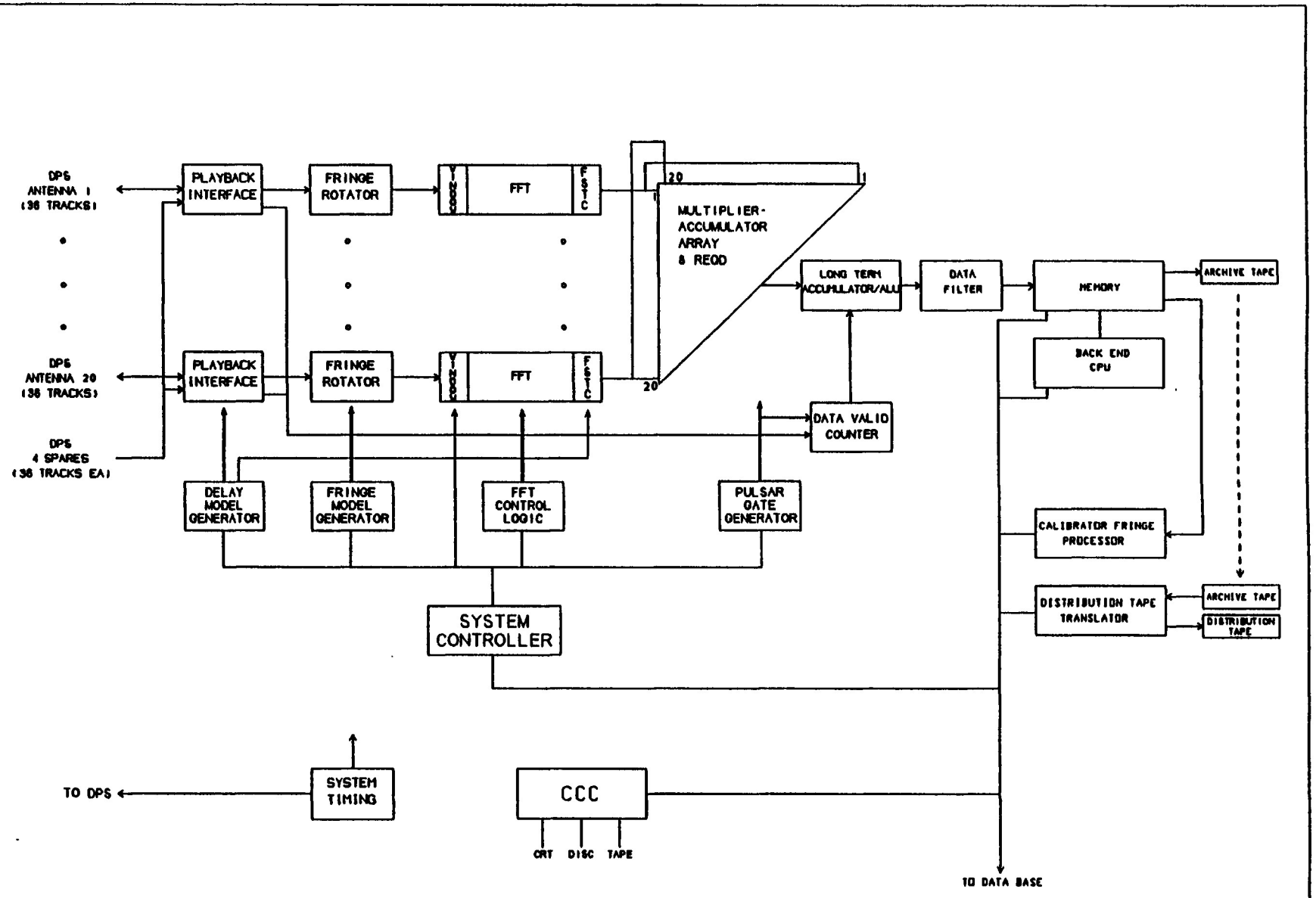
DPS ANTENNA 1 (36 TRACKS)
DPS ANTENNA 20 (36 TRACKS)
DPS 4 SPARES (36 TRACKS EA)
PLAYBACK INTERFACE
PLAYBACK INTERFACE
FRINGE ROTATOR
FRINGE ROTATOR
FFT
FFT
20
1
MULTIPLIER-ACCUMULATOR ARRAY & REQD
LONG TERM ACCUMULATOR/ALU
DATA FILTER
MEMORY
ARCHIVE TAPE
BACK END CPU
DATA VALID COUNTER
DELAY MODEL GENERATOR
FRINGE MODEL GENERATOR
FFT CONTROL LOGIC
PULSAR GATE GENERATOR
CALIBRATOR FRINGE PROCESSOR
SYSTEM CONTROLLER
DISTRIBUTION TAPE TRANSLATOR
ARCHIVE TAPE
DISTRIBUTION TAPE
TO DPS
SYSTEM TIMING
CCC
CRT
DISC
TAPE
TO DATA BASE
FX CORRELATOR BLOCK DIAGRAM
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Figure 2

2.4 CORRELATOR BACK END

The correlator back end is comprised of the long term accumulator, the data filter, the calibrator fringe processor, and the archive writer. The long term accumulator and data filter are to be implemented in discrete logic. The calibrator fringe processor and archive writer will be part of the correlator computer system described below.

2.5 CORRELATOR COMPUTER SYSTEM

The correlator computer system consists of four Motorola 68020 VME processor boards and a small VAX class computer. The four 68020 boards perform the functions of the system controller, the archive tape writer, the distribution tape translator, and the calibrator fringe processor. The VAX class machine will perform all of the activities required of the Correlator Control Computer.

2.6 MODEL GENERATORS

Delay, fringe, and pulsar models are generated in dedicated logic. The delay model will track the delay of a source and generate integral and fractional bit delay values with which to program the delay line and the fractional sample correction logic. The fringe model generator produces fringe phases for the station fringe rotator. The pulsar gate generator produces a mask across the pulsar period and allows spectral averaging during selected portions of the pulsar period.

3.0 SYSTEM SPECIFICATIONS

This section gives a review of the VLBA correlator specifications.

3.1 NUMBER OF STATIONS AND DPS UNITS

The correlator will support up to 20 active stations at any one time. There will be a total of 24 DPS transports at the correlator. For each 5 active DPS playback drives there will be a "hot spare" playback drive which can be substituted for one of the 5 either to support efficient tape changing or in the event of a transport failure. The four hot spare playback units will drive a cross bar switch so that any of the four may be assigned to a given set of 5 active DPS stations. In summary, playback drives will be grouped into 4 sets of 6 units each, 5 of the 6 have dedicated paths through the correlator. The sixth unit can be selected freely from the group of 4 spare drives with the cross bar switch and a multiplexer at the input of playback interface logic can

substitute this spare playback unit for any of the 5 normal drives.

3.2 CORRELATOR CLOCK RATE

The basic correlator system clock rate will be 32-MHz. All of the FFT and cross-multiplication operations will use a continuously running 32-MHz clock. When samples from the data playback system drive the FFT system input at less than a 32-Msamp/sec rate, the extra data processing capacity of the FFT system is used to offer processing options that will enhance the overall performance.

3.3 SAMPLE QUANTIZATION

The correlator will support both 2-bit, 4-level and 1-bit, 2-level sampling. The 2-bit data convention will be sign-magnitude.

3.4 DPS DATA INTERFACE

The DPS interface to the correlator will be raw track data and track clocks from the data recovery logic of the DPS. The correlator playback interface system will synchronize the independent track signals and do the track to channel conversion.

3.4.1 DPS VALIDITY

A data validity bit for each channel will be developed from an analysis of the playback integrity by microprocessors in the playback interface system. The validity bits will mark channel data driving the FFT logic as valid or invalid. Invalid data for a given channel will result if any playback track which contributes to that channel is either out of sync for a period of time or has a parity error count higher than a selectable threshold. Data from the DPS will be judged for validity on a frame basis (a frame being about 22,500 bits in length). Exclusion of invalid channel data will be done on an FFT basis.

3.5 GEOMETRIC ARRAY TRACKING

Delay range:	8 msec minimum (exact value depends on the sample rate)
Delay change rate:	-50 to +50 samples per second
Delay model update period:	32 microseconds for the fractional bit portion and 4 msec for the integral bit portion
Delay resolution:	1/256 of a bit (fractional part of delay)
Delay models:	4

Fringe rate range:	-128 to +128 kHz
Fringe tracking error:	< 0.05 deg times (speedup factor)**2
Fringe model update rate:	32-Mhz
Fringe phase resolution:	8-bits
Fringe models per ch:	4

3.6 FOURIER TRANSFORM SIZE

The correlator will perform station Fourier transforms of 2048, 1024, 512, 256, 128, and 64 points per channel. The only restrictions set on the transform length by the observation is that 2048 point transforms cannot be performed with more than 4 active channels per station (20 station mode) and a maximum transform length of 512 points is set when doing polarization observations.

3.7 FOURIER TRANSFORM PRECISION

Data points within the FFT will be expressed in complex floating point arithmetic with 7-bit real and 7-bit imaginary mantissas expressed in sign-magnitude with the two having a common 4-bit negative exponent (or in a short hand notation, 7,7,4). The trig table twiddle factors will be expressed, using the short hand form, in 5,5,0 complex floating point. Trig table performance will be enhanced by having 32 tables that average to 10,10,0 accuracy that will be multiplexed in time into the FFT logic.

3.8 FRACTIONAL SAMPLE CORRECTION

The delay model generator will track the delay to 1/256 of a sample, the fractional part of the sample delay is used to generate a phase ramp of 16-bit accuracy that will be used to twist the FFT output spectrum. The point by point correction will be done using the 8 most significant bits of the 16-bit ramp.

3.9 PULSAR GATE

The phase of a pulsar will be tracked using a 40-bit initial phase that is updated every 32-microsec by adding a 40-bit phase change rate to it. The most significant 10-bits of the resulting 40-bit pulsar phase are used to provide 1024 point resolution across the pulsar period. Each spectral frequency point will be provided with an individually programmable 1024 point mask across the pulsar period. There will be a total of 4 phase generators that develop a total of 8 sets of masks.

3.10 CROSS MULTIPLICATION RESOLUTION

Spectral points out of the station hardware driving the cross multipliers will be expressed with 4,4,4 precision. Cross-

and auto-spectra will be generated in the cross multiplier system and short term accumulation will take place there using complex floating point addition and storage. Short term accumulation will take place with 15,15,6 precision. The short term accumulator will be dumped into the long term accumulator every 100 msec.

3.11 CORRELATOR LONG TERM ACCUMULATOR

The correlator accumulator will allow the integration of a maximum of 262,144 complex terms. The correlator will support a minimum integration time of 100 msec. Long term accumulation will be done in 32-bit IEEE floating point.

3.12 POST ACCUMULATION DATA FILTERING

A digital filter will be provided at the long term accumulator output to allow for other than boxcar averaging of the archive data. A 32-tap programmable filter is envisioned with a possible data rate decimation of a factor of 4.

3.13 ARCHIVE DATA

Data will probably be archived by the correlator system using a rotary head technology high density storage tape unit. Archive rates of up to 0.5 Mbyte/sec will be supported.

3.14 DISTRIBUTION FORMAT

The archived data will be translated into a distribution tape following the FITS tape format.