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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
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14 July 1988

508
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To: VLBA Recorder/Data Acquisition Group

From: Alan E.E. Rogers

Subject: Minutes of VLBA Recorder/Data Acquisition Group
Telecon Held 13 July 1988 at 1300 EDT

Attendees:

Dick Thompson	- NRAO, Charlottesville
Ray Escoffier	- NRAO, Charlottesville
Jon Romney	- NRAO, Charlottesville
Larry D'Addario	- NRAO, Charlottesville
Phil Doolie	- NRAO, VLA
Ron Heald	- NRAO, VLA
Alan Rogers	- Haystack
George Peck	- Haystack
Roger Cappallo	- Haystack

1] Status of Problems Noted in REC #1

a) Recorder Controller Monitor Board - "Bit Offset"

A wiring error was found on the decoder portion of the recorder controller monitor board of REC #1. After correction of the error (made during hand wiring modifications) the "bit offset" now agrees with that expected from the timing diagram and with the monitor board in REC #2. Ron Heald has agreed to update the bit offset numbers in the program TDC.

b) Recorder Controller VME Computer Crashes

Crashes have been observed in the Motorola 68010 computer in both REC #1 and #2. So far no pattern or clues as to the cause have been found.

2] Status of New Modules Needed for PYB #1

a) Parallel Bit Synchronizer Board

Ed Nesman has the responsibility for this board and he has tested a commercially available bit synchronizer chip made by AT&T. The error rates, sync loss and lock range using this chip appear to be better than the ECL circuit used in the Mark III. Further evaluation may be needed but preliminary results look

very good. If the AT&T chip (T7033) can be used the parallel bit synchronizer board will be simpler, consume less power and will not require distribution of the X21 clock.

b) Parallel Reproduce Board (36 Reproduce Channels)

Hans Hinteregger has responsibility for this board and he is proceeding with a design that is packaging many parallel sections of the circuit using the monitor channels of the acquisition recorder. Recent tests have shown that a "D.C. restoration" circuit prior to the comparator might be advantageous and provision for the addition of this circuit will be considered.

3] Second Ambiguity Problems

Good quality fringes have been obtained to Pie Town and other sites in a recent NUG run. However, the Pie Town clock was one second late (from processing at Haystack and Bonn) and there was considerable difficulty in monitoring and setting the Pie Town formatter clock during the NUG run. In addition, the Pie Town clock may have jumped several times. Further processing should verify these jumps and might shed further light on their nature. After much discussion it was agreed that -

a) Alan Rogers will discuss the implementation of a one minute mark LED and BNC output on the formatter.

b) Alan Rogers will work with Ron Heald and George Peck to further determine the nature of the jumps and what error flags, if any, are present in the formatter following a jump.

4] DAR #1

Alan Rogers proposed that DAR #1 (now at the VLA) return to Haystack for use as a test tool for the recorders being built at Haystack. Eventually DAR #1 should be upgraded and made available as a spare rack.