VLBA ACQUISITION MEMO #195

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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Area Code 508
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To: VLBA Data Recording Group

From: Alan E.E. Rogers, Edwin F. Nesman, Jonathan E. Hargreaves

Subject: Tests of Parallel Playback Electronics

New Parallel Reproduce Electronics

The new parallel reproduce electronics incorporates two improvements which have been previously examined in separate tests. These are "D.C. Restoration" (see VLBA Acquisition Memo #169) and the AT&T VLSI bit Synchronizer (see VLBA Acquisition Memo #145). The parallel read board (designed by Jonathan Hargreaves) is contained in a NIM module while the parallel bit synchronizer board (designed by Ed Nesman) is on a VME wire wrap panel.

Tests at 56 Kb/inch with D1K

The performance of the new electronics has been tested by recording and playing back a 9 Mb/sec MKIIIA format at 160 IPS which corresponds to a linear bit density of 56,000 bits per inch.

Figure 1 shows the playback circuit for a single channel. Figures 2A and 2B shows the bit pattern with the tape played in reverse to deliberately produce severe baseline D.C. shifts. The middle trace shows the D.C. restored waveform seen by the differential input of the comparator (i.e., sum of bottom and top traces which are the signal and inverted reference signals to the comparator respectively). Figure 2C shows the same D.C. restored signal in the forward direction and Figure 2D shows the conventional "eye" pattern obtained by synchronizing the scope on the restored clock.

Error rates have been measured (on 1 second of data = 400 frames) and are generally in the range 0-20 parity errors (per million), 0-2 CRC errors, 0 sync and resync errors for a "good" recording.

Tracks initially showing high error rates tended to be consistently high, and have been traced to one of the following causes:

- "old" version of AT&T chip (acceptable date codes are 00689 and later),
- bad recording, or dropouts on tape ,
- chip or equalizer failure on parallel reproduce board.

The spectrum of the signal measured at the D.C. restore circuit (output of L.P.F.) is shown in Figure 3A.

Figure 3B is the signal in an adjacent channel whose inputs from the preamp have been shorted to ground. From this, the crosstalk arising in the parallel reproduce board is deduced to be approximately -31 dB with 11 other channels active.

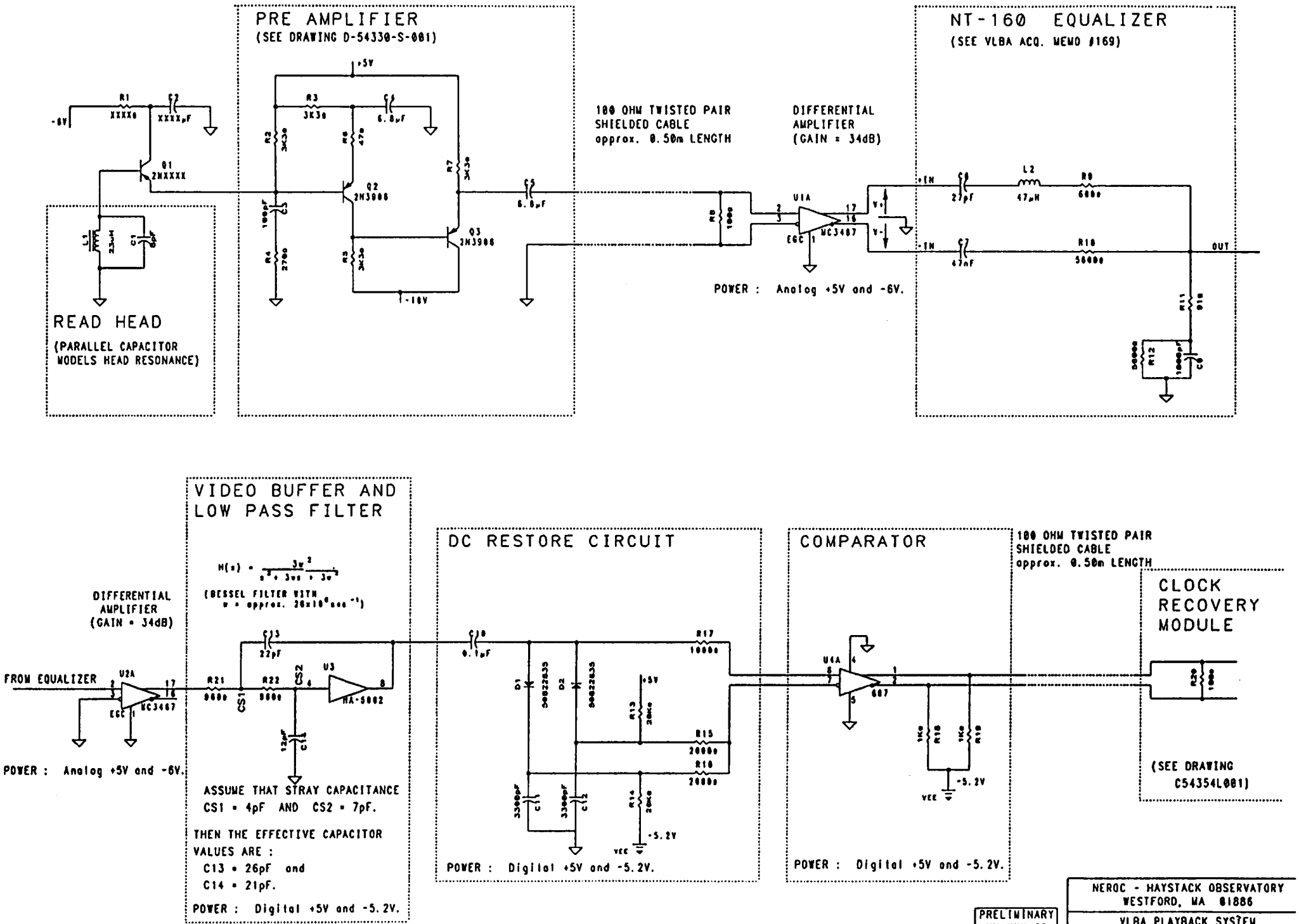
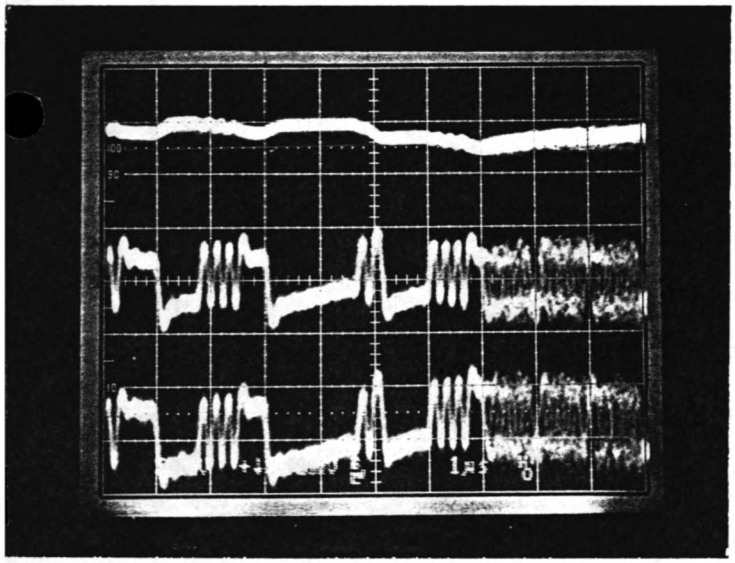
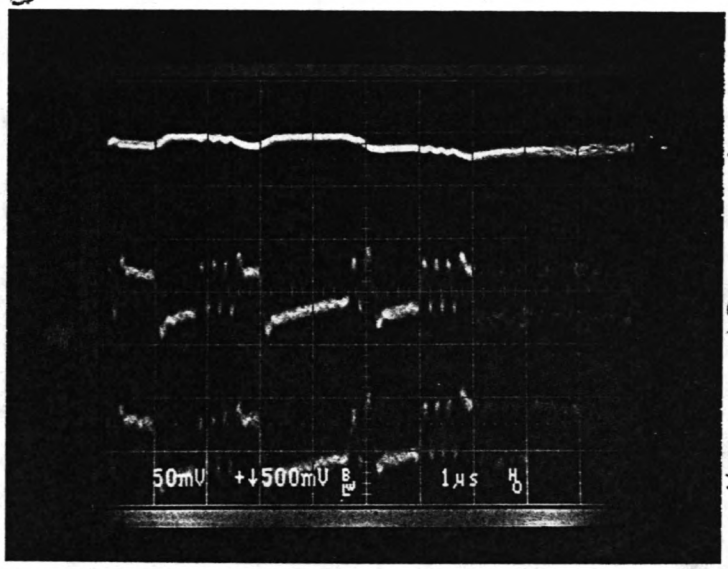

PRE AMPLIFIER
(SEE DRAWING D-54330-S-001)
READ HEAD
(PARALLEL CAPACITOR MODELS HEAD RESONANCE)
100 OHM TWISTED PAIR SHIELDED CABLE approx. 0.50m LENGTH
DIFFERENTIAL AMPLIFIER (GAIN = 34dB)
NT-160 EQUALIZER
(SEE VLBA ACQ. MEMO #169)
POWER : Analog +5V and -6V.
VIDEO BUFFER AND LOW PASS FILTER
DIFFERENTIAL AMPLIFIER (GAIN = 34dB)
FROM EQUALIZER
POWER : Analog +5V and -6V.
ASSUME THAT STRAY CAPACITANCE CS1 = 4pF AND CS2 = 7pF.
THEN THE EFFECTIVE CAPACITOR VALUES ARE :
C13 = 26pF and
C14 = 21pF.
POWER : Digital +5V and -5.2V.
DC RESTORE CIRCUIT
POWER : Digital +5V and -5.2V.
COMPARATOR
POWER : Digital +5V and -5.2V.
100 OHM TWISTED PAIR SHIELDED CABLE approx. 0.50m LENGTH
CLOCK RECOVERY MODULE
(SEE DRAWING C54354L001)
NEROC - HAYSTACK OBSERVATORY
WESTFORD, MA 01886
VLBA PLAYBACK SYSTEM
READ SIGNAL PATH
PRELIMINARY
XX-XXX-89

FIGURE 1

A

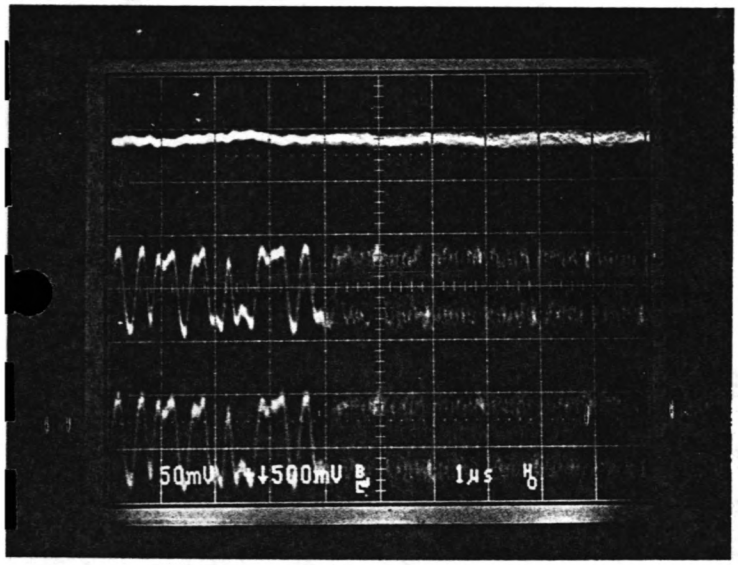


B



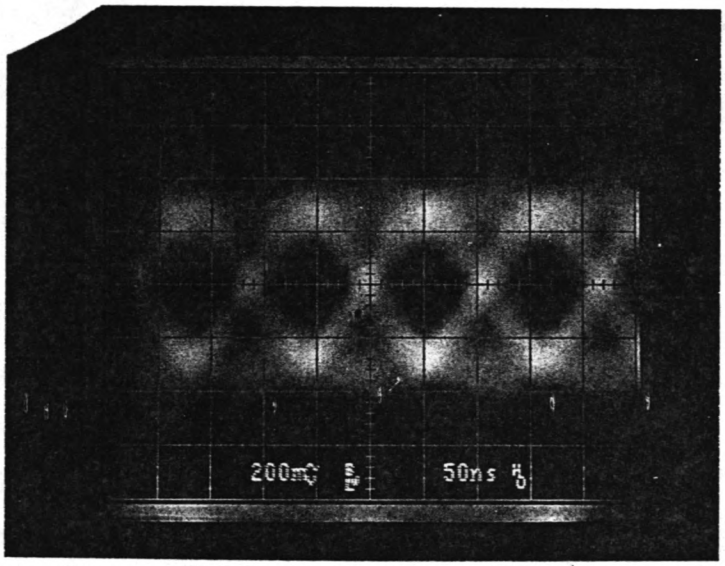
REVERSE

C



FORWARDS 56 Kb/sec

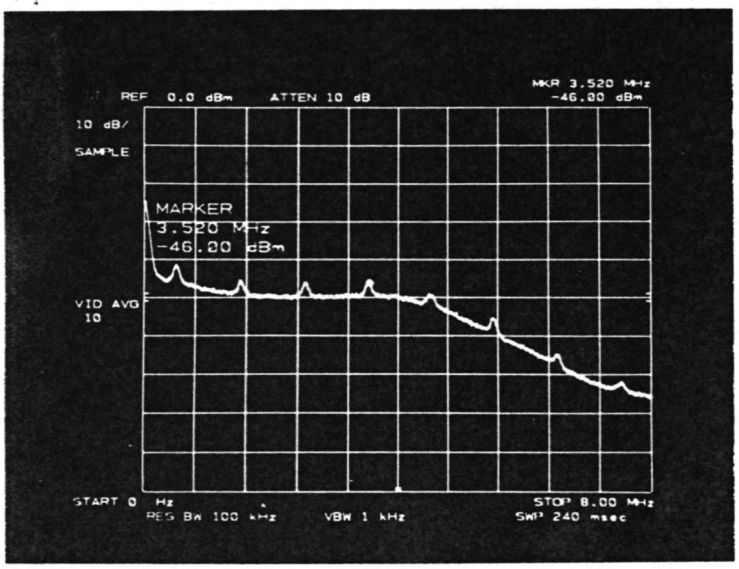
D



CH A "EYE" 27 JAN 90

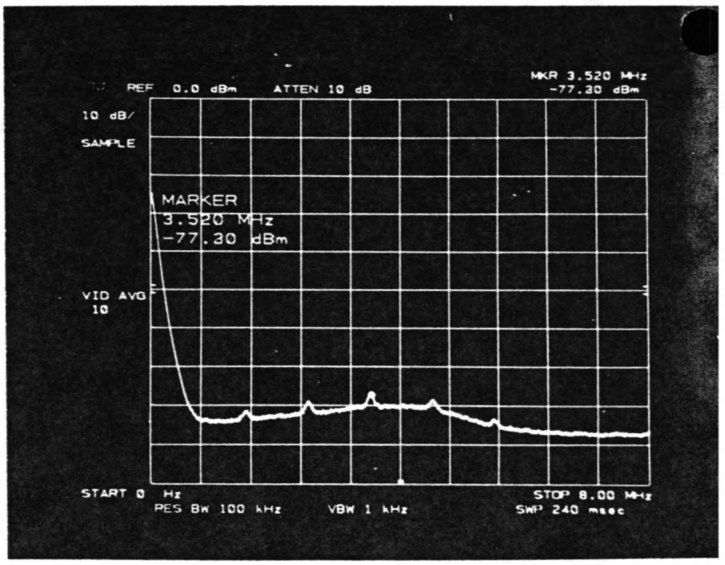
FIGURE 2A, B, C, D

A



PLAYBACK SIGNAL

B



COMM-TALK CHECK 1 FEB 90

FIGURE 3 A, B