VLBA ACQUISITION MEMO #250

VLBA TAPE RECORDER AND FORMATTER STATUS/ERROR MONITOR POINTS

George Peck
National Radio Astronomy Observatory
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TAPE RECORDER

The tape recorder status register, located at register 0x73 can be monitored to determine the following conditions:(0|1 false|true)

error exists	bit 0
the tape is moving	bit 1
the headstack is moving	bit 2
reels are ramping	bit 3
the headstack is positioning	bit 4
the tape is positioning	bit 5
the vacuum is ok	bit 6
the 5 MHZ is present	bit 7
the 1PPS is present	bit 8
the headstack is peaking	bit 9
the headstack is tracking	bit 10
forward tape motion	bit 11

I recommend the following procedures to detect problems as soon as possible:

1. Monitor bits 0 and 4 immediately after any command to move the headstack. After bit 4 returns to 0, monitor bit 0 to be sure that no error flags have been set.

2. Before commanding the tape to move, monitor bit 6 to be sure that that the vacuum is ok. If the vacuum is not ok, an attempt should be made to load the tape. After the motion command has been issued, bit 0 should be monitored to determine if an error flag was set as a result of attempting to move the tape. Bit 1 can be monitored to insure that the tape is moving, and bit 11 can be monitored to determine the direction of tape motion.

3. After a LOAD command has been sent, bit 0 can be monitored to determine if an error flag was set as a result of attempting to load the tape, and bit 6 can be monitored to determine that the vacuum is ok.

4. Periodically monitor bit 0 to detect errors as soon as possible.

5. If bit 0 of the status register is set, indicating that an error exists, monitor the error register (0x74) to find out what the error is.

6. It is not important to monitor the 5MHZ and 1PPS for the tape recorder, but it may be useful if it is suspected that there is a problem with one of these at the station.

7. If error bits 0 or 7 are set, they indicate a probable software bug. It would be useful to be able to recover the aproximate time of such an error from the monitor data, but it is not useful for the operator to be immediately alerted to one of these errors.

Following are the error flags which should be monitored in the event that bit 0 of the status register is set. The error register (at location 0x74) is automatically cleared every time that it is read. (0¦1 false¦true)

bit 0	data out of range*
bit 1	unused
bit 2	unable to attain vacuum w/ load
bit 3	failed attempt to change active head*
bit 4	head index out of range
bit 5	head block parm # out of range
bit 6	A/D conversion time out
bit 7	attempted write to 0x0-0x7f*
bit 8	attempt to move without tape loaded
bit 9	head movement time out
bit 15	software error

* implemented in next version of firmware

Bit 0 is currently unused.
Bit 3 is currently unable to position head.
Bit 7 is currently failed attempt to change active head.

FORMATTER

The system status register, at relative address 0x20, is useful because it reports the presence of any errors, and reports if the formatter is busy for any reason. Following are the bit assignments: (Bit 12 probably does not need to be monitored, since these errors are extremely rare, and deal with the microprocessor in the formatter.)

1.	Any Error Detected	Bit 15
2.	MCB Error Detected	Bit 14
3.	Hardware Error Detected	Bit 13
4.	Software Error Detected	Bit 12
5.	Interrupt System Error Detected	Bit 11
6.	Formatter Is Busy Initializing	Bit 3
7.	Formatter Is Busy Configuring	Bit 2
8.	Formatter Is Busy Retreiving Q/A Data	Bit 1
9.	Formatter Is Waiting For FIFOs to Fill	Bit 0

The following formatter errors are fatal, and the operator should be informed when they occur. These errors may be cleared by configuring the formatter, however persistent problems will immediately cause the flags to be reset after a configure.

1. Sampler 1 Clock Dropout Error (0¦1 false¦true)

Bit 13 of relative address 0x41 indicates that the 32 MHZ clock from sampler 1 to the formatter is missing.

2. Sampler 2 Clock Dropout Error (0¦1 false¦true)

Bit 12 of relative address 0x41 indicates that the 32 MHZ clock from sampler 2 to the formatter is missing. This error will not be set until the firmware believes that 2 sampler modules are present. ADMGR_H must be modified and recompiled to indicate the presence of the second sampler module.

3. FIFO Error (0¦1 false¦true)

Bit 12 of relative address 0x42 indicates a FIFO error. When this error occurs, bits 0-12 of relative address 0x43 should be examined to determine the state of the FIFOs at the time of the error. For this register, 1 implies true, as usual. Bits 0-3 indicate that FIFOS 0-3 are empty. Bits 4-7 indicate that FIFOs 0-3 are full. No FIFOs should ever be full or empty. Bits 8-11 indicate that the 1PPS marker was detected in FIFOs 0-3 at the time of the error. These four bits should always be the same. Bit 12 indicates that the firmware believes that the 1PPS should have been present. Bit 12 should always be the same as bits 8-11. The following error conditions should be immediately reported: any FIFO empty errors, any FIFO full errors, and any instance when bits 8-12 are not the same.

4. Timed Out Waiting For 1PPS Interrupt

Bit 13 of relative address 0x23 is set when the formatter fails to receive the 1PPS from the sampler module.

5. Illegal Combination of Sample Rate and Multiplex Mode

Bit 11 of relative address 0x23 is set when the sample rate and multiplex mode selected are incompatible.

6. Timed Out Waiting For FIFOS To Fill

Bit 10 of relative address 0x23 indicates that the FIFOs didn't become half full in a reasonable amount of time, so the firmware timed out.

7. Timed Out Waiting For Tape Time 1PPS

Bit 9 indicates that the pulse which occurs when the firmware expects to tag a particular bit as the first bit in a one second epoch is missing.

The following errors indicate a possible software bug, and it would be helpful if the monitor data recorded the approximate time of these errors. These errors may be cleared by a command to location 0xa1. (0¦1 false¦true)

1. MCB Communication Error

Bit 15 of relative address 0x21 indicates an MCB communication error. The other bits in this register should be examined in the event of this error.

2. Timing Conflict

Bit 14 of relative address 0x21 indicates that an initialize or configure command was attempted while the formatter was still busy with the last operation. This flag is usually set because a command was sent while register 0x02 still contained 0x8002, indicating that the formatter is busy configuring.

3. Command Conflict

Bit 13 of relative address 0x21 indicates that an attempt was made to configure the auxiliary data buffer when register 0x03 contained either 0x8001 or 0x8002, indicating that it was already busy configuring.

4. Formatter Busy During Conrol Access To Array

Bit 11 of relative address 0x21 is set when an attempt is made to send a command to one of the formatter arrays when the formatter is busy. The usual cause of this error is that relative address 0x02 contains 8001, indicating that the formatter is busy configuring.

5. Formatter Busy During Monitor Access To Array

Bit 10 of relative address 0x21 is set when an attempt is made to monitor one of the formatter arrays when the formatter is busy. The usual cause of this error is that relative addres 0x02 contains 8001, indicating that the formatter is busy configuring.

6. Array Pointer Went Out Of Limits

Bit 8 of relative address 0x21 is set when a pointer to one of the formatter arrays points to an address which is beyond the highest address of the array.

7. Control Access Attempt To A Monitor Only Register

Bit 5 of relative address 0x21 is set when an attempt is made to write to addresses 0x0-0x7f.

8. Ilegal Control Parameter Received

Bit 4 of relative address 0x21 is set when data sent to the formatter is not one of the allowed control parameters for the address to which it is sent.

9. Formatter Busy During Control Access To A Register

Bit 3 of relative address 0x21 is set when an attempt is made to send a command to the formatter when the formatter is busy. The usual cause of this error is that a command is sent when register 0x02 indicates that the formatter is busy configuring.

10. Formatter Busy During Monitor Access To A Register

Bit 2 of relative address 0x21 is set when an attempt is made to monitor the formatter when the formatter is busy. The usual cause of this error is that a monitor request is issued when register 0x02 indicates that the formatter is busy configuring.

11. Non-Existing Control Register Access Attempted

Bit 1 of relative address 0x21 is set when an attempt is made to send a command to an address which has not been defined.

12. Non_Existing Monitor Register Access Attempted

Bit 0 of relative address 0x21 is set when an attempt is made to monitor an address which has not been defined.