VLBA ACQUISITION MEMO #258

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To: VLBA Data Acquisition Group

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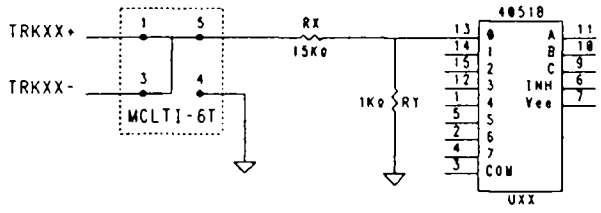
Subject: Write Driver Asymmetry Improvements

Further studies of the VLBA write driver by Hans Hinteregger have pointed out that the symmetry of the signal is poor. The asymmetry measured at the output of a write driver IC is about 11.6 ns in delay (see Figure 1A) and was briefly noted in VLBA Acquisition Memo #210. Further tests have suggested four simple fixes:

1] Change input coupling to DS0026 from 0.1 μf to 47 pf in parallel with 1KΩ. This reduces the asymmetry from 11.6 to 9.0 ns. (see Figure 1B)
2] Replace 74AS822 with 74F822. Since about 2 ns of the asymmetry arises in the reclocking flip-flops replacing them with fast logic further reduces the asymmetry from 9.0 to 8.6 ns. (see Figure 1C)
3] Replacing the 100Ω resistor in series with the output with a 33Ω makes a further improvement in both symmetry and rise time.
4] Replacing the MCLTI-6T (RF Transformer) with the circuit as below:



Additional tests made by heating and cooling the DS0026 drivers show little temperature dependence of the asymmetry (with driver with a fast logic) over the temperature range 0 - 100° C.

We are investigating the inclusion of these changes in the new PC board, and will implement these changes in the new PC board version of the write driver.

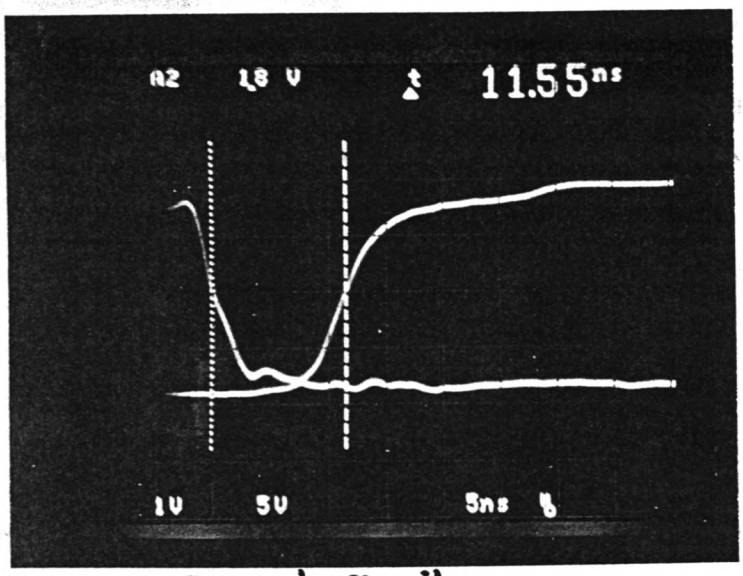


Figure 1A

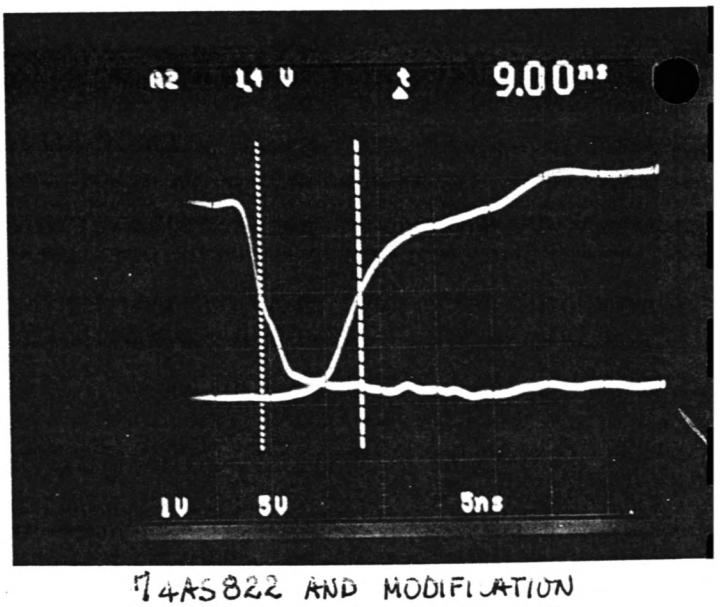


Figure 1B

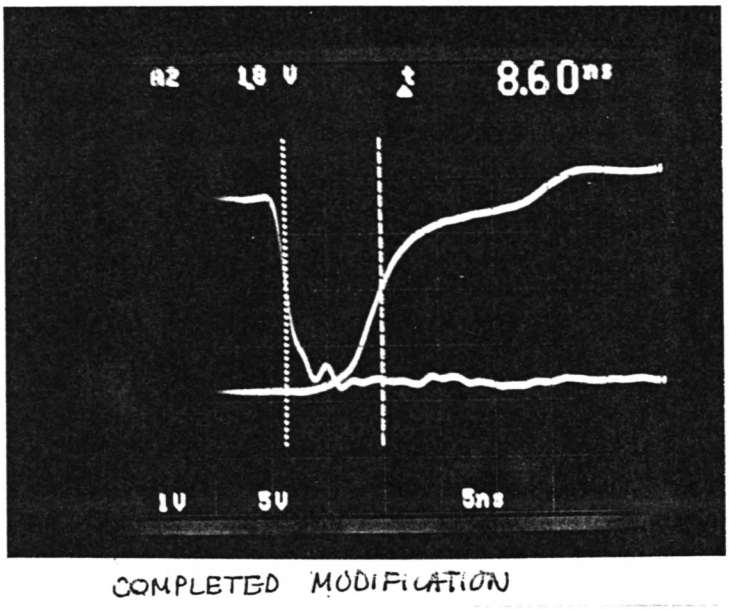
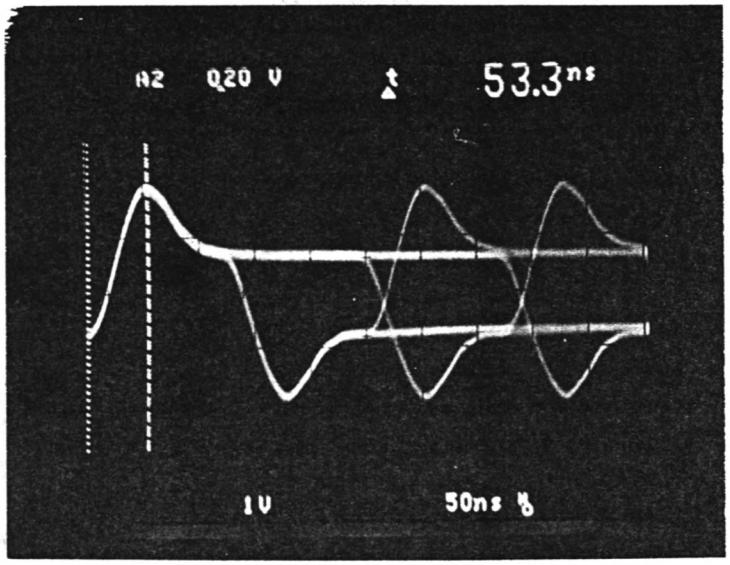
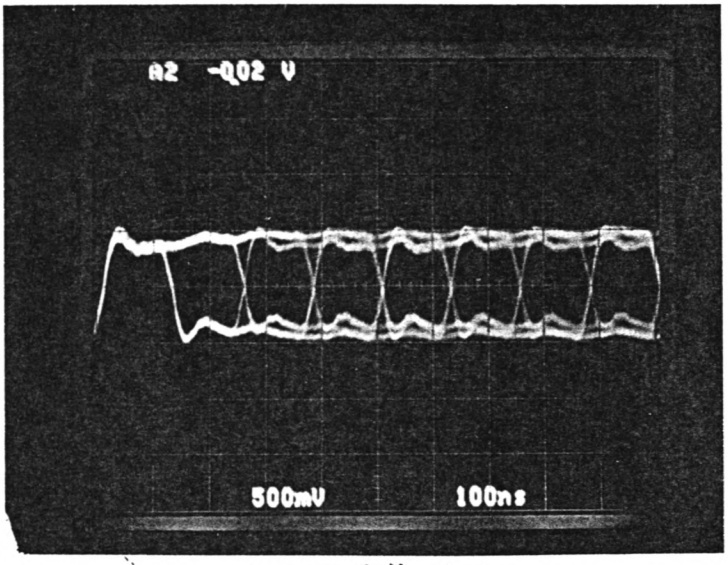


Figure 1C



PRESENT CIRCUIT

Present Circuit Output



15KΩ AND 1KΩ

Modified Circuit Output