VLBA ACQUISITION MEMO #337

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5 October 1992

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To: VLBA Data Acquisition Group

From: Alan E.E. Rogers
E.F. Nesman

Subject: Preliminary MCB protocol for digital switch and tone extractor

A new board has been designed (see VLBA Acquisition Memos #248 & 249) and prototyped to replace the "A/D" board in the VLBA formatter. We call this new board the DIGITAL SW. The new board solves the problems of the analog switch (see VLBA Acquisition Memo #235) and provides circuitry to perform digital tone extraction and/or state counting of 8 channels.

The MCB protocol for the A/D to track selection is unchanged (except that it is now safe to assign all tracks to one A/D without provoking errors).

Attached is the preliminary MCB protocol for the new pcal features of the board.

Relative Address

PCAL STATUS

0x06	Monitor	pcal status	bit 0: 0 =	tables are current*
			1 =	needs configure to load new tables into pacal extractor RAMs
			bit 1: 0 =	counters stopped
			1 =	pcal counters running
			bits 2-15:=	unassigned

PCAL CONTROL (global all extractors)

0x86	Command/mon	pcal control	bit 0: =	unassigned
			bit 1: 0 =	stop pcal
			1 =	start pcal
			bit 2: 0 =	normal
			1 =	load test patterns
			bit 3: 0 =	test pattern = all 0's
			1 =	test pattern = all 1's
			bit 4-7: =	pcal mode (see below)
			bit 8-14: =	unassigned
			bit 15: 1 =	control
			(JIL's convention)	

*Following any control access to 0x76 tables will not be current until configure is issued.

INDIRECT ACCESS TO PCAL A/D ASSIGNMENT

0x70	mon/control	high address	bits(16-31) 0
0x71	mon/control	low address	bits(00-15) extractors number 0-7
0x72	mon/control	data transfer	bits 0-7 A/D input code for "sign" input i.e., 03 = USB 1
			bits 8-15 A/D input code for "magn" input
0x73	check sum register		

INDIRECT ACCESS TO PCAL SET-UP

0X74	mon/control	high address	0
0x75	mon/control	low address	extractor number 0-7
0x76	mon/control	data transfer	bits 0-10: pcal frequency in units of 10 KHz (0-1600). zero for state counting
			bit 11: 0 = normal 1 = double number of extractors
			bits 12-14: unassigned
			bit 15: 0 = 1-bit data 1 = 2-bit data
0x77	checksum		

INDIRECT ACCESS TO PCAL COUNTERS

0x78	mon/control	high address	0
0x79	mon/control	low address	index = extractor number x 8 + counter number x 2 + hilow (0 = LSW, 1 = MSW)
0x7A	mon/control	data transfer	
0x7B	checksum		

pcal mode = 0:

integration for 9 seconds, blanked for 1 second so that pcal indirect access to counters can be safely made anytime from unit seconds x 0 thru x 8 to give results from previous 10 second period (9 integration + 1 blanked).

pcal mode = 1:

integrate for 1 second on even seconds blanked for 1 second on odd seconds

pcal mode = 8 counters always running "read on the fly". In this mode at least one extractor should be used to count states so that the data can be normalised.

Counter number:

For state counting	counter #	=	0	=	count of state 00
		=	1	=	count of state 01
		=	2	=	count of state 10
		=	3	=	count of state 11
For tone extraction	counter #	=	0	=	sine LSBs
		=	1	=	sine MSBs
		=	2	=	cosine LSBs
		=	3	=	cosine MSBs

Doubling mode (bit 11 of 0x76):

With doubling mode for a given extractor (bit 11 of 0 x 76 data transfer) bit 12 is ignored and data is assumed to be 1 - bit. In this mode each extractor can serve as a state counter or tone extractor for 2 channels. Only the sign bits are used.

For this mode:

0 x 72 bits 0 - 7: A/D code for sign channel "A"
bits 8 -15: A/D code for sign channel "B"

Counter number:

For state counting	counter #	=	0	=	count of state 0 for ch. A
		=	1	=	count of state 1 for ch. A
		=	2	=	count of state 0 for ch. B
		=	3	=	count of state 1 for ch. B
For tone extraction	counter #	=	0	=	sine ch. A
		=	1	=	cosine ch. A
		=	2	=	sine ch. B
		=	3	=	cosine ch. B

Checks that can be made on the hardware:
1] For mode = 0 and pcal frequency = 0 the sum of counts in all states should be $9x32x10^6$ = 112A8800
2] Set A/D code to 40 with connect a constant 0 while 60 will connect a constant 1.

*REVISED VLBA ACQUISITION MEMO #337

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5 October 1992
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The MCB protocol for the A/D to track selection is unchanged (except that it is now safe to assign all tracks to one A/D without provoking errors).

Attached is the MCB protocol for the new pcal features of the board.

Relative Address					
			PCAL STATUS		
0x06	Monitor	pcal status	bit 0:	0 =	tables are current*
				1 =	needs configure to load new tables into pacal extractor RAMs
			bit 1:	0 =	counters stopped
				1 =	pcal counters running
					(this is not a direct read of the A/D board use 0x41 for direct read)
			bits 2-15:=		unassigned
			PCAL CONTROL (global all extractors)		
0x86	Command/mon	pcal control	bit 0:	=	unassigned
			bit 1:	0 =	stop pcal
				1 =	start pcal
					(will be stopped by configure (0x82))
			bit 2-3:	=	unassigned
			bit 4-7:	=	pcal mode (see below)
			bit 8:	1 =	reload Xilinx configuration code
					(since this takes some time it is done just prior to loading the pcal RAMs)
			bit 9-14:	=	unassigned
			bit 15:	1 =	control
					(JIL's convention)

*Following any control access to 0x76 tables will not be current until configure is issued.

INDIRECT ACCESS TO PCAL A/D ASSIGNMENT

0x70	mon/control	high address	bits(16-31)	0
0x71	mon/control	low address	bits(00-15)	extractors number 0-7
0x72	mon/control	data transfer	bits 0-7	A/D input code for "sign" input i.e., 03 = USB 1 ("B" input on circuit diagrams) (FF for connection to fixed zero)
			bits 8-15	A/D input code for "magn" input i.e., 02 = USB 1 ("A" input on circuit diagrams)
0x73		check sum register		

INDIRECT ACCESS TO PCAL SET-UP

0X74	mon/control	high address		0
0x75	mon/control	low address		extractor number 0-7 (8-15 for "doubling" mode mates i.e. channel "A" freqs)
0x76	mon/control	data transfer	bits 0-10:	pcal frequency in units of 10 KHz (0-1600). zero for state counting
			bit 11:	0 = normal 1 = double number of extractors
			bit 12:	0 = normal 1 = load test pattern for this extractor (for test pattern frequency must also be set to zero)
			bit 13:	0 = test pattern = all zeros 1 = test pattern = all ones
			bit 14:	unassigned
			bit 15:	0 = 1-bit data 1 = 2-bit data
0x77		checksum		

INDIRECT ACCESS TO PCAL COUNTERS

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For state counting	counter #	=	0	=	count of state 00
		=	1	=	count of state 01
		=	2	=	count of state 10
		=	3	=	count of state 11
For tone extraction	counter #	=	0	=	sine LSBs
		=	1	=	sine MSBs
		=	2	=	cosine LSBs
		=	3	=	cosine MSBs

DOUBLING mode (bit 11 of 0x76):

With doubling mode for a given extractor (bit 11 of 0 x 76 data transfer) bit 15 is ignored and data is assumed to be 1 - bit. In this mode each extractor can serve as a state counter or tone extractor for 2 channels. Only the sign bits are used.

For this mode:

0 x 72 bits 0 - 7: A/D code for sign channel "B" input
bits 8 -15: A/D code for sign channel "A" input

0 x 76 "B" channel frequencies are in index 0-7 of 0x75
"A" channel frequencies are in index 8-15 of 0x75

Counter number:

For state counting	counter #	=	0	=	count of state 0 for ch. B
		=	1	=	count of state 1 for ch. B
		=	2	=	count of state 0 for ch. A
		=	3	=	count of state 1 for ch. A
For tone extraction	counter #	=	0	=	sine ch. B
		=	1	=	cosine ch. B
		=	2	=	sine ch. A
		=	3	=	cosine ch. A

Checks that can be made on the hardware:
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