VLB ARRAY MEMO No. 138

NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

MEMORANDUM October 29, 1982

To: VLBA Proposal Group

From: Craig Moore

Subj: The Implications of Geodetic and Astrometric Observations on the VLBA IF Processor Design

Some doubts have been expressed on the ability of the proposed VLBA IF scheme to handle observations for the geodetic and astrometric communities. At present these observations are done with 4 to 10 IF frequencies (of 5 or 10 MHz bandwidth) spaced across receiver passbands of 100 to 350 MHz each. The proposed technique for bandwidth synthesis in the VLBA is to frequency switch one of the four 50 MHz BW IF channels across the selected receiver passband on successive integration periods, thus achieving a time-multiplexed frequency-spaced array. The purpose of this memo is to enumerate the requirements such a scheme imposes on the LO synthesizers and to show that these requirements are not severe from the equipment designer's viewpoint.

If we consider integration periods on the order of 200 ms as being typical for the VLBA, then the frequency agile LO in the IF processor should be capable of switching (and phase settling) in 10 ms or less. To account for phase settling, the geodetic community defines synthesizer switching time as the time elapsed from the initiation of a frequency step from frequency A until the output at frequency B is within 0.05 rad (3°) of its final value. Additionally, they want the fringe phase to be continuous for each IF frequency. This means that the LO synthesizer output should be phase repeatable, i.e., upon returning to frequency A the output should be within 0.05 rad of the previous frequency A output. The output should then be phase stable to this order during the dwell at frequency A in the face of various environmental influences. Of course, the phase reference for all of these requirements is the local frequency standard. The L6 module (2-4 GHz) at the VLA provides phase repeatability and stability on the order of 1°-2° at the present time.

We will now attempt to describe how the proposed VLBA IF processor satisfies these requirements. Figure 1 is a block diagram of the IF scheme, the lower portion of which appeared as Figure IV-7 in the VLBA proposal. The uppor portion is of interest to this discussion, but was a technical detail understandably left out of the VLBA proposal. As can be seen from Figure 1, the basic frequency synthesis is done at 100 to 200 MHz. This is then translated up to 2.3 to 3.5 GHz in 100 MHz steps where a phase-locked YIG tuned oscillator (YTO) provides the output. A similar scheme is employed in the 5-25 GHz Cassegrain receiver at Green Bank to provide an 18-26 GHz LO. Figure 2 shows the switching times achieved with this K-band YIG tuned oscillator system. Switching

time in this case is until the lock indicator is activated, which occurs when the YTO output is within about 0.33 rad (20°) of the reference frequency. It takes only an additional few tenths of a microsecond to be within 0.05 rad. The key to ms switching times with this technique is presteering of the oscillator frequency in order to reduce the required loop pull-in-range. The main component of the switching time in Figure 2 is the needed time to change the current in the YIG tuning coil, which is an electromagnet that provides a variable magnetic bias for the YIG (yttrium, iron, garnet) sphere frequency determining element. Hyperabrupt varactor tuned oscillators are available in the 2-4 GHz range which can be presterred over a 40% frequency step to within 50 kHz of their final value in 0.1 ms (Watkins-Johnson model 2853). Thus, switching time of the microwave oscillator is not a limiting factor for the VLBA design.

The frequency translation, as indicated in Figure 1, is to be done by selecting one of a number of outputs from a 100 MHz comb generator. PIN diode switches and bandpass filters will provide μs switching time and the requisite phase repeatability and stability if environmental influences are controlled, as is done at the VLA. It should be pointed out that when phase locked the output will have a phase error equal to the sum of the errors introduced by the switched filter and 100-200 MHz synthesizer (assuming a reasonably high loop gain). Thus, the main burden for switching time and phase repeatability falls on the 100-200 MHz synthesizer. This synthesizer will have to be different in design from the one used in the MKIII video processors, as that design was not intended for frequency switched operation. However, a UHF, 10 kHz step size, phase-locked loop (PLL) frequency synthesizer should be capable of switching times on the order of 3 ms according to an article by Gorski-Popiel of MIT Lincoln Laboratory [1]. Again, presteering of the output oscillator would be required to achieve this speed. If we consider that the lower order digits would probably not have to be switched during bandwidth synthesis, then considerable improvement in the switching time could be realized with a design employing a PLL for the higher order digits and either a second PLL or a direct synthesizer for the lower order digits.

In summary, it seems feasible that the proposed VLBA IF processor LO could achieve switching times on the order of 1 ms when 10 ms would appear to meet the requirements of geodetic and astrometric observations.

Reference:

[1] Gorski-Popiel, Frequency Synthesis: Techniques and Applications", IEEE Press, 1975, pp. 71-72.

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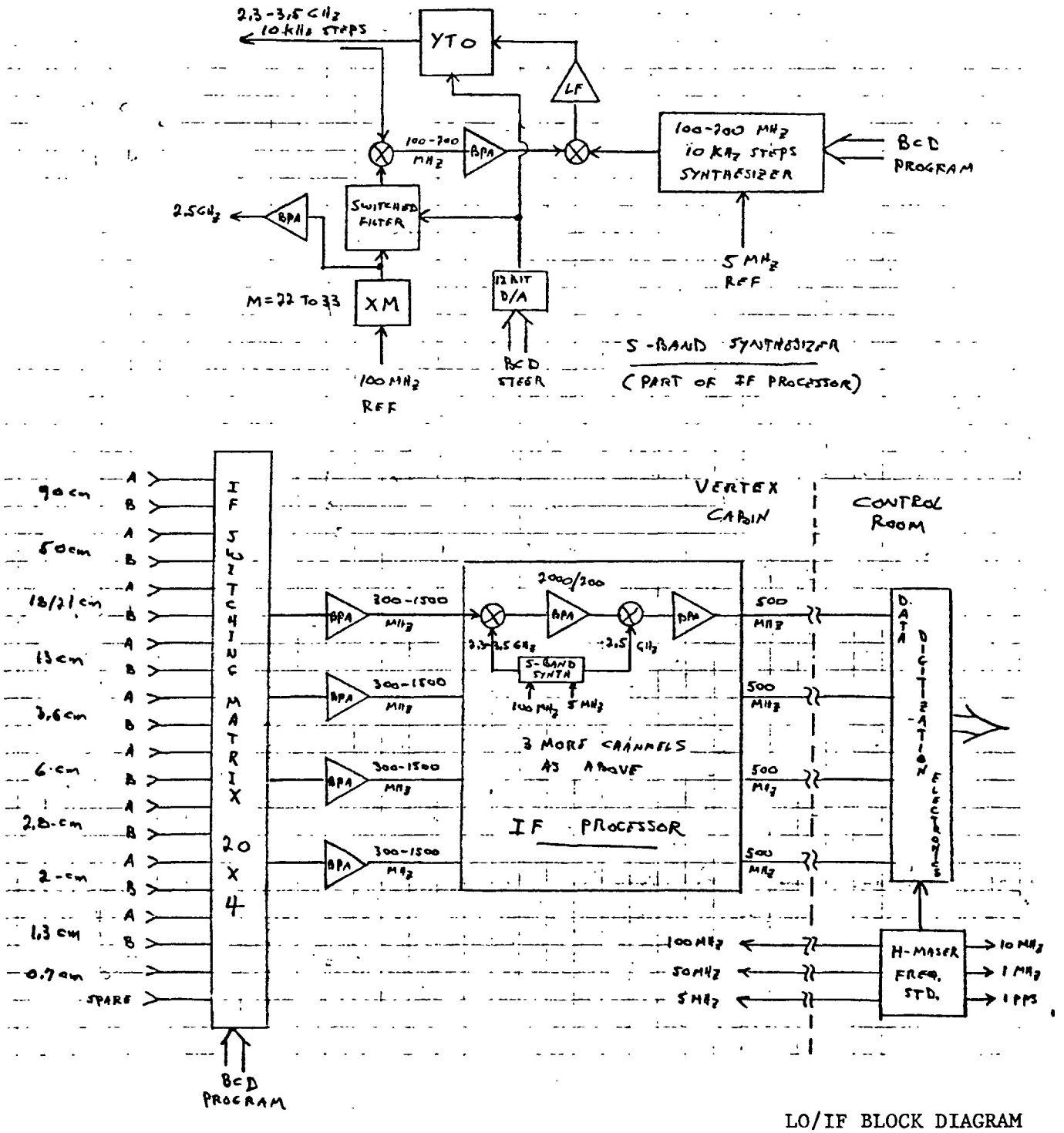
Enclosures
Figure 1: LO/IF Block Diagram, VLBA Proposal
Figure 2: Switching Time for 5-25 GHz Receiver K-Band LO



LO/IF BLOCK DIAGRAM

VLBA PROPOSAL

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FIGURE 1

LO FREQUENCY SWITCHING

ΔF ± (MHz)	T (millisec)
2	<1
28	2
56	3
112	4
560	7
1000	8
18-26 GHz	40

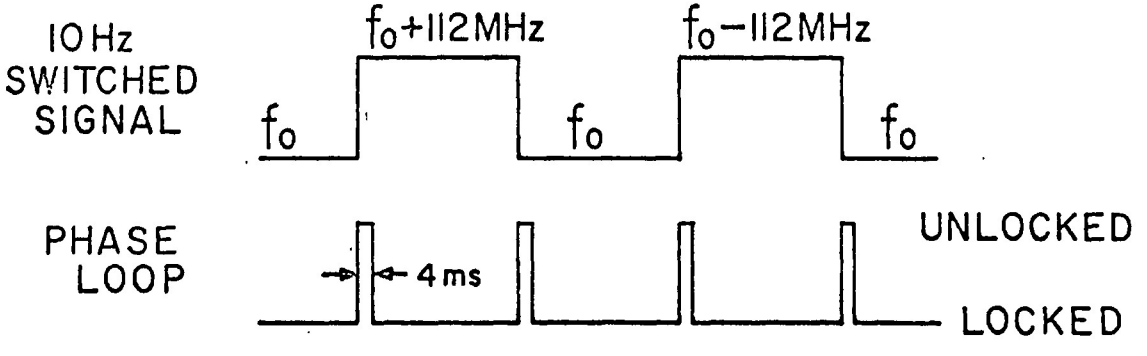

FIGURE 2: Switching time for 5-25 GHz Receiver K-Band LO.

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