VLB ARRAY MEMO No. 176

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VLBA Correlator Design Group
DRAFT CORRELATOR SPECIFICATION

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1.0 INTRODUCTION

This document presents a possible VLBA correlator design, based on the deliberations of both the VLBA Data Recording Group and the Correlator Group. It is tentative insofar as it assumes a particular data recorder interface philosophy and as it is based on the availability of a particular VLSI correlator chip. In addition, it has been necessary to make allowance for the possible inclusion of substantially more antennas (outside the U.S.) than were initially contemplated.

It is anticipated that further iterations of correlator specifications will be required. However, at this time there is a need for concrete proposals to form the basis of such refinements.

2.0 RECORD/PLAYBACK SYSTEM INTERFACE

2.1 General Considerations

VLBA Memos #164 and #170 discuss an IF "architecture" permitting up to 32 IF channels each with a bandwidth selectable from the set

(25, 16, 8, 4, 2, 1, 0.5, 0.25, 0.125 MHz).

This scheme is adopted here with a minor change. The maximum bandwidth will be taken as 32 MHz, corresponding to 64 Mb/s data rate. As will be seen below, the correlator will naturally support this rate. The 25 MHz bandwidth can easily be achieved, if desired, through slowing the system clock.

The data record/playback system will, at least initially, be unable to support the full aggregate data rate implied above: 2,048 Mb/s. In this document a maximum aggregate data rate of 256 Mb/s per telescope will be assumed. The correlator is also specified to accept this rate.

2.2 Detailed Specification

For concreteness it is assumed that the principal output of the data playback system will be 32 bit-serial lines clocked at up to 16 Mb/s. Thus an aggregate rate of 512 Mb/s is permitted. The 16 Mb/s clock rate is conveniently manageable with conventional cable (or optical) transmission methods. IF bandwidths above 8 MHz (16 Mb/s clock) are handled by transmitting the data in 2-bit smidgens or 4-bit nibbles in parallel.

The 16 Mb/s line rate is more appropriate than 8 Mb/s, which would also carry the required data, since four lines are sufficient to handle the 64 Mb/s maximum IF channel. Four is the convenient number for the bandwidth doubling scheme to be described below.

Table 1 presents the proposed IF/data recording options. Note that the mapping of frequency channels to data playback line numbers is somewhat arbitrary. It is meant to suggest a reasonable system.

Each IF mode is further divisible into two cases - polarization mode (P) and normal mode (NP). In a P mode, two streams are devoted to each frequency channel, one for each of left- and right-circular polarizations.

IF mode	Channel BW	Bit rate per chan.	No. Streams	Stream No.	Line No.	Bit rate per line
1	32 MHz (25)	64 Mb/s (50)	4	1 2 3 4	1- 4 9-12 17-20 25-28	16 Mb/s (12.5)
2	16	32	8	1 2 ... 8	1- 2 5- 6 29-30	16
3	8	16	16	1 2 ... 16	1 3 31	16
4	4	8	32	(one-to-one)		8
5	2	4	32	"		4
6	1	2	32	"		2
7	0.5	1	32	"		1
8	0.25	0.5	32	"		0.5
9	0.125	0.25	32	"		0.25

Table 1: Assumed IF/Data System/Correlator Interface

3.0 OVERALL CORRELATOR DESIGN

Figure 1 presents an overall block diagram of the VLBA correlator system. Two basic module types and various special processors form the bulk of the correlator. The Station Electronics module (SE) receives data from the playback unit for a single antenna, according to the arrangement described in Table 1. It performs the geometric delay correction (and possibly a limited deskewing of the playback clock), extracts phase calibration information, and performs other housekeeping functions, such as extracting time code or other information present in the data stream.

The SE modules are controlled by the Control / Housekeeping Processor, which also communicates with the playback system. This processor is responsible for maintaining synchronization between the playback units for the various antennas, keeping track of the "tape time," accepting tape quality information from the playback systems and the SE modules, and coordinating delay

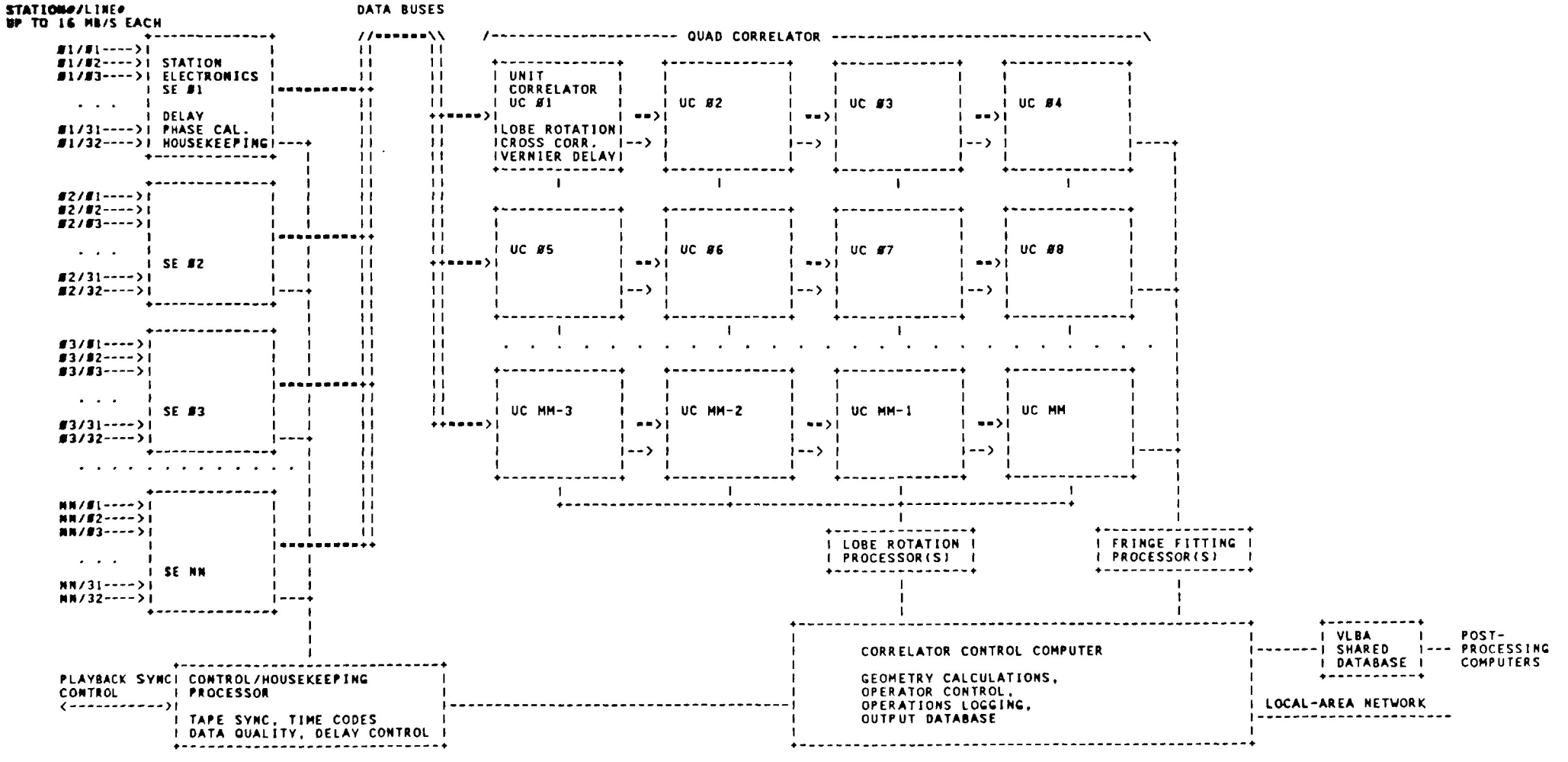


FIGURE 1. OVERALL CORRELATOR DESIGN

and phase calibration operation under the instructions of the main Correlator Control Computer.

Data buses connect the SE modules to the correlator array. The correlator is made up of Unit Correlator (UC) modules, which are capable of operating up to 32 Mb/s. UC modules are grouped into "quad correlators" for operation at 64 Mb/s. (In a distinct sense, UC modules may also be organized by fours for full polarization processing.)

UCs contain minimal lobe rotation logic, with phase adders that are controlled by a number of Lobe Rotation Processors under control of the main computer.

Output of the UCs is integrated and first steps of fringe fitting are performed in a number of Fringe Fitting Processors. In a partially reduced form, the data are fed to the main computer for final fringe fitting, calibrations, and storage in a large database which is shared with the VLBA post-processing computer system.

A Local-Area Network (LAN), such as Ethernet, connects the Correlator Control Computer with the other major processors of the VLBA operations facility. These include the post-processing computers and the operations control computer.

4.0 STATION ELECTRONICS DESIGN

The Station Electronics (SE) systems consist of 32 identical data stream processors for each antenna playback system. A typical unit is shown in Figure 2. Presumeably the data arriving from the playback unit (up to 16 MB/s per stream) is assembled into frames comparable, e.g., with the Mark III VLBI frame. It is required primarily to ensure precise time-tagging of data bits, but it also may contain time of day and other "housekeeping" information. The frame decoder provides such information for the possible use of the playback control and housekeeping processor, although in general the information from the 32 streams may be redundant.

The data playback system will have the primary responsibility for data quality determination, but the frame decoder will also be able to provide some information on data playback quality. For the correlator's use it will regenerate the serial data stream, with framing information and bad data masked out under the control of a validity data stream, in which one bit masks out a number of data bits (8, for example).

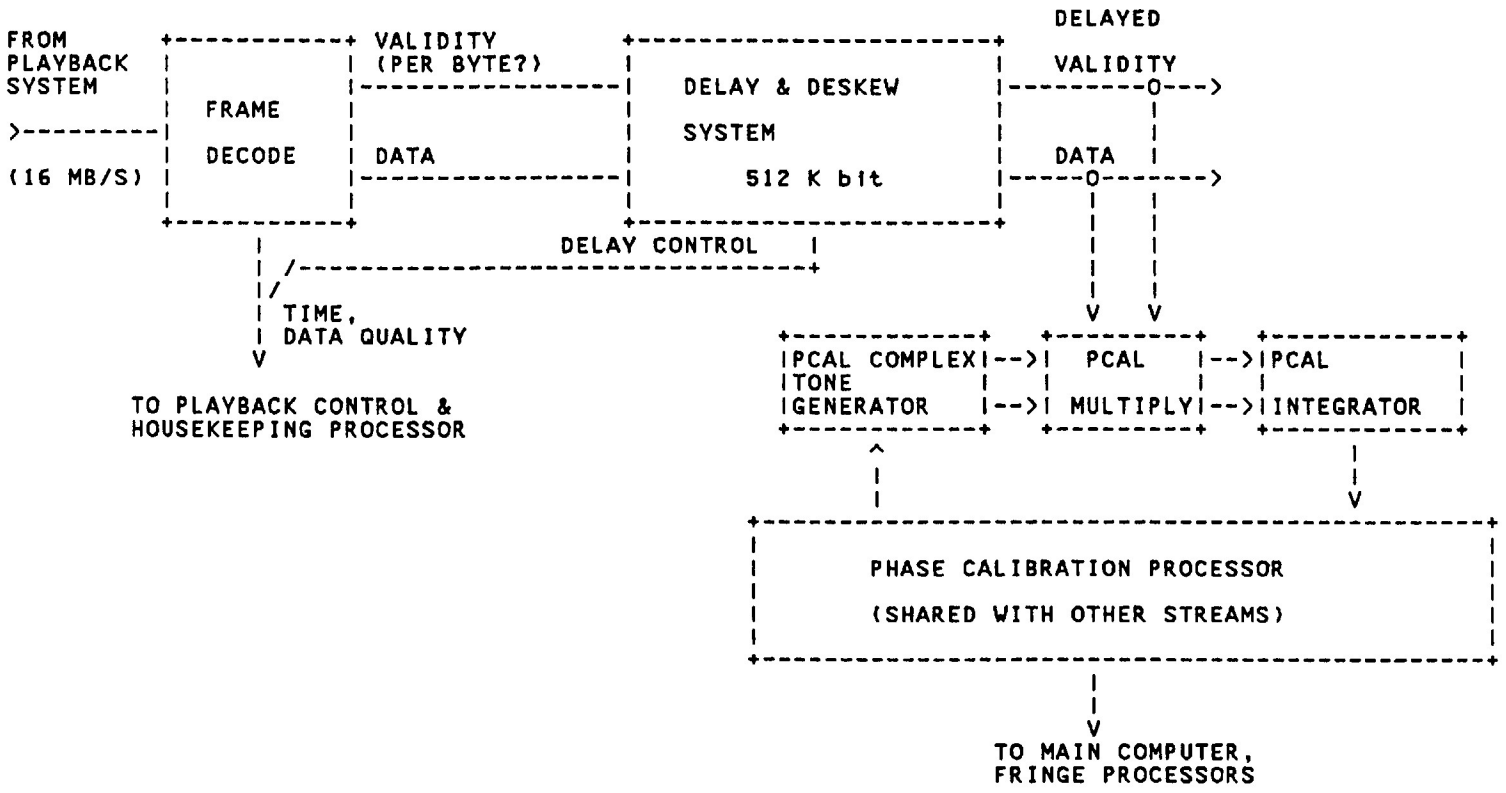


FIG. 2. STATION ELECTRONICS FOR A SINGLE DATA STREAM

A 512 K bit RAM system provides delay and deskew capability up to 32 msec per stream. A smaller RAM provides corresponding delay for validity bits.

Delayed data is detected in a phase calibration (PCAL) multiplier with a 128-level tone generator. Each IF passband will have at least one calibration tone which can be used to cross-calibrate passband phases and amplitudes. The tone may lie anywhere within the passband, and there may be more than one tone. The phase calibration detector can be multiplexed among multiple tones under control of the phase calibration processor.

5.0 CORRELATOR DESIGN

The correlator array is based on a Unit Correlator (UC) module which consists or four VLSI correlator ICs. An array of 64 UCs per baseline is proposed as offering acceptable frequency resolution (up to 2,048 frequency channels) and sufficient flexibility to accomodate enlarged antenna arrays at reduced performance.

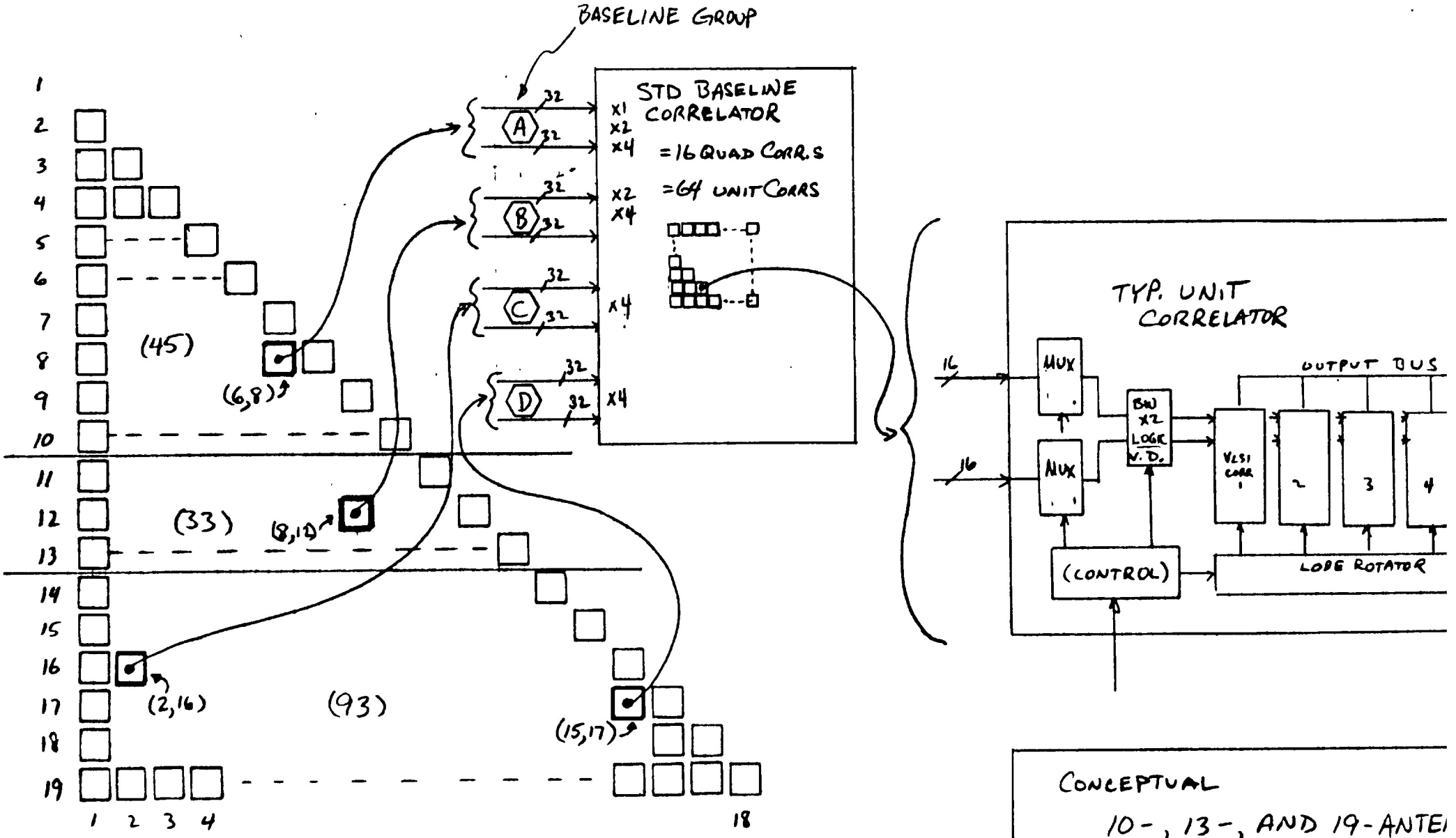
Figure 3 demonstrates the organization of the correlator array. For this example, a 10-antenna full-function system is assumed. In its "normal" mode, the correlator consists of 45 standard "baseline" correlators, all identical. Each baseline correlator consists ot 16 quad correlators, or 64 UCs.

To support larger numbers of antennas, the baseline correlator can be split in two or four segments. In the split "X2" mode, there are enough baseline correlators available to support 13 antennas. (Actually, with the addition of 1 extra baseline unit the X2 mode would support 14 antennas.) In this mode, a particular baseline accepts two input pairs corresponding to two locations in the correlator array ([6,8] and [8,12] in Fig. 3). Many, but not all, IF modes can be supported in the X2 split.

In the four-way split, "X4" mode, up to 19 antennas may be supported. In this case a particular baseline correlator must be wired to four positions in the 19-antenna correlator array.

5.1 The Unit Correlator

The UC design is based on the VLSI correlator circuit being designed by JPL. The chip is described in VLBA Memos #117 and #118 by John Peterson. It is assumed to provide complex cross correlations at 16 lags and a 16 Mb/s data rate. It will handle



19-ANTENNA BASELINE MATRIX

CONCEPTUAL

10-, 13-, AND 19-ANTE

CORRELATOR

2/5/83 MSE

FIG. 3

2- or 3-level input data, although the present correlator system is only designed for 2 levels.

The UC is designed to operate at 16 and 32 Mb/s. The "bandwidth doubling" technique is used to combine the four correlation products of "even" and "odd" bits of the two data streams. (A second stage of bandwidth doubling is used external to the UC for 64 Mb/s operation.) Four correlator ICs are required for the 32 Mb/s rate. These will deliver 32 effective lags in the 32 Mb/s mode or 64 lags at 16 Mb/s or less. The UC is summarized in Table 2.

MODE	AGGREGATE BIT RATE	BW MULT FACTOR	AVAILABLE LAGS
1	16 MB/S	X 1	64
2	32 MB/S	X 2	32

USING 4 VLSI IC CHIPS, 16 COMPLEX ACCUMULATORS, 16 MB/S CLOCK

TABLE 2. UNIT CORRELATOR MODES

As shown in Fig. 3, the UC contains input multiplexors (16-way selection is apparently sufficient), bandwidth doubling logic, and vernier delay. Since each VLSI correlator may be operating on independent data streams, independent lobe rotation must be applied. A simple linear phase adder is sufficient, with updates and higher-order corrections supplied for many phase adders by microprogrammed processors, which in turn communicate with the main control computer.

5.2 Correlator Modes

Each IF/data recording mode (Table 1) must be accomodated by corresponding correlator modes. In the correlator, the distinction between polarization (P) and non polarization (NP) submodes is significant. Certain modes also permit correlator splitting into two or more subcorrelators; this allows processing of more antennas at reduced lag coverage. The correlator modes are summarized in Table 3.

IF MODE	P/NP	IND. STREAMS	STREAM CLOCK	UC/ STREAM	NO. LAGS/BSL	ALLOWED SPLITTINGS
1	P	2	64 MB/S	32*	64	1,2
	NP	4	64	16*	256	1,2,4
2	P	4	32	16*	512	1,2,4
	NP	8	32	8*	2048	1,2,4,(8)
3	P	8	16	8	1024	1,2
	NP	16	16	4	4096	1,2,4
4	P	16	8	4	1024	1
	NP	32	8	2	4096	1,2
5	P	16	4	4	1024	1
	NP	32	4	2	4096	1,2
6	P	16	2	4	1024	1
	NP	32	2	2	4096	1,2
7	P	16	1	4	1024	1
	NP	32	1	2	4096	1,2
8	P	16	0.5	4	1024	1
	NP	32	0.5	2	4096	1,2
9	P	16	0.25	4	1024	1
	NP	32	0.25	2	4096	1,2

* UNIT CORRELATOR IN MODE 2 (32 MB/S).

TABLE 3. CORRELATOR MODES.

5.3 Numbers Of Antennas Supported

With a splittable correlator, as indicated above, how many telescopes can be accomodated starting with an N-telescope full-capability processor? Table 4 indicates the possibilities under the assumption that the numbers of telescopes under consideration range from 8 to 20.

N	N 2-split	N 4-split	No. of UCs
8	11	15	1,792
9	12	17	2,304
10	13	19	2,880
11	15	>20	3,520
12	16	>20	4,224
13	18	>20	4,992
14	19	>20	5,824
15	20	>20	6,720
16	>20	>20	7,680

Table 4. Capability of Split Processor

The penalties incurred by splitting and supporting more antennas include (1) additional SE and playback units; (2) more complex cabling and switching; (3) reductions by factors of 2 or 4 of the lags per baseline. Item (3) is minor for continuum work, since for all but full-polarization broadband work, at least 1 us delay coverage is provided.

6.0 SPECIAL PROCESSORS

Figure 1 indicates the use of special processors for delay control/tape synchronization, lobe rotation control, and fringe fitting. These functions could, in principle, be performed by a sufficiently large general-purpose computer that would also handle the general control and dataflow of the correlator. However, these functions are intensively computational and logically separable; they involve no disk or tape input/output. Thus they are good candidates for implementation as separate, specialized systems.

7.0 MAIN CORRELATOR COMPUTER

Overall control of the VLBA correlator system resides in a general-purpose computer. This computer should have the following characteristics:

1. Efficient execution of 32- and 64-bit floating-point instructions. Calculations of interferometer geometry require 64-bit capability.

2. Large address space. At least 2 MB per process is required, suggesting a 32-bit address, virtual memory system.

3. Moderate computing capability. A rating of at least 0.5 Mips is required, assuming that as much of the computing burden as possible is placed in the special-purpose processors.

4. Real-time operations. The operating system must be capable of efficient scheduling of time-critical tasks, interactive users, and batch jobs. The number of timesharing users would not be more than about six.

5. Input/Output Capability. Efficient multiport disk subsystems must be available to transfer data to the VLBA post-processing facility. Independent I/O channels should be available to support transfer of correlator output into the main computer. Support of a local-area network is needed to enable coordination with other VLBA computers.

6. Compatibility with other VLBA systems. To simplify VLBA system programming and maintenance, all major VLBA computers should be chosen from a single, compatible family, with consistent selection of peripheral devices.

8.0 DISCUSSION

8.1 Packaging

Rough estimates of "real estate" suggest that 4 or 5 moderately large (14" x 14") printed circuit boards are required for a baseline correlator. Some 16 baselines would then fit into a standard EIA rack, and 3 racks would hold a full 10-antenna correlator.

Similar estimates for the SE units give 1 to 2 racks for 20 antennas.

8.2 Costs

Only rough cost figures are available for the VLSI correlator chip (see VLBA memo #117). At the suggested $40 per chip, a UC might cost about $250 (including packaging and power). The correlators for a 10-station processor would then cost about

$$2880 \times \$250 = \$720{,}000.$$

A very rough estimate for the SE cost is $500 per stream (50 ICs at $10 each). Thus the cost of 10 antennas would be

$$10 \times 32 \times \$500 = \$160,000.$$

To this should be added $16,000 per additional antenna to be supported.

Note that, like the IF converters, SE costs scale directly with the number of streams to be supported by each antenna. The initial implementation may be restricted to a subset of the maximum number of streams, according to budget limitations.

8.3 General

This correlator is apparently the minimum design consistent with use ot the 16 Mb/s 16 lag VLSI chip and full-polarization work in the "narrowband" modes (4-9). Adequate channels are provided without recirculation.

Baseline correlators are splittable in binary fashion only. This simplifies interconnection and packaging of modules while providing reasonable capability for up to 20-antenna arrays.

Switching in the SE modules (or in the data record/playback system) permits the same signal to be fed to many correlator input streams. By staggering delays for input streams, high-resolution spectroscopy will be supported. In the "narrowband" modes (4-9) up to 2,048 frequency channels (4,096 lags) are available in a single band. Up to 16 independent bands with 128 frequency channels each may be had. (The IF channels come in USB/LSB pairs, permitting only 16 independent IF bands.)

If a factor ot two reduction in total number of lags (and frequency channels) is acceptable, the UC cost can be cut by at least 30% by a small redesign of the VLSI correlator to permit each chip to act as two independent 8-lag correlators.

Since this design calls for one lobe rotator function per unit correlator (4 VLSI correlators), it is very desireable to reduce the number ot ICs necessary for the lobe rotation. A second VLSI chip, custom-designed or gate-array, is a possiblity. Such a chip should be able to support 4 - 8 lobe rotation functions.

This correlator design may be replicated up to 7 times to handle the full 2 Gb/s potential data rate of the IF architecture. Only the correlator section needs to be copied; the SE units are adequate as they are.

8.4 Needs For Further Study

The VLSI correlator project needs careful examination to see if it is realistic to expect a useable quantity of ICs in time to meet the VLBA schedule. The VLBA project may have to make a financial and manpower commitment to support and coordinate with the JPL work.

A decision must be reached on the IF - data recording - correlator interface. In particular, is the 32 channel x "25 MHz" scheme acceptable?

Board level designs and interconnection schemes must be attempted to define the correlator cost estimates to the 10% level.