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To: VLBA Design Group
From: Martin Ewing
Subject: Miscellaneous Correlator Issues

1.0 NUMBER OF CHANNELS.

If the requirement of Memo #127 is definite, then 184,320 correlator lags (i.e., complex accumulators) are required for the correlator. In terms of the JPL "CCS" chip (Memo #117), this is 11,520 ICs, estimated to cost about $500K.

An estimated 30-40% of the correlator electronics cost could be saved by reducing the number of lags by a factor of two. Full continuum capability would be preserved, but two processing passes would be required for the "large" spectral line experiments.

2.0 MULTI-LEVEL SAMPLING.

Although not emphasized in memo #176, "Correlator 176" would easily support 3-level sampling. The JPL VLSI chip already has 3-level capability (+1, 0, -1 states). There is no significant penalty in carrying two bits per sample through the remainder of the correlator system, as long as the clock rate per stream does not exceed 8 Mb/s.

Multiplication on the chip is performed through programmed logic arrays (PLAs). It is quite conceivable to allow various quantization rules to be programmed externally. In particular, 4-level (+2, +1, -1, -2) arithmetic should be possible. Four-level operation has significant advantages in selecting IF filter widths, particularly if 2-level sampling must also be supported.

3.0 OVERSAMPLING.

Present designs for the VLSI chip include extra delay flip-flops between correlator stages to handle data that is oversampled by a factor of two. This capability does not appear to cost very much. In fact it has been suggested to include higher orders of oversampling, such as 2X, 4X, and 8X.

4.0 VLBA SPECIAL NEEDS FOR THE VLSI DESIGN.

Certain aspects of the correlator chip design are of special interest for the VLBA project. The following should be considered for possible changes to the design of memo #117.

1. Oversampling. For 2X oversampling, it is desirable to have a 2-bit delay between correlator stages. Selectable 2X, 4X, and 8X oversampling is desirable also.

2. Multilevel sampling. 3 x 3 level sampling is certainly desired, and 4 x 4 levels could be used. Memo #117 includes 3 x 3, but not 4 x 4.

3. Divisibility. In those cases (like the VLBA) in which correlators must be combined for "bandwidth multiplication," it will be helpful to have a chip mode providing dual 8-lag correlators. On-chip signal multiplexors should provide selectable 8- or 16-lag modes. If there are opportunities to provide additional gating to support bandwidth multiplication on the same chip, these should be considered also.

   Some consideration might be given to a quadruple 4-lag mode which could implement all bandwidth doubling signal routing on one chip. (Two or more chips would provide the desired number of lags.)

4. Packaging. For large systems implemented on printed circuit cards it is very desireable to use leadless chip carrier packaging, which requires only about 1/3 the board area of conventional DIP packaging.

5. Speed-power tradeoffs. If the correlator chip has speed capability significantly higher than 16 Mb/s, but not close to 32 Mb/s, it may be desireable to modify the chip for 16 Mb/s operation and lower power dissipation. Power dissipation will be a significant problem in the large VLBA system.