MONITOR AND CONTROL BUS SPECIFICATION

L. R. D'Addario, B. G. Clark, D. Weber, and K. Sowinski
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Attached is a preliminary version of the specification for the signaling scheme which will be used to transmit control information from the station computer to the equipment at each station, and to collect monitor information from the equipment. Designers of equipment which must communicate with the station computer are urged to study this specification and communicate comments to the authors. We plan to finalize the specification shortly after the design review meeting now scheduled for January 31-February 1, 1984.

In order to ease the task of most device designers and to avoid unnecssary duplication, we will develop and make available a "standard interface" to the bus. A detailed description of the standard interface will be given in a separate specification; this is in preparation and will be issued in preliminary form shortly. Meanwhile, a brief description is included in the attached bus specification.

Monitor and Control Bus at Each VLBA Station

- Preliminary Specification -
83/12/20

GENERAL DESCRIPTION

This specification describes the characteristics of a serial digital data bus for controlling and monitoring all equipment at a station in the VLBA. To avoid possible confusion, some terms will be defined here. A CONTROLLER is considered to be the station computer and its interface to the bus. A MONITOR AND CONTROL INTERFACE, or simply INTERFACE, is something that connects a piece of equipment in a station to the bus. A DEVICE is such a piece of equipment; e.g., a front end or a local oscillator module might be a device.

The bus will consist of two logic signals, each on a shielded twisted pair, wired as a multi-drop party line. The signals are called Transmit Data (XMT) and Receive Data (RCV). There will be one Controller and numerous Interfaces connected to the bus. The Controller will be the only source of Transmit Data, and the Interfaces (one at a time) will be the only sources of Receive Data. Data will be bit-serial at a rate of 56 kbaud and the transmissions will be byte asynchronous, each byte consisting of 8 data bits, one parity bit (odd) and start and stop bits.

Detailed specifications of bus line characteristics, levels, timing tolerances, routing and other conventions are stated below. Unless otherwise specified, EIA standard RS-422 and EIA PN 1360 will be followed.

MESSAGE FORMAT AND SEMANTICS

Every message on the XMT line will be exactly five bytes long, with the bytes called SYNC, Address High (ADH), Address Low (ADL), Control Data High (CDH) and Control Data Low (CDL). The SYNC byte is a fixed code to indicate the beginning of a message and shall have even parity to distinguish it from ordinary data. If the most significant bit of ADH is 1, then the message is a control message; otherwise it is a monitor request message. The remaining 15 bits of ADH/ADL form a binary address in the range 0 through 32767.

Messages on the RCV line will be either one byte acknowledgements or three byte monitor data responses, as discussed below.

BUS PROTOCOLS

Each Interface must receive ADH and ADL of every message on the XMT line (that is, there must be no dead time during which an interface is not listening). Each Interface is assigned a block of contiguous addresses to which it alone responds. The block may be of any length, but it must be disjoint with the address blocks of all other Interfaces. The last few addresses of each block are dedicated to functions occuring within the Interface, as specified below.

If the address transmitted was within the assigned block of an Interface, then within 100 microseconds of the end of the last bit of ADL, that Interface must begin to transmit a one-byte acknowledge code on the RCV line. If the message was a control message, then the Interface must also receive and store CDH and CDL, and within 100 microseconds of the end of CDL it must begin to transmit a second acknowledge byte on RCV. The codes for acknowledge bytes are defined below. If the message was a monitor request, the (single) acknowledge byte must be followed immediately by two bytes of monitor data obtained from the address specified by ADH/ADL. (Thus, the time available to acquire the monitor data is 100 microseconds plus the time for transmission of one byte.)

The Interface must check parity on all bytes received. If SYNC, ADH or ADL has a parity error, the Interface shall not respond (just as if the address were outside its block), but shall increment an internal counter and look for the next valid SYNC. If SYNC, ADH and ADL have valid parity and a control message is specified, but CDH or CDL has a parity error, then the second acknowledge byte must be replaced by a negative-acknowledge code (NAK), CDH/CDL must not be passed to other equipment and a second parity error counter shall be incremented. The values of both these counters shall be assigned to monitor addresses.

The Controller may begin transmitting another message as soon as all acknowledge bytes have been received. For control messages, this means the second acknowledge byte. For monitor requests, a new message may be started immediately after the single acknowledge byte, without waiting for the two monitor data bytes. The maximum-speed timing for a sequence of control messages and for a sequence of monitor requests is illustrated in Figure 1.

The Controller must also check parity on all bytes received on the RCV line. If an acknowledge byte has incorrect parity or an incorrect code, the Controller may note that there is a possible problem, and may take remedial action, but no particular action is specified. If no response is received within 200 microseconds, then the Controller may again note a possible problem, and proceed to transmit the next message. If a parity error is detected on a monitor data byte, then both bytes of the monitor word shall be ignored.

BUS SIGNAL CHARACTERISTICS AND CONVENTIONS

It is expected that more than 32 Interfaces will be required at a station. In that case, the bus will be split into several lines with up to 32 drivers and/or receivers per line. Thus a RCV line would have up to 32 drivers and one receiver (the Controller), and a XMT line would have one driver (the Controller) and up to 32 receivers. At the Controller, each line shall have its own transmitter or receiver. Control messages shall be broadcast on all XMT lines; there shall not be any line selection based upon the presence of the addressed Interface on any given line.

These conventions shall be followed:

Transmission rate: 56 kbaud, including all framing and parity bits;

Transmission lines: #24 twisted pair, shielded (roughly 100 ohms characteristic impedance), max length 500 feet, terminated with a 100 ohm resistor;

Drivers and receivers shall be bridged across lines with stubs less than 20 feet;

RCV drivers shall be tri-state, connected to the bus only when required to respond to a monitor request.

Line HV safety:

Clipping surge arrestors shall be used on the bus lines between the control building and the antenna. The surge arrestors shall be located at each end of the bus run and shall shunt the surge currents to a suitable ground.

Interfaces which service equipment subject to lightning-induced currents shall be protected by high voltage isolators such as optical isolators. The isolators shall be interposed in the lines between the Interface and the Device. Examples of such Devices are the subreflector drive and the weather instruments.

Bus signals shall conform to EIA RS-422 and EIA PN 1360; particular attention is called to the following items:

Mode - Differential transmission and reception, ± 2 to ± 6 volt signal range.

Drivers and receivers capable of operating in the presence of Common mode voltages over the range of -7 to +12 volts.

No device damage due to line contention of two drivers.

Max driver output current, hi Z state - ± 100 uA.

Max driver output current, power off - ± 100 uA.

Receiver input sensitivity - ± 200 mV, min.*

Receiver input resistance - 12 kohms, min.

Driver output signal - ± 1.5 V min. into a 54 ohm load.

No device damage due to loss of power on one or more drivers or receivers.

*(On the RCV line, which has numerous tri-state drivers, it may be necessary to use a larger receiver threshold to ensure that the receiver can detect the state in which all drivers are inactive, and do so even in the presence of noise. There are several ways of doing this, including biasing the RCV line and adding an extra line to the bus, and the actual method has not yet been chosen. The final version of this specification will include a description of the actual method. Device designers should be aware that this might affect the requirements for the Interface drivers.)

STANDARD CODES

The defined hexadecimal codes for special characters are given below. The SYNC byte will be transmitted in even parity, so that it is a truly unique byte that will never be encountered in data.

SYNC	16
ACK	06
NAK	15

ADDRESS AND DATA CONVENTIONS

The last sixteen monitor addresses of an Interface's block are reserved for internal functions of the interface; all Interfaces must report the following information when a monitor request with one of these addresses is received:

Address	Value
BE-15 thru BE-10	(reserved for future use)
BE-9	Address of last control message received
BE-8	Control data for last control message received
BE-7	Address parity error counter, all messages
BE-6	Control data parity error counter, all messages
BE-5	Invalid SYNC character counter
BE-4	Control data parity error counter, messages in block
BE-3	(reserved for special use by standard interface)

BE-2 Count of correctly received control messages
BE-1 Count of correctly received monitor data requests
BE-0 Address of beginning of block

where BE is the Block End address. When a control message is received with an address of one of the counters, that counter shall be loaded with the control data (normally zero, to reset the counter).

It is strongly recommended that each device devote at least one monitor address to identification information. This should include information about the revision level of the device, especially if it affects the required control word formats or the meaning of monitor data. The designer must decide at what level of complexity to specify this information (e.g., circuit board, module, subsystem). It is recognized that a subsystem may use more than one interface, and that an interface may service two or more logically separate devices.

It is also strongly recommended that logically distinct functions not be mixed within a single control word, even if this means that only a few bits of each word are used.

When a monitor word is used to convey status information, the syntax for "normal" status should include at least one bit set to logical 1 and at least one bit set to logical 0. This avoids having certain failure states (where all bits appear the same) interpreted as "normal."

It is recommended that each address used by a device for control messages have a corresponding monitor address (preferably the same address) on which the last control data received may be read back. It is also helpful if monitor data which represents the state of a device has a format similar to that of the control data which sets its state (i.e., corresponding bits should have the same meaning). It is strongly suggested that distinct addresses be used for monitor and control functions, except for the read back function mentioned above.

STANDARD INTERFACE TO EQUIPMENT

A standard interface which satisfies the requirements of this specification will be specified in a separate document, and an implementation of the standard interface will be made available to all device designers. It is intended that the standard interface will meet the needs of most devices, and its use wherever possible is encouraged. However, device designers may develop their own interfaces provided that they conform to the present specification.

The following is a summary of the characteristics of a standard interface; please see the separate specification for

details. The interface is basically a serial-to-parallel and parallel-to-serial converter, where the serial side is the bus and the parallel side connects to the device. The device connections will consist of: (1) the relative address of messages which fall within the interface's assigned block (difference between the actual address and the beginning of the block); (2) a control data word with the most recently received control message in the block; (3) input for a monitor data word; (4) appropriate handshaking lines; (5) optionally, 8 differential analog inputs for -10 V to +10 V signals. If installed, the analog interface will automatically convert the 8 signals to 12-bit twos-complement representations and assign these numbers to the first 8 addresses in the block; conversion will take place when a monitor data request for the corresponding address is received. (The control data and monitor data words might be multiplexed onto the same lines; see the specification.)

The implementation of the standard interface will include a microcomputer and appropriate firmware in PROM. Detailed documentation on the hardware and firmware will be made available to device designers. It will be possible for designers to use this microcomputer to add small amounts of computing ability to their devices, if they provide their own firmware. The interfacing functions of the standard firmware will be organized into subroutines in such a way that the special firmware need only replace a relatively short main program.

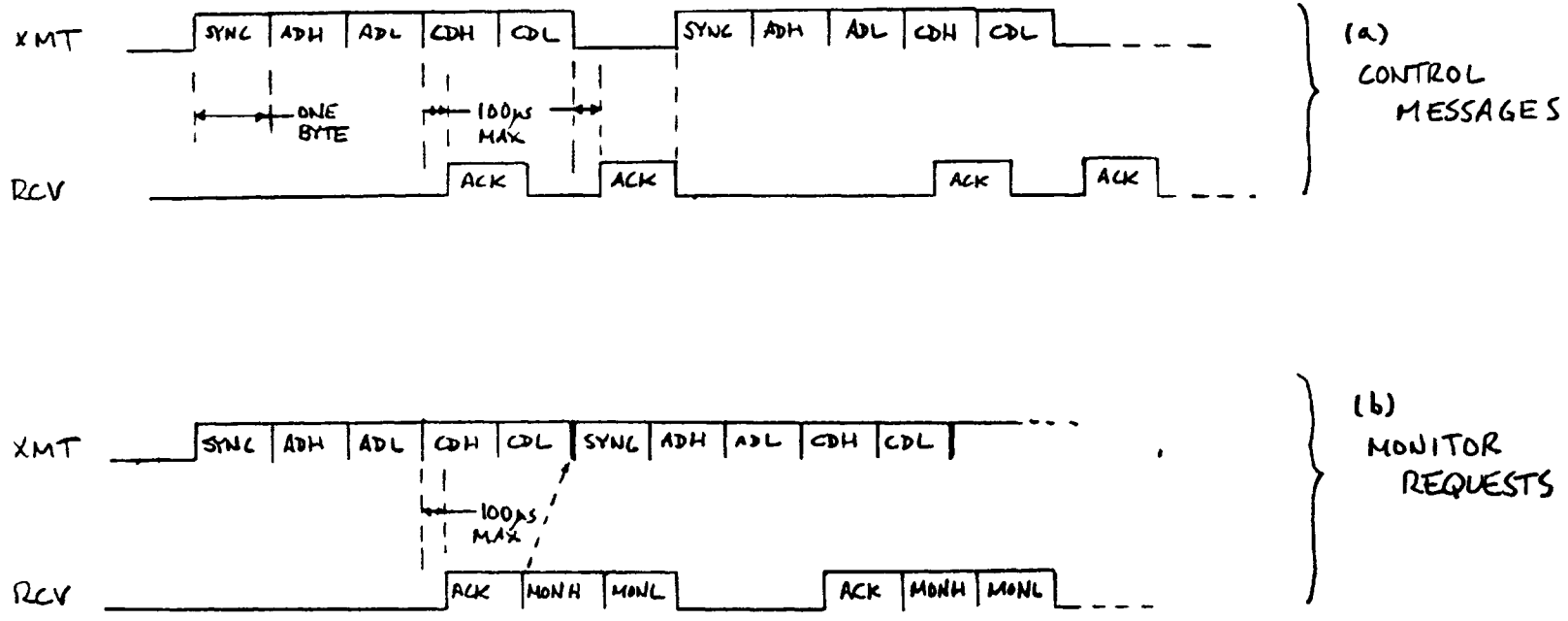

Figure 1: Timing for maximum transmission rate in case of (a) sequence of control messages; and (b) sequence of monitor requests.