VLB ARRAY MEMO No. 329

To: M. Ewing

From: B. Clark

Subj: Lobe rotator at the antenna

Date: 84feb24

It seems to me that the burden of Alan's remarks at the correlator meeting the other day were that simply displacing the maser to the center of the earth takes care of a lot of problems that otherwise need to be worried about in detail. On the other hand, it makes me extremely nervous to talk about fiddling with the master oscillator and clock; I think we should instead do a bit of detailed worrying. The system can, and should, be made to look as if the maser were transported to the center of the earth, without actually fiddling with its precious hardware.

I did not understand the argument about phase referencing at all. However, it is my impression that, if a fourier transform into the frequency domain is done rapidly compared to the time taken for a bit time change in the relative delay of the two sources, the problem reduces to that of estimating the complex part by Hilbert transform, which is suggested to be harmless.

If we do not fiddle the maser, each IF channel must have a separate lobe rotator. The most convenient place to put them is in the IF of the final synthesizer for the baseband LO. I suggest that the most economical way to do it is to have a synthesizer for this signal consisting of a D/A converter, a ROM lookup table of a sine wave (256*6 bits would do fine), a phase register (8 bits is needed), a phase increment register, and an adder, the whole to run with a 2 MHz clock. Among the things I do not off hand know: will the synthesizer be happy with a 5-15 kHz comparison frequency instead of a 10 kHz tone? Will there be an unpleasant phase step when we switch a 20 kHz harmonic (can happen up to six times in a track at 43 GHz)? In any event, it sounds to me like about a dozen chips per channel, so we are probably talking about a total cost somewhere near the $50-$100 K range, much less than the money for a double correlator (but not counting extra costs in the synthesizers).

The main complication of the delay tracking samplers (resynchronizing to a standard clock, if desirable, only costs a couple of chips at most) is to make sure that the sampler delay changes from 0.F (hexadecimal) to 0.0 at the same time the correlator changes its delay from n to n+1 bits. There are four possible approaches.
1) The station makes careful notes of these times, transmits them to the array control computer, which organizes them for the correlator computer, which distributes them to the delay line controlers. In the worse case, bit changes occur at 300 times a second (double bandwidth mode). Even if we employ an efficient code, this requires at least 5 kBaud of bandwidth, station to central, which I find unacceptable.
2) The world model of each station is carefully recorded and sent to the correlator computer, which calculates when the station must have inserted the bits. This seems too fraught with possibilities of software errors for me to find it acceptable.
3) The delay line settings can be recorded on the IF tapes in the auxiliary data portion. The delay controler at the correlator would

then simply add this number to a station clock constant (or near constant) and use it directly to control the delayline. I am not overjoyed with this concept because of the error rate one is likely to encounter in the aux data and the necessity to interface the aux data promptly into the delay controlers, but it seems to me the best of the choices. 4). We can record an earth center clock instead of (as well as?) the station clock. This has the further interesting property that no delaylines are needed at the correlator other than those required to remove the fluctuation of tape mechanical motion (this at the usual cost of being unable to switch delays rapidly for a "four antenna" experiment, because of the inability of the playback recorder to follow the clock glitch introduced at record time). The earth center clock would be set up from the master clock at beginning of observation and thereafter simply run by counting down the (variable phase) sampler clock.

My attitude is one of cautious optimism about the lobe rotator. Elimination of half of the lags, the lobe rotators, the vernier bit and the controls therefor seem to me likely to result in greater cost savings in the correlator than the increased costs in the IF processor. There is, clearly, not a million dollars to be found, but perhaps well over a hundred thousand.