VLB ARRAY MEMO No. 368

VLBA M&C STANDARD INTERFACE SPECIFICATION

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Attached is a preliminary version of the specification for the VLBA Standard Interface which is a general-purpose control interface that interacts with the Monitor and Control Bus (described in VLB ARRAY MEMO No 302) to execute control commands and gather monitor data.

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GENERAL DESCRIPTION

This specification describes the characteristics of the Standard Interface between the VLBA serial digital command/data bus and the devices to be controlled. This document is intended to be a companion to the Monitor and Control Bus Specification, VLBA MEMO No 302.

STANDARD INTERFACE TO EQUIPMENT

In order to keep the interfaces between the VLBA Monitor and Control Bus and the various controlled devices as similar as possible, a Standard Interface described in this specification shall be used whenever possible. The Standard Interface is essentially a microcomputer based serial to parallel converter which connects on one side to the two bus signals and on the other side to specialized equipment, (referred to as devices in this specification). A block diagram of the Standard Interface is shown in Figure 1.

The interface will be availabale in two versions, discussed below, depending on which analog multiplexer is used.

INTERFACE LINES

The connections on the serial side were described in the earlier document: VLB ARRAY MEMO No 302. The complete set of serial, parallel and power connections are:

Parallel Control Signals (Connector P1):

INTERFACE CONTROL I/O

Address	(ADDR-x)*	8 lines	out
Read/not Write	(R/-W)	1 line	out
Control/Monitor Data	(CON/MON-n)#	16 lines	out/in
Device Request	(DEV REQ)	1 line	out
Device Acknowledge	(DEV ACK)	1 line	in
Analog Signals	(ANLG-yz)**	8 pairs	in
External Analog Mux Enable	(ANENB)	1 line	in
Hi/Lo Select	(HI/LO SEL)	1 line	in

POWER

+/- 15 Common	(HIQ GND)	1 line	in
+15 Volts	(+15V)	1 line	in
-15 Volts	(-15V)	1 line	in
+5 Volts	(+5V)	1 line	in
5 Volt Common	(5V COMM)	1 line	in

* x denotes address lines 0,1,2,....7, bit 7 is msb
# n denotes bits 0,1,2.....15, bit 15 is msb
** y denotes signal 0,1,2,3.....7, z denotes H (hi) and L(lo) signal polarity
In the "S" version the ANLG-yL signals are connected together and to signal ground on the interface board.
CON/MON are bi-directional tri-state lines used for command and monitor data arguement transfer.

Serial BUS Signals, Activity Indicators and Redundant Power (Connector P2):

BUS SIGNALS

Transmit Data	(XMT- +/-)	1 pair	in
Receive Data	(RCV- +/-)	1 pair	out

ACTIVITY INDICATORS

XMT Line Active	(XACT)	1 line	out
Message Active	(MSG)	1 line	out
Interface Active	(BUSY)	1 line	out
Data Output	(DOUT)	1 line	out
XMT Parity	(PARX)	1 line	out

REDUNDANT POWER

+-15 common	(HIQ GND)	1 line	in
+15 Volts	(+15V)	1 line	in
-15 Volts	(-15V)	1 line	in
+5 Volts	(+5V)	1 line	in
5 volt common	(5V COM)	1 line	in

Power demand is: 5v - 1200 ma; +15 - 50 ma; -15 - 75 ma.

Redundant power is made available on P2 to enable the Standard Interface to operate with P1 disconnected.

Details of the signals level, drive, loading, timing etc are described below.

P1 and P2 are "D" series connectors, details of connector type and pin assignment are described below.

STANDARD INTERFACE OPERATION

Upon receipt of a message on the XMT line with a valid address in the defined block, the difference between the address and the first address of the block, the Relative Address (RA), is placed on ADDR. If a monitor request was received, R/-W is set true; if a control message, then R/-W is set false and CON/MON is set to CDH/CDL. When all output lines have been set, DEV REQ is set true. The device must now respond. For a control message, it must accept the data on the CON/MON lines and route it as specified by ADDR. In the case of a monitor request for digital data, it must place the data from the device specified by ADDR on the CON/MON lines. In either case, when it is ready it must set DEV ACK true. When DEV ACK becomes true, the Control Interface will latch the data from the CON/MON lines (if appropriate) and then set DEV REQ to false. In the case of a monitor request for analog data, the device shall respond with ANENB instead of DEV ACK. The state of the output lines is described below.

The time available for the device to respond is variable up to certain time-out limits as follows:

For control messages, the value on CON/MON will be held until DEV ACK is either set by the device or a 500 microsecond time-out occurs. In the event that this time-out occurs, DEV REQ will be set to false and the CON/MON lines shall revert to tri-state disconnect. In cases where the response time of the commanded device exceeds 500 microseconds, the attainment of the commanded state shall be confirmable via Monitor Data readout. The Response Time for this class of slow response devices is not specified. For details on the command timing relationships and the conventions to be followed for these slow response cases, see the Command Timing specifications below.

Monitor data must be available within 500 microseconds from the time that DEV REQ goes true. If RA designates an analog data address, ANENB must be set true by the device logic within 5 microseconds from the time DEV REQ goes true. The Standard Interface provides about 400 microseconds analog multiplexer settling time before the analog signal is sampled for A/D conversion; the conversion operation is completed by about 460 microseconds. In the event that RA designates digital monitor data, the device must respond with a DEV ACK signal within 500 microseconds. If the device fails to respond in these times, the Standard Interface will set DEV REQ to false and will transmit the monitor bytes with incorrect parity and all data bits set to zero.

The device must not attempt to set Dev Ack if Dev Req is false. For details on the monitor data timing relationships, see the Monitor Data Timing specifications below.

The 8-bit RA capacity and R/-W line enable the Standard Interface to service a device having up to 256 command addresses and gather up to 256 monitor data samples. Up to 64 of these monitor data samples may be analog data.

The contents of the interface control program prom shall define the lower and upper Block Addresses, and contain the Control Interface Serial Number and Revision Level. The Control Interface Serial Number and Revision Level shall be be capable of being read out as monitor data words.

The Standard Control Interface shall be implemented on a 6 1/4 by 5 1/2 inch pc board(including connectors). For details on the physical package and pin assignments see the Physical Description section.

EXTERNAL ACTIVITY INDICATORS

Five time-stretched LED drive lines shall be provided for front panel indication of interface activity. These lines shall be capable of sinking 8ma. These lines indicate:

1) XACT - XMT line is active, i.e. signal transitions are present on the XMT line, (in conjunction with 2) this permits detection of garbled messages on the XMT line).

2) MSG - Message active, i.e. valid messages are being detected on the XMT line.

3) BUSY- The interface has detected a command or monitor data request within its RA block.

4) DOUT - The interface is transmitting monitor data on the RCV line.

5) PARX - Command or monitor data request messages on the XMT line are parity error-tainted.

DIGITAL SIGNAL DRIVE/LOAD SPECIFICATIONS:

Signal sense & levels - positive true, all lines

Logic outputs - +2.7 volts min = logic 1
+0.7 volts max = logic 0

Logic inputs - +2.0 volts min = logic 1
+0.7 volts max = logic 0

Signal drive/loading -
All outputs shall be capable of driving 20 standard 74LS loads.
All inputs shall present no more than 1 standard 74LS load.

Tri-state (disconnect) output current - +-20ua

Quiescent (between message states*)
ADDR - static at most recent message RA state
CON/MON - Tri-state
R/-W - logic 0 (write state)
DEV REQ - logic 0
DEV ACK - must be logic 0

* Quiescent state ends as much as 140 microseconds before DEV REQ is set.

ANALOG DATA CAPABILITIES

The Standard Interface has an optional 12 bit analog to digital converter and 8 channel analog multiplexer. In applications where this feature is used, the lower portion of the RA space is reserved for this analog data.

Analog data signals connected to any of these 8 inputs shall be multiplexed, sampled and converted if the RA designated by a monitor data request falls in the RA space reserved for analog data. The RA conventions for analog data are described below.

In the event that the Interface is not used to gather analog data, the A/D Converter and Multiplexer need not be installed and the Analog Enable (ANENB) to the Interface shall be logic 0, (logic ground). In this case, RA for digital monitor data shall begin at 0 and range to the value appropriate for the application.

The A/D quantization shall be 5mv/bit, 2's complement format and the analog signal range is +10 to -10 volts. Data will be returned on the serial bus left justified in the 16 bit Monitor Data word.

In the event that more than 8 analog data signals need to be multiplexed and converted, remote multiplexers in the device may be connected to the board analog inputs to multiplex up to 64 analog channels. These external multiplexers may be arranged in any convenient configuration within the constraints of compatibility with the on-board 1-of-8 multiplexer. Eight channel multiplexers are recommended but for example, two 4-channel multiplexers connected as an 8-channel unit or one 16 channel unit connected to two ANLG inputs may be used. These external multiplexers shall be controlled by the ADDR lines provided by the Interface and shall be structured such that the RA address space starts at 0 and is continuous up to the highest analog RA used by the particular application.

The first (8 channel) external multiplexer shall be connected to ANLG-1. If more analog multiplexing is required, the second shall be connected to ANLG-2 and additional multiplexers may be added in this ascending sequence as required. The table below details these connections.

When analog data is multiplexed by an external multiplexer, the lower order RA bits shall control channel selection in these external multiplexers and the higher order RA bits control the the selection of these external multiplexers via the on-board multiplexer.

Two logic terms associated with analog multiplexing shall be fed back to the interface from the device logic. These are: ANENB and HI/LO SEL. HI/LO SEL is used by the interface to select either the lowest 3 RA bits (RA:0,1,2) or the next 3 higher bits (RA:3,4,5) for control of the on-board multiplexer. These multiplexer control terms are switched as a function of the current analog RA so that the remaining on-board (i.e. those not connected to external multiplexers) multiplexer inputs can be used in conjunction with the external multiplexers. If only the on-board multiplexer is used the HI/LO SEL line shall be grounded. The ANENB signal must be a logic product of R/-W, DEV REQ and the inclusive decode of RA over the address space dedicated to analog data. If external analog multiplexers are used the HI/LO SEL and ANENB signals shall conform to the following rules:

EXT MUX	CONNECT TO:	HI/LO SEL*	ANENB DECODE*	MUX CAPACITY
NONE	------	ALWAYS LOW	0 -< RA -<7	8 CHANNELS
1st	ANLG-1	10 -< RA -< 17	0 -< RA -<17	15 CHANNELS
2ND	ANLG-2	10 -< RA -< 27	0 -< RA -<27	22 CHANNELS
3RD	ANLG-3	10 -< RA -< 37	0 -< RA -<37	29 CHANNELS
4TH	ANLG-4	10 -< RA -< 47	0 -< RA -<47	36 CHANNELS
5TH	ANLG-5	10 -< RA -< 57	0 -< RA -<57	43 CHANNELS
6TH	ANLG-6	10 -< RA -< 67	0 -< RA -<67	50 CHANNELS
7TH	ANLG-7	10 -< RA -< 77	0 -< RA -<77	57 CHANNELS
8TH	ANLG-0	ALWAYS HIGH	0 -< RA -<77	64 CHANNELS

* Addresses in octal code, high true

The reason that the channel capacity does not increase in groups of 8 is a consequence of the use of the on-board multiplexer in conjunction with the external multiplexers. For example: if an 8-channel multiplexer is connected to the ANLG-1 input, the remaining 7 on-board analog inputs (ANLG-0, ANLG-2 through ANLG-7) may be used. Thus a multiplexing capacity of 15 channels is realized by the addition of just one 8-channel multiplexer. If a second 8 channel multiplexer is connected to ANLG-2, the remaining 6 on-board analog inputs may be used which provides a multiplexing capacity of 22 channels. The table above indicates the resultant channel capacity for all cases.

In the event that the Monitor Data request was for analog data, the device shall not set DEV ACK true.

For settling time considerations, tandem connections of external multiplexers beyond this one tier are not recommended. The external multiplexers shall be settled to within 0.02% by 450us after the RA states are set. External multiplexers shall have break-before-make switching characteristics.

The character of the data being gathered (ie analog data via internal or external multiplexers-A/D versus digital data on the CON/MON lines) shall be transparent to the Control Interface in that the control firmware shall not depend upon whether the data was input via the A/D or via CON/MON.

Details on interfacing to typical controlled devices will be presented in a "Standard Interface User's Guide" which will be available soon.

A/D VERSIONS

Two versions of the Standard Interface are available which differ only in the type of analog multiplexer used. These are:

VERSION S - which uses a low-cost, single-ended 8 channel multiplexer - A/D Converter. This version is recommended for applications in which common-mode noise effects are minimal. An example of this application is installation of the Standard Interface board in a module in which all analog data is generated within the module. A typical example might be an IF Processor module. Version S signal characteristics are described below.

VERSION D - which uses a differential 8 channel analog multiplexer - A/D Converter for applications where common-mode noise is more likely to be a problem. Examples of this application are cases in which analog signals to be sampled and converted originate from sources with ground references different from the Interface ground reference or situations in which signals are noise-contaminated by cable or wire runs. An example might be a Front End control module monitoring voltages within the Dewar, a nearby amplifier etc. Version D signal characteristics are described below.

Both versions have identical signal/power pin assignments. See the Physical Description section for details.

VERSION S SPECIFICATIONS:

Analog data acquisition chips: Hybrid Systems Inc. HS 9412 Data Acquisition System

1) 8 input signals, single-ended, max signal voltage:
   -11 volts < Vin < +11 volts. Analog signals shall not exceed these bounds or inter-channel cross-talk may occur.

2) Conversion signal range: -10.240 volts to +10.235 volts

3) Input bias current - +- 30 na max per channel

4) Input Impedance -
   On channel - 1*10E10 ohms, shunted by 250 pf
   Off channel - 1*10E10 ohms, shunted by 100 pf

5) Cross-talk between channels - < 80db

6) Resolution - 12 bits

7) Gain error - < +- 0.3% FSR, adjustable to zero via an on-board pot, adjustment range - +- 13 lsb

8) Offset error - < +- 0.25% FSR, adjustable to zero via an on-board pot, adjustment range - +- 20 lsb

9) Temperature coefficients -
gain - +- 50ppm/deg C
offset - +- 10ppm/deg C
linearity - +- 0.5ppm/deg C

10) Analog signal settling time before S/H acquisition - 400us

11) Sample/Hold acquisition time - 10us

12) Multiplexer switching transitions are break-before-make with a make delay of 1 microsecond

ERSION D SPECIFICATIONS:

Analog data acquisition chips: Burr-Brown SDM 854BG Data Acquisition System and Burr-Brown INA101 Instrumentation Amplifier

1) 8 input signals differential, max signal voltage (each line): -11 volts < Vin < +11 volts. Analog input signals shall not exceed these bounds or interchannel cross-talk may occur.

2) Conversion signal range - -10.240 to +10.235 volts.

3) Scaling - 5mv/lsb

4) Input bias current - +- 50 na max per channel

5) Input Impedance -
on channel - 1*10E10 ohms, shunted by 250pf
off channel - 1*10E10 ohms, shunted by 210pf

6) Common Mode Rejection - 70db, min @ 1khz, 20 volts P-P common mode signal, 1000ohms source impedance.

7) Cross-talk between channels - any off channel to any on channel - < 80db @ 1khz, 20 volts P-P off signal.

8) Resolution - 12 bits

9) Gain error - < +- 0.05% FSR, adjustable to zero via an on-board pot, adjustment range - +- 1%

10) Offset error - < +- 10mv, adjustable to zero via an on-board pot, adjustment range - +- 4 lsb

11) Linearity error - +- 1/2 lsb, max

12) Differential linearity error - +- 1 lsb, max

13) Relative accuracy - +- 0.025% of FSR

14) Noise error - 1mv P-P, 0 to 1mhz

15) Temperature coefficients -
    gain - +- 30ppm/deg C, max
    offset - +- 10ppm/deg C, max
    differential linearity - no missing codes over the 0 deg to 70 deg C range

16) Analog signal settling time before S/H acquisition - 400us

17) Sample/Hold acquisition time - 18us

18) S/H Feed through - < 70db max @ 1 khz

19) Multiplexer switching transitions are break-before-make with a make delay of 1 microsecond

COMMAND TIMING

Times stated below are software-dependant. The final software is not written, so times below are approximate.

Signals: ADDR, R/-W, DEV REQ, CON/MON, DEV ACK (assumes that a command message was detected and the message address was within the address block)

1) ADDR goes true 140us before DEV REQ goes true.

2) R/-W goes low at the same time thata DEV REQ goes high.

3) CON/MON states are stable 300ns before DEV REQ goes true.

4) If DEV ACK from the device goes true within 500 us after DEV REQ goes true, the Control Interface interprets this to mean that the device has decoded the RA and read the command arguement. DEV ACK must be held true until DEV REQ becomes false which will be about 35us after DEV ACK goes true. CON/MON will revert to the Tri-state when DEV REQ goes false. R/-W will remain in the logic 0 (write) state when DEV REQ goes false.

5) If DEV ACK has not been made true until after 500 us, the Control Interface assumes that the device was unable to respond. In this case DEV REQ will go false 500us after it was raised and CON/MON will revert to Tri-state. R/-W will remain in the logic 0 (write) state when DEV REQ goes false. This NO RESPONSE condition will increment a counter (BE-3) in the Standard Interface Internal Function block; see the Monitor And Control Bus Specification, (VLB ARRAY MEMO 302) for details. This NO RESPONSE count may be read out as Monitor Data by the Station Controller; the readout process shall reset the counter to zero. (See Note 1 below)

6) ADDR stays at the RA state of this message after 4) or 5).

Note 1 If devices which are controlled by the Standard Interface have a response time which exceeds 500 usec, (e.g. electromechical relays, contactors, actuators etc) the device control logic shall have provivisions to verify via the Monitor Data readout that the commanded state has been attained. If the command format consists of discrete command bits, the format of the associated confirming monitor data shall be identical to the command format. If the command format is an arguement then the confirming monitor data shall correspond to the command arguement.

DIGITAL MONITOR DATA TIMING

Signals: ADDR, R/-W, DEV REQ, CON/MON, DEV ACK (assumes that a monitor data request message was detected and the message address was within the portion of the address block dedicated to digital monitor data)

1) ADDR is set 10us before DEV REQ goes true.

2) DEV REQ goes high and at the same time, R/-W is set high (read state, it was left in the write state after executing the last message)

3) DEV ACK must go true within 500us after DEV REQ goes true. This signals to the Control Interface that monitor data is available and stable on the CON/MON lines. When DEV ACK goes true, the Control Interface will sample and format the data. DEV ACK must be held true for 18us after it was set high. At this time the Control Interface will set DEV REQ false.

4) DEV REQ will be set false 18us after DEV ACK went true. DEV ACK shall revert to the false state within 10us after DEV REQ went false.

5) In the event that DEV ACK does not go true within 500us after DEV REQ went true, the MDH and MDL components of the Monitor Data message shall be set to an all 0 state and the parity bit of MDH and MDL shall be set to even parity which will induce a parity error in the receiving circuitry in the Antenna Controller. DEV REQ will be set to false

at this 500us point. This NO RESPONSE condition will increment a counter (BE-2) in the Standard Interface Internal Function Block which may be read out as Monitor Data by the Station Controller; the readout process shall clear the counter.

6) The CON/MON lines must revert to the Tri-state disconnect when DEV REQ goes false.

7) ADDR stays at the RA state of this message after 4) or 5).

ANALOG MONITOR DATA TIMING

Signals: ADDR, R/-W, DEV REQ, ANENB, HI/LO SEL (assumes that a monitor data request message was detected and the message address was within the portion

of the address block dedicated to analog data)

1) ADDR is set 10us before DEV REQ goes true.

2) R/W- and DEV REQ are set true at the same time.

3) ANENB must go true within 5us after DEV REQ is set. ADDR must be connected to external multiplexers (if any) so that the analog signals may begin to settle, and HI/LO SEL must be in the correct state.

4) The selected analog signal will be sampled and A/D conversion initiated approximatly 450us after ANENB goes true.

5) DEV REQ will go false approximatly 30us after A/D conversion is initiated. ANENB must revert to false within 10us after DEV REQ becomes false. After the A/D conversion the Interface will read and format the data.

6) If ANENB is not set within 5us of DEV REQ, monitor data will be returned set to all zero with even parity, which will induce a parity error indication in the Antenna Controller. DEV REQ will be set false by 500us after it was initially set true.

7) The device shall not attempt to drive the CON/MON lines during the processing of an analog data request.

8) ADDR stays at the RA state of the message after 4) or 6).

ADDITION OF USER MICROPROGRAMMING TO THE STANDARD INTERFACE

The microprocessor in the Standard Interface may be used for control applications providing that the Command and Monitor Data capabilities described in this specification are not compromised; these tasks shall always be interruptable to service the higher priority Command and Monitor Data request messages.

Three entry points will be provided for users to add code of their own to the Standard Interface. Care must be taken that user routines do not disrupt the timing of the Monitor and Control serial bus.

The entry points are:

1) The command processor entry point. Will be entered with RA (Relative Address) pushed onto the processor stack below the subroutine return address and command data in the AB register. This entry point operates at interrupt level, and so must complete operations and return within 250us (approximatly 200 instructions) in order to be ready for the next command/monitor request.

2) A computed monitor point entry. Will be entered with RA pushed onto the processor stack. Must return with hexadecimal 8000 in the AB register to indicate no interest in the RA, or with the computed monitor value to be placed on the RCV bus in the AB register. This routine also executes at interrupt level and must return within 100us if the returned value is 8000H or within 250us if a value is returned.

3) Background task entry. This routine would execute when no command or monitor request is being processed. It has no restrictions on timing but is restricted in what it may do the the Device Interface: for instance, if it is to set DEV REQ, it must first set R/-W, and the device logic must constructed to tolerate the unexpectad dropping of DEV REQ when a command or monitor request arrives while the background has it set. The background task will be restarted at its entry point whenever a command or monitor request is received. The passage of commands on the XMT bus not addressed to this interface (outside its RA block) will not affect the background (except for loss of CPU time for processing).

PHYSICAL DESCRIPTION

Figure 2 depicts the Standard Interface Board package, physical envelope, mounting hole locations and connector orientations. The board envelope is 6.25(H) x 5.5(W) x .75(T) inches including I/O connectors. The board may be mounted on the NRAO module rails, or on standoff spacers. .25 inch may be trimmed from each side of the 6.25 dimension for installation in an rfi shielded enclosure or mounting between the rails. I/O connectors are compact "D" series connectors mounted on one edge of the board.

I/O CONNECTOR DETAILS

Parallel I/O - P1 (see note below)
Type: Cinch or Amphenol DD-50PC
Mating type: DD-50S

Pin	Signal
1	ANLG-0H
2	ANLG-1H

Serial I/O - P2
Type: Cinch or Amphenol DB-25PC
Mating type: DB-25S

Pin	Signal
1	+5V
2	N/U

3	ANLG-2H	3	N/U
4	ANLG-3H	4	N/U
5	ANLG-4H	5	N/U
6	ANLG-5H	6	N/U
7	ANLG-6H	7	N/U
8	ANLG-7H	8	N/U
9	CMD/MON-15	9	N/U
10	CMD/MON-13	10	DOUT
11	CMD/MON-11	11	PARX
12	CMD/MON-9	12	MSG
13	CMD/MON-7	13	5V COMM
14	CMD/MON-5	14	+5V
15	CMD/MON-3	15	+15V
16	CMD/MON-1	16	-15V
17	HI/LO SEL	17	HIQ GND
18	ANLG-0L	18	XACT
19	ANLG-1L	19	RCV+
20	ANLG-2L	20	RCV-
21	ANLG-3L	21	XMT+
22	ANLG-4L	22	XMT-
23	ANLG-5L	23	N/U
24	ANLG-6L	24	BUSY
25	ANLG-7L	25	5V COMM
26	CMD/MON-14		
27	CMD/MON-12		
28	CMD/MON-10		
29	CMD/MON-8		
30	CMD/MON-6		
31	CMD/MON-4		
32	CMD/MON-2		
33	CMD/MON-0		
34	5V COMM		
35	DEV REQ		
36	DEV ACK		
37	ANENB		
38	HIQ GND		
39	-15V		
40	+15V		
41	ADDR-7		
42	ADDR-6		
44	ADDR-5		
45	ADDR-4		
46	ADDR-3		
47	ADDR-2		
48	ADDR-1		
49	ADDR-0		
50	+5V		

NOTE: Both versions have identical functional connections to P1 and P2 so that either board may be plugged into a given module. On Version S of the Standard Interface, (single-ended analog multiplexing/conversion), the ANLG-0L through ANLG-7L (analog signal low connections) are tied to HIQ GND.