VLB ARRAY MEMO No. 417

CALIFORNIA INSTITUTE OF TECHNOLOGY
VLBA Memorandum

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Subject: Notes from "Dump Rate" Meeting 12/7/84

Present: Benson, Fort, Pearson, Romney, Ewing

This is to summarize an informal meeting held to discuss the implications of various correlator dump rates and related issues. Some of the discussion involved the "SIS" architecture (Simplified Interconnect System - to be described in a later memo).

-The Fringe Processor function may be split into two major sections, FP1 and FP2. In some interconnection schemes (e.g., SIS), this split is required, but in others the two sections may be merged into one physical processor.

FP1 can perform the following functions, which are at least potentially interesting for the VLBA:

1. Boxcar integration of correlations from the VLSI accumulator chip's dump rate (several hundred Hz) down to the official "correlator dump rate" (a few Hz). This is the very minimum function.

2. Efficient integration via an improved "sample rate reduction" algorithm, a digital filter. Such a filter increases the range of fringe rates which may accurately be handled with a given dump rate. It requires more computation than the boxcar, however.

3. "Software Fringe Rotation" according to one or more models would allow multiple phase centers, other than the one specified by the hardware rotator and delay centers. This function requires both memory and computing power. Fringe rotation could be performed at slowly varying rates (i.e., rate offsets from the beam center).

4. Related to No. 3, a full fringe rate spectrum could be computed, producing N fringe rate channels for every N input samples.

5. Global fringe fitting on a channel-by-channel basis would be possible with sufficient memory and computing power.

Items 3-5 are not part of the current correlator plan; they are presented in order to show some options potentially available to us that could improve correlator throughput in some cases. We also note that AIPS is apparently only interested in time-domain fringes, not fringe rate spectra, so that item 4 may not be very useful.

We recognise that a large data reduction occurs in FP1. If we select the simplest processor for items 1 or 2 above, we may lose the opportunity for improved calibration throughput and multiple phase centers. On the other hand, the budget may not permit an elaborate processor. Perhaps we can allow for a future hardware upgrade to FP1.

Items 1-4 might be carried out in single chip microprocessors as described in memo VC028.

-The second section of the FP is called FP2. FP2 receives data from FP1 sorted by baseline. The sort is required to permit calculation of Fourier transforms of the cross-correlation functions for spectral line work and bandwidth synthesis. Data compression in FP2 may be (only) a factor of 2, arising from suppressing "negative frequency" channels. We are considering one or more array processors (on the Archive Writer?) to provide the FP2 function.

-Multiple phase centers can be supported through splitting the correlator for simultaneous processing or by multipass processing. These methods seem to meet the current VLBA specs without extra complications in FP1.

-The relationship between average error rates, burst rates, and various integration and normalisation schemes is not completely understood. Where should normalisation be performed - in FP1? Should we seek a better specification on burst error rates to ensure highest map dynamic range?

-The Archive Writer (AW) accepts all FP2 outputs and writes to the archive medium. We feel we can comfortably sustain an AW output rate of 0.5 MB/s with present technology (6 minutes to fill a 6250 bpi tape). A factor of two or three higher might be available in bursts. In any case, the AW function can be enhanced almost arbitrarily with parallel processors and tape drives. The 0.5 MB/s rate is consistent with a overall correlator dump rate of 2 Hz.

-We looked at the worst case known spectral line source - Orion A in H2O. One might have to analyse a field with a radius of 4 arcseconds. With care, this should be possible given a 2 Hz dump rate and an efficient algorithm such as No. 2 above.

-Maximum required dump rate may also have an impact on correlator prescaling. If there is a N-bit prescaler whose value is not read out, we must be sure that the noise level in the maximum dump rate case is comfortably above 2**N counts. This could be a problem for low sample rates even with correlator speedup, since dump rate must be scaled up along with the tape speedup factor. We will have to require substantial oversampling of narrowband observations to preserve correlator significance, as well as to reduce the playback speedup factor.