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2-16 GHz SYNTHESIZER, L104
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VLBA | PROJECT NO. 53300 PROJECT NAME 16 GHz SYNTHESIZER

ITEM	DRAWING NUMBER	TITLE	DESIGN BY	DRAWN BY	DATE DRAWN	COMPUTER CODE & REMARKS
1	D53300M001	MODULE, FRONT & BACK PANEL	B.MAUZY	BOWYER	5/6/85	NOT IN COMPUTER
2	D53300M002	LEFT & RIGHT SIDE & MOUNTING PLATE	"	"	5/9/85	"
3	D53300M003	TOP & BOTTOM SUPPORT, FRONT & REAR SHIELD	"	"	5/13/85	"
4	D53300M005	MODULE, TOP & BOTTOM SUPPORT	"	"		
5	D53300M006	MOUNTING PLATE R.F. SIDE	"	"		
6						
7	B53300M004	PHASE DETECTOR BOX	L.BEALE	"	2/12/86	
8	B53300M005	SAMPLER DRIVE BOX	"	"		
9	B53300M006	RELAY BRACKET	"	"		RELAYBKT
10	B53300M007	HEAT SINK	"	"		HEAT SINK
11	B53300M008	SPACER & BRACKET	"	"		SPCR_BKT
12	B53300M009	MIXER BOX	"	"	8/27/86	MIXERBX
13	A53300M009	MIXER MOUNT SPACER	"	"	2/25/87	MIXMOSPA

3.0 General Description

The 2-16 GHz Synthesizer, L104, uses 100 and 500 MHz signals referenced to from the hydrogen maser frequency standard to generate a phase stable LO frequency of N x 500 ± 100 MHz in the range of 2.1 to 15.9 GHz, N having integer values from 4 to 32. The output frequency is set by a command from the computer through the Monitor and Control System (M&C) that coarse tunes a YIG oscillator. A digital sweep circuit provides a search mode until the phase lock circuit detects the oscillator and stops the sweep. Lock lights on the front panel indicate whether the lock frequency is above or below the closest N500 harmonic or if lock is not achieved. The YIG frequency range is limited to 2 to 8 GHz, so a doubler is used for the 8 to 16 GHz portion of the band. Refer to the block diagram, C53300K001.

The output frequency is converted to a 100 MHz IF by a harmonic mixer driven from a 500 MHz Comb Generator. The amplified IF is then fed to the phase and quadrature detectors and the amplified phase detector output drives the FM tuning coil in the YIG to complete the phase lock loop. The quadrature detector furnishes such functions as high and low lock, lock fail, sweep disable, 100 MHz signal level and upper/lower sideband. The 100 MHz reference signal is used for both detectors. The main output is monitored through a coupler, detector and leveling circuit to reduce variations in output level produced by the oscillator and amplifier-doubler. Samples of the main and IF signals are available on the front panel for

monitoring and troubleshooting.

A standard M&C card provides communication with the computer, receiving serial frequency data from the control bus and feeding parallel data to the Interface card. This card stores the frequency data and by way of a D/A furnishes a coarse tuning voltage for the YIG. The Interface card also generates the band switching signal, frequency sweep for acquisition and provides unit identification (ID) and serial number information back to the M&C card. Eight analog and three digital monitor functions from throughout the unit are fed to the M&C system for use at other locations.

The system is packaged in a three-wide custom module built to provide good EMI isolation between the digital cards and the analog equipment and to also shield both from the outside environment. All power and signal lines entering the two compartments are filtered except for four Monitor and Control bus lines.

4.0 Operational Description

4.1 Digital Control

Computer control and monitoring of the system is implemented through serial transmit and receive buses feeding standard Monitor and Control (M&C) cards located throughout the system. In this module the digital Interface card links a M&C unit to the analog portions of the 2-16 GHz Synthesizer. The card provides voltage to control a YIG oscillator and monitors some important

test points in the system. A block diagram is shown on drawing A53300K002. A discussion of the logic diagrams follows. Note: Persons needing detailed understanding of this unit must also understand the M&C unit (specification A55001N002-A).

First refer to Logic Diagram B53300L005, sheet 2. U01A, U01B, U02B, U13A, U07A, U02D, U14A, and U02C decode the relative address outputs of the M&C unit. Read addresses 0 to 7 are analog inputs to the M&C A/D converter. Read address 8 enables 8 tristate buffers in U03 that the M&C unit reads for dumping to the control computer. The 555 in U16 and discrete components in slot U22 form a free running oscillator at approximately 100 Hertz. This frequency establishes the sweep rate of the ramp generator. If the systhesizer is not phase locked, U14B enables the oscillator output to count up in U26 and U27 counters. The 5 lower stages of the counter count from zero to 31, step to zero, and start again. In order to reduce the discontinuity of the 31 to zero step, the sixth counter stage and U28 and U29A transform the count to a smoother count: up 0 to 31, then down 31 to 0, and repeat. Inversion of the most significant bit in U29B converts the count to a two's complement signed number that counts from -16 through zero to +15; reverses and counts from +15 through zero to -16 and repeats. The SW1 input to the counter stages inhibits counting and loads a zero into the signed number out. This signal can be pulled low by a manual dip switch for testing. It is also pulled low for .22 second each time new data

is strobed into the latch.

Next refer to sheet 1 of the logic diagram. Sixteen bits of tristate data from the M&C unit are strobed into latches U04 and U05. Three of the bits are not used at the current time. The 13 low order bits can be thrught of as a count from 0 to 8191. Counts from 0 to 4095 are LO band frequency settings: 0 to 8 GHz (actually 2 to 8 GHz). If the MSB (13) is set, the counts are from 4096 to 8191. This represents a frequency command from 8 to 16 GHz or high band. The oscillator is doubled to get this frequency band so it must track 4 to 8 GHz. The count in the latch must be divided by 2 to cover this range (i.e., 2048 to 4095 counts out). This division is accomplished by the 12-pole double-throw switch consisting of U10, U11, and U12. Division is accomplished by shifting each bit one position down in the word when bit 13 is set. To assist with lock up of the systhesizer loop, a sweep is digitally combined with the M&C count out of the switch. The signed number discussed above is added to the count in U17, U18, and U19. Each count represents approximately 1.95 MHz at the oscillator output. The sweep of -16 to +15 counts, then sweeps the oscillator around ± 30 MHz. The summer output is buffered by U23 and U24 and drives a digital-to-analog converter (D/A) U25. The D/A is strapped to output 0 volts for 0 counts and +5 volts for 4095 counts. Resistors in slot U31 provide isolation and gain setting for the next stages. One output drives the YIG oscillator tuning driver and one output goes to the M&C unit for monitoring.

Now refer to sheet 3 of the logic diagram. It has two 8-bit tristate buffers, U09 and U30, that are enabled by the M&C ID Req line to put identification numbers (ID) on the data buss. Five ID bits are selected with a dip switch, U20, and two are determined by wiring on the bin connector to identify the unit and its location. The module serial number is read by six bits determined by wiring on the card edge connector. The card is a 10 row by 55 pin wire wrap board with 100 pin edge connector and is fully utilized.

One word of caution! The summer that combines the sweep count and the M&C count can overflow. If a count between 4091 and 4095 is commanded, the addition of 15 counts will cause the summer out to go to 0. This would cause a severe glitch in the D/A output. Similarly, a command count between 8160 and 8191 would have the same problem since it would be seen as 4080 to 4095 at the summer input. Given the normal mode of operation, this should not be a problem.

4.2 Main Tuning

The main or coarse tuning of the YIG oscillator is set by a frequency command from the control computer thru the M&C card to the Interface card. Only frequencies corresponding to multiples of 500 MHz ± 100 MHz between 2100 and 15900 MHz are acceptable. These frequencies are spaced alternately 300 and 200 MHz; for example, 2100, 2400, 2600, 2900, 3100, etc. The YIG tuning range is limited to 8 GHz. The 8 to 16 GHz range is covered by

inserting a doubler. The Interface card divides all frequency commands above 8 GHz by two and generates a bit to switch the amplifier-doubler into the signal path. See block diagram ...K001.

A 12-bit digital signal enters the D/A converter generating a 1.25 to 5 V signal in 1.22... mV increments, giving 1.953... MHz steps up to 8 GHz. An additional bit is added for the 8 to 16 range. The analog voltage from the Interface card (drawing ...L001,sheet 1) goes to the Tune In pin on the Yig Driver and Leveler board (YD&L) (drawing ...S004, sheet 1) where a feedback amplifier converts the input voltage to a tuning current. The D/A output voltage is reduced by resistors on the Interface card and on the YIG driver card to a range of 0.1 to 0.4 V at the + input of op amp U1. The op amp output voltage is fed to a power stage consisting of cascaded emitter followers Q_1 and Q_2 on the Regulator card (drawing ...S008) to generate a current of 100 to 400 mA in the YIG main tuning coil. This current is measured by the drop across 2 ohms that is amplified by a second op amp, U2, and applied to the negative input of U1. Gain and offset (OS) pots allow adjustment of the slope and zero offset to reduce errors from op amp offsets, YIG current/frequency slope differences, D/A errors, etc., so that the output more closely tracks the commanded frequency. The bandwidth of the main tuning circuit is 18 Hz.

Some YIG's have significant tuning nonlinearity ($\geq$ 0.15%), most often characterized by compression at the high end of the

range. If this problem should occur, additional components may be added to the Main Tuning circuit to trim out most of the error. The Lin Knee and Non Lin pots and associated components make up this circuit.

Frequency errors due to D/A converter, driver and YIG tuning nonlinearities, pulling, hysteresis, temperature changes, etc., are much too great to permit pull-in to phase lock without a search mode. Snap-in occurs from about ± 2 MHz maximum while the total error is estimated to be as high as 20 MHz. The search range needs to be at least this large but other considerations limit the maximum deviation. When searching around 15.9 GHz the digital sweep cannot exceed the equivalent of +50 MHz at the YIG output or the counter will overflow. Also, a 50 MHz peak sweep with a 50 MHz error would be sufficient offset to chance lock on the wrong sideband. The most convenient sweep range between these constraints is +15, -16 counts or +29.3, -31.25 MHz. The sweep steps up and down at the same rate completing a cycle in about 0.7 sec. This slew rate is about 1/6 the speed that produces marginal locking.

4.3 RF Section

The YIG oscillator (Avantek AV7248) chosen for this application is a combined oscillator and bandpass filter. The oscillator for the prototype unit not having a filter produced harmonics about 18 dB below the main output. With the phase detector levels being used at that time, false lock points would

occur on the harmonics. Increased level discrimination in the detector eliminated the problem, but if the harmonics were near the 12 dB limit allowed the margin of susceptability to false lock points would be seriously compromised.

A fixed pad following the YIG reduces power to an acceptable level for the PIN attenuator and provides a better match. Latching type coax relays switch in the amplifier-doubler for 8 to 16 GHz operation. The relay drivers (drawing ...S001) located on a card on the digital side of the module, convert a TTL positive transition from the Interface card to a 28 V pulse approximately 36 ms long. Monitor contacts within the relays are used to change the FM loop and provide switching verification back thru the M&C system.

The doubler (TRW RX 16000) will provide adequate output power but requires more drive than can be provided without amplification. The amplifier used (Aydin Microwave AMA 4080B5) will provide up to +25 dBm from 4 to 8 GHz with at least 15 dB gain.

Three 20 dB couplers (Sage C218-20) on the output line provide front panel monitoring, a signal for the harmonic mixer, and one for the leveling loop. The leveling signal is detected by a Schottky diode (Aertech D18Z3) amplified from about 7 mV by an offset op amp (U5) on the YIG Driver and Leveler board (drawing ...S004-3) to drive a PIN attenuator driver and attenuator (General Microwave 311 and LM190). The output level is set with the offset pot (Output Level) to +3 dBm average across the band. Variations in coupling, detector efficiency,

match and cable loss with frequency produce output level changes up to ± 1.4 dB. The detected output is also amplified to a nominal 4 V level for the M&C system. The Monitor Gain and Zero pots control this output.

4.4 Down Conversion and IF

The signal for phase locking feeds an HP harmonic mixer (sampler). The LO drive is a pulse generated by the Comb Generator (drawing ...S009). A 500 MHz reference signal is amplified to +19 dBm and fed to a step recovery diode (SRD). The resulting output pulse contains useful harmonics to more than 16 GHz. The slope of the comb from 2 to 16 GHz is about 35 dB. Phase stability of an uncompensated diode and driver measured-0.7°ϕ/°C/GHz. This is improved by adding temperature compensation to the SRD bias voltage. Temperature sensing diodes potted in the case near the SRD produce a voltage change that is amplified and applied through a resistor (R8) as bias to the SRD. Three adjustments allow setting the bias level and slope for the desired compensation. The bias resistor value and source voltage were chosen to minimize phase change with drive level changes around the nominal +19 dBm available into 50 ohms. This compensation produces a change of about 1.5°ϕ/dB/GHz for ± 1 dB. The bias current is monitored as an indication of SRD performance, therefore of drive level and of 500 MHz reference input level. Op amp gain is adjustable (Mon. Adj.) to provide a nominal 4 V level output to the M&C system.

The harmonic mixer, driven by the comb generator, produces a 100 MHz IF signal when the module output frequency is 100 MHz above or below a harmonic of 500 MHz. The conversion loss is about 30 dB with 2.5 to 3.0 dB slope over the band. The mixer output impedance is high (~ 7 pF) so is matched to 50 ohms with a series inductor. The 100 MHz amplifier (drawing ...S007) provides about 54 dB gain to produce +7 dBm into the phase detector. A 3 section bandpass filter 30 MHz wide is included to prevent false locks on subharmonics of 100 MHz. The filter may contain temperature compensating capacitors to reduce system phase shifts with temperature that are not frequency related. Those changes that are proportional to frequency can be absorbed in the Comb Generator compensation. The mixer error of about 0.1°ϕ/°C/GHz is removed this way. The amplifier has an auxiliary output feeding -13 dBm to a front panel jack (Monitor 100 MHz IF) for troubleshooting.

4.5 Phase Detection and Monitoring

The Phase Detector unit (drawing ...S002) contains both phase and quadrature detectors, a 100 MHz reference level detector and several circuits to drive sideband indicators, provide TTL lock indication to the Interface board and a 100 MHz signal level indication. The phase detector is operated with the IF being a high level signal (+7 dBm) and the external reference operating about -7.5 dBm. This arrangment reduces detector susceptability to spurious signals in the IF and prevents typical

IF level changes with frequency from changing the loop characterstics. The reference level is not sufficient to turn the detector diodes on so the IF level must be within about 14 dB of nominal to generate a detectable output. The detector output goes thru a filter to terminate the sum frequency and reduce 100 MHz leakage into the FM Driver circuits that follow.

For the quadrature detector the levels are reversed, the reference driving at +7 dBm and the signal operating about 0 dBm. With a lower signal level the output will be a function of IF level which is desired, and the polarity is determined by the sideband. The output is, therefore, usable to generate the sideband, lock, fail and signal level monitor functions. Transistor drivers operate three LED's on the front panel to show the phase lock status. The necessary phase shift for the quadrature detector is produced by a small capacitor (C1) tap off the IF signal line. A separate diode detector on the +7 dBm reference line monitors the level for the M&C system. These and other monitor circuits are adjusted for +4 V out at nominal operating levels.

4.6 PLL and Acquisition

The FM tuning section (drawing ...S004-2) of the Yig Driver and Leveler board (YD&L) receives its input from the phase detector and generates a current of either polarity in the FM coil for rapid frequency change over a limited range. A wide band, low noise op amp (U3) drives complementary emitter followers (Q1 and Q2) that can furnish up to 50 mA in either

direction to tune the YIG ± 15 MHz. Loop determining components were chosen for unity damping and $W_n = 9 \times 10^5$ (143 kHz). Tuning sensitivity would double on the high band because of multiplication, but a contact on a band switching relay doubles the resistance in the load, thereby maintaining the same FM tuning characteristic. A monitor circuit (U4) senses this tuning current providing information to the M&C system and providing a fudging voltage to the main tuning driver to increase DC gain and reduce offsets. This centering circuit has a response time of about 86 ms (1.8 Hz).

When a new frequency is designated, two latches on the Interface card are reloaded, a timing circuit sets the sweep count to the center, the D/A generates a corresponding voltage and the YIG changes frequency. After 200 ms of settling time for the main tuning, the timer allows the sweep circuit to begin searching above and below the nominal frequency. When the YIG frequency sweeps through a point 100 MHz away from a 500 MHz harmonic, a sweeping IF signal appears at the phase detector. As the IF signal frequency crosses 100 MHz the phase lock loop captures the signal and the quadrature detector generates a signal to the Interface card to stop the sweep. The sweep rate is about 11 ms/step and 1.95 MHz/step on the low band.

5.0 Tests, Adjustments and Further Details

5.1 PS Filter Board (C53300S003)

Experience on previous systems indicated that hash on the

power supply lines may be quite high, so users were urged to allow for up to 100 mV of noise. All power enters the RFI shielded compartments through 5 nF feed-thru capacitors to suppress components above 30 MHz. L section filters on this board for the ± 15 and +28 V supplies extend suppression down to less than 10 kHz. Regulators that filter below 10 kHz are used on other boards where a 3 V supply reduction is permissible.

5.2 Regulator Board (C53300S008)

The Regulator board receives ± 15 V from the P.S. Filter board and regulates down to ± 12 V to provide clean power for some of the more sensitive circuits. Trim pots R7 and R9 are adjusted for +12 and -12 V, respectively, at the output terminals.

The +5 and -5.2 V inputs come from the back panel connector via feed-thru capacitors to suppress higher frequency hash. Lower frequency filtering is provided by LC filters on the board. The current drive stage for the YIG main tuning uses ± 5 V and is also located on this board. Low frequency suppression for the driver is provided by the transistors and a -2.5 V regulator.

5.3 Main Tuning (C53300S004, Sheet 1 and ...S008)

To adjust the YIG main tuning curve for minimum error over the band, it is necessary to measure the tuning nonlinearity. This is done as follows:

1. Slide the sweep switch on the Interface card to off.

2. Remove op amp U4 on the YIG Driver and Leveler board (YD&L).

3. Disconnect and ground the shield of the ϕ Error cable (white coax) from the Phase Detector.

4. Enter frequencies via the M&C bus.

5. Read the main output or front panel monitor with a counter with at least 1.0 MHz resolution.

As a starting condition for new oscillators or driver boards it is suggested that the offset pot (OS), R10, on the YD&L board be set for 0 V on the wiper (end of R11, 4.7 M toward edge of board), a frequency of about 6600 MHz be entered and the GAIN control, R9, set for the same output frequency. If the curve is not expected to be far off (same YIG oscillator and YD&L board previously adjusted), the initial adjustment of R9 and R10 can be skipped. Frequencies from 2100 to 7900 should then be entered and the errors recorded. With this info plotted a best fit straight line can be drawn through the error curve and the GAIN and OS pots trimmed for the desired result. Because of interaction beween the controls it is necessary to trim the OS pot at a low frequency (say, 2500 MHz) and the GAIN pot at the upper frequency (about 6600 MHz) several times for the desired result or set the GAIN pot for the desired upper frequency, f_2, enter the lower frequency, f_1, note the output frequency, subtract from the desired frequency, multiply the difference, Δf by $f_1/(f_2-f_1)$ and set the OS pot beyond the desired frequency by this amount. With f_2 re-entered, resetting the GAIN pot for the

correct output should also make f_1 correct. It is assumed that some error will be set in at both frequencies to obtain the minimum peak errors over the band.

If the tuning error measurement shows a strong increase as 7.9 GHz is approached, say more than 20 MHz, and the error is due to tuning compression (output frequency below input command), and a best fit straight line will not reduce peak errors below ± 15 MHz, then the LIN pots (R16 and R20) and associated circuitry should be added. A small p.c. short between pins 1 and 2 on the NON LIN pot (R16) must be cut. The LIN KNEE pot (R20) will determine the frequency above which the NON LIN pot will compensate for YIG tuning compression. A small readjustment of the GAIN pot (R9) should be made once the tuning curve has been linearized. This linearization was not necessary on early production because the YIG's were bought to a ± 0.1% maximum linearity specification. Maximum errors were less than 8 MHz. When the errors have been reduced to less than 15 MHz, replace U4 on the YD&L board, reconnect the phase error cable and turn on the sweep switch.

5.4 Relay Driver (B53300S001)

The coax band-switching relays are of the latching type that require a 35 ms pulse to operate. Control lines X2 and $\overline{X2}$ from the Interface board provide a positive transition for switching. This step turns on both transistors in the driver to furnish approximately 28 V to the coils. The voltage is sustained until

the series time constant at the input (C2, R3 + 2K source) can no longer furnish sufficient base current to the first transistor to drive the second stage. Feedback speeds up the switching rates. Diodes protect transistor junctions on the reverse cycle.

5.5 Leveler (C53300S004, Sheet 3)

The leveler circuit should keep the output power at +3 dBm over the band even though the YIG output level can change ± 3 dB and power amplifier and doubler gain will change several dB with frequency. However, output fluctuations up to ± 1.4 dB may exist because the detector is not flat (± 0.5 dB) and the coupler side port flatness is ± 0.4 dB with frequency. Mismatch adds additional ripple and the cable loss from the detector coupler to the output adds slope. The result can be an unexpected variation in level that can be best set by monitoring the level at many points across the total range and adjusting the Output Level control (R43) on the YD&L card for +3 dBm average output. The Monitor Zero control (R59) is set for minimum output voltage (as read on the CRT) with C11 shorted (end of R48, 510 ohms, toward Log Driver shorted to gnd). With the short removed the Monitor Gain pot (R54) can be set for 4 V out. Detector output will be about ≈7 mV.

5.6 Comb Generator (C53300S009)

For the initial setup on a new unit, or if the power amplifier A1 (AH507) has been changed, the power available to the

SRD matching network must be set. This is done by disconnecting L1 from the amplifier output and soldering the end of a RG188U coax in its place. The exposed center conductor should be short, say 1/8 inch. With no attenuation in the input pad, the 500 MHz input level can be adjusted for +19 dBm out of the attached coax. Correct output reading for coax loss of 0.22 dB/ft. The input level should then be measured and a pad added to make the input +5 dBm. Remove the test coax and connect L1. Set trim pot C (R16) maximum CCW and A (R17) for 0.65 V bias at op amp output U1-7. With +5 dBm, 500 MHz input, adjust L2 and L3 for maximum comb output and flatness to 16 GHz. The 2 GHz component level should average about +5 dBm and the 16 GHz component should measure about ~30 dBm. A typical comb spectrum is shown in Section 7. Recheck the bias level as temperature changes will change this reading. Adjust MON ADJ for +4 V on the monitor output pin. Final adjustment of the trim pots will be made with the Comb Generator combined with the mixer and 100 MHz Amplifier and tested over a range of temperature as described later.

5.7 100 MHz Amplifier (C53300S007)

This amplifier boosts the harmonic mixer output of about ~47 dBm to +7 dBm available for the phase detector. The mixer output impedance including teflon socket is approximately 7 pF in parallel with a high resistance (500 to 1000 ohms), so a matching network is used on the amplifier input. For testing the amplifier alone, a simulating input circuit such as shown in

Section 6.1 should be used. The jig is useful for checking the input matching network, amplifier gain, tuning the bandpass filter, and when making phase stability measurements. Allow for a loss of 17 dB in this network. The capacitance value may not be correct for a particular layout because of strays. To check the jig, first feed a variable frequency RF signal into the mixer and monitor the IF at the output of amplifier A1 by disconnecting C4 from the filter and tacking in a small coax line. Do not forget that the DC block is still required. Having measured the center frequency with this hookup, the input jig can then be substituted for the mixer and the 3.3 pF trimmed for the same center frequency. The matching network alone will have a bandwidth around 32 MHz. The bandpass filter is designed for 36 MHz and the combination should measure near 28 MHz.

The phase stability with temperature for the unit is typically -.016°ϕ/°C but expect a spread from at least 0 to-.035°ϕ/°C. Final adjustment of the attenuator must be done in a system after the main ouput level has been set. With the output averaging +3 dBm the attenuator is selected for +7 dBm average available to the phase detector. The monitor output should be near -13 dBm under the same conditions.

A bandpass filter that has been previously tuned can be trimmed by stretching or squeezing L3 and L6 and adjusting C6. For a new circuit do not install L3, C5, L6, and C7. With L4, C6 only in the circuit, trim C6 for a 100 MHz center frequency. Then add L3, C5 and trim L3. Finally, add L6, C7 and trim.

If a thermal check of the Comb Generator, Mixer, 100 MHz Amplifier package indicates a significant non-frequency dependent phase change with temperature that should be improved, then C5 and/or C7 in the amplifier can be changed to temperature compensating types. Parallel combinations of available negative temperature coefficient and NPO capacitors can generate a range of coefficients while meeting the combined value requirement. The magnitude of compensation required and the many possibilities to achieve it are too numerous to describe here.

5.8 Comb Generator - Mixer - 100 MHz Amplifier

This procedure is to set the temperature compensating pots on the Comb Generator bias board to correct for the generator and mixer phase variations with temperature. Refer to Section 6.2 for a suggested test setup. The generator, mixer and amplifier should be mounted together on a flat mounting plate that can be attached to a conducting thermal control device such as a Scientific Columbus heat pump. Adjust the thermal control for 20 C plate temperature. Set pot C (R16) maximum CCW, minimum resistance. Set pot A (R17) for 0.62 V on R18, 3.9 K (upper end) and pot B for (R14) for 0.62 V at U1-7 (upper end of diodes CR2 and CR3). With a 500 MHz input of +5 dBm and the output connected to a phase measuring system at 15.1 GHz, change the temperature to 30 C. When the temperature has stabilized, adjust pot C for the same phase reading as measured at 20 C. Change the measurement frequency to 2.6 GHz, return to 20 C and note the

phase change. The change should be less than 2° (0.2°ϕ/°C). If this limit is not met, make a measurement near mid-band (8.6 GHz) to see if the error is linear with frequency. An error inversely proportional to frequency indicates non-frequency dependent phase change that should be correctable in the amplifier. However, measurements on two systems indicate this error is less than 0.1°/°C. See the 100 MHz Amplifier section for further comments.

This procedure for phase compensation and measurement is recommended because these three units include the most critical parts of the system for phase stability and, though awkward to test, are not nearly as awkward as trying to change temperature and get repeatable results on an entire module. This statement is made with some confidence because testing a module in an oven has been tried. Changing the temperature of so much thermal mass in an air medium is very slow allowing other time related errors to become more significant. The metal-to-metal "hot plate" method is much faster and more repeatable. A legitimate question is, what about the components not included such as the couplers and phase detector. Three Sage C218-20 couplers performed as follows:

	2.6 GHz	5.1 GHz	15.1 GHz
Thru port	0 to +.02 °/°C	+.02 to +.12	+.18 to +.32
Coupled port	-.01 to +.04	-.01 to +.03	+.06 to +.25

The worst case error is .15°ϕ/°C for the mixer coupler or .029°ϕ/°C/GHz. The leveling coupler contribution is smaller since only the thru port is involved. A Model RPD-1 phase

detector measured less than .002°ϕ/°C. These numbers are well under a system target of less than 0.2°ϕ/°C/GHz. Should another brand of coupler be used these tests should be repeated.

5.9 Phase Detector (C53300S002)

With power connected, check that the regulators U3 and U4 are providing ± 12 V within ± 0.5 V. Provide +7 and +5 dBm 100 MHz signals to J1 and J3 from an in-phase power divider and equal length lines including the 2 dB pad. The DC output at J2 with 1 K load should be +0.29 ± 0.03 V. Measure the DC at the end of R10 (51 ohms) adjacent to C6 (1 nF). It should be less than .08 V. Add 19.5" of polyethylene type coax to the J1 line. The output at J2 should be 0 ± 0.03 V. If this requirement is not met, verify that the input phase difference is 90 ± 2.5° using a vector voltmeter. The quadrature detector output should be a maximum. If an RF voltmeter with high impedance probe is available, the amplifier A1 and A2 output levels should measure within 2 dB of 0 and +7 dBm. The output at C6 should be +0.65 ± 0.2 V. Adjust the Signal Level pot, R5, for 4 V on feed-thru terminal 13. Measure +4 ± 0.2 V at output terminal 10. Adjust Ref Level pot, R31, for 4 V on terminal 12. By moving the 19.5" cable to J3 the input phase is changed 180° and the voltage at terminal 13 becomes -4 V ± 0.1 V. Terminal 10 should again be +4 V ± 0.3 V. Verification of outputs under appropriate conditions on terminals 9, 11, 14 and 15 require external pull-up resistors (5 or 10 K suggested). These can be measured now or checked in

the module. When terminal 13 is positive, terminals 9, and 15 will be low; the others high. With 13 negative, 9 and 14 will be low; the others high. With either 100 MHz input disconnected, terminals 9, 14 and 15 will be high and 11 low.

5.10 FM Tuning (C53300S004)

The YIG FM coil driver contains no adjustments but some additional information may be helpful. The unit is designed to furnish up to ± 50 mA to the coil for ± 15.5 MHz swing. The tuning sensitivity as measured across the 150 ohm resistors is 2.07 MHz/V and is equivalent to about 45 MHz/V at the cable input. At the monitor output the figure is 1.55 MHz/V. Please note that these numbers are for the FM tuning only and do not reflect the effect of the feedback to the main tuning. When testing on the low band this feedback can be disabled by removing op amp U4. For the high band either end of R40 (200 K) should be grounded (U4 removed).

The comparatively low value of R28 (100 K) in the FM feedback limits loop gain at low frequencies and permits oscillator frequency pulling to generate significant phase offsets. Feedback to the main tuning corrects this problem. For higher FM gain the excess loop delays or phase shifts produce a measurable push-off voltage peaking around 2.3 MHz from lock. The sweep drive will override this for modest gain increases, but it effectively limits the range of the sweep. When push-off is not present the lock frequency will be approached smoothly to

about 2 MHz separation when snap-in occurs. The push-off phenomenon is accommodated by leaving the FM low frequency loop gain low and using feedback to the main tuning below 1.8 Hz (88 ms TC) to boost DC gain. Attempts at diddling the phase did not help. The low frequency gain is about 6.5 MHz/°ϕ or .15°ϕ/MHz. If oscillator drift is 0.3 MHz/°C maximum, then phase drift will be less than .045°ϕ/°C. If this is considered marginal, the gain could be doubled without serious push-off problems but further increases could be a problem.

As mentioned under Operational Description, the FM tuning sensitivity is changed when switching bands to maintain the same overall tuning sensitivity on both bands. R38 (150 ohms) is inserted by auxiliary contacts in relay K1 to halve the tuning current on the hgih band. The 16 ohms, R34, across the YIG FM coil provides damping that reduces ripple in the sideband noise. Typical sideband spectrums are shown in Section 7. The amplifier input is a low level signal on coax from the Phase Detector. To reduce the possibility of pickup from ground loops the input circuit has an isolated common, grounded only through the coax. It is, therefore, necessary to ground the shield whenever the loop is opened by disconnecting the Phase Detector output, J2.

5.11 Front Panel

Because of the system guidelines for remote control and monitoring of modules thru the M&C bus the front panel has no controls and a minimum of displays and test points. The three

LED's indicate the status of the phase lock loop. When the unit is not locked for any reason, the red FAIL light should be on. When lock occurs, one of the green lights will show whether the lock frequency is above or below the closest harmonic of 500 MHz.

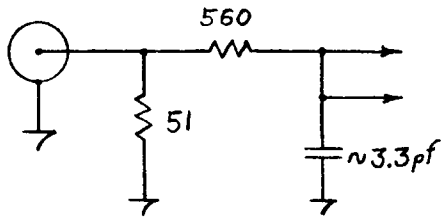
The main output is sampled with a 20 dB coupler that provides about -16 dBm at the 2-16 GHz Monitor jack for checking freqeuncy, sidebands and general testing. The tap point is inside the loop so that the load changes on this line have minimal effect on phase. The 100 MHz IF Monitor jack provides an isolated sample of about -13 dBm of the IF signal for observing the spectrum at a more convenient frequency. An open-to-termination change on this line generates a maximum phase step of about .05°.

5.12 Acknowledgements

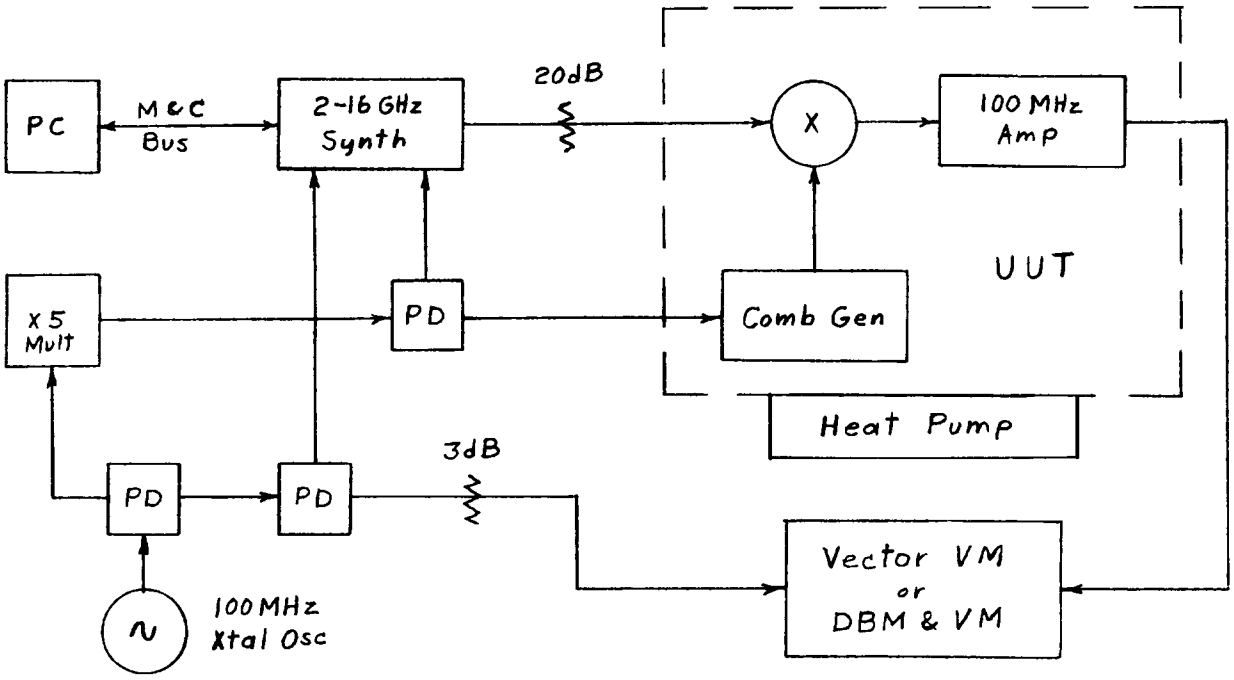
Recognition is given to Lewis Beale for his efforts in breadboarding, testing, mechanical designs, and as current producer of these systems; to Ron Weimer for the Interface card design and its description; to Rich Bradley for the computer display program and help in the digital area; and to Omar Bowyer for mechanical designs and drafting.

6.0 Suggested Test Circuits

6.1 100 MHz Amplifier Input Matching Circuit

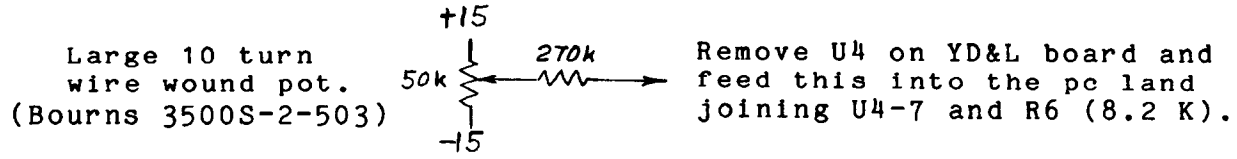


6.2 Comb Generator - Mixer - 100 MHz Amplifier Phase Stability vs. Temperature Measurement



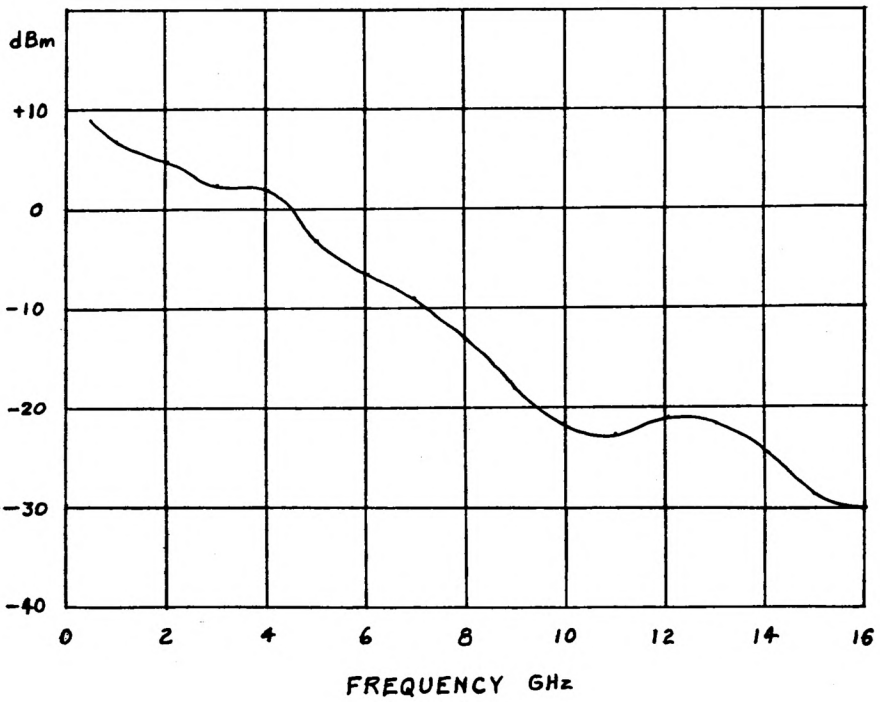
6.3 Manual Tuning of YIG

For small deviations around a commanded frequency

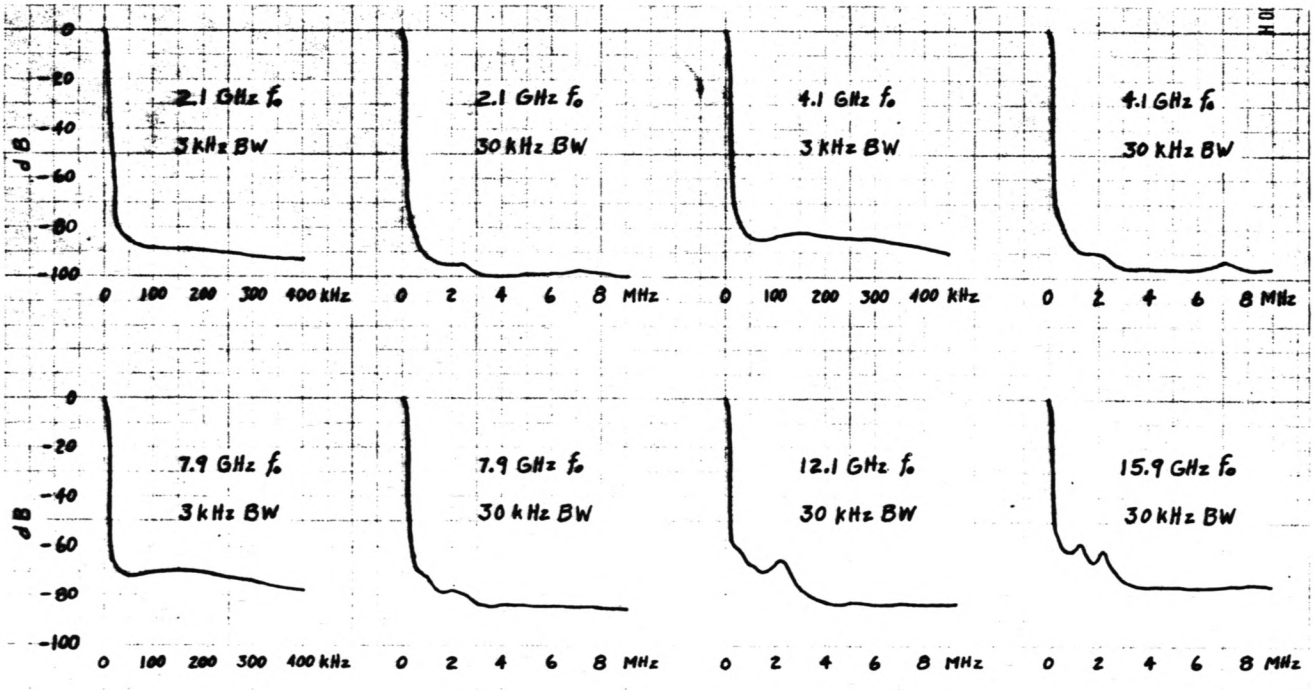


7.0 Graphs

7.1 Comb Generator Spectrum



7.2 Noise Spectra



7.3 CRT Display (Proposed)

Operating Frequency	xxxxx.xxx	
Band	2-8/8-16	
Sideband	Upper/Lower	(> ± 2 V limit)
Phase-Lock Status	Locked/Unlocked	

Description	Status	Limits		Remarks (Warning Limits)
D/A Converter Output 1600 MHz/V	x.xx	1.29	5.00	(0%)
YIG Main Tuning Voltage	x.xx	1.96	8.10	(2%)
YIG FM Tuning Voltage	x.xx	-0.40	0.40	(25%)
Phase-Lock and 100 MHz SIG Level	x.xx	2.90	5.50	(7%)
100 MHz REF Level	x.xx	3.20	5.00	(5%)
Comb Gen/500 MHz REF Level	x.xx	3.10	5.10	(8%)
Output Level	x.xx	1.50	8.20	(12%)

8.0 Input-Output Functions, Levels, and Connections

8.1 Monitor and Control I/O

Analog Inputs

Read and Relative Address	P1, Pin No.	Function
0	1 (0H)	D/A Converter Output
1	2 (1H)	YIG Main Tuning Voltage
2	3 (2H)	YIG FM Tuning Voltage
3	4 (3H)	Phase-Lock & 100 MHz Sig Level
4	5 (4H)	Sideband (+ Upper, - Lower)
5	6 (5H)	100 MHz REF Level
6	7 (6H)	Comb Gen/500 MHz REF Level
7	8 (7H)	Output Level

Digital Inputs

Relative address 8 and Read

M&C Input	Interface Input	Function
CM0	40	Phase Lock Status (Lock, low)
CM1	46 (LM1)	Relay K1 Monitor |High, 2-8 band|
CM2	48 (LM2)	Relay K2 Monitor |Low, 8-16 band|

ID Request

M&C Input

CM0 thru CM7	Unit and location identification. CM7=Parity. CM6=MSB. CM0 & CM1-location.
CM8 thru CM13	Unit serial number. CM8-LSB. CM13-MSB.

Digital Output

Relative address 8 and Write.

Outputs CM0 thru 12	LO Frequency Control. Count 1024 to 8191.

8.2 Back Panel

AMP 42 pin mixed connector, P11 204186-5, 202394-2, Block, hood

Pin No.	Function		Pin Type No.
10	+5 V	1.6 A	201578-1
16	+15 V	1.2	|
17	-15 V	0.17	|
29	+28 V	0.22	|
11	-5.2	0.50	|
34	Pwr. G		|
42	Sig. G		|
8	M/C Bus XMT +		|
9	M/C Bus XMT -		|
14	M/C Bus RCV +		|
15	M/C Bus RCV -		|
22	ID LSB		|
23	ID		210578-1

Coax Connectors, OSP

		Omni-Spectra
P5	Output 2-16 GHz +3 ± 1.4 dBm	4503-7941-00
P6	100 MHz Ref. In +5 ± 1.0 dBm	"
P7	500 MHz Ref. In +5 ± 1.0 dBm	"

8.3 Front Panel

		Omni-Spectra
P12	Monitor, 100 MHz IF -13 dBm	2004-7941-00
P13	Monitor, 2-16 GHz Out -16 dBm	"

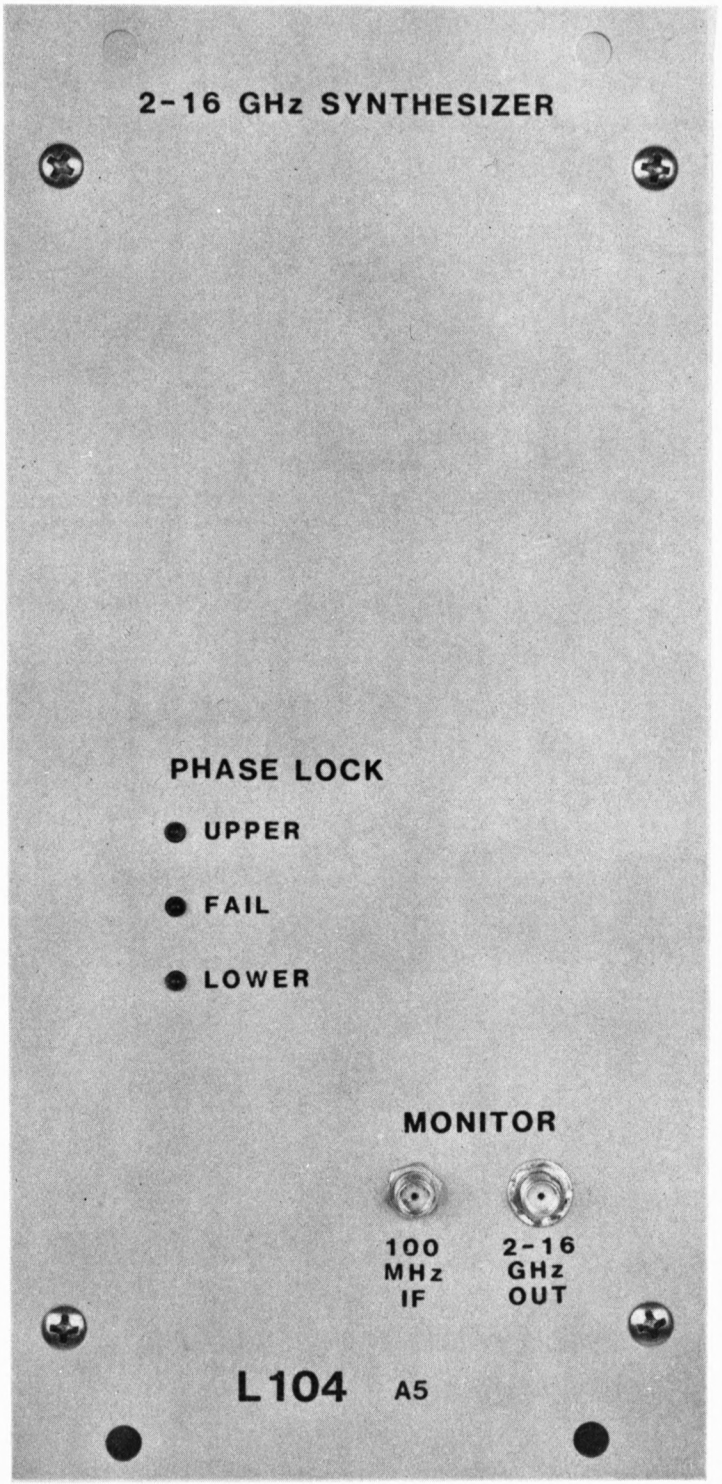
9.0 Photos

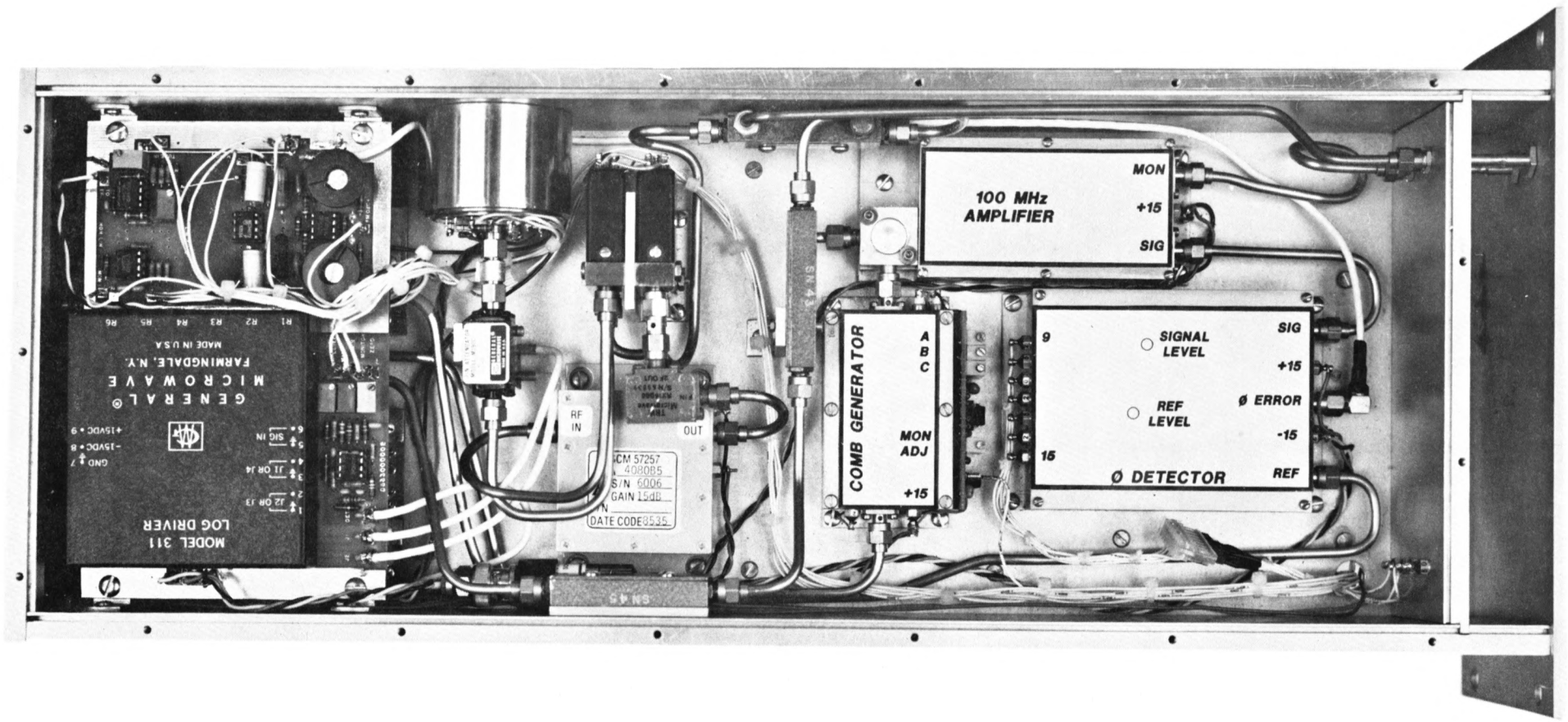
Front view.

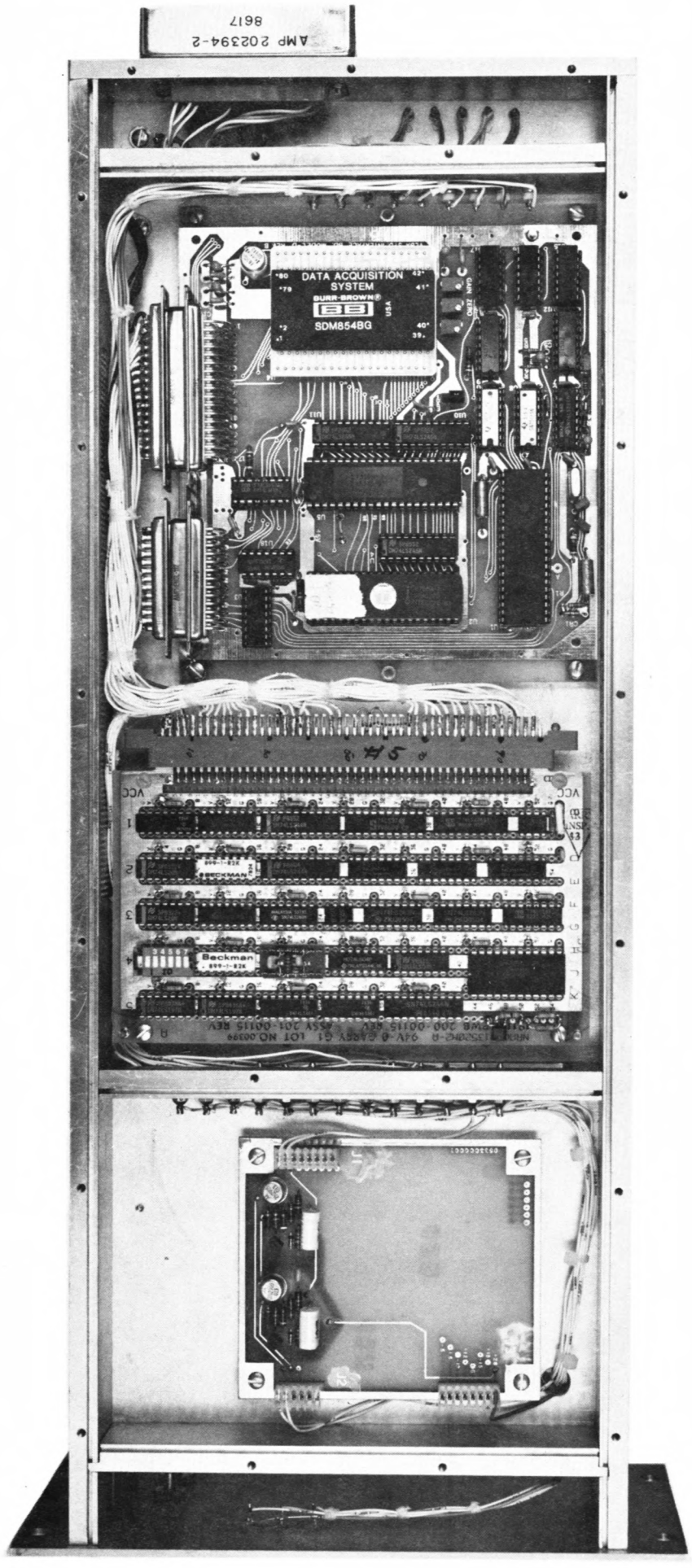
Right side view.

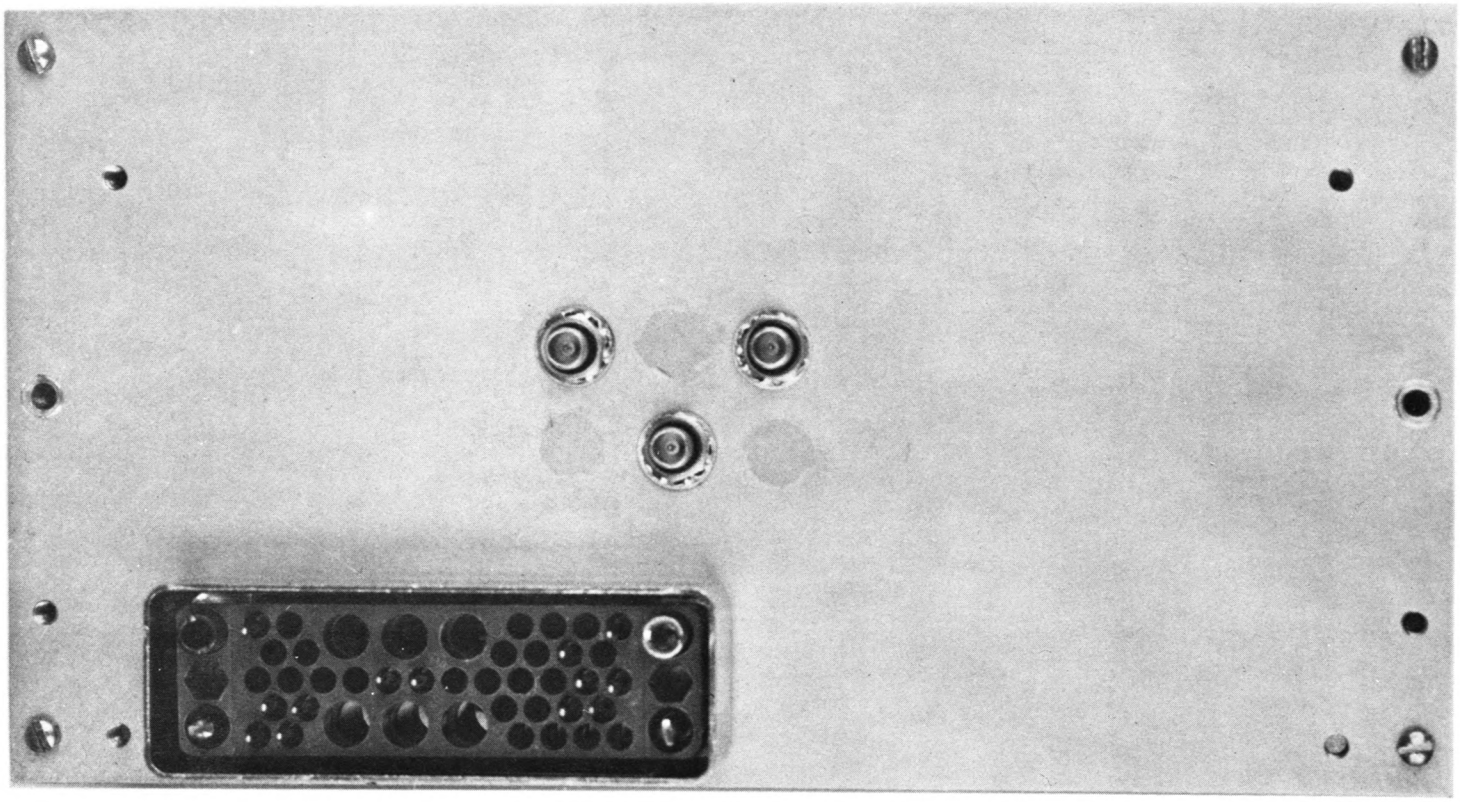
Left side view.

Back side view.


2-16 GHz SYNTHESIZER
PHASE LOCK
UPPER
FAIL
LOWER
MONITOR
100 MHz IF
2-16 GHz OUT
L104 A5


100 MHz
AMPLIFIER
MON
+15
SIG
COMB GENERATOR
A
B
C
MON
ADJ
+15
9
SIGNAL
LEVEL
SIG
+15
Ø ERROR
REF
LEVEL
-15
15
Ø DETECTOR
REF
RF
IN
OUT
SN 43
SN 45
GENERAL ®
MICROWAVE
FARMINGDALE, N.Y.
MADE IN U.S.A
MODEL 311
LOG DRIVER
SIG IN
J1 OR J4
J2 OR J3
+15VDC • 9
-15VDC • 8
GND 7
DATE CODE 8535

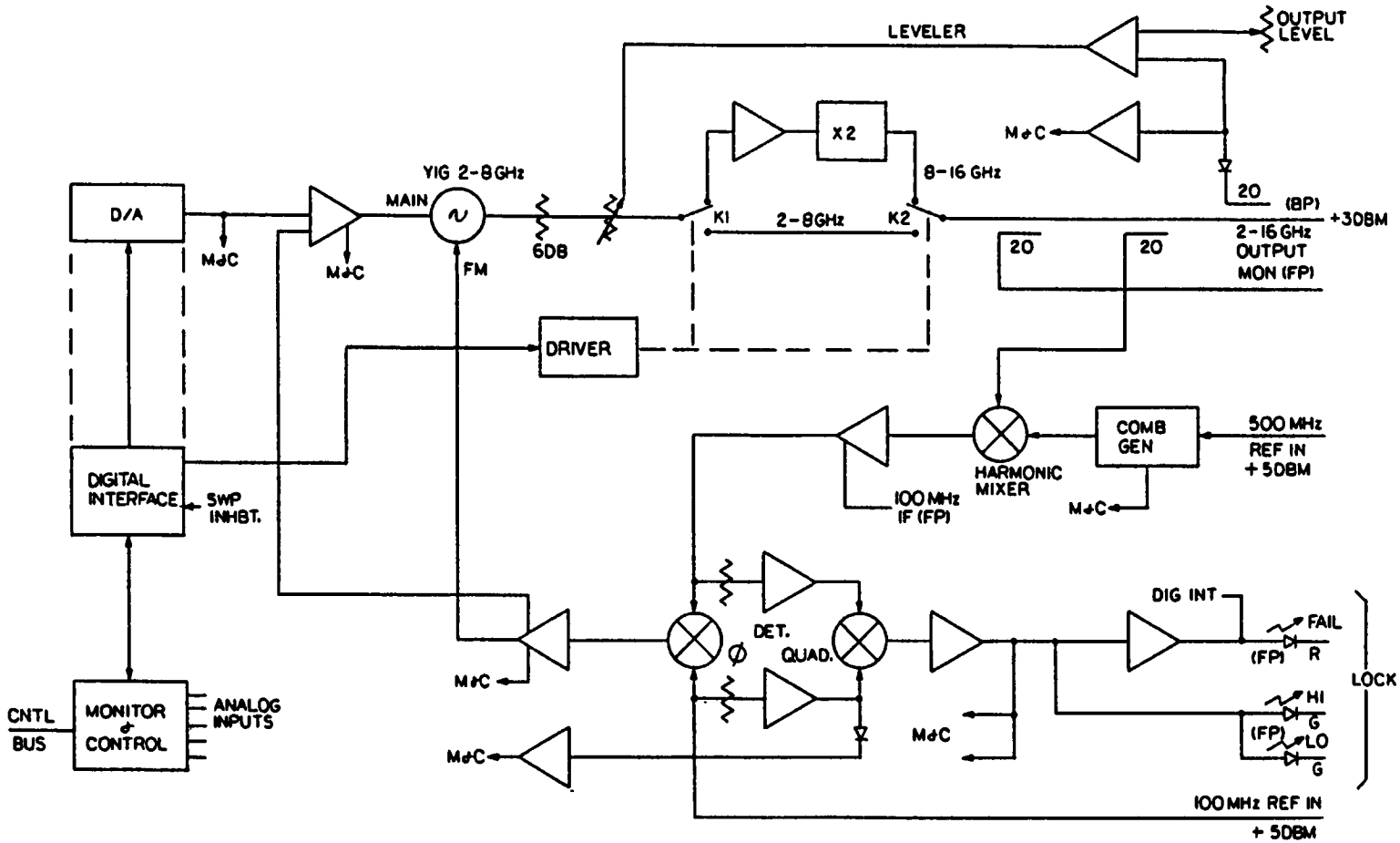

AMP 202394-2
8617
DATA ACQUISITION SYSTEM
BURR-BROWN®
SDM8548G
USA
Beckman



10.0 Block Diagrams

Module

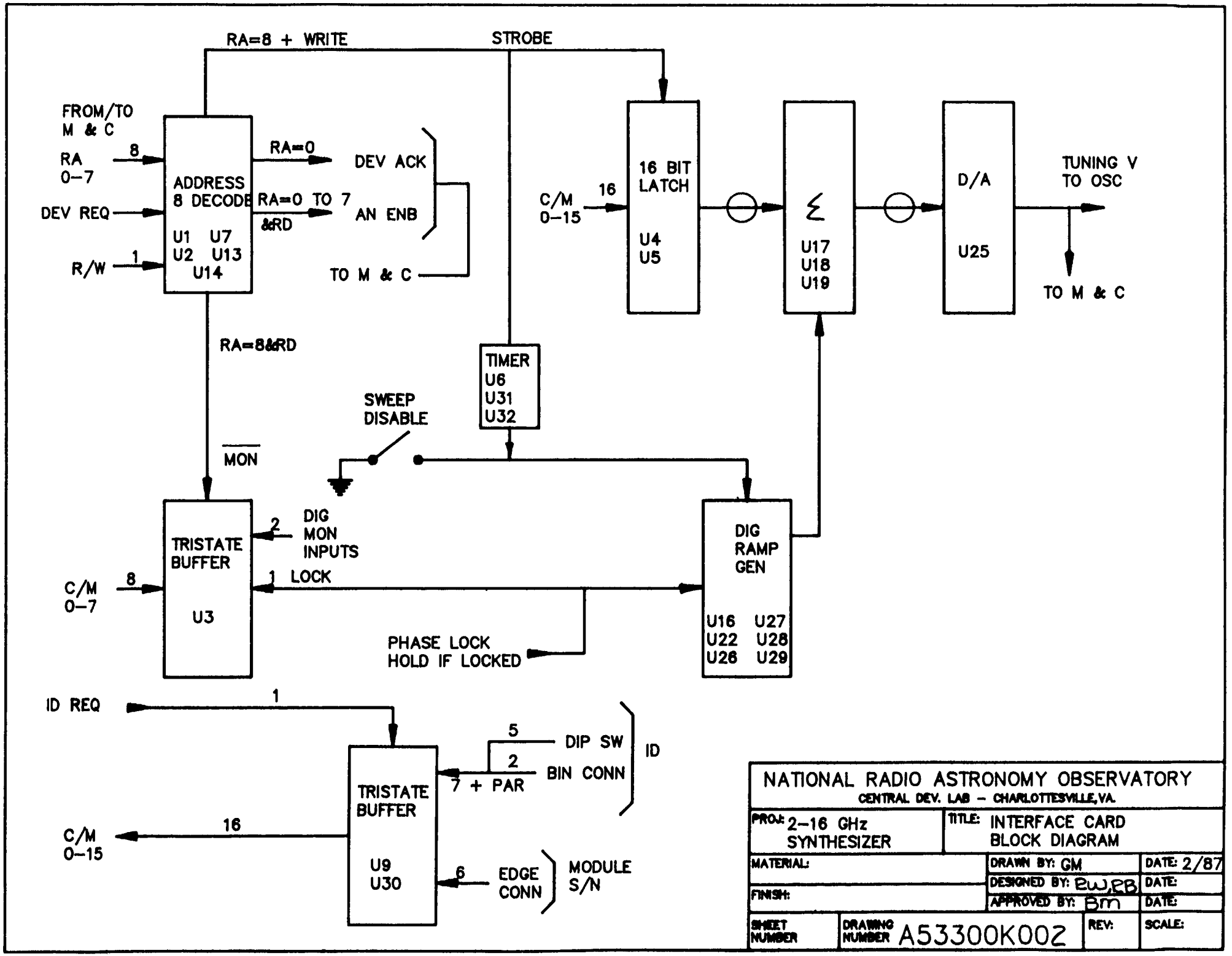
Interface card.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	VLBA PROJECT: 2-16 GHz SYNTHESIZER
MATERIAL:	TITLE: BLOCK DIAGRAM MODULE
FINISH:	NATIONAL RADIO ASTRONOMY OBSERVATORY
NEXT ASSY / USED ON	DRAWN BY G MORRIS 9-86 · DESIGNED BY · APPROVED BY · DATE
	SHEET NUMBER · DRAWING NUMBER C53500K001 · REV. · SCALE

D C B A

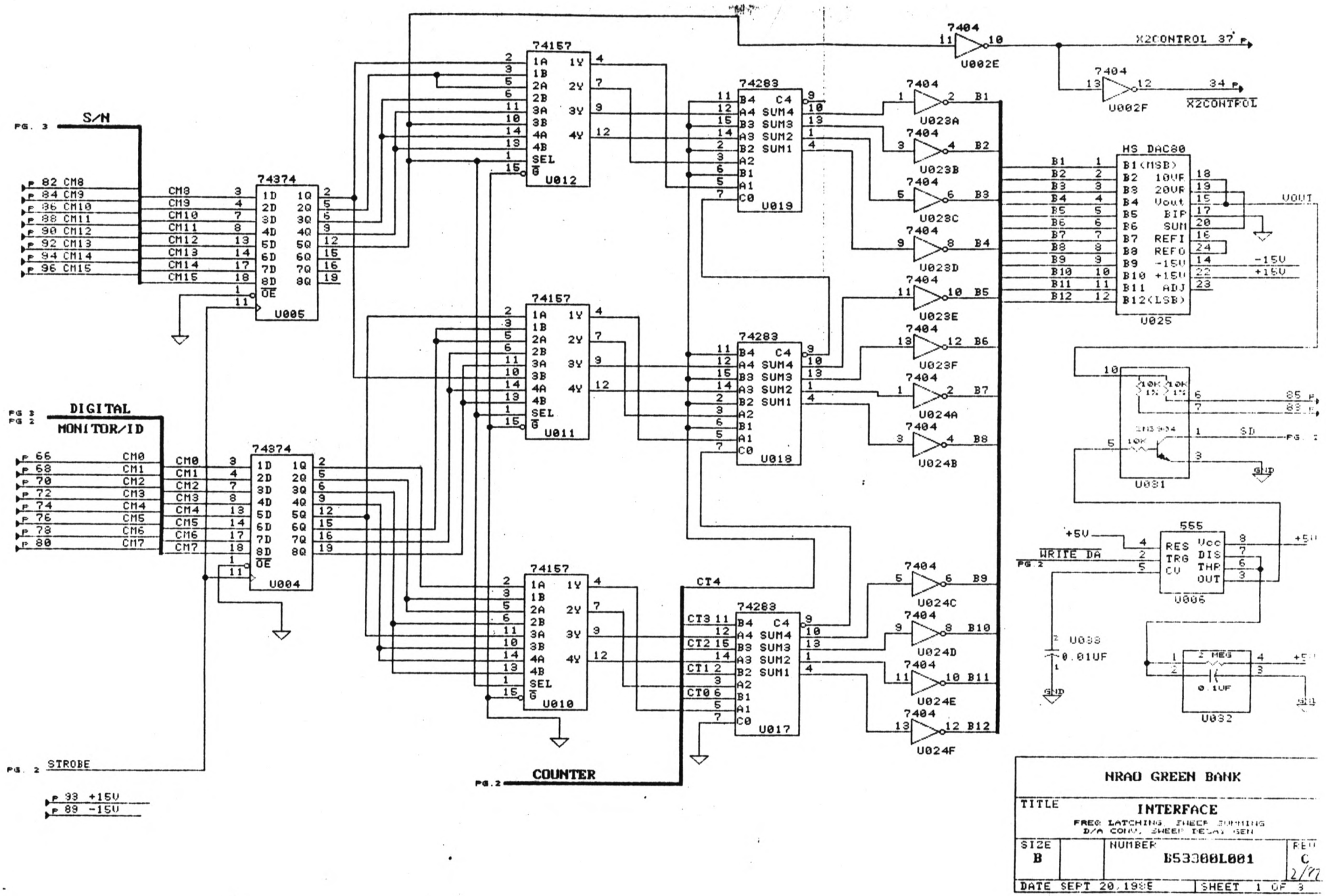
4 3 2 1

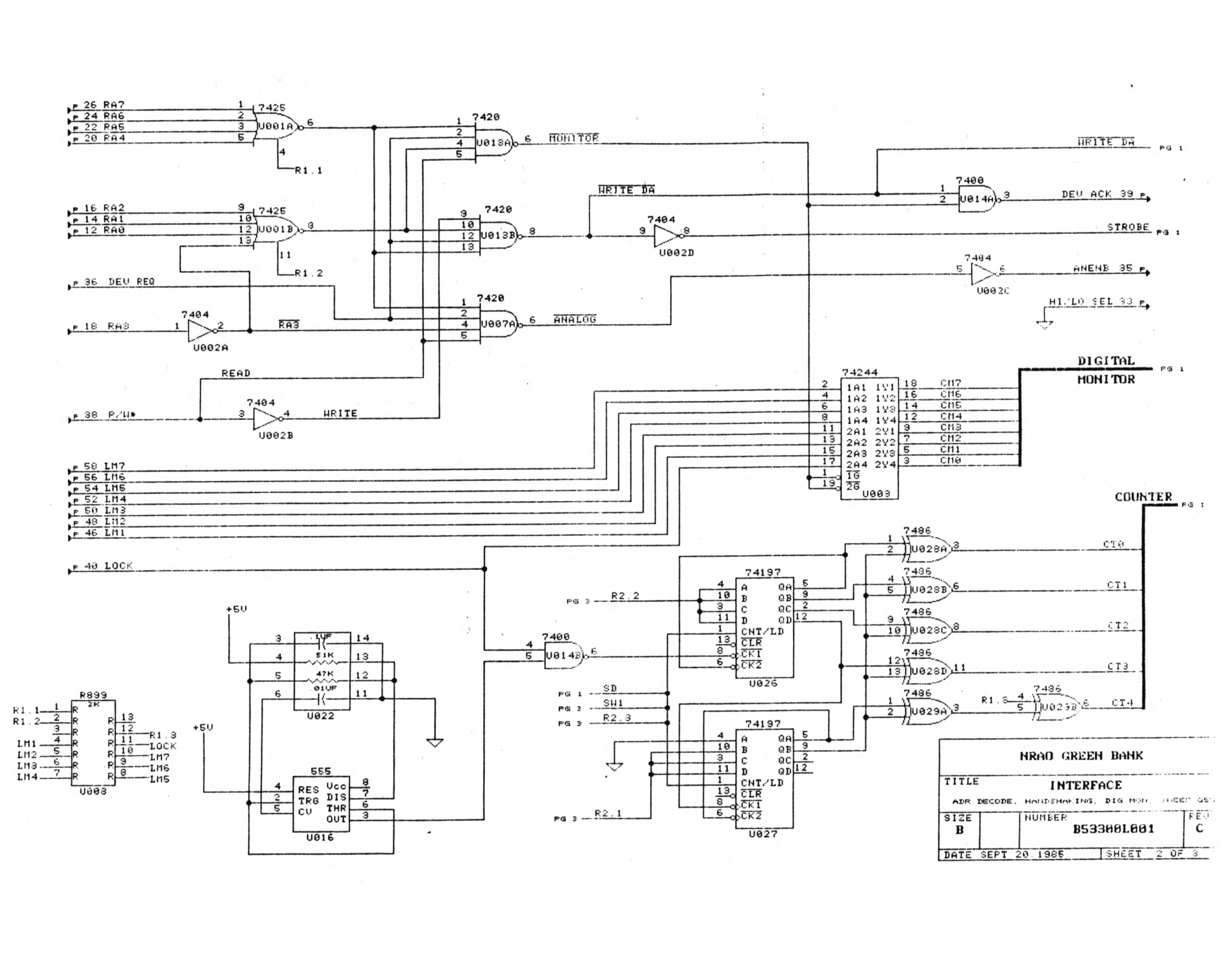


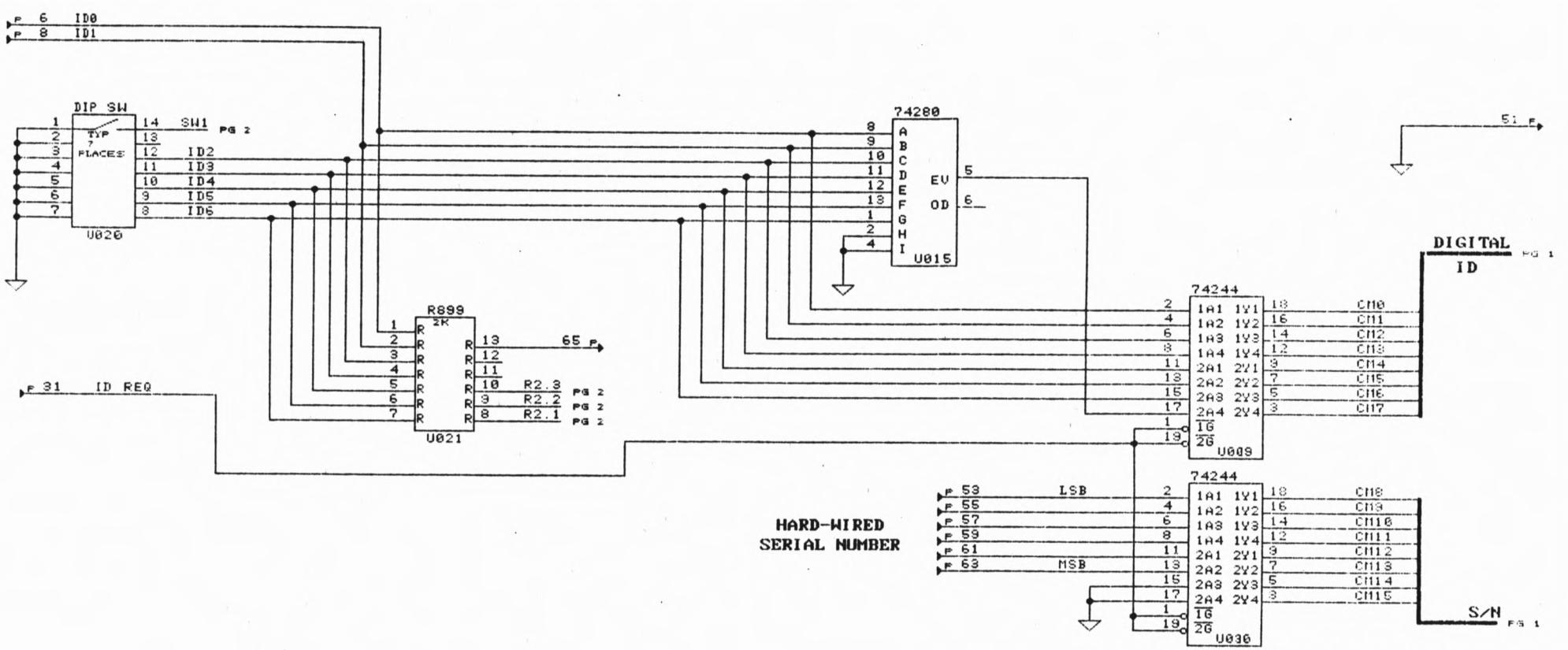
NATIONAL RADIO ASTRONOMY OBSERVATORY CENTRAL DEV. LAB – CHARLOTTESVILLE, VA.			
PROJ: 2–16 GHz SYNTHESIZER	TITLE: INTERFACE CARD BLOCK DIAGRAM		
MATERIAL:		DRAWN BY: GM	DATE: 2/87
FINISH:		DESIGNED BY: RW, RB	DATE:
		APPROVED BY: BM	DATE:
SHEET NUMBER	DRAWING NUMBER A53300K002	REV:	SCALE:

11.0 Logic Diagram

Interface card.


S/N
PG. 3
DIGITAL
MONITOR/ID
PG 3
PG 2
STROBE
PG. 2
P 93 +15V
P 89 -15V
74374
U005
U004
74157
U012
U011
U010
74283
U019
U018
U017
7404
U002E
U002F
U023A
U023B
U023C
U023D
U023E
U023F
U024A
U024B
U024C
U024D
U024E
U024F
X2CONTROL 37
X2CONTPOL 34
HS DAC80
U025
VOUT
-15V
+15V
U031
SD
555
U006
+5V
WRITE DA
PG. 2
U033
0.01UF
2 MEG
0.1UF
U032
CT4
COUNTER
PG.2
NRAO GREEN BANK
TITLE
INTERFACE
FREQ LATCHING, SWEEP SUMMING
D/A CONV, SWEEP DELAY GEN
SIZE
B
NUMBER
B53000L001
REV
C
2/92
DATE SEPT 20,1988
SHEET 1 OF 3


P 26 RA7
P 24 RA6
P 22 RA5
P 20 RA4
7425
U001A
R1.1
7420
U013A
MONITOR
WRITE DA
PG 1
7400
U014A
DEV ACK 39 P
P 16 RA2
P 14 RA1
P 12 RA0
U001B
R1.2
U013B
7404
U002D
STROBE
PG 1
7404
U002C
ANENB 35 P
P 36 DEV REQ
HI/LO SEL 33 P
P 18 RA3
U002A
RA3
U007A
ANALOG
READ
P 38 R/W
U002B
WRITE
74244
U003
DIGITAL
MONITOR
PG 1
P 58 LM7
P 56 LM6
P 54 LM5
P 52 LM4
P 50 LM3
P 48 LM2
P 46 LM1
P 40 LOCK
COUNTER
PG 1
7486
U028A
U028B
U028C
U028D
U029A
U023B
CT0
CT1
CT2
CT3
CT4
74197
U026
U027
PG 3 R2.2
PG 3 R2.3
PG 3 R2.1
PG 1 SD
PG 3 SW1
7400
U014B
+5V
.1UF
51K
47K
.01UF
U022
555
RES
TRG
CV
Vcc
DIS
THR
OUT
U016
R899
2K
U008
R1.1
R1.2
R1.3
LM1
LM2
LM3
LM4
LOCK
LM7
LM6
LM5
NRAO GREEN BANK
TITLE
INTERFACE
ADR DECODE, HANDSHAKING, DIG MON, SHEET 05
SIZE
B
NUMBER
B53008L001
REV
C
DATE SEPT 20 1986
SHEET 2 OF 3



NRAO GREEN BANK			
TITLE: INTERFACE			
ID AND SERIAL NUMBER IDENTIFICATION			
SIZE: B		NUMBER: B53A0001001	REV: C
DATE: JANUARY 8, 1986		SHEET 3 OF 3	

12.0 Schematics

Relay Driver.

Phase Detector.

Power Supply Filter.

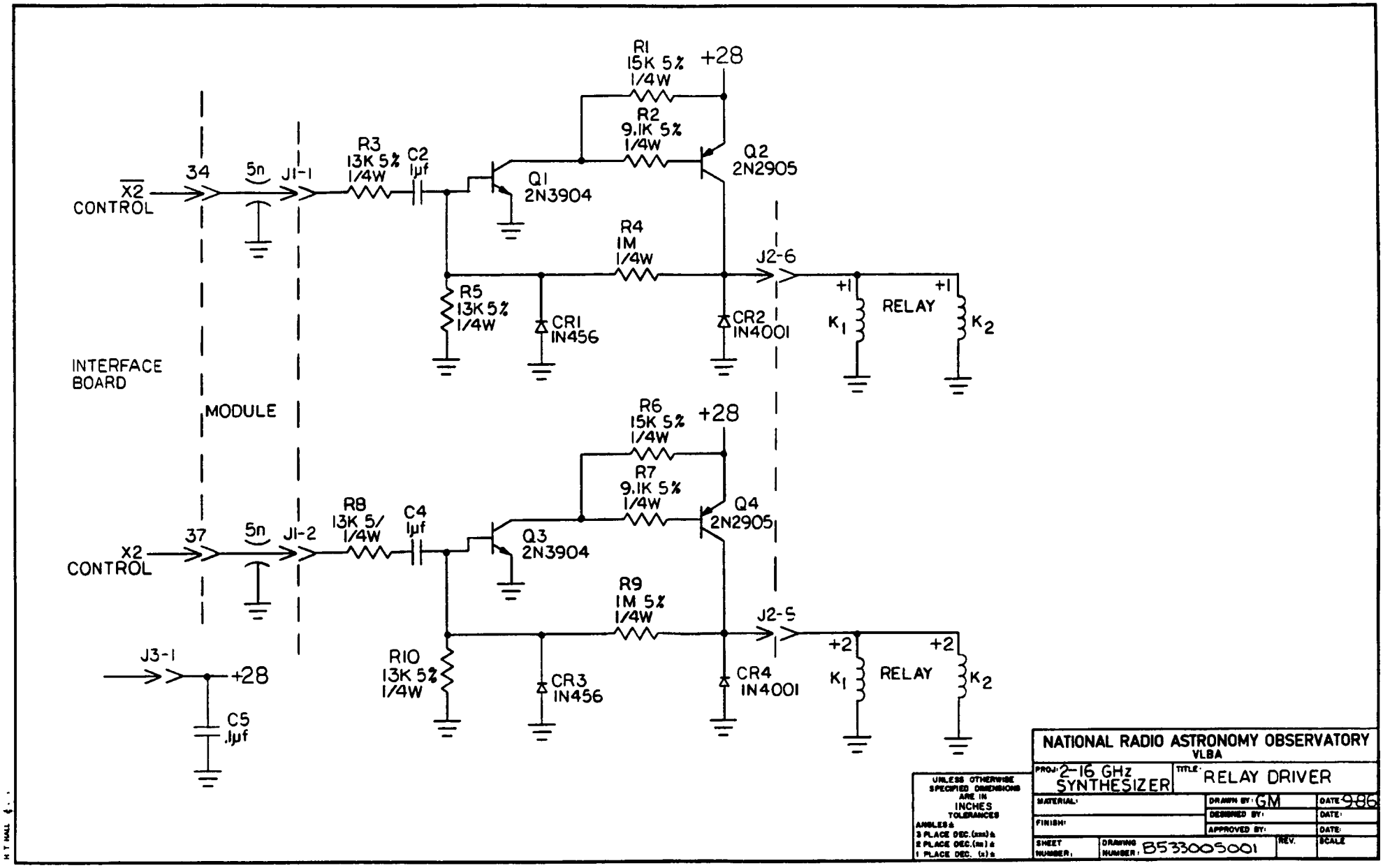
YIG Driver and Leveler.

Module.

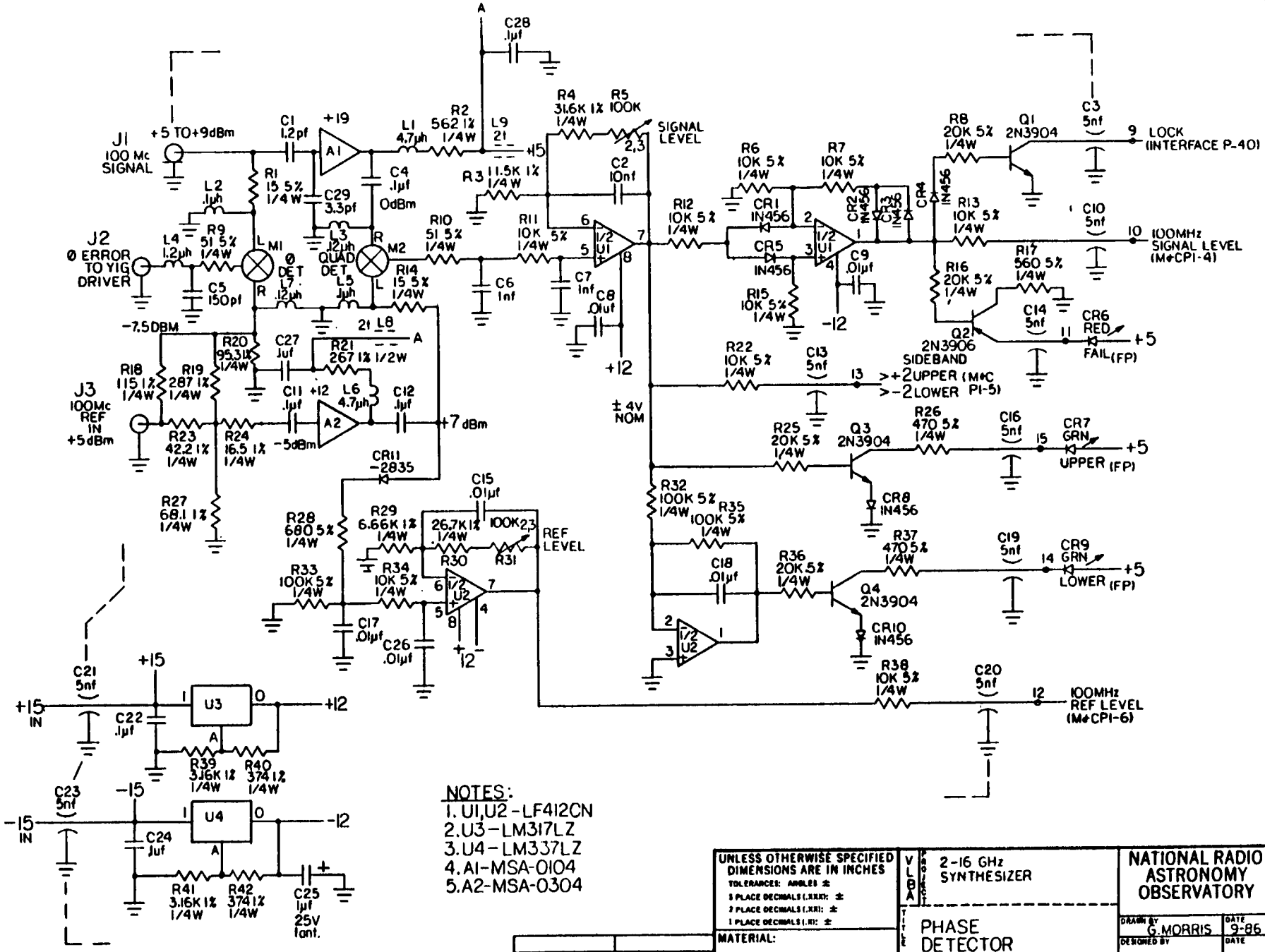
100 MHz Amplifier.

Regulator.

Comb Generator.


R1
15K 5%
1/4W
+28
R2
9.1K 5%
1/4W
Q2
2N2905
R3
13K 5%
1/4W
C2
1µf
34
5n
J1-1
X2
CONTROL
Q1
2N3904
R4
1M
1/4W
J2-6
R5
13K 5%
1/4W
CR1
IN456
CR2
IN4001
+1
K1
RELAY
+1
K2
INTERFACE
BOARD
MODULE
R6
15K 5%
1/4W
+28
R7
9.1K 5%
1/4W
Q4
2N2905
R8
13K 5%
1/4W
C4
1µf
37
5n
J1-2
X2
CONTROL
Q3
2N3904
R9
1M 5%
1/4W
J2-5
J3-1
+28
R10
13K 5%
1/4W
CR3
IN456
CR4
IN4001
+2
K1
RELAY
+2
K2
C5
.1µf
NATIONAL RADIO ASTRONOMY OBSERVATORY
VLBA
PROJ: 2-16 GHz SYNTHESIZER
TITLE: RELAY DRIVER
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±
3 PLACE DEC. (.xxx) ±
2 PLACE DEC. (.xx) ±
1 PLACE DEC. (.x) ±
MATERIAL:
FINISH:
DRAWN BY: GM
DESIGNED BY:
APPROVED BY:
DATE: 9-86
SHEET NUMBER:
DRAWING NUMBER: B533005001
REV.
SCALE
H T HALL

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	11-20 86	G.M		C2 WAS .10nf
B	2-24 87	G.M		R2 WAS 620 5% 1/4W R21 WAS 300 5% 1/2W ADDED C29



NOTES:
1. U1,U2 - LF412CN
2. U3 - LM317LZ
3. U4 - LM337LZ
4. A1 - MSA-0104
5. A2 - MSA-0304

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY | USED ON

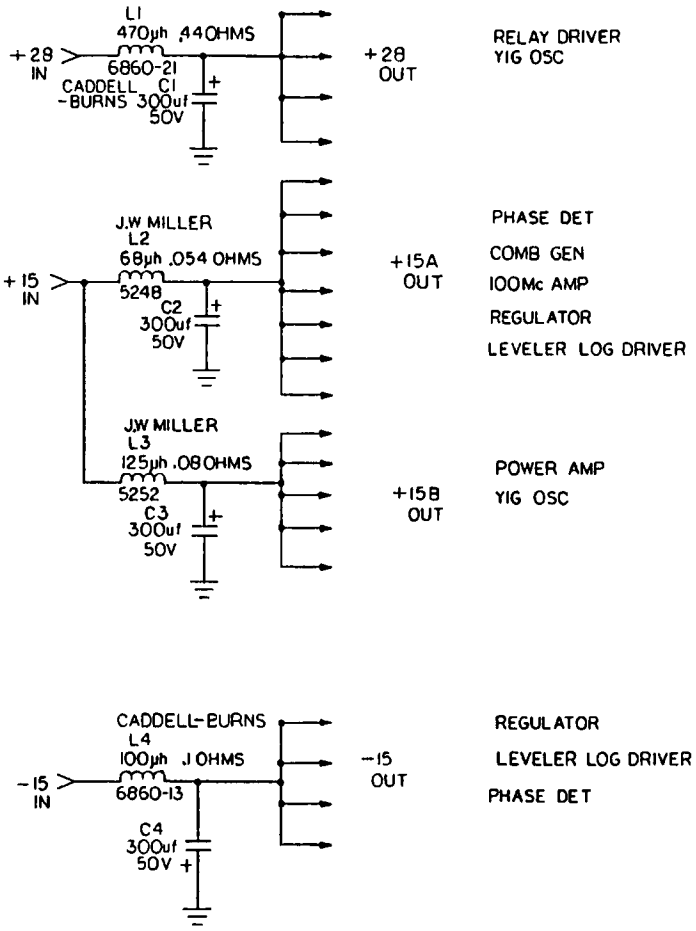
VLBA PROJECT: 2-16 GHz SYNTHESIZER

TITLE: PHASE DETECTOR

NATIONAL RADIO ASTRONOMY OBSERVATORY

DRAWN BY G.MORRIS DATE 9-86
DESIGNED BY DATE
APPROVED BY DATE

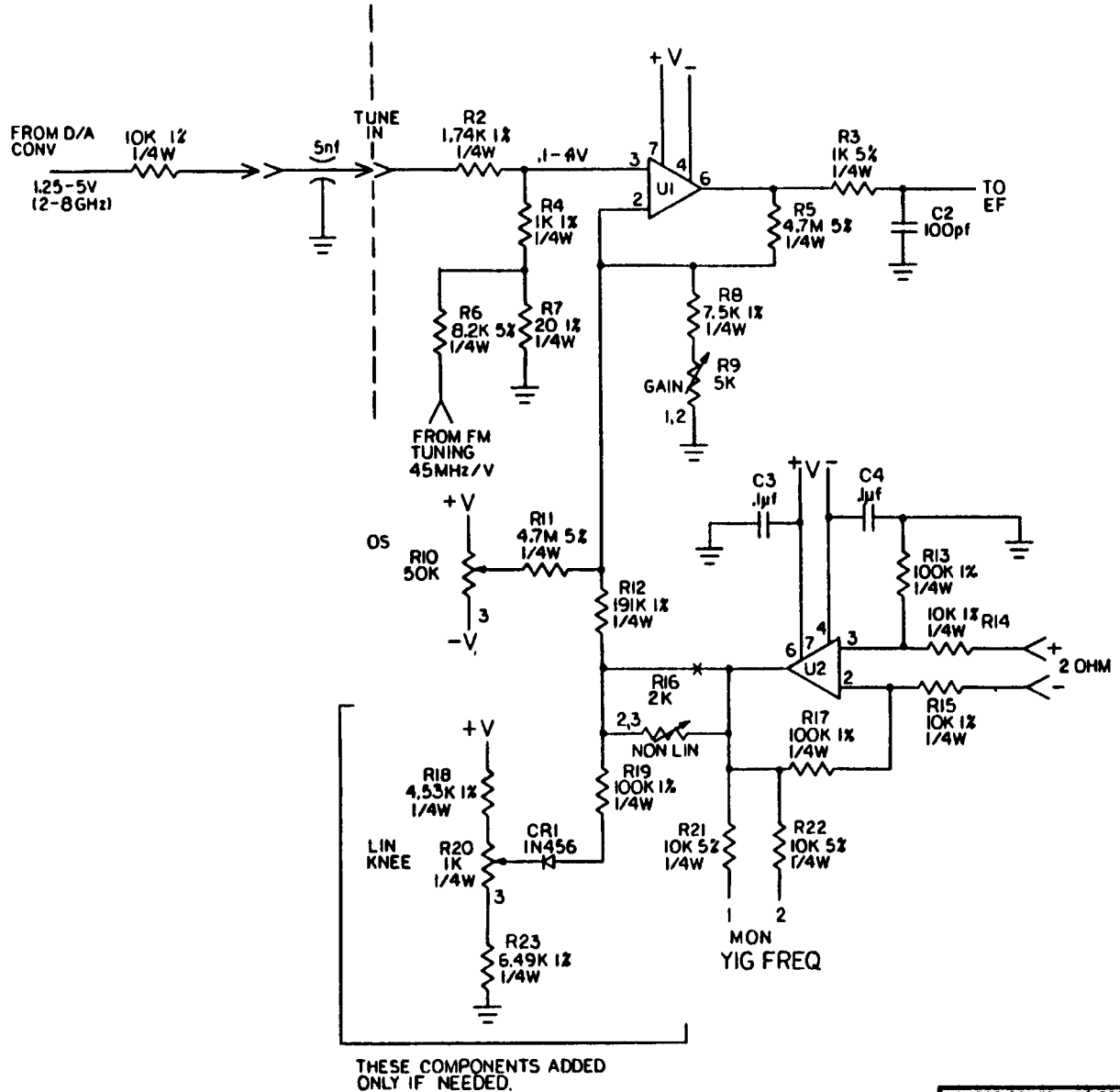
SHEET NUMBER | DRAWING NUMBER 9533002002 | REV. B | SCALE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	PROJECT: VLBA — 2-16 GHz SYNTHESIZER
MATERIAL:	TITLE: P.S. FILTER
FINISH:	DRAWN BY: G MORRIS — DATE: 9-86
NEXT ASSY / USED ON	DESIGNED BY — DATE
	APPROVED BY — DATE
	SHEET NUMBER — DRAWING NUMBER C533005003 — REV. — SCALE

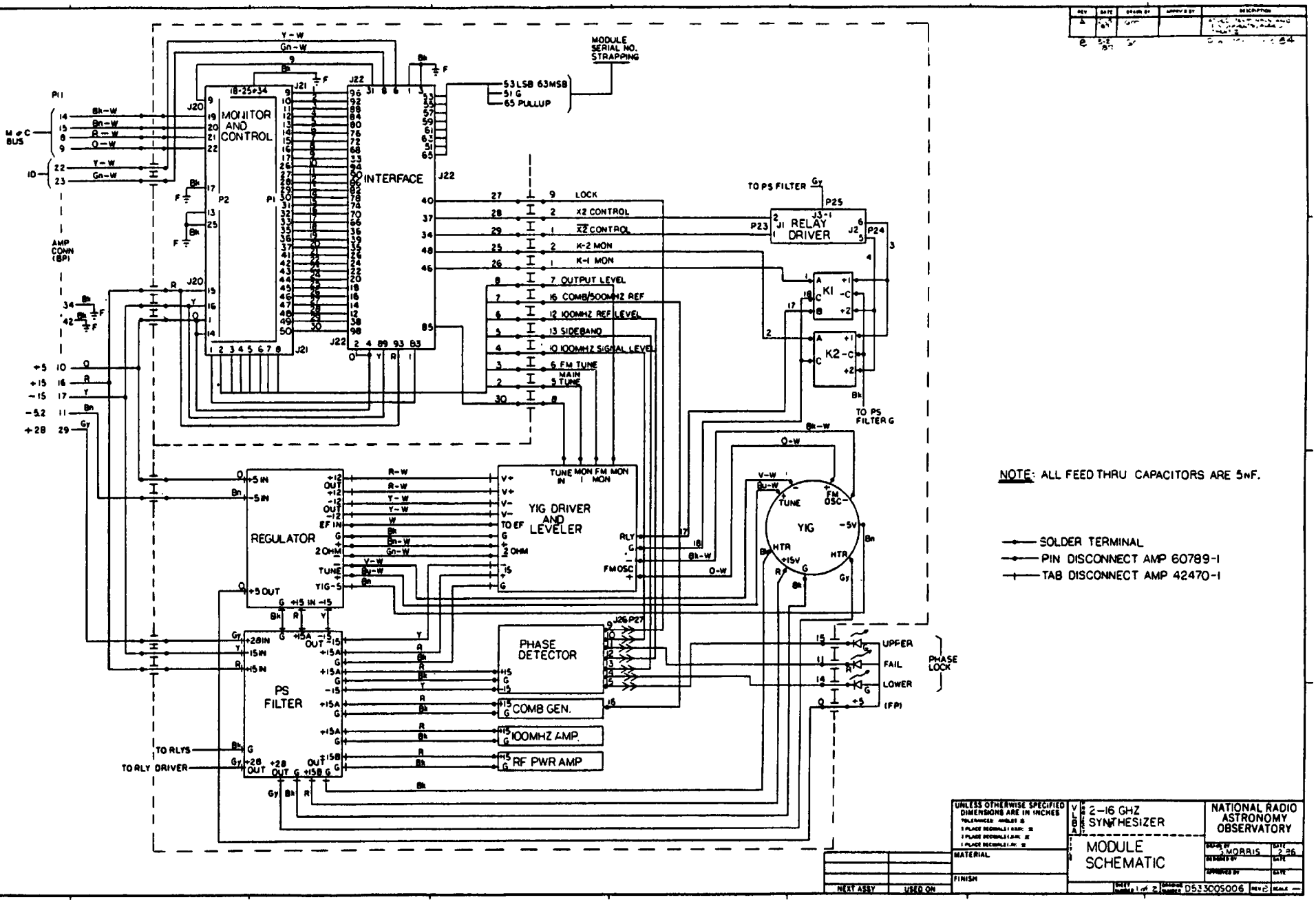
NATIONAL RADIO ASTRONOMY OBSERVATORY

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	2-24 87	GM		E2 WAS 15K 1% 1/4W E6 WAS 100K 5% 1/4W



NOTE
1. U1, U2 – HA-5135-5 OR OP-07CN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	VLBA SYSTEM 2-16 GHz SYNTHESIZER
MATERIAL:	TITLE YIG DRIVER AND LEVELER MAIN TUNING
FINISH:	NATIONAL RADIO ASTRONOMY OBSERVATORY
NEXT ASSY / USED ON	DRAWN BY G MORRIS DATE 9-86 DESIGNED BY DATE APPROVED BY DATE
	SHEET 1 of 3 DRAWING NUMBER C533005004 REV. A SCALE



REV	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION
A				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

FINISH

NEXT ASSY | USED ON

VLBA

2-16 GHZ SYNTHESIZER

MODULE SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY

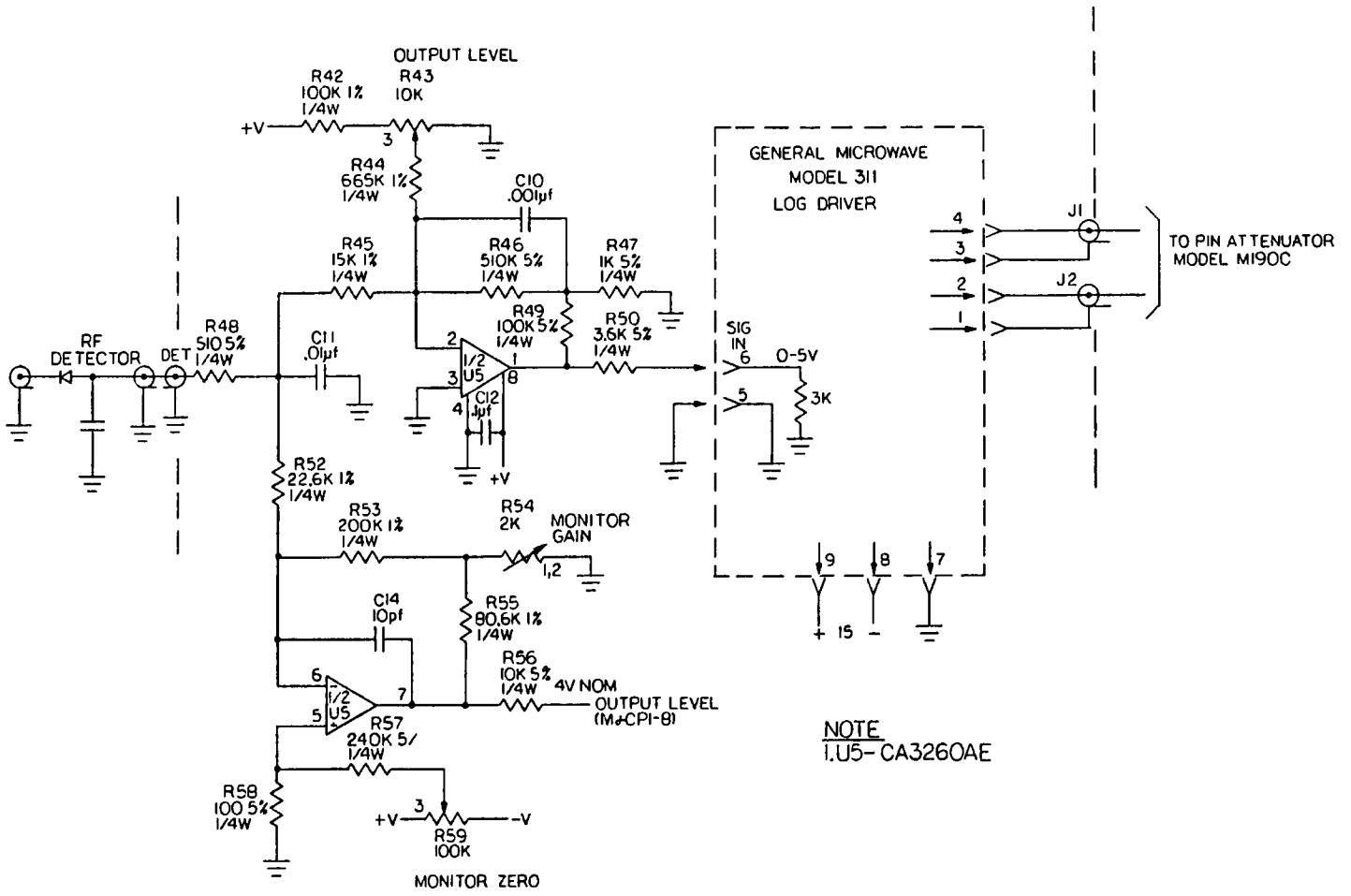
DRAWN BY J. MORRIS 2-26

CHECKED BY

APPROVED BY

SHEET 1 of 2 D53005006 REV E

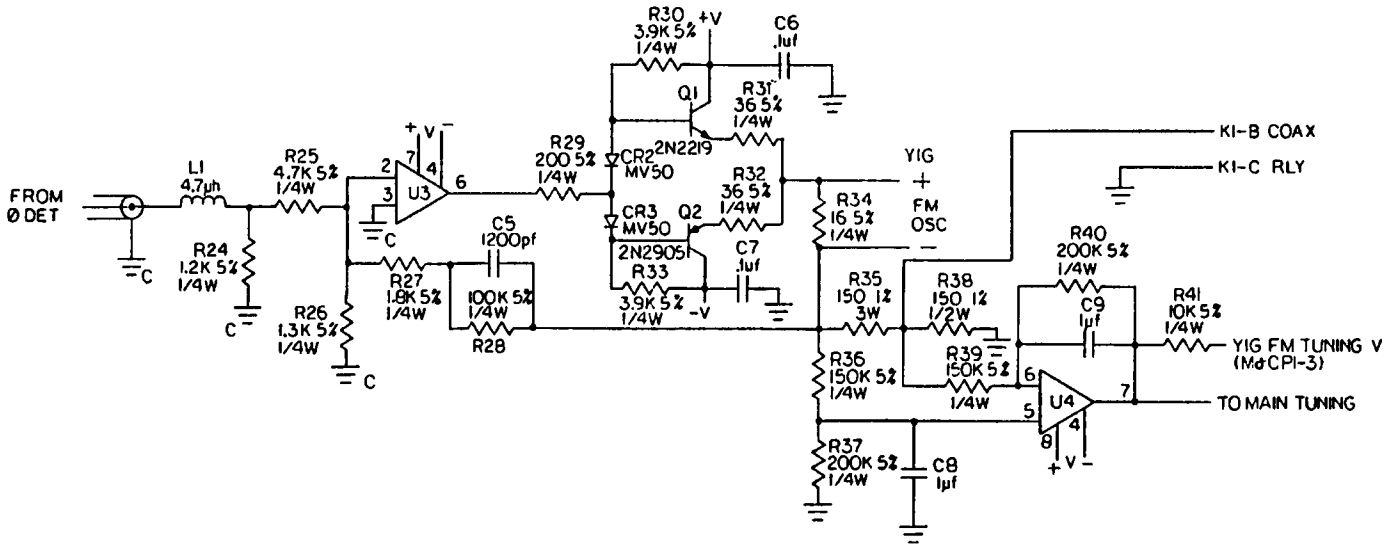
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	11-18-86	GM		REVISED REF DESIGNATIONS



NOTE
1. U5 - CA3260AE

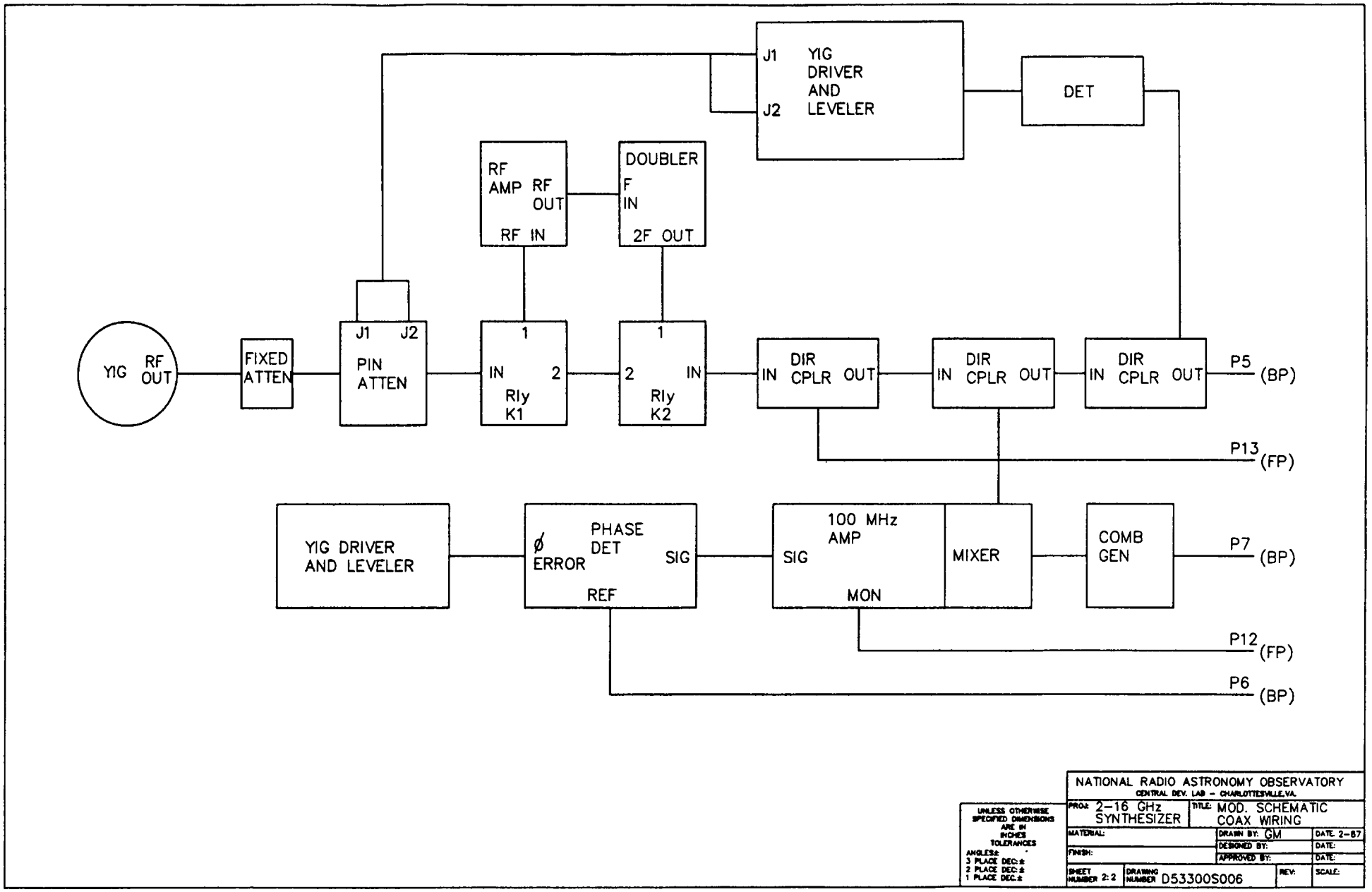
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	VLBA PROJECT: 2-16 GHz SYNTHESIZER	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL:	TITLE: YIG DRIVER AND LEVELER LEVELER	DRAWN BY G MORRIS DATE 9-86
FINISH:		DESIGNED BY DATE
NEXT ASSY / USED ON		APPROVED BY DATE
	SHEET NUMBER 3 of 3	DRAWING NUMBER C53005002A REV. A SCALE

REV.	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	11-18-86	GM		REVISED REF. DESIGNATIONS



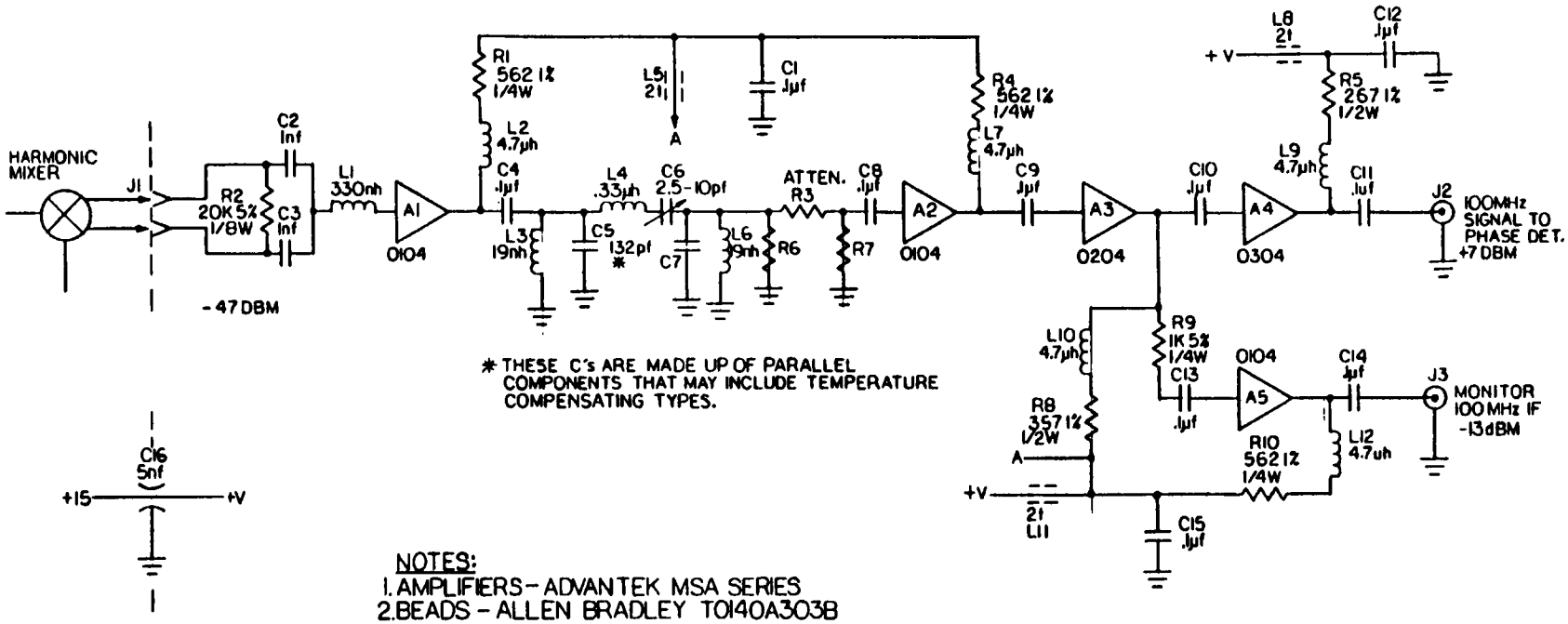
NOTES
1. U3-OP-27GN
2. U4-MC-34072P

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	PROJECT: VLBA 2-16 GHz SYNTHESIZER
MATERIAL:	TITLE: YIG DRIVER & LEVELER FM TUNING
FINISH:	NATIONAL RADIO ASTRONOMY OBSERVATORY
NEXT ASSY / USED ON	DRAWN BY G MORRIS DATE 9-86 DESIGNED BY DATE APPROVED BY DATE
	SHEET NUMBER 2 of 3 DRAWING NUMBER C533005004 REV. A SCALE



NATIONAL RADIO ASTRONOMY OBSERVATORY CENTRAL DEV. LAB – CHARLOTTESVILLE, VA.			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 3 PLACE DEC: ± 2 PLACE DEC: ± 1 PLACE DEC: ±	PROJ: 2–16 GHz SYNTHESIZER	TITLE: MOD. SCHEMATIC COAX WIRING	
	MATERIAL:	DRAWN BY: GM	DATE: 2-87
	FINISH:	DESIGNED BY:	DATE:
		APPROVED BY:	DATE:
	SHEET NUMBER 2:2	DRAWING NUMBER D53300S006	REV: SCALE:

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	1-15 86	GM		REVISED C6 & L4
B	2 24 87	GM		C1, C4 & R10 WAS 620 5% 1/4 W R5 WAS 300 5% 1/2 W R6 WAS 430 5% 1/2 W R7 WAS 20K 5% 1/4W



* THESE C's ARE MADE UP OF PARALLEL COMPONENTS THAT MAY INCLUDE TEMPERATURE COMPENSATING TYPES.

NOTES:
1. AMPLIFIERS - ADVANTEK MSA SERIES
2. BEADS - ALLEN BRADLEY T0140A303B
3. ATTEN. - ADJUSTED FOR +7 DBM AVERAGE OUTPUT AT J2 TYPICALLY 7 DB.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

NEXT ASSY	USED ON

VLBA PROJECT: 2-16 GHz SYNTHESIZER

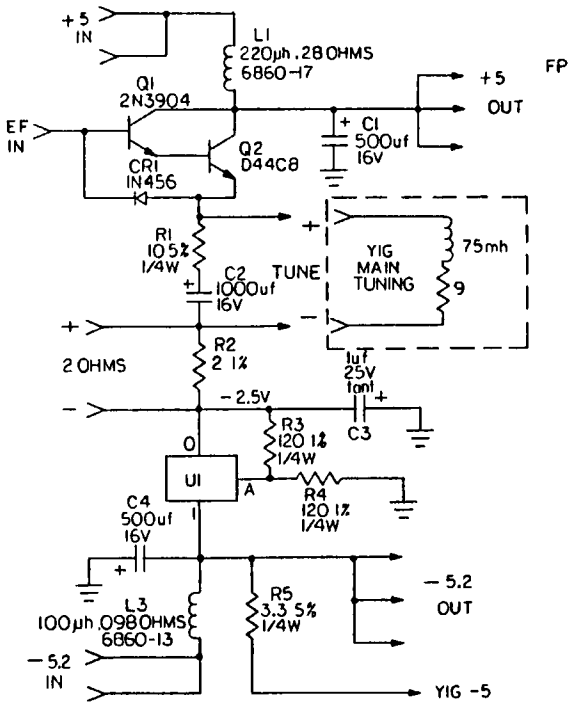
TITLE: 100 MHz AMPLIFIER

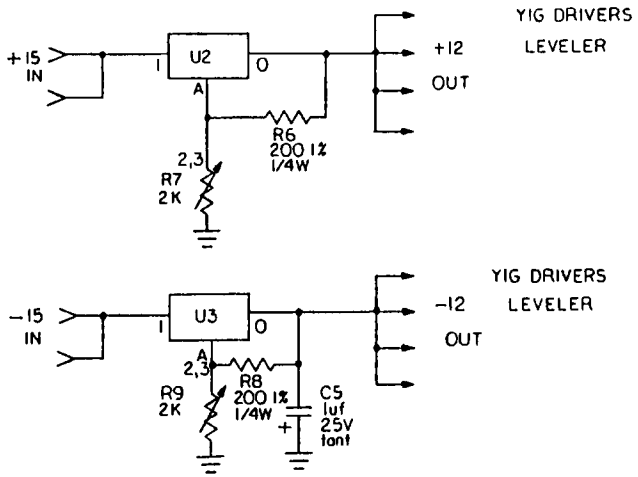
NATIONAL RADIO ASTRONOMY OBSERVATORY

DRAWN BY G MORRIS	DATE 9-29	
DESIGNED BY	DATE	
APPROVED BY	DATE	

SHEET NUMBER | DRAWING NUMBER C53300S007 | REV. B | SCALE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION





NOTES
1. CHOKES BY CADDELL-BURNS.
2. U1, U3 - LM337T
3. U2 - LM317T

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLBA PROJECT: 2-16 GHz SYNTHESIZER

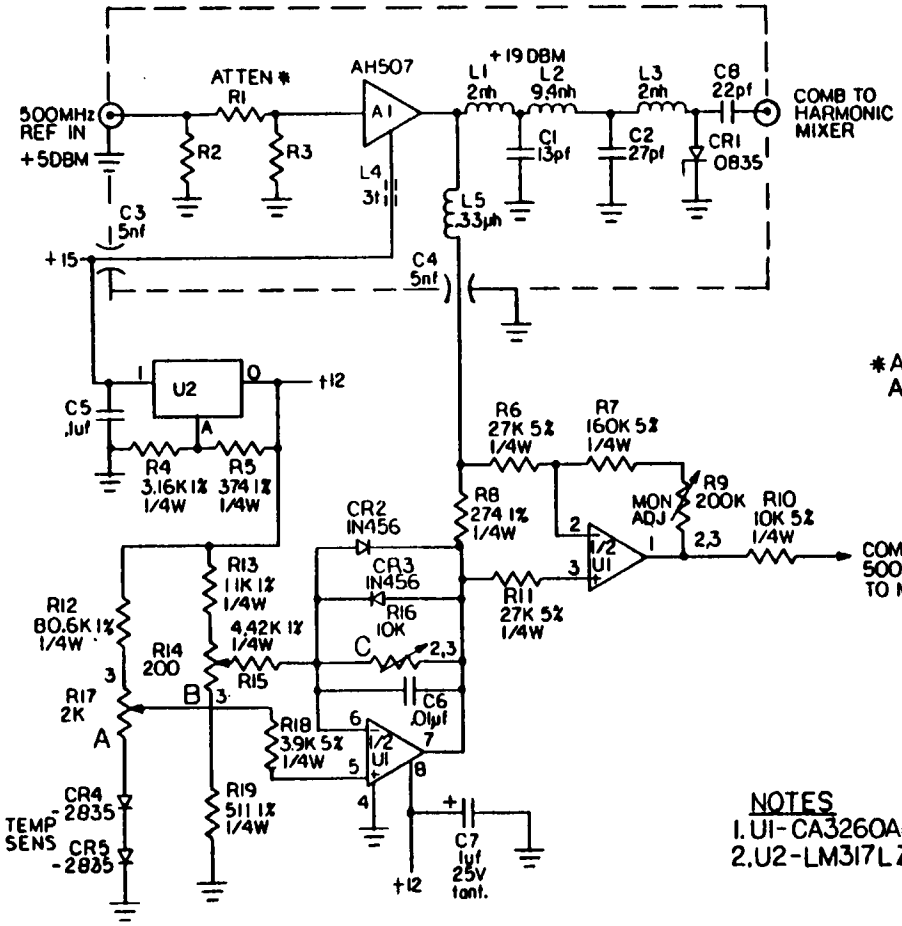
TITLE: REGULATOR

NATIONAL RADIO ASTRONOMY OBSERVATORY

DRAWN BY	G MORRIS	DATE	9-86
DESIGNED BY		DATE	
APPROVED BY		DATE	

SHEET NUMBER | DRAWING NUMBER C53005008 | REV | SCALE

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	11-18-86	GM		ADDED C8



*ADJUST FOR +19DBM AT AMPLIFIER OUTPUT.

NOTES
1. U1-CA3260AE OR MC34072
2. U2-LM317LZ

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

VLBA PROJECT: 2-16 GHz SYNTHESIZER

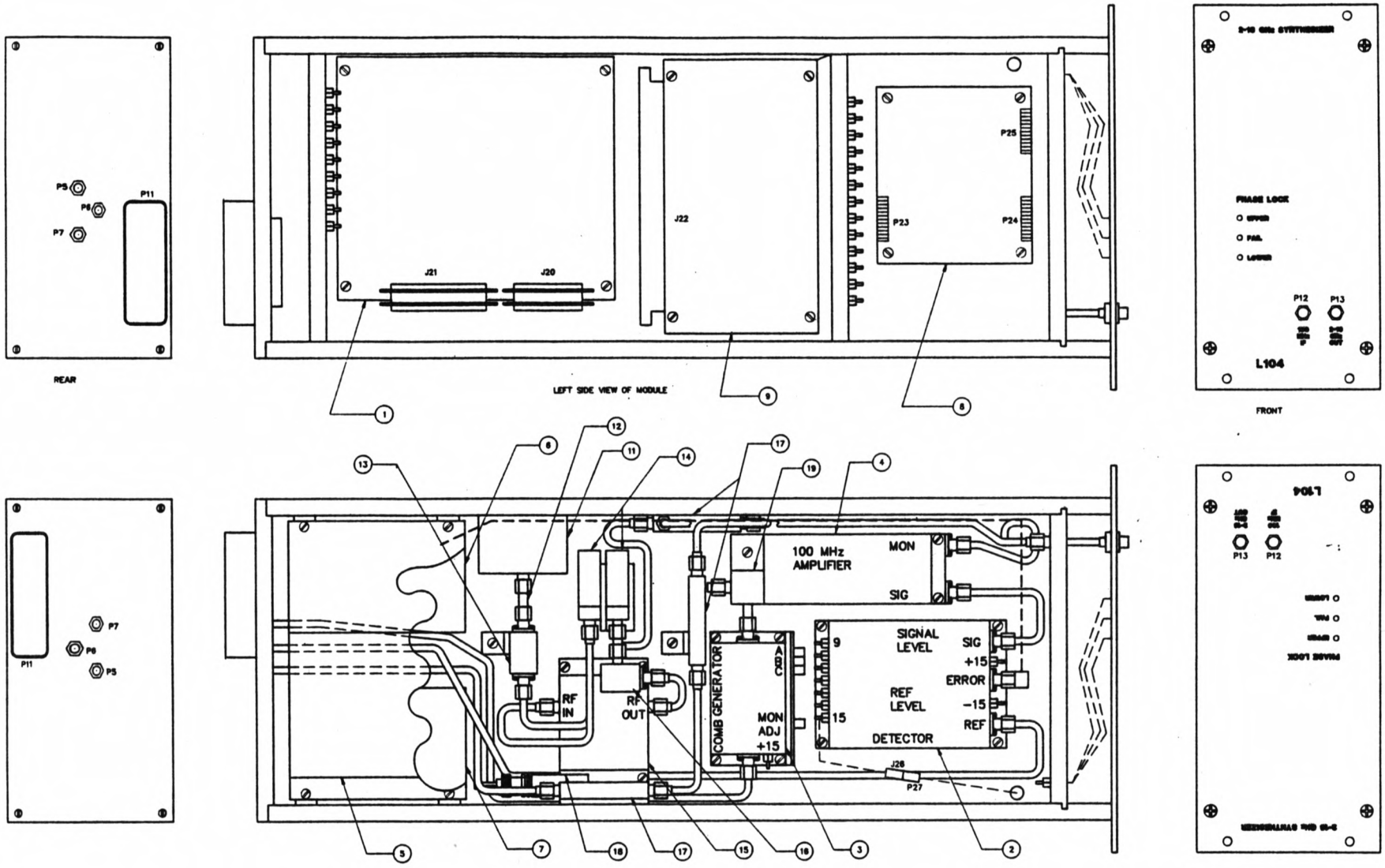
TITLE: COMB GENERATOR .

NATIONAL RADIO ASTRONOMY OBSERVATORY

DRAWN BY G MORRIS	DATE 9-86		
DESIGNED BY	DATE		
APPROVED BY	DATE		
SHEET NUMBER	DRAWING NUMBER C53005009	REV. A	SCALE

13.0 Assembly Drawing

Module.



REV	DATE	DRAWN BY	APPVD BY	DESCRIPTION

2-16 GHz SYNTHESIZER	NATIONAL RADIO ASTRONOMY OBSERVATORY	
2-16 GHz SYNTHESIZER ASSY	DRAWN BY: Gregers	DATE: 7-87
	CHECKED BY	DATE
	APPROVED BY	DATE
	03300A001 REV.	SCALE: 1:1

14.0 Bill of Materials

Module.

Phase Detector.

Comb Generator.

100 MHz Amplifier.

YIG Driver and Leveler.

Regulator.

Power Supply Filter.

Relay Driver.

Interface Card.

A53300B001-2-16 GHz SYNTHESIZER
BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY
VLBA

ITEM NUM.	MANUFACTURER	MANUFACTURER'S PART NUMBER	DESCRIPTION	QUAN. REQ.
1	NRAO		MONITOR AND CONTROL CARD	1
2	NRAO	A53300B003	PHASE DETECTOR	1
2		C53300S002	PHASE DETECTOR SCHEMATIC	
2		C533000Q001	PHASE DETECTOR PCB	1
2	NRAO	B53300M004	PHASE DETECTOR BOX	1
3	NRAO	A5330B004	COMB GENERATOR	1
3		C53300S009	COMB GENERATOR SCHEMATIC	
3		B533000Q006	COMB GENERATOR PCB	1
3		B533000Q009	COMB GENERATOR PCB	1
3	NRAO	B53300M005	COMB GENERATOR BOX	1
4	NRAO	A53300B005	100 MHz AMPLIFIER	1
4		C53300S007	100 MHz AMPLIFIER SCHEMATIC	
4		D533000Q008	100 MHz AMPLIFIER PCB	1
4	NRAO	B53300M009	100 MHz AMPLIFIER BOX	1
5	NRAO	A53300B006	YIG DRIVER AND LEVELER	1
5		C53300S004	YIG DRIVER AND LEVELER SCHEMATIC	
5		D533000Q002	YIG DRIVER AND LEVELER PCB	1
6	NRAO	A53300B007	REGULATOR	1
6		C53300S008	REGULATOR SCHEMATIC	
6		C533000Q003	REGULATOR PCB	1
7	NRAO	A53300B008	PS FILTER	1
7		C53300S003	PS FILTER SCHEMATIC	
7		C533000Q004	PS FILTER PCB	1
8	NRAO	A53300B009	RELAY DRIVER	1
8		B53300S001	RELAY DRIVER SCHEMATIC	
8		D533000Q007	RELAY DRIVER PCB	1
9	NRAO	A53300B010	INTERFACE	1
9		B53300L001	INTERFACE DIAGRAM	
10				
11	AVANTEK	Y085-2185	YIG	1
12	RLC ELECTRONICS	A-8-3RM	ATTEN,FIXED	1
13	GENERAL MICROWAVE	LM190C WITH DRV 311	ATTEN,PIN	1
14	TELEDYNE	CS-33SC6	RELAY,COAC	2
15	AYDIN MICROWAVE	AMA 4080B5	RF AMPLIFIER	1
16	TRW MICROWAVE	RX16000	DOUBLER	1
17	SAGE	C218-20	DIRECTIONAL COUPLER	3
18	TRW MICROWAVE	D18Z3	DETECTOR	1
19	H-P,SAMPLER	5088-7022	MIXER	1

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
** 53300 B003			
A1	Amplifier	AVANTEK	MSA-0104
A2	Amplifier	AVANTEK	MSA-0304
C1	Capacitor 1.2pf	ERIE	8101-100-C0K0-129B
C2	Capacitor .01uf	CENTRALAB	CY15C103P
C3	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C4	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C5	Capacitor 150pf	CENTRALAB	CW15A151K
C6	Capacitor 1nf	CENTRALAB	CW15A102K
C7	Capacitor 1nf	CENTRALAB	CW15A102K
C8	Capacitor .01uf	CENTRALAB	CY15C103P
C9	Capacitor .01uf	CENTRALAB	CY15C103P
C10	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C11	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C12	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C13	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C14	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C15	Capacitor .01uf	CENTRALAB	CY15C103P
C16	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C17	Capacitor .01uf	CENTRALAB	CY15C103P
C18	Capacitor .01uf	CENTRALAB	CY15C103P
C19	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C20	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C21	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C22	Capacitor .1uf	CENTRALAB	CY20C104P
C23	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C24	Capacitor .1uf	CENTRALAB	CY20C104P
C25	Capacitor 1uf 25V tant.	SPRAGUE	199D105X0025AA1
C26	Capacitor .01uf	CENTRALAB	CY15C103P
C27	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C28	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C29	Capacitor 3.3pf	ERIE	8101-100C0K0339B
CR1	1N456	AM POWER DEVICES	1N456
CR2	1N456	AM POWER DEVICES	1N456
CR3	1N456	AM POWER DEVICES	1N456
CR4	1N456	AM POWER DEVICES	1N456
CR5	1N456	AM POWER DEVICES	1N456
CR6	RED	HEWLETT-PACKARD	HLMP 1301
CR7	GRN	HEWLETT-PACKARD	HLMP 1501
CR8	1N456	AM POWER DEVICES	1N456
CR9	GRN	HEWLETT-PACKARD	HLMP 1501
CR10	1N456	AM POWER DEVICES	1N456
CR11	2835	HEWLETT-PACKARD	5082-2835
L1	Inductor 4.7uh	NYTRONICS	DD-4.70
L2	Inductor .1uh	NYTRONICS	DD-0.10
L3	Inductor .12uh	NYTRONICS	DD-0.12
L4	Inductor 1.2uh	NYTRONICS	DD-1.20
L5	Inductor .1uh	NYTRONICS	DD-0.10
L6	Inductor 4.7uh	NYTRONICS	DD-4.70
L7	Inductor .12uh	NYTRONICS	DD-0.12
M1	PHASE DETECTOR	MINI-CIRCUITS	RPD-1

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
M2	PHASE DETECTOR	MINI-CIRCUITS	RPD-1
R1	Resistor 15 1/4W 5%	ALLEN-BRADLEY	CB1505
R2	Resistor 562 1/4W 1%	CORNING	RN55D5620F
R3	Resistor 11.5K 1/4W 1%	CORNING	RN55D1152F
R4	Resistor 31.6K 1/4W 1%	CORNING	RN55D3162F
R5	100K TRIM	BOURNS	3329H-1-104
R6	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R7	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R8	Resistor 20K 1/4W 5%	ALLEN-BRADLEY	CB2035
R9	Resistor 51 1/4W 5%	ALLEN-BRADLEY	CB5105
R10	Resistor 51 1/4W 5%	ALLEN-BRADLEY	CB5105
R11	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R12	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R13	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R14	Resistor 15 1/4W 5%	ALLEN-BRADLEY	CB1505
R15	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R16	Resistor 20K 1/4W 5%	ALLEN-BRADLEY	CB2035
R17	Resistor 560 1/4W 5%	ALLEN-BRADLEY	CB5615
R18	Resistor 115 1/4W 1%	CORNING	RN55D1150F
R19	Resistor 287 1/4W 1%	CORNING	RN55D2870F
R20	Resistor 95.3 1/4W 1%	CORNING	RN55D95R3F
R21	Resistor 267 1/2W 1%	CORNING	RN60D2670F
R22	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R23	Resistor 42.2 1/4W 1%	CORNING	RN55D42R2F
R24	Resistor 16.5 1/4W 1%	CORNING	RN55D16R5F
R25	Resistor 20K 1/4W 5%	ALLEN-BRADLEY	CB2035
R26	Resistor 470 1/4W 5%	ALLEN-BRADLEY	CB4715
R27	Resistor 68.1 1/4W 1%	CORNING	RN55D68R1F
R28	Resistor 680 1/4W 5%	ALLEN-BRADLEY	CB6815
R29	Resistor 6.66K 1/4W 1%	CORNING	RN55D6661F
R30	Resistor 26.7K 1/4W 1%	CORNING	RN55D2672F
R31	100K TRIM	BOURNS	3329H-1-104
R32	Resistor 100K 1/4W 5%	ALLEN-BRADLEY	CB1045
R33	Resistor 100K 1/4W 5%	ALLEN-BRADLEY	CB1045
R34	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R35	Resistor 100K 1/4W 5%	ALLEN-BRADLEY	CB1045
R36	Resistor 20K 1/4W 5%	ALLEN-BRADLEY	CB2035
R37	Resistor 470 1/4W 5%	ALLEN-BRADLEY	CB4715
R38	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R39	Resistor 3.16K 1/4W 1%	CORNING	RN55D3161F
R40	Resistor 374 1/4W 1%	CORNING	RN55D3740F
R41	Resistor 3.16K 1/4W 1%	CORNING	RN55D3161F
R42	Resistor 374 1/4W 1%	CORNING	RN55D3740F
U1	LF412CN	NATIONAL	LF412CN
U2	LF412CN	NATIONAL	LF412CN
U3	LM317LZ	NATIONAL	LM317LZ
U4	LM337LZ	NATIONAL	LM337LZ

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
** 53300 B004			
A1	Amplifier	ALPHA	AH507
C1	Capacitor 13pf Chip	DIELECTRIC LABS	M17AH130K4SXL
C2	Capacitor 27pf Chip	DIELECTRIC LABS	M17AH270K4SXL
C3	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C4	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C5	Capacicor .1uf	CENTRALAB	CY20C104P
C6	Capacitor .01uf	CENTRALAB	CY15C103F
C7	Capacitor 1uf 25V tant.	SPRAGUE	199D1W5X0025AA1
C8	Capacitor 22pf Chip	AM. TECH. CERAMICS	100A220JP
CR1	0835	HEWLETT-PACKARD	5082-0835
CR2	1N456	AM POWER DEVICES	1N456
CR3	1N456	AM POWER DEVICES	1N456
CR4	2835	HEWLETT-PACKARD	5082-2835
CR5	2835	HEWLETT-PACKARD	5082-2835
L1	Inductor 2nh	NRAO	BRASS STRIP .15 LONG
L2	Inductor 9.4nh	NRAO	BRASS STRIP .6 LONG
L3	Inductor 2nh	NRAO	BRASS STRIP .15 LONG
L4	Inductor 3 Turns	NRAO	ABT0140A3035
L5	Inductor .33uh	NYTRONICS	DD-0.33
R1	Value Determined During Manufacture	ALLEN-BRADLEY	CB___5
R2	Value Determined During Manufacture	ALLEN-BRADLEY	CB___5
R3	Value Determined During Manufacture	ALLEN-BRADLEY	CB___5
R4	Resistor 3.16K 1/4W 1%	CORNING	RN55D3161F
R5	Resistor 374 1/4W 1%	CORNING	RN55D3740F
R6	Resistor 27K 1/4W 5%	ALLEN-BRADLEY	CB2735
R7	Resistor 160K 1/4W 5%	ALLEN-BRADLEY	CB1645
R8	Resistor 274 1/4W 1%	CORNING	RN55D2740F
R9	200K TRIM	BOURNS	3006P-1-204
R10	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R11	Resistor 27K 1/4W 5%	ALLEN-BRADLEY	CB2735
R12	Resistor 80.6K 1/4W 1%	CORNING	RN55D8062F
R13	Resistor 11K 1/4W 1%	CORNING	RN55D1102F
R14	200 TRIM	BOURNS	3006P-1-201
R15	Resistor 4.42K 1/4W 1%	CORNING	RN55D4421F
R16	10K TRIM	BOURNS	3006P-1-103
R17	2K TRIM	BOURNS	3006P-1-202
R18	Resistor 3.9K 1/4W 5%	ALLEN-BRADLEY	CB3925
R19	Resistor 511 1/4W 1%	CORNING	RN55D5110F
U1	CA3260AE	RCA	CA3260AE
U2	LM317LZ	NATIONAL	LM317LZ

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
++ 53300 B005			
A1	Amplifier	AVANTEK	MSA-0104
A2	Amplifier	AVANTEK	MSA-0104
A3	Amplifier	AVANTEK	MSA-0304
A4	Amplifier	AVANTEK	MSA-0304
A5	Amplifier	AVANTEK	MSA-0104
C1	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C2	Capacitor 1nf	CENTRALAB	CH15A102K
C3	Capacitor 1nf	CENTRALAB	CH15A102K
C4	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C5	Capacitor 132pf	CENTRALAB	CH15A- 101J & 330J
C6	Capacitor 2.5-10pf	JOHANSON	9622
C7	Capacitor 132pf	CENTRALAB	CH15A- 101J & 330J
C8	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C9	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C10	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C11	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C12	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C13	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C14	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C15	Capacitor .1uf Chip	CENTRALAB	W050FH104M
C16	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
J1	Socket	AUGAT	8060-166
J2	Coax Connector	APPLIED ENG. PRDTS.	
J3	Coax Connector	APPLIED ENG. PRDTS.	
L1	Inductor 330nh	NYTRONICS	DD-0.33
L2	Inductor 4.7uh	NYTRONICS	DD-4.70
L3	Inductor 19nh	NRAO	3 TURNS #22
L4	Inductor .33uh	NYTRONICS	DD-0.33
L5	Inductor 2 Turns	NRAO	ABT0140A303B
L6	Inductor 19nh	NRAO	3 TURNS #22
L7	Inductor 4.7uh	NYTRONICS	DD-4.70
L8	Inductor 2 Turns	NRAO	ABT0140A303B
L9	Inductor 4.7uh	NYTRONICS	DD-4.70
L10	Inductor 4.7uh	NYTRONICS	DD-4.70
L11	Inductor 2 Turns	NRAO	ABT0140A303B
L12	Inductor 4.7uh	NYTRONICS	DD-4.70
R1	Resistor 562 1/4W 1%	CORNING	RN55D5620F
R2	Resistor 20K 1/8W 5%	ALLEN-BRADLEY	EB2035
R3	Value Determined During Manufacture	ALLEN-BRADLEY	CB__5
R4	Resistor 562 1/4W 1%	CORNING	RN55D5620F
R5	Resistor 267 1/2W 1%	CORNING	RN60D2670F
R6	Value Determined During Manufacture	ALLEN-BRADLEY	CB__5
R7	Value Determined During Manufacture	ALLEN-BRADLEY	CB__5
R8	Resistor 357 1/2W 1%	ALLEN-BRADLEY	RN60D3570F
R9	Resistor 1K 1/4W 5%	ALLEN-BRADLEY	CB1025
R10	Resistor 562 1/4W 1%	CORNING	RN55D5620F

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
++ 53300 B006-1			
C2	Capacitor 100pf	CENTRALAB	CN15A101K
C3	Capacitor .1uf	CENTRALAB	CY20C104P
C4	Capacitor .1uf	CENTRALAB	CY20C104P
CR1	1N456	AM POWER DEVICES	1N456
R2	Resistor 1.74K 1/4W 1%	CORNING	RN55D1741F
R3	Resistor 1K 1/4W 5%	ALLEN-BRADLEY	CB1025
R4	Resistor 1K 1/4W 1%	CORNING	RN55D1001F
R5	Resistor 4.7M 1/4W 5%	ALLEN-BRADLEY	CB4755
R6	Resistor 8.2K 1/4W 5%	ALLEN-BRADLEY	CB8225
R7	Resistor 20 1/4W 1%	CORNING	RN55D20R0F
R8	Resistor 7.5K 1/4W 1%	CORNING	RN55D7501F
R9	5K TRIM	BOURNS	3299W-1-502
R10	50K TRIM	BOURNS	3299W-1-503
R11	Resistor 4.7M 1/4W 5%	ALLEN-BRADLEY	CB4755
R12	Resistor 191K 1/4W 1%	CORNING	RN55D1913F
R13	Resistor 100K 1/4W 1%	CORNING	RN55D1003F
R14	Resistor 10K 1/4W 1%	CORNING	RN55D1002F
R15	Resistor 10K 1/4W 1%	CORNING	RN55D1002F
R16	2K TRIM	BOURNS	3299W-1-202
R17	Resistor 100K 1/4W 1%	CORNING	RN55D1003F
R18	Resistor 4.53K 1/4W 1%	CORNING	RN55D4531F
R19	Resistor 100K 1/4W 1%	CORNING	RN55D1003F
R20	1K TRIM	BOURNS	3299W-1-102
R21	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R22	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R23	Resistor 6.49K 1/4W 1%	CORNING	RN55D6491F
U1	OP-07C	ANALOG DEVICES	ADOP-07CN
U2	OP-07C	ANALOG DEVICES	ADOP-07CN

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
** 53300 B006-2			
C5	Capacitor 1200pf	CENTRALAB	CW15C122K
C6	Capacitor .1uf	CENTRALAB	CY20C104P
C7	Capacitor .1uf	CENTRALAB	CY20C104P
C8	Capacitor 1uf	ELECTROCUBE	e50B1A105K
C9	Capacitor 1uf	ELECTROCUBE	e50B1A105K
CR1	MV50	GENERAL INSTRUMENTS	MV50
CR2	MV50	GENERAL INSTRUMENTS	MV50
Q1	Transistor 2N 2219	MOTOROLA	2N 2219
Q2	Transistor 2N 2905	MOTOROLA	2N 2965
R24	Resistor 1.2K 1/4W 5%	ALLEN-BRADLEY	CB1225
R25	Resistor 4.7K 1/4W 5%	ALLEN-BRADLEY	CB4725
R26	Resistor 1.3K 1/4W 5%	ALLEN-BRADLEY	CB1325
R27	Resistor 1.8K 1/4W 5%	ALLEN-BRADLEY	CB1825
R28	Resistor 100K 1/4W 5%	ALLEN-BRADLEY	CB1045
R29	Resistor 200 1/4W 5%	ALLEN-BRADLEY	CB2015
R30	Resistor 3.9K 1/4W 5%	ALLEN-BRADLEY	CB3925
R31	Resistor 36 1/4W 5%	ALLEN-BRADLEY	CB3605
R32	Resistor 36 1/4W 5%	ALLEN-BRADLEY	CB3605
R33	Resistor 3.9K 1/4W 5%	ALLEN-BRADLEY	CB3925
R34	Resistor 16 1/4W 5%	ALLEN-BRADLEY	CB1605
R35	Resistor 150 3W 1%	DALE	RS-2B
R36	Resistor 150K 1/4W 5%	ALLEN-BRADLEY	CB1545
R37	Resistor 200K 1/4W 5%	ALLEN-BRADLEY	CB2045
R38	Resistor 150 1/2W 1%	DALE	RN65D1500F
R39	Resistor 150K 1/4W 5%	ALLEN-BRADLEY	CB1545
R40	Resistor 200K 1/4W 5%	ALLEN-BRADLEY	CB2045
R41	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
U3	OP-27GN	ANALOG DEVICES	ADOP-27GN
U4	MC-34072-P	MOTOROLA	MC-34072-P

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
++ 53300 E006-3			
C10	Capacitor .001uf	CENTRALAB	CW15C102K
C11	Capacitor .01uf	CENTRALAB	CY15C103P
C12	Capacitor .1uf	CENTRALAB	CY20C104P
C14	Capacitor 10pf	CENTRALAB	CN15A100K
R42	Resistor 100K 1/4W 1%	CORNING	RN55D1003F
R43	10K TRIM	BOURNS	3006P-1-103
R44	Resistor 665K 1/4W 1%	CORNING	RN55D6653F
R45	Resistor 15K 1/4W 1%	CORNING	RN55D1502F
R46	Resistor 510 1/4W 5%	ALLEN-BRADLEY	CB5115
R47	Resistor 1K 1/4W 5%	ALLEN-BRADLEY	CB1025
R48	Resistor 510 1/4W 5%	ALLEN-BRADLEY	CB5115
R49	Resistor 100K 1/4W 5%	ALLEN-BRADLEY	CB1045
R50	Resistor 3.6K 1/4W 5%	ALLEN-BRADLEY	CB3625
R51			
R52	Resistor 22.6K 1/4W 1%	CORNING	RN55D2262F
R53	Resistor 200K 1/4W 1%	CORNING	RN55D2003F
R54	2K TRIM	BOURNS	3006P-1-202
R55	Resistor 80.6K 1/4W 1%	CORNING	RN55D8062F
R56	Resistor 10K 1/4W 5%	ALLEN-BRADLEY	CB1035
R57	Resistor 240K 1/4W 5%	ALLEN-BRADLEY	CB2445
R58	Resistor 100 1/4W 5%	ALLEN-BRADLEY	CB1015
R59	100K TRIM	BOURNS	3329H-1-104
U5	CA3260AE	RCA	CA3260AE

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
++ 53300 B007			
C1	Capacitor 500uf	SPRAGUE	TVA-1162
C2	Capacitor 1000uf	SPRAGUE	TVA-1163
C3	Capacitor 1uf 25V tant.	SPRAGUE	199D105X0025AA1
C4	Capacitor 500uf	SPRAGUE	TVA-1162
C5	Capacitor 1uf 25V tant.	SPRAGUE	199D105X0025AA1
CR1	1N456	AM POWER DEVICES	1N456
L1	Inductor 220uh	CADDELL-BURNS	6866-17
L2			
L3	Inductor 100uh	CADDELL-BURNS	6860-13
Q1	Transistor 2N 3904	MOTOROLA	2N 3904
Q2	Transistor D44C8	GENERAL ELECTRIC	D44C8
R1	Resistor 10 1/4W 5%	ALLEN-BRADLEY	CB1005
R2	Resistor 2 3W 1%	DALE	RS 2B
R3	Resistor 120 1/4W 1%	CORNING	RN55D1200F
R4	Resistor 120 1/4W 1%	CORNING	RN55D1200F
R5	Resistor 3.3 1/4W 5%	ALLEN-BRADLEY	CB3R35
R6	Resistor 200 1/4W 1%	CORNING	RN55D2000F
R7	2K TRIM	BOURNS	3006P-1-202
R8	Resistor 200 1/4W 1%	CORNING	RN55D2000F
R9	2K TRIM	BOURNS	3006P-1-202
U1	LM337T	MOTOROLA	LM337T
U2	LM317T	MOTOROLA	LM317T
U3	LM337T	MOTOROLA	LM337T

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
++ 53300 B008			
C1	Capacitor 300uf 50V	MALLORY	TT50M300A
C2	Capacitor 300uf 50V	MALLORY	TT50M300A
C3	Capacitor 300uf 50V	MALLORY	TT50M300A
C4	Capacitor 300uf 50V	MALLORY	TT50M300A
L1	Inductor 470uh	CADDELL-BURNS	6860-21
L2	Inductor 68uh	J W MILLER	5248
L3	Inductor 125uh	J W MILLER	5252
L4	Inductor 100uh	CADDELL-BURNS	6860-13

BILL OF MATERIALS

ITEM	DESCRIPTION	MANUFACTOR	PART NUMBER
** 53300 B009			
C1	Capacitor 1uf	ELECTROCUBE	650B1A105K
C2	Capacitor 1uf	ELECTROCUBE	650B1A105K
C3	Capacitor 5nf	TUSONIX	2425-001-X5W0-502AA
C4	Capacitor 1uf	ELECTROCUBE	650B1A105K
C5	Capacitor .1uf	CENTRALAB	CY20C104Z
CR1	1N456	AM POWER DEVICES	1N456
CR2	1N4001	INT'L RECTIFIER	1N4001
CR3	1N456	AM POWER DEVICES	1N456
CR4	1N4001	INT'L RECTIFIER	1N4001
Q1	Transistor 2N 3904	MOTOROLA	2N 3904
Q2	Transistor 2N 2905	MOTOROLA	2N 2905
Q3	Transistor 2N 3904	MOTOROLA	2N 3904
Q4	Transistor 2N 2905	MOTOROLA	2N 2905
R1	Resistor 15K 1/4W 5%	ALLEN-BRADLEY	CB1535
R2	Resistor 9.1K 1/4W 5%	ALLEN-BRADLEY	CB9125
R3	Resistor 13K 1/4W 5%	ALLEN-BRADLEY	CB1335
R4	Resistor 1M 1/4W 5%	ALLEN-BRADLEY	CB1055
R5	Resistor 13K 1/4W 5%	ALLEN-BRADLEY	CB1335
R6	Resistor 15K 1/4W 5%	ALLEN-BRADLEY	CB1535
R7	Resistor 9.1K 1/4W 5%	ALLEN-BRADLEY	CB9125
R8	Resistor 13K 1/4W 5%	ALLEN-BRADLEY	CB1335
R9	Resistor 1M 1/4W 5%	ALLEN-BRADLEY	CB1055
R10	Resistor 13K 1/4W 5%	ALLEN-BRADLEY	CB1335

A53300B010-INTERFACE CARD
BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY
VLBA

ITEM NUM.	MANUFACTURER	MANUFACTURER'S PART NUMBER	DESCRIPTION
U1		7425N	DUAL INPUT NOR GATE
U2		74LS04	HEX INVERTER
U3		74LS244	OCTAL BUFFER
U4		74LS374	OCTAL D-TYPE FLIP FLOP
U5		74LS374	OCTAL D-TYPE FLIP FLOP
U6		NE555	TIMER
U7		74LS20	NAND GATE
U8	BOURNS	4114R-002	2K RES. NET.
U9		74LS244	OCTAL BUFFER
U10		74LS157	2 TO 1 LINE DATA SELECT
U11		74LS157	2 TO 1 LINE DATA SELECT
U12		74LS157	2 TO 1 LINE DATA SELECT
U13		74LS20	NAND GATE
U14		74LS00	NAND GATE
U15		74LS280	9 BIT PARITY GENERATOR
U16		NE555	TIMER
U17		74LS283	4 X 4 BIT PARALLEL MULTIPLIER
U18		74LS283	4 X 4 BIT PARALLEL MULTIPLIER
U19		74LS283	4 X 4 BIT PARALLEL MULTIPLIER
U20	GRAYHILL	78RB07	DIP SWITCH
U21	BOURNS	4114R-002	2K RES. NET.
U22	CAMBION	702-3728-01-03	16 PIN CARRIER
U22	CENTRALAB	CY20C104P	CAP. .1uF PINS 3-14
U22	ALLEN-BRADLEY	CB5135	RES. 47K 1/4W 5% PINS 4-13
U22	ALLEN-BRADLEY	CB4735	RES. 47K 1/4W 5% PINS 5-12
U22	CENTRALAB	CY15C103P	CAP. .01uF PINS 6-11
U23		74LS04	HEX INVERTER
U24		74LS04	HEX INVERTER
U25	ANALOG DEVICES	AD DAC80N-CB1-V	D/A CONVERTER
U26		74LS197	PRESETABLE BINARY COUNTER
U27		74LS197	PRESETABLE BINARY COUNTER
U28		74LS86	EXCLUSIVE OR GATE
U29		74LS86	EXCLUSIVE OR GATE
U30		74LS244	OCTAL BUFFER
U31	SAMTEC	TS-1-20-T-D-1-2	10 PIN CARRIER
U31	CORNING	RN55D1002F	RES. 10K 1/4W 1% PINS 6-10
U31	CORNING	RN55D1002F	RES. 10K 1/4W 1% PINS 7-10
U31	CORNING	RN55D1002F	RES. 10K 1/4W 1% PINS 5-2
U31		2N3904	TRANS. PINS 3-2-1
U32	ALLEN-BRADLEY	CB2055	RES. 2M 1/4W 5% PINS 1-4
U32	ELECTROCUBE	650D1A104	CAP. .1uF PINS 2-3
U33	CENTRALAB	CY15C103P	CAP. .01uF

15.0 Data Sheets

YIG.

Fixed Attenuator.

Pin Attenuator.

Coax Relay.

Power Amplifier.

Doubler.

Directional Coupler.

Diode Detector.

Phase Detector.

OP-07 Op Amp.

D44C8 Power Transistor.

OP-27 Op Amp.

DAC-80 N D/A Converter.

MSA-0104 Amplifier.

MSA-0204 Amplifier.

MSA-0304 Amplifier.

LM317T Regulator.

LM317L Regulator.

LM337T Regulator.

LM337L Regulator.

LF 412 Op Amp.

AH 507 Amplifier.

HP -0835 Step Recovery Diode.

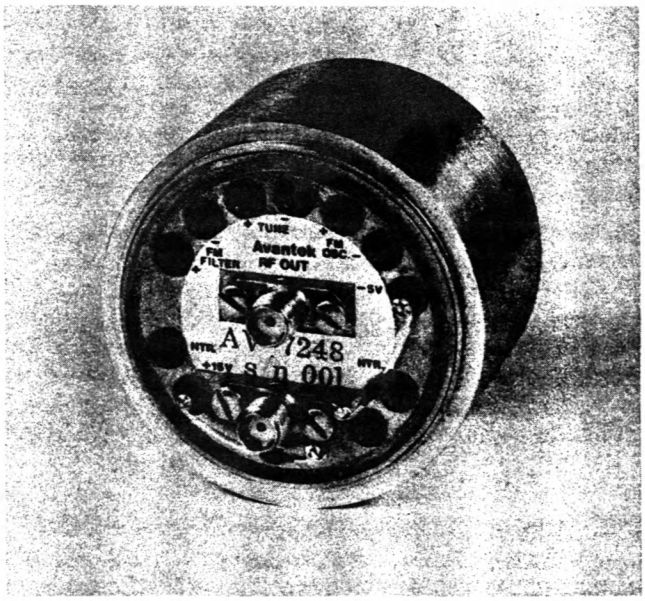
CA-3260AE Op Amp.

MC-34072AE Op Amp.

Avantek

DATA SHEET

2 to 8 GHz
YIG-tuned Oscillator
With Integral YIG Filter
AV-7248
August, 1980



FEATURES

- **−40 dBc Maximum Harmonics**
- **30 mW Mininum Output Power**
- **Automatic Filter Tracking[1]**
- **±0.1% Tuning Linearity**
- **FM/Phase-Lock Port**
- **Rugged, Hermetic Package**
- **Gold Thin-Film Hybrid Construction**

DESCRIPTION

The Avantek® AV-7248 is a fundamental-output, buffered YIG-tuned transistor oscillator with an integral tracking YIG filter providing −40 dBc maximum harmonic output over the 2 to 8 GHz frequency range. It offers +14.8 dBm (30 mW) minimum output power with ±3.0 dB maximum variation and ±0.1% tuning linearity over the full operating band. This complete YIG-tuned silicon bipolar transistor oscillator, two-stage GaAs FET buffer amplifier and high-Q tracking YIG filter is packaged in a compact, hermetic case with a 2 inch diameter and 1.4 inch length[2], weighing approximately 17 oz.

An AV-7248 is ideal as the swept signal source in a laboratory signal generator due to its low harmonic output, extremely linear tuning curve and excellent frequency resettability. It may also be used as a local oscillator in spectrum analyzers and microwave receivers.

EASY TO APPLY

In the AV-7248, both the frequency-determining oscillator YIG sphere and the filter YIG sphere are under the same pole piece in the same magnetic circuit. Since the mechanical configuration of the magnetic circuit is carefully optimized, the tracking between oscillator and filter is inherently very close. For most applications, the unit is simply used as a conventional YIG-tuned transistor oscillator and no further design work is required. However, by applying current to the special filter fine-tuning (FM) coil provided on the AV-7248, the output power may be increased by approximately 1 dB at a particular frequency (approximately 100 mA at 8 GHz). This current may be fixed—for example to peak the output power at the high end of the frequency range to overcome external circuit losses—or swept with the main tuning current as desired.

As with all other Avantek AV-7000 Series YIG-tuned oscillators, the AV-7248 also includes a low-inductance FM tuning coil as a standard feature. This small coil is in close proximity to the YIG sphere and may be used to fine-tune the oscillator frequency, to phase lock the oscillator or to frequency modulate the output signal. The tuning sensitivity of this coil is less than that of the main tuning coil, but it has a 400 KHz, 3 dB bandwidth and can vary the output frequency as much as 40 MHz at 400 KHz rate.

BUILT FOR CONSISTENCY AND RELIABILITY

All Avantek YIG-tuned transistor oscillators, both commercial and military versions, share a number of unique construction features which improves their performance and helps assure long term reliability under severe operating conditions. The oscillator and buffer circuitry is fabricated with gold thin-film microstripline conductors and tantalum nitride thin-film resistors deposited on a precision ceramic substrate. The oscillator and buffer transistors and all capacitors are in unpackaged chip form, bonded directly to gold pads on the substrate to minimize parasitic reactances and assure good heat dissipation. To assure frequency stability under both high

[1] A filter fine-tuning port is incorporated in the oscillator. See text.

[2] Less connectors. 2.12 inch diameter, 2.12 in. length with optional mu-metal magnetic shield.

vibration conditions and with ambient temperature changes, the YIG spheres are mounted on a mechanically stable nonconducting rod to locate them in their optimum positions within the magnetic field and coupling loops. The sphere temperature is controlled by a self-regulating positive temperature coefficient heater.

AVANTEK TRANSISTORS THROUGHOUT

Avantek designs and manufactures its own silicon bipolar and GaAs field effect transistors specifically for this oscillator and buffer application. Avantek microwave transistors are noted for uniformity and this in-house vertical integration allows the oscillator and transistor designers to work closely to assure that the best possible devices are designed, fully characterized and continually available. These transistors are fabricated with a highly reliable gold metal system with excellent adhesion, junction and contact performance, corrosion resistance and freedom from metal migration under high current, high temperature operation.

QUALITY ASSURANCE

The Avantek Quality Assurance department functions independently of both engineering and manufacturing. Its purpose is to assure that Avantek products continue to meet the rigid quality standards that have been maintained from the formation of the company, and maintains an effective system of QA and QC that meets the requirements of MIL-Q-9858A. Qualification to the environmental conditions of MIL-E-5400, MIL-E-16400 and other applicable military specifications is available.

YIG-TUNED OSCILLATOR WITH TRACKING YIG FILTER, AV-7248

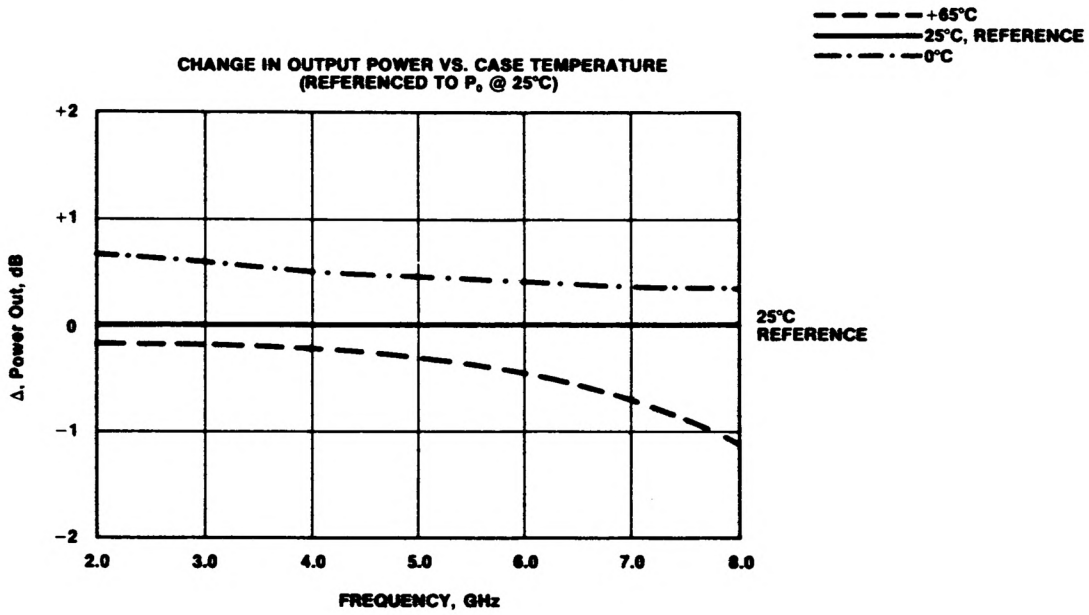
Specifications @25°C case temperature

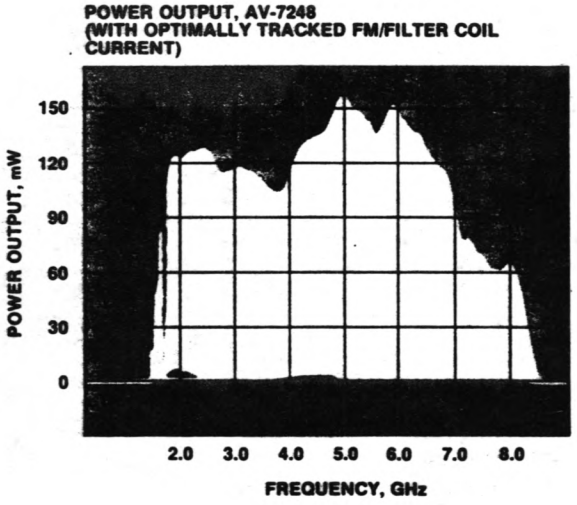
Parameters	
Frequency Range, min.	2 to 8 GHz
Power Output (50 Ω load), min.	30 mW +14.8 dBm
Power Output Variation, max.	±3.0 dB
Operating Temperature Range (Case Temperature)	0 to 65°C
Frequency Drift over Operating Temp., max.	20 MHz
Pulling Figure (12 dB return loss), typ.	0.2 MHz
Pushing Figure, typ.	
+15V supply	0.1 MHz/V
−5V supply	2.0 MHz/V
Magnetic Susceptibility, typ. @ 60 Hz.	50 kHz/Gauss[1]
Second Harmonic (Below Carrier), min.	40 dB
Third Harmonic (Below Carrier), min.	40 dB
Spurious Output (Below Carrier), min.	60 dB
Main Tuning Port Characteristics	
Sensitivity, typ.	20 MHz/mA
Bandwidth (3 dB), typ.	5 KHz
Linearity, typ.	±0.1%
Hysteresis, typ.	8 MHz
Input Impedance, typ.	9 Ω in series with 75 μH mH
FM Port Characteristics (oscillator and filter)	
Sensitivity	310 KHz/mA
Bandwidth (3 dB), typ.	400 KHz
Deviation @ 400 KHz rate, max.	40 MHz
Input Impedance, typ.	1 Ω in series with 1.25 μH
Filter Tracking Current*	300 mA @ 8 GHz
+15 VDC Circuit Current, max.	200 mA
−5 VDC Circuit Current, max.	60 mA
YIG-Heater Power	20 to 28 VDC 4 W max @ 25°C 6 W max @ 0°C
Weight (Nominal)	17 oz.

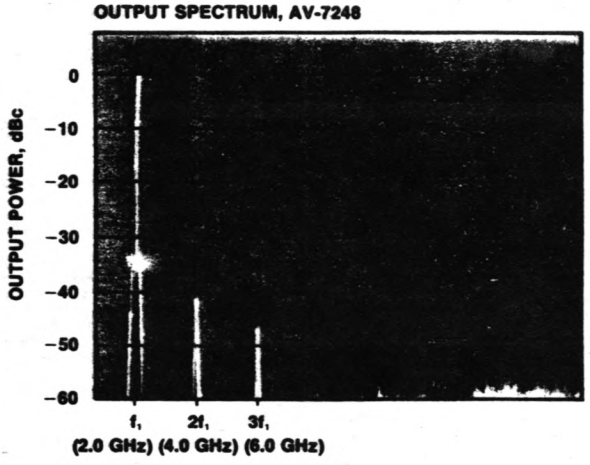
[1] 20 KHz/Gauss with optional mu-metal shield

* Maximum (applied to filter FM port)

TYPICAL PERFORMANCE (@25°C UNLESS OTHERWISE INDICATED)







Broadband Miniature Attenuators

Actual Size

RLC Electronics' Broadband Miniature Attenuators offer precision impedance matching and bi-directional handling over the extremely broad frequency of DC to 18 GHz. They are also available in the reduced frequency ranges of DC to 12.4 GHz, DC-8 GHz, and DC-1.5 GHz. These miniature microwave structures are uniquely constructed thin film elements combined with precise SMA connectors meeting the full requirements of MIL-C-39012. Units can be supplied in standard attenuation values as listed or other values for specific requirements. Three combinations of connectors are available in the standard models.

Specifications

A-[1]-[2]-[3]

Model No.	Attenuation Value (dB) [1]	Accuracy (± dB)	VSWR Max	Model No.	Attenuation Value (dB)[1]	Accuracy (± dB)	VSWR Max
A-1-3-	3	.1	1.20	A-12-3-	3	.3	1.35
A-1-6-	6	.1	1.20	A-12-6-	6	.3	1.35
A-1-10-	10	.2	1.20	A-12-10-	10	.5	1.35
A-1-20-	20	.2	1.20	A-12-20-	20	.5	1.35
A-1-30-	30	.3	1.20	A-12-30-	30	.8	1.35
A-8-3-	3	.3	1.25	A-18-3-	3	.3	1.35
A-8-6-	6	.3	1.25	A-18-6-	6	.3	1.35
A-8-10-	10	.4	1.25	A-18-10-	10	.5	1.35
A-8-20-	20	.5	1.25	A-18-20-	20	.5	1.35
A-8-30-	30	.8	1.25	A-18-30-	30	1.0	1.35

Power Rating: 2 watts avg. 1 KW peak
Impedance: 50 ohms
Connectors: SMA male or female.
Weight: 0.4 oz.
Material: Stainless Steel
Environment: MIL-A-3933

To designate the attenuator desired use:

(1) 1, 8, 12, 18 for 1.5, 8, 12.4 and 18 GHz
(2) 3, 6, etc. for attenuation value
(3) R for SMA male and female, RF for SMA female and female, or RM for SMA male and male.

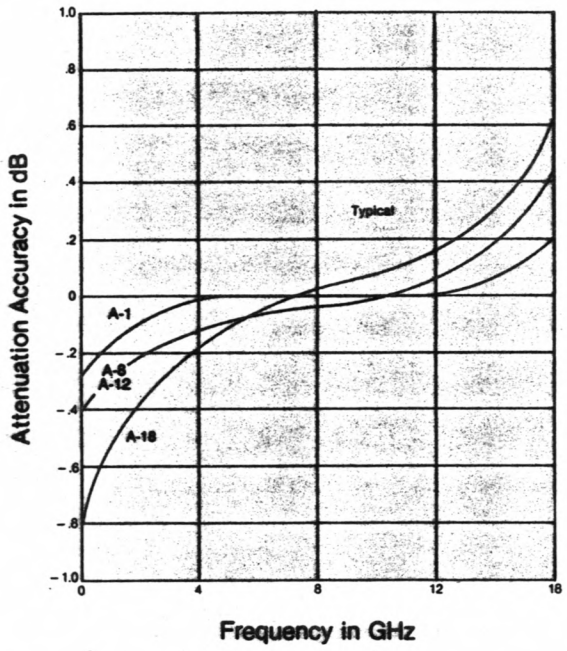
Example: A-18-20-R is a DC-18 GHz, 20 dB attenuator with SMA male and female connectors.

Specials requiring closer tolerances, different frequency ranges, special connectors, different materials, finishes, etc., can be furnished upon request.
Specifications subject to change without notice.

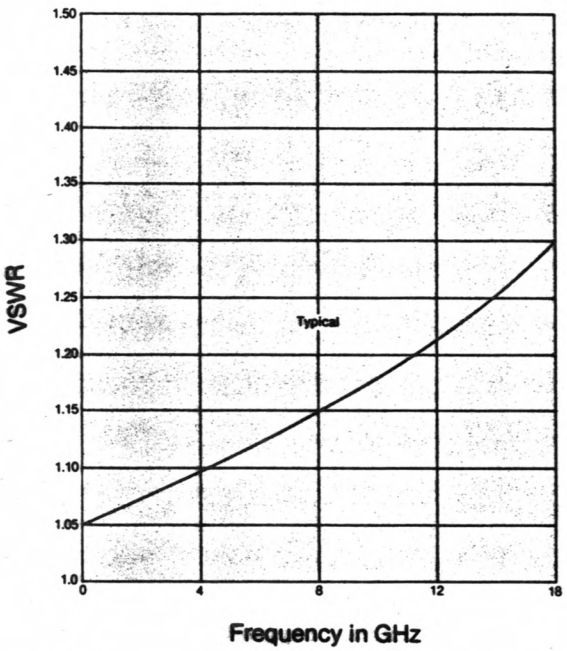
RLC ELECTRONICS, INC.
83 Radio Circle, Mt. Kisco, N.Y. 10549 • (914) 241-1334

Typical Operating Curves

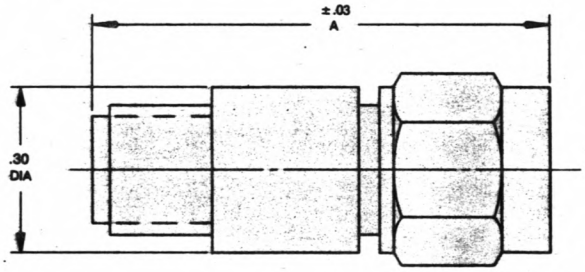
Attenuation Accuracy Vs. Frequency



VSWR Vs. Frequency



Outlines



Model No.	A
A- -3-	.87
A- -6-	.87
A- -10-	.87
A-1,8-20-	.87
A-12,18-20-	1.02
A- -30-	1.02

Tolerances unless otherwise specified are: .xx ± .02; .xxx, ± .005.

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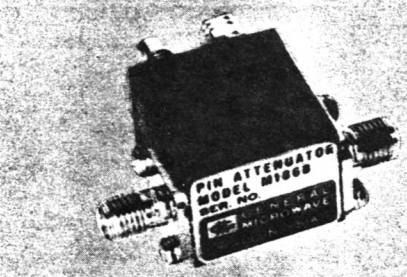
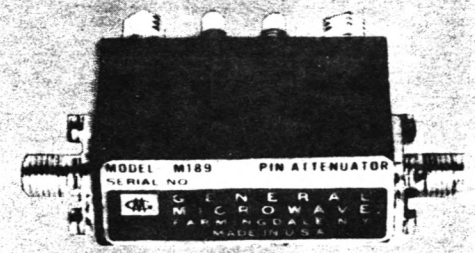
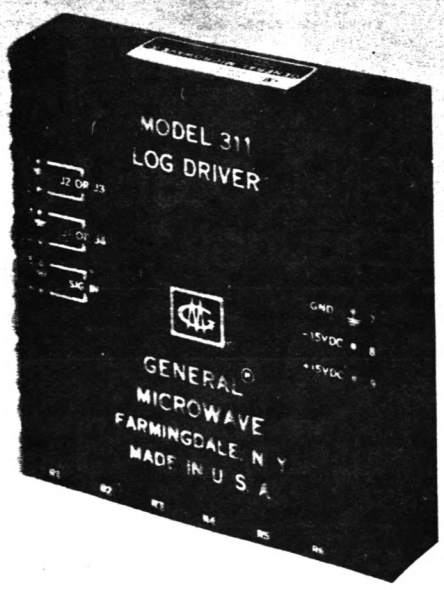
Models M186C, M189C and M190C Ultra-Broadband PIN Diode Attenuator/Modulators

- **Absorptive**
- **0.2 to 18 GHz frequency range**
- **Attenuation range up to 65 dB**
- **Flatness as low as ±0.5 dB**







MODELS M186C, M189C AND M190C

This family of absorptive PIN diode attenuator/modulators operates over the instantaneous frequency range from 0.2 to 18 GHz. Their multi-octave bandwidth makes them highly suitable for wideband ECM and measurement systems.

The rf circuit consists of a T-pad arrangement of shunt and series diodes in a microstrip integrated circuit transmission line, as shown in figures 1 and 2 below, and a resistive low-loss bias line. The arrangement permits operation as a bilaterally-matched device at all attenuation levels by separately controlling the bias currents through the series and shunt diodes.

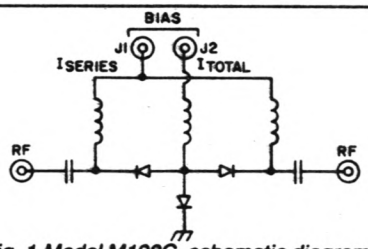


Fig. 1-Model M190C, schematic diagram (Model M189C consists of two such sections)

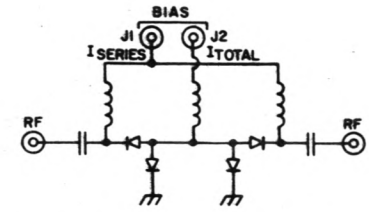


Fig. 2-Model M186C, schematic diagram

Attenuation Levels

The Models M190C and M186C are rated for attenuation levels up to 35 and 45 dB, respectively. The Model M189C, which consists of the equivalent of two independently-controlled M190C attenuators in a single rf assembly, is rated up to 65 dB. Model M189C is also available with digitally-programmable drivers under the Model 3250 designation (see page 30) for full description).

Power Ratings

Although all three models will survive input powers up to 2 watts from −65°C to +25°C, the maximum power levels at which they operate without performance degradation is limited to those shown in figure 5 on page 13. For higher power applications, the narrower band LM186C, LM189C and LM190C models are available.

Models M186C, M189C and M190C Ultra-Broadband PIN Diode Attenuator/Modulators

Drivers

The proper levels of series and shunt diode currents required for operation as a matched attenuator can be provided by either the user's circuitry, or by the GMC Model 311 Driver. (See figure 4 on page 12 for typical Bias Current/Attenuation transfer curves.) The Model 311 provides voltage controlled linear attenuation with a nominal transfer function of 10 dB per volt for the Models M186C and M190C. For the Models M189C or LM189C, two Model 311 drivers are required and the transfer function is 20 dB per volt.

When attenuators are ordered with drivers, the assemblies are adjusted for optimum accuracy at 2 GHz. Optimization at customer-specified frequencies is available on special order.

For Use As Reflective Switches

By reducing the series diode current to zero in the isolations tate, these units can be operated as high-isolation reflective switches for low frequency applications. A typical response curve of the Model M186C operating in this mode is shown in figure 3 on page 12.

Specifications

MODEL NO.	CHARACTERISTIC	FREQUENCY (GHz) 0.2 to 8.0	8.0 to 12.4	12.4 to 18.0	MODEL NO.	CHARACTERISTIC	FREQUENCY (GHz) 0.2 to 8.0	8.0 to 12.4
M186C	Max Insertion Loss (dB)	1.5	2.2	3.0	LM186C	Max Insertion Loss (dB)	1.5	2.6
	Max VSWR	1.5	1.75	2.0		Max VSWR	1.5	1.75
	Min Attenuation (dB)	45[1]	45	40		Min Attenuation (dB)	40[2]	40
M189C	Max Insertion Loss (dB)	2.5	3.0	5.0	LM189C	Max Insertion Loss (dB)	2.5	3.5
	Max VSWR	1.75	2.0	3.0		Max VSWR	1.75	2.0
	Min Attenuation (dB)	65	65	50		Min Attenuation (dB)	65	60
M190C	Max Insertion Loss (dB)	1.5	1.8	2.5	LM190C	Max Insertion Loss (dB)	1.5	1.8
	Max VSWR	1.5	1.6	2.0		Max VSWR	1.5	1.75
	Min Attenuation (dB)	35	35	30		Min Attenuation (dB)	35	30

ATTEN. (dB)	FLATNESS (±dB) FREQUENCY (GHz) 0.2 to 8.0 M190C	M189C	LM190C	LM189C	0.2 to 12.4 M190C	M189C	LM190C	LM189C	12.4 to 18.0 M190C	M189C
10	0.5	0.5	0.5	0.5	0.7	0.7	0.7	0.7	1.0	1.0
20	0.5	0.5	0.5	0.5	1.0	1.0	1.2	1.2	1.0	1.0
30	0.7	0.7	1.0	1.0	1.5	1.5	2.0	2.0	1.0	1.5
40	—	1.0	—	1.0	—	1.5	—	2.0	—	1.5
50	—	1.0	—	1.5	—	1.5	—	2.0	—	1.5
60	—	1.0	—	2.0	—	1.5	—	2.5	—	1.5

(1) Except 40 dB up to 2 GHz.
(2) Except 35 dB up to 2 GHz.

Models M186C, M189C and M190C Specifications

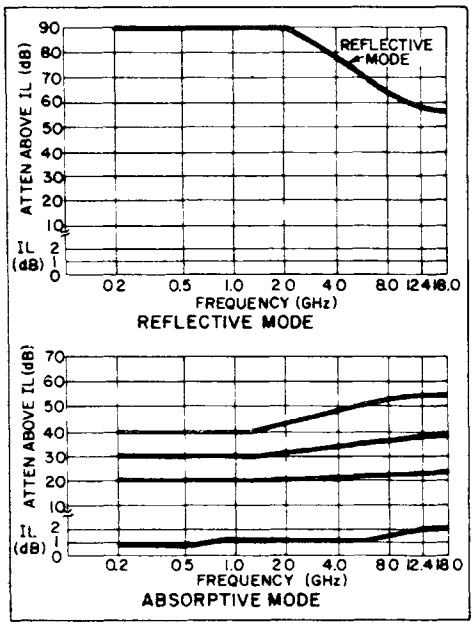


Fig. 3-Typical response curves of Model M186C

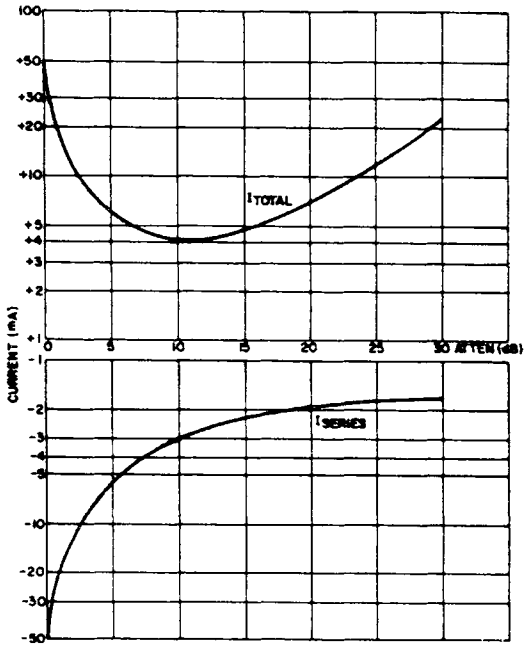


Fig. 4-Typical Models M186C and M190C bias current/attenuation transfer curves

PERFORMANCE CHARACTERISTICS

Power Handling Capability
Without Performance Degradation

M186C, M189C, M190C . . . . . From 0.4 to 100 mW cw or peak (see figure 5 on page 13)

LM186C, LM189C, LM190C . . . . . 100 mW cw or peak

Survival Power (from −65°C to +25°C; see power derating curve, figure 6 on page 13, for higher temperatures)

All units . . . . . 2W average or peak (1μsec max pulse width)

Phase Shift . . . . . See page 5

Typical Small Signal Bandwidth

M186C, M189C, M190C . . . . . 500 kHz

LM186C, LM189C, LM190C . . . . . 50 kHz

Bias Current Requirements (see figure 4 above)

M189C, LM189C . . . . ±100 mA max.

M186C, LM186C, M190C, LM190C . . . . . ±50 mA max.

ENVIRONMENTAL RATINGS (RF UNIT)

Operating Temperature Range . . . −65°C to +85°C

Non-Operating Temperature Range . . . −65°C to +125°C

Humidity . . . . . MIL-STD-202F, Method 103B, Cond. B (96 hrs. at 95%)

Shock . . . . . MIL-STD-202F, Method 213B, Cond. B (75G, 6 msec)

Vibration . . . . . MIL-STD-202F, Method 204D, Cond. B (.06"double amplitude or 15G, whichever is less)

Altitude . . . . . MIL-STD-202F, Method 105C, Cond. B (50,000 ft.)

Temp. Cycling . . . . . MIL-STD-202F, Method 107D, Cond. A, 5 cycles

MODEL 311 CHARACTERISTICS(1)

Nominal Transfer Function . . . . . 10 dB/volt

Accuracy at Calibration Frequency (2 GHz) . . . . . ±1 dB starting from 5 dB above insertion loss

Typical Small Signal Bandwidth When Used With:

M186C, M189C, M190C . . . . . 500 kHz

LM186C, LM189C, LM190C . . . . . 50 kHz

Control Signal Input Voltage Range . . . . . 0 to +5 volts dc

Control Signal Input Impedance . . . . . 3K ohms (nominal)

(1) *Specifications listed are for each Model 311 Driver in use.*

Models M186C, M189C and M190C Specifications

MODEL 311 CHARACTERISTICS[1] (cont)

Switching Time . . . . . 100 μsec max

Power Supply Requirements . . . . . +15V ±0.1%, 125 mA
−15V ±0.1%, 125 mA

Operating Temperature Range . . . . . −55°C to +75°C

Non-Operating Temperature Range . . . . −55°C to +85°C

AVAILABLE OPTIONS (RF UNIT)

Option No.	Description
7	Two SMA male rf connectors
10	One SMA male and one SMA female rf connector
33	EMI filter solder-type bias terminals
35	High-temperature design (+125°C)

(1) *Specifications listed are for each Model 311 Driver in use.*

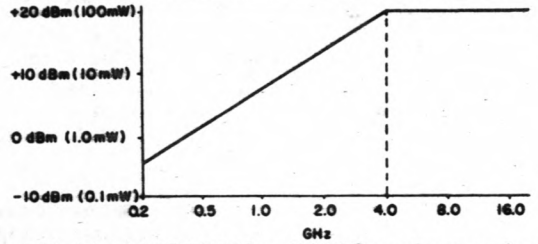


Fig. 5-Models M186C, M190C and M189C, maximum peak and average operating power without performance degradation

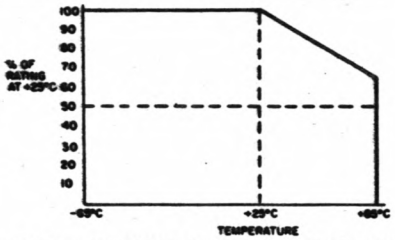
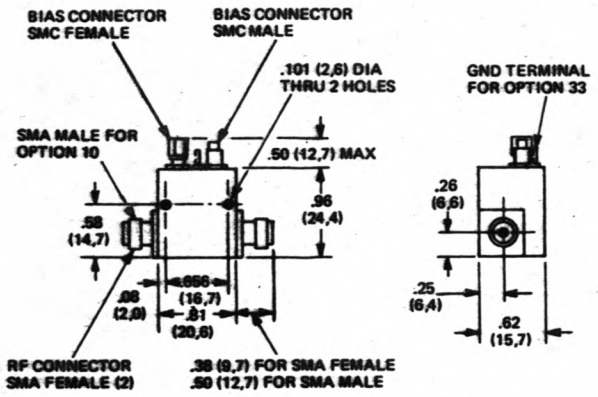
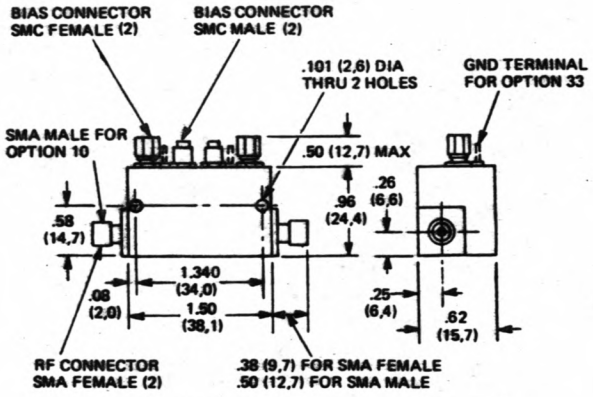


Fig. 6-Models M186C, LM186C, M189C, LM189C, M190C and LM190C, survival power derating factors

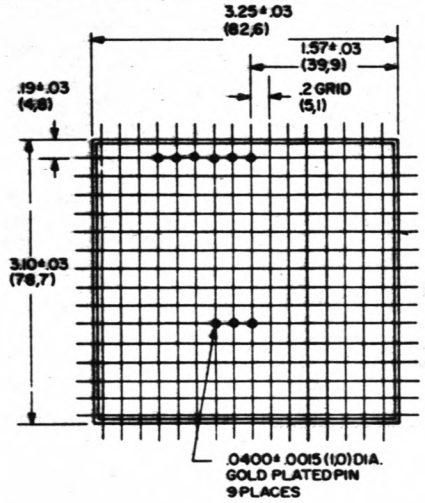
DIMENSIONS AND WEIGHTS

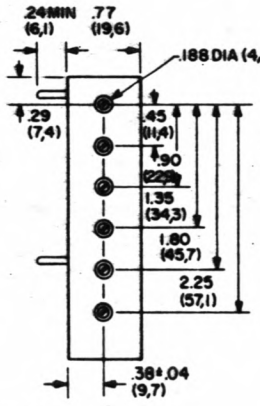


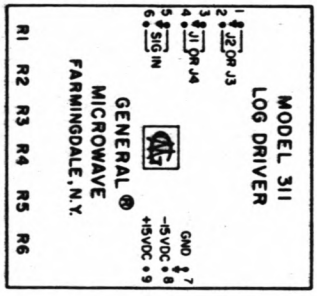
MODELS M186C, LM186C, M190C AND LM190C
Wt. 1 oz (28 gm) approx.



MODELS M189C AND LM189C
Wt. 2 oz. (57 gm) approx.





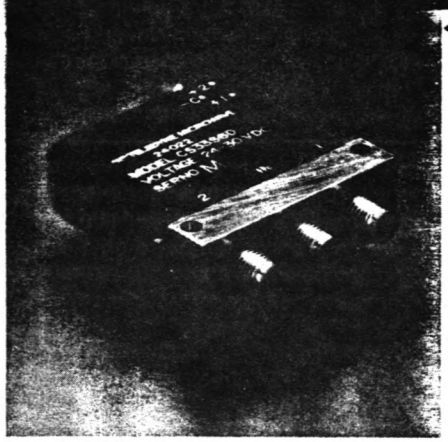


MODEL 311 DRIVER
Wt: 4 oz. (113 gm) approx.

Dimensional Tolerances, unless otherwise indicated: .XX ± .02; .XXX ± .005

ATTENUATORS PHASE SHIFTERS

Miniature SPDT Switches



◀ CS-33S60

Latching Actuator CS-33 Series

DC-18 GHz
SMA Connectors

Description

The Type CS-33 Latching Switch is a broadband SPDT electro-mechanical switch designed to switch microwave signals from a common input to either of two outputs. Designed for 50 ohm transmission lines, the unit is set up for minimum size compatible with SMA connector spacing.

The switches on this page are provided with a magnetic latching actuator (for failsafe types see Page 12) which is particularly desirable in applications where actuator power consumption must be kept to an absolute minimum. The latching type actuator requires less switching current than the failsafe type. In the self-cutoff version, power is applied only for the very short duration (approximately 50 msec. max.) of the actuator transfer from one position to the other. This makes this type of actuator especially suitable for space vehicles or portable battery operated systems.

Specifications

RF Contacts:
Break before make

Actuator Voltage:
24–30 VDC; 12, 15, 20 VDC, and 115 VAC on special order

Actuator Current:
60 mA @ 28 VDC and 20°C

Switching Time:
10 msec.

Weight:
1.65 oz.

Temperature Range:
−54°C to +85°C

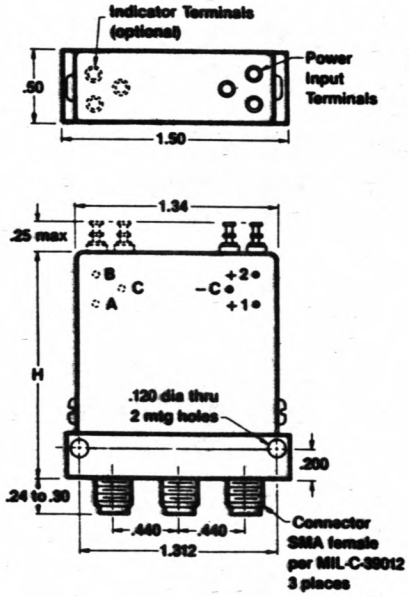
Life:
1 million cycles

RF Power Handling:
See graph on page 6

Optional Features

- Indicator Circuits
- Special Actuator Voltages
- TTL Compatible Drivers
- Arc Suppression Diodes
- Power Connectors
- Inboard Mounting

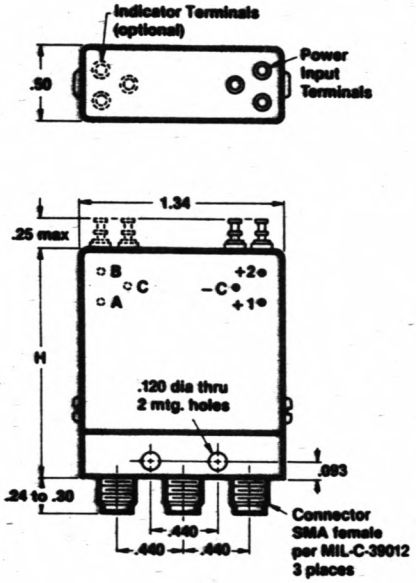
Outboard Mounting ▶



H = 1.55 max STD Model
H = 2.10 max TTL Model
H = 2.10 max CS33S6E

Figure 20

Inboard Mounting ▶



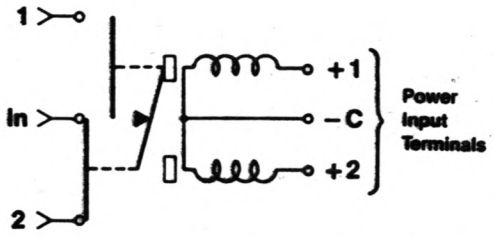
H = 1.55 max STD Model
H = 2.10 max TTL Model
H = 2.10 max CS33S6E

Figure 21

RF Performance

Frequency	DC–6 GHz	6–12 GHz	12–18 GHz
VSWR (maximum)	1.25:1	1.40:1	1.50:1
Insertion Loss (maximum)	0.2 dB	0.4 dB	0.5 dB
Isolation (minimum)	70 dB	60 dB	60 dB

CS33S60 ▶



Position	Voltage	RF continuity
1	+1 & –C	IN & 1
2	+2 & –C	IN & 2

Figure 23

▼ TTL Option (See Page 8)

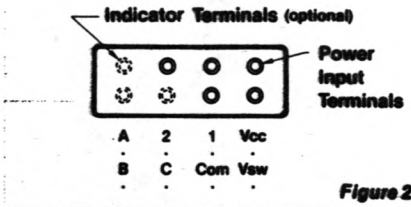
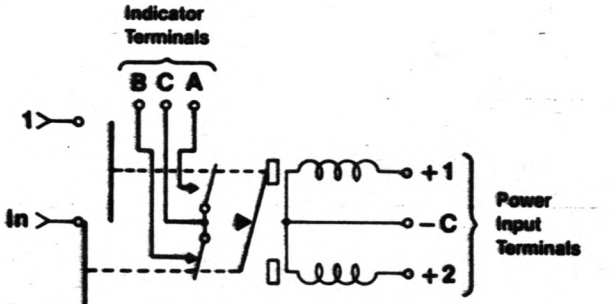


Figure 22

CS33S6C ▶



Position	Voltage	RF continuity	Indicator
1	+1 & –C	IN & 1	A & C
2	+2 & –C	IN & 2	B & C

Figure 24

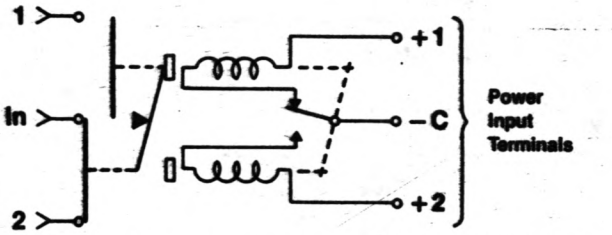
Part Number Table

All units have SMA-Female connectors

For TTL Drivers add -T to Part No.

Actuator Type	Without Indicators	With Indicators
Latching without Self-Cutoff	CS-33S60	CS-33S6C
Latching with Self-Cutoff	CS-33S6D	CS-33S6E

CS33S6D ▶

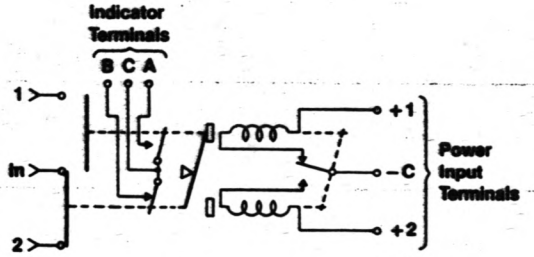


Position	Voltage	RF continuity
1	+1 & –C	IN & 1
2	+2 & –C	IN & 2

Figure 25

For Models CS-33S60 and CS-33S6C power is applied in a pulse form of sufficient duration (20 msec. min.) to cause switching. For Models CS-33S6D and CS-33S6E steady voltage may be applied continuously, but switch only draws current during the actual switching cycle.

CS-33S6E ▶



Position	Voltage	RF continuity	Indicator
1	+1 & –C	IN & 1	A & C
2	+2 & –C	IN & 2	B & C

Figure 26

AYDIN MICROWAVE DIVISION

75 EAST TRIMBLE ROAD
SAN JOSE, CA 95131
TELEPHONE 408-946-5600
TWX 910-338-0216

TEST DATA SHEET FOR SOLID STATE AMPLIFIER

AMD MIC DEPT.

MODEL: AMA 4080B5 S/N 4499

FREQUENCY RANGE: FROM 4 GHz TO 8 GHz

POWER SUPPLY: +15 VDC 550 mA (MAX: _____ mA)

MAXIMUM BASE PLATE TEMPERATURE: +50°C

FREQUENCY IN GHz		4	6	8		
GAIN IN dB	MAX _____ MIN 15	21	21.6	21.2		
POWER OUTPUT AT 1 dB COMPRESSION	MAX _____ MIN 25	25.5 dBm WATT	26 dBm WATT	26 dBm WATT	dBm WATT	dBm WATT
VSWR IN	MAX 2	1.6 :1	1.6 :1	1.8 :1	:1	:1
VSWR OUT	MAX 2	1.5 :1	1.5 :1	1.5 :1	:1	:1
POWER OUTPUT SATURATED	MAX _____ MIN _____	28 dBm WATT	28.5 dBm WATT	28 dBm WATT	dBm WATT	dBm WATT
NOISE FIGURE IN dB	MAX 8	7. 7	6.5	6.5		

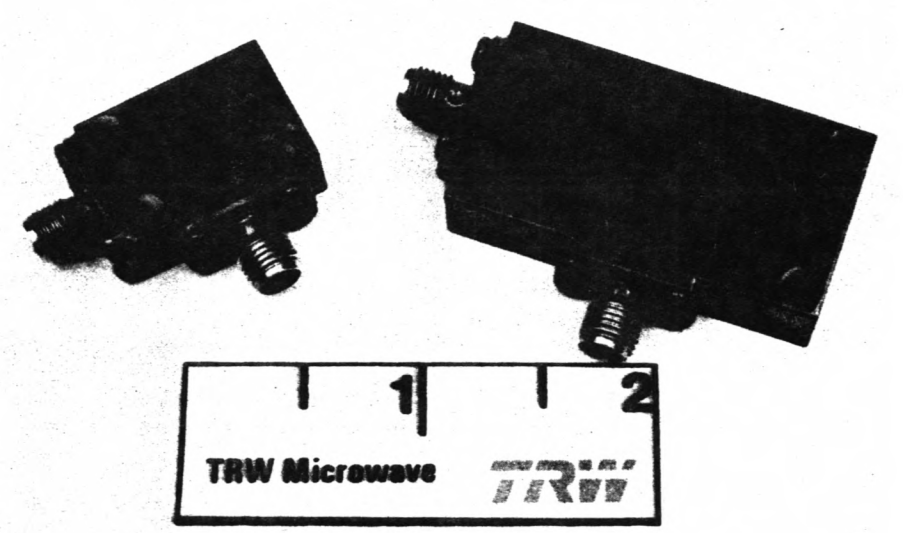
GAIN FLATNESS OVER FREQUENCY RANGE MAX ± 1 ± .9 dB

TESTED BY: Long Dang
DATE: 8-13-84

Frequency Doublers

Features

- Octave Band
- Low Conversion Loss
- High Isolation



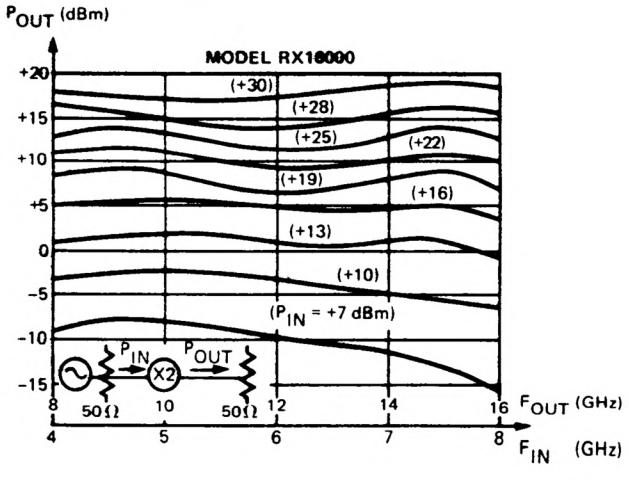
Specifications @ +25°C

Model	Input Frequency (GHz)	Output Frequency (GHz)	Conversion Loss (Max.)	Input Power (dBm)	Min.[2] Isolation (dB)	Outline
RX8000	2.0–4.0	4.0–8.0	12	+20	30	D-1
RX12000	3.0–6.0	6.0–12.0	13	+20	30	D-2
RX16000	4.0–8.0	8.0–16.0	13	+20	30	D-3
RX18000	6.0–9.0	12.0–18.0	14	+20	30	D-4

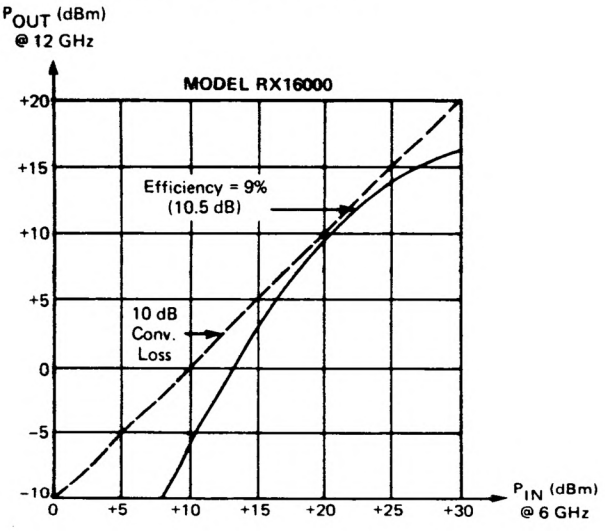
Notes:
1. All data are measured in a 50 ohm system at room ambient.
2. Power output of fundamental is 30 dB below the input power.

Typical Electrical Performance

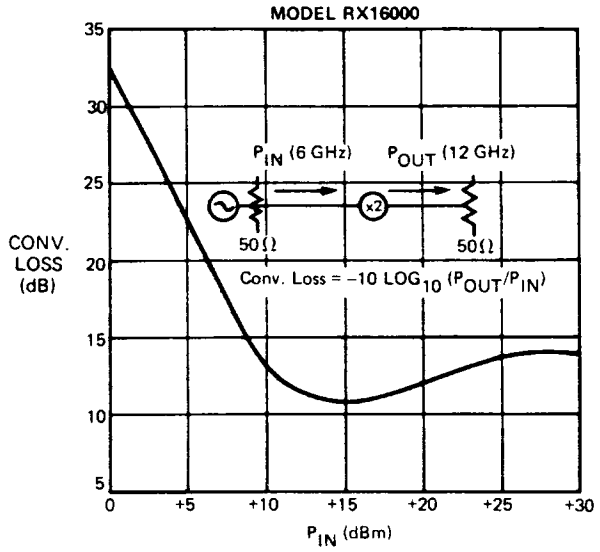
Frequency Response



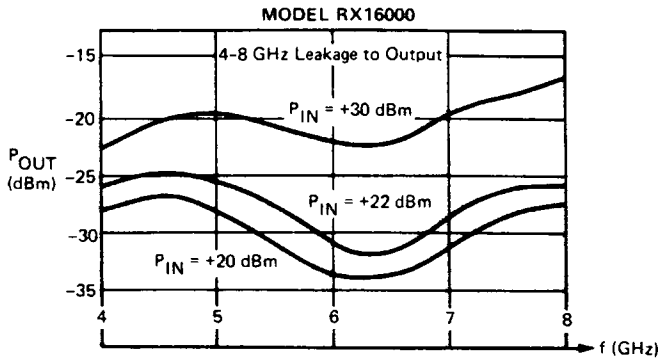
Power Transfer Characteristic



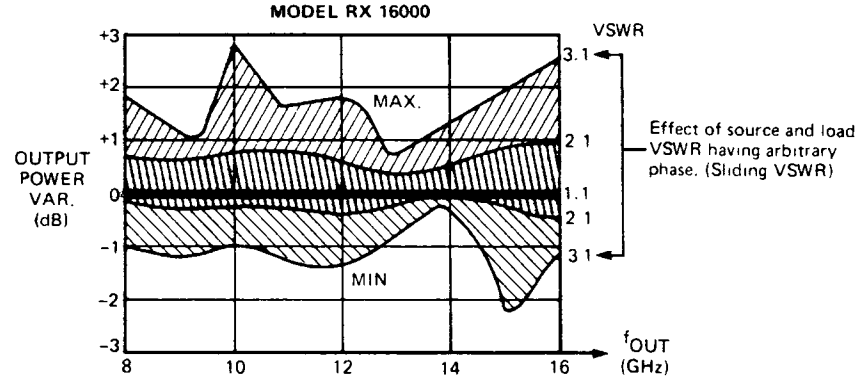
Conversion Loss (dB)



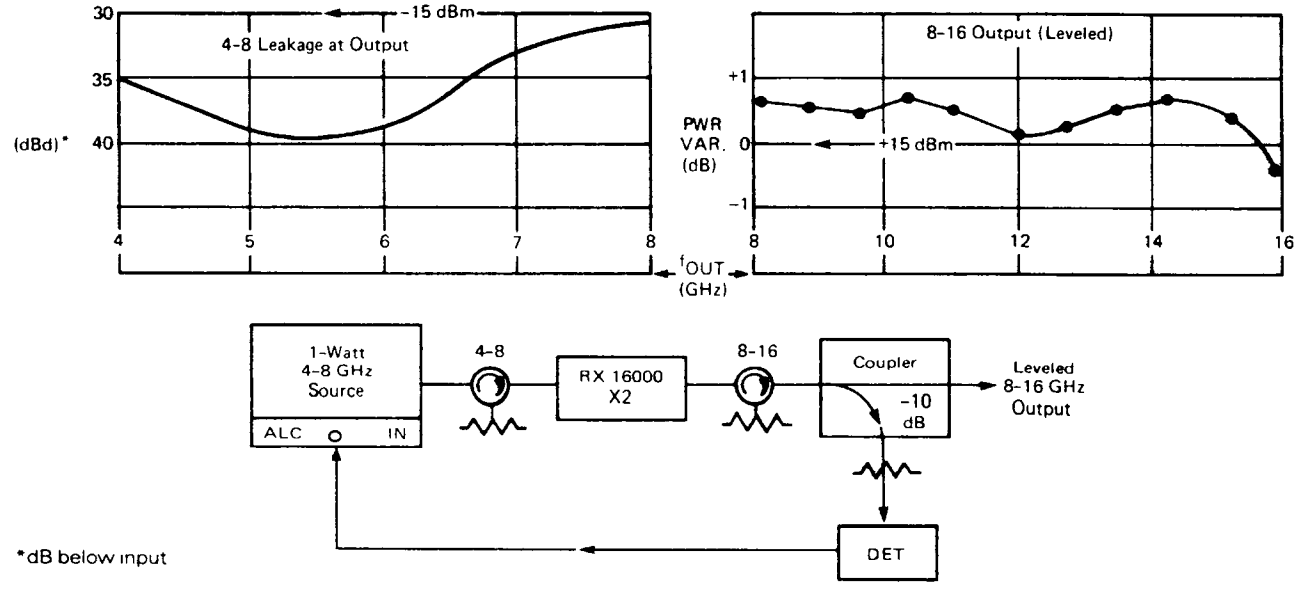
Isolation



Effect of Source and Load VSWR on Conversion Loss



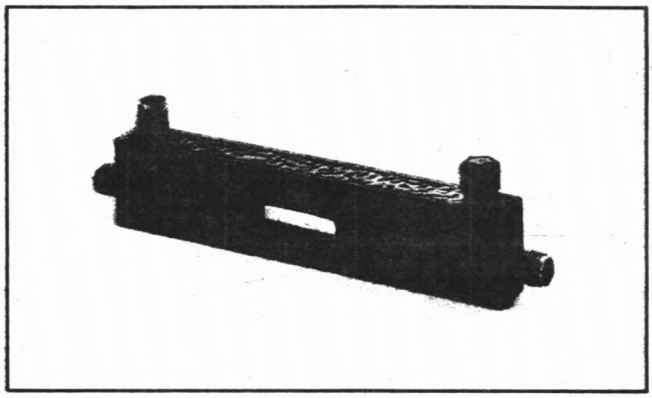
Application



*dB below input

STANDARD MINIATURE BROADBAND DIRECTIONAL COUPLERS

1-12.4 GHz, 1-18 GHz, 2-18 GHz BANDWIDTHS
6, 10, 16 & 20 dB COUPLING LEVELS



FEATURES

- Up to 18:1 bandwidths
- Small size
- Guaranteed to meet MIL-E-5400 Class 2 (−54°C to +95°C, 0-70,000 feet)
- Flat coupling

DESCRIPTION

Sage broadband miniature couplers are designed to operate reliably in both military and laboratory environments, and over bandwidths as broad as 18:1. These couplers use asymmetric continuously tapered coupled lines which are etched on low loss stripline dielectric. The circuits are enclosed in milled aluminum housings, and are epoxy sealed. Connectors are stainless steel SMA female with interfaces per MIL-C-39012. These couplers can be used in broadband ECM and measurement systems, or in reconfigurable narrowband systems where it would be impractical to change directional couplers when switching bands. The 16 dB couplers are intended for use in leveling circuits.

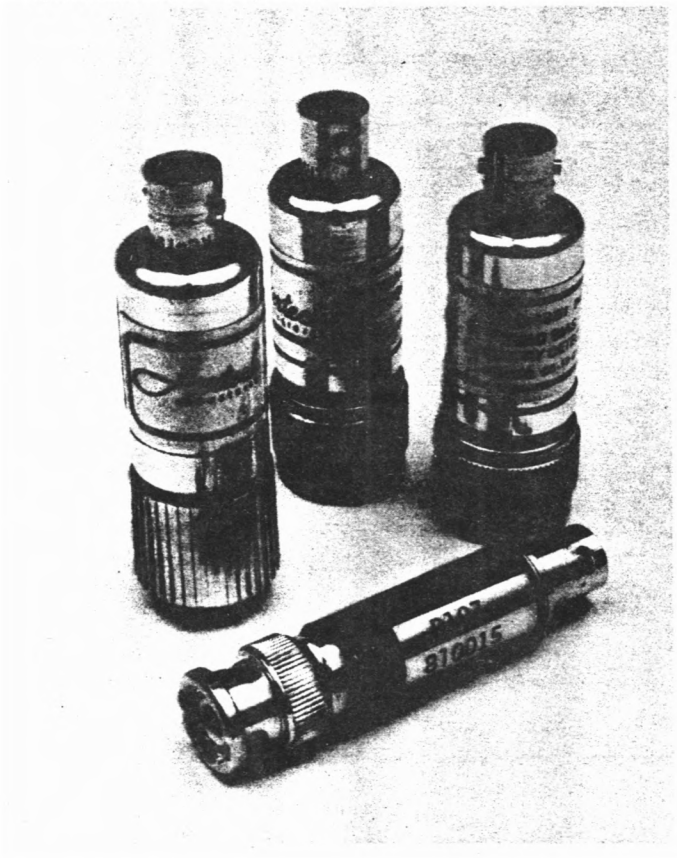
SPECIFICATIONS

MODEL NUMBER	FREQUENCY (GHz)	COUPLING (dB)	FLATNESS (dB)	MAXIMUM VSWR		MAXIMUM LOSS (dB)	DIRECTIVITY (dB) MIN./TYP.		POWER HANDLING CAPABILITY**			
				MAIN LINE	COUPLED LINE		TO 12 GHz	12 TO 18 GHz	AVG. INCIDENT (WATTS) (1 GHz)	AVG. REFLECTED (WATTS)	PEAK (KW)	CASE STYLE
C112-6	1-12.4	6±1	±.5	1.30	1.40	.9	15/25	—	100	2	1.5	1
C112-10	1-12.4	10±1	±.4	1.30	1.40	.7	15/20	—	100	5	1.5	1
C112-16	1-12.4	16±1*	±.4	1.30	1.40	.7	15/20	—	100	25	1.5	1
C112-20	1-12.4	20±1	±.4	1.30	1.40	.7	15/20	—	100	25	1.5	1
C118-6	1-18	6±1	±.5	1.40	1.50	1.2	15/25	12/20	100	2	1.5	1
C118-10	1-18	10±1	±.5	1.40	1.50	1.0	15/20	12/18	100	5	1.5	1
C-118-16	1-18	16±1*	±.5	1.40	1.50	.8	15/20	12/18	100	25	1.5	1
C118-20	1-18	20±1	±.5	1.40	1.50	.8	15/20	12/18	100	25	1.5	1
C218-6	2-18	6±1	±.5	1.35	1.45	1.0	20/25	17/20	100	2	1.5	2
C218-10	2-18	10±1	±.5	1.35	1.45	.8	20/25	17/20	100	5	1.5	2
C218-16	2-18	16±1*	±.4	1.35	1.45	.6	20/25	17/20	100	25	1.5	2
C218-20	2-18	20±1	±.4	1.35	1.45	.5	20/25	17/20	100	25	1.5	2

*Reference to main line output port . . . for use as a leveling coupler.
**Power derating vs. altitude see page 85 and vs. frequency see page 189.

Special Applications
Zero Bias Schottky Diode Detector 100 kHz to 18 GHz

Series D10Z, D12Z, D18Z



Features

- Broadband
- Excellent Flatness
- Low VSWR
- No Bias Required
- Metallurgically Bonded Diode
- High Burnout Protection
- Choice of APC-7, Type N or SMA Input Connectors

Description

The Aertech D10Z, D12Z and D18Z Series of broadband coaxial detectors are designed for use in laboratory measurement, microwave instrumentation and broadband EW system applications. Since they do not require a dc bias and can be used with common oscilloscopes, their ease of use and broadband performance make them very useful measurement accessories. Their superior broadband flatness, VSWR, ruggedness and burnout protection, relative to point-contact models, make them excellent for microwave instrumentation and system applications.

The D18Z and D12Z Series include a choice of APC-7, Type N or SMA input connector models. All models have BNC female output connectors. Standard models have Negative output polarity with Positive polarity and matched pairs available as options.

Specifications*

Model Number	Connectors		Mech. Dimensions		Frequency Range	VSWR	Frequency Response		Low Level Sensitivity	Input Power
	Input	Output	Length	Diameter			Octave	Broadband		
D10Z	BNC Male	BNC Female	2.42 in (61mm)	0.51 in (13mm)	100kHz to 2.5 GHz	1.4:1 max	±0.1dB in any 100kHz increment +0.3dB to 2.5GHz		400mV/mW min.	Maximum Operating 200mW; Short Duration (Less than 1 minute) 1 Watt (typical)
D12Z7	APC-7		2.59 in (65.8 mm)	0.75 in (19mm)	10MHz to 12.4GHz	1.20:1 max (to 4.5GHz) 1.30:1 max (to 7GHz) 1.40:1 max (to12.4GHz)	±0.2dB	±.5dB (to 12.4GHz)		
D12ZN	Type N Male		2.46 in (62.5 mm)	0.75 in (19mm)						
D12Z3	SMA Male		2.50 in (64mm)	0.56 in (14mm)						
D18Z7	APC-7		2.59 in (65.8 mm)	0.75 in (19mm)	0.01 to 18GHz	1.2:1 (to4GHz) 1.4:1 to 18GHz)	±0.2dB (to 8GHz)	±0.3dB (to 8GHz) ±0.5dB (to 18GHz)		
D18ZN	Type N Male		2.46 in (62.5 mm)	0.75 in (19mm)		1.2:1 (to 4GHz) 1.4:1 (to 18GHz)				
D18Z3	SMA Male		2.50 in (64mm)	0.56 in (14mm)		1.2:1 (to 4GHz) 1.5:1 (to 18GHz)				

*Specifications given for T_A = +25°C

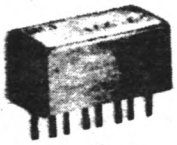
Output Polarity
Negative Polarity Standard. Positive Polarity available at no extra charge. (For Positive Polarity models, add "R" suffix to part number.)

Matched Pairs
Pairs matched within ±0.3dB from 0.01 to 18GHz are available at an extra charge of $20.00 per unit. (For matched pairs, add a 'P' after the part number for individual units—i.e., matched pairs of positive polarity D18Z3's would be ordered as D18Z3RP.)

MINI-CIRCUITS **q&a** PHASE DETECTORS

High-Figure-Of-Merit
PHASE DETECTORS

RPD SERIES



MODEL	FREQUENCY	Z (Ohms)	COST
RPD-1	1-100 MHz	50	$15.95(5-24)

DESCRIPTION — These new high efficiency phase detectors offer state-of-the-art performance while still economically priced. These are the only units in the world offering a figure-of-merit greater than 125—at only $15.95.

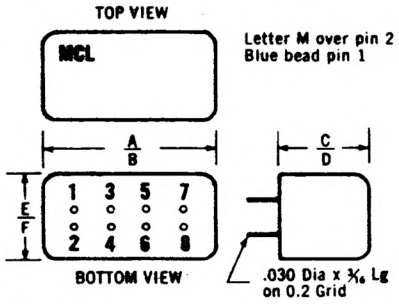
The figure-of-merit M or efficiency of a phase detector can be defined as the ratio of maximum DC output voltage (in mV) divided by the RF power (in dBm). The maximum DC output of the RPD-1 is 1000 mV with +7 dBm applied to the LO and RF ports. Thus, its figure-of-merit M is 143, which represents a highly efficient phase detector. For comparison, a standard phase detector offers 350 mV DC output with the same LO and RF inputs for a figure-of-merit M of 50.

Only 0.40 inches high, the low profile RPD series of phase detectors covers a very broad frequency range from 1 to 100 MHz. Exhibiting a flat frequency response, these units are designed to operate with a 50 ohm impedance at the L & R ports, and 500 ohms at the I port. Output is 1000 mV (typ) and isolation is greater than 50 dB (typ).

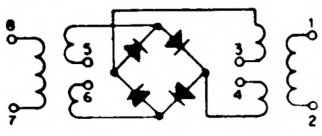
Packaged within an RFI shielded metal enclosure and hermetically sealed header, these high performance units have their 8 pins located on a 0.2 inch grid.

High reliability is a characteristic of the RPD series. Each unit carries a one-year guarantee by Mini-Circuits.

DIMENSIONS AND CONNECTIONS



	A	B	C	D	E	F
IN.	.770	.800	.385	.400	.370	.400
MM	19.5	20.3	9.7	10.1	9.3	10.1



PIN LAYOUT

Model No.	-1
LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

WEIGHT 5.2 grams .18 ounces

FEATURES

Broadband, 1-100 MHz
High Output, 1000mV
High Figure-Of-Merit, M, 143 typical
High Isolation, typically greater than 50dB
Low DC Offset, 0.2 mV typical
Miniature, 0.128 in. cu., 0.4 in x 0.8 PC area, 0.4 in. high
High Reliability, 100% tested
Low Cost, $15.95 (5-24)

APPLICATIONS

- Radar
- ECM Systems
- Test instruments
- Phase-lock loops

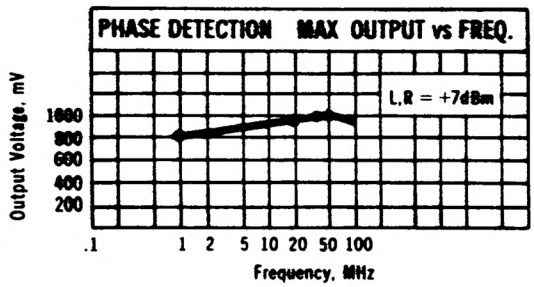
ABSOLUTE MAXIMUM RATINGS

- **Input Power:** 50 mW
- **Peak IF Input Current:** 40 mA
- **Operating and Storage Temp.:** −55° C to +100° C
- **Pin Temperature:** (10 sec.) +260° C

RPD-1 SPECIFICATIONS

FREQUENCY RANGE: L and R ports Output ports	 1-100 MHz DC-50 MHz
SCALE FACTOR	8 mV/Degree
IMPEDANCE L and R ports I port	 50 ohms 500 ohms
L and R SIGNAL LEVELS	+7 dBm
ISOLATION, L-R	40 dB min
MAXIMUM DC OUTPUT, mV	1000 mV typ 750 mV min
DC OUTPUT POLARITY (L and R in-phase)	 Negative
DC OUTPUT OFFSET VOLTAGE	0.2 mV typ 1 mV max
FIGURE-OF-MERIT, M	143 Typical

MODEL RPD-1



Mini-Circuits 2625 E. 14th St., Brooklyn, NY 11235 (212) 769-0200 Dom. Telex 125460 Int'l. Telex 620156

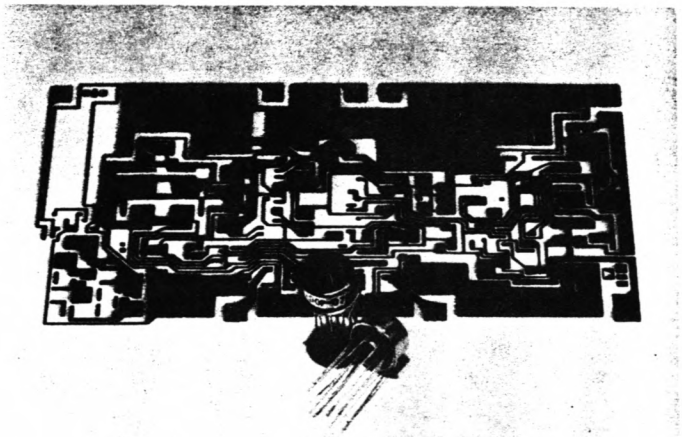
ANALOG DEVICES

Ultra-Low Offset Voltage Op Amp

AD OP-07

FEATURES

- Ten Times More Gain Than Other OP-07 Devices (3.0M min)
- Ultra-Low Offset Voltage: 10μV
- Ultra-Low Offset Voltage Drift: 0.2μV/°C
- Ultra-Stable vs. Time: 0.2μV/month
- Ultra-Low Noise: 0.35μV p-p
- No External Components Required
- Monolithic Construction
- High Common Mode Input Range: ±14.0V
- Wide Power Supply Voltage Range: ±3V to ±18V
- Fits 725, 108A/308A, 741 Sockets



PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as 10μV, bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C and long-term stability of 0.2μV/month eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range (±14V) high common mode rejection ratio (up to 126dB) and high differential input impedance (50MΩ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. Full processing to the requirements of MIL-STD-883, Class B, is available on the AD OP-07 and AD OP-07A. All devices are packaged in TO-99 hermetically-sealed metal cans.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-07EH			AD OP-07CH			AD OP-07DH		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	2,000	5,000		1,200	4,000		1,200	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0	
		±12.0	±12.8		±11.5	±12.8		±11.5	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	75		60	150		60	150
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift							(Note 3)			(Note 3)
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
							(Note 3)			(Note 3)
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8 (Note 3)	35		12 (Note 3)	50		12 (Note 3)	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	±4.0		±1.8	±7.0		±2.0	±12
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13 (Note 3)	35		18 (Note 3)	50		18 (Note 3)	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{IN} CM		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	±13.0	±14.0		±13.0	±14.0		±13.0	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common Mode Rejection Ratio	CMRR	106	123		100	120		94	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	4.0		3.5	5.0		3.5	5.0
Power Consumption	P_D		90	120		105	150		105	150
			6.0	8.4		6.0	8.4		6.0	8.4
Rejection Ratio	PSRR	94	107		90	104		90	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE										
RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PRICES										
(1-24)			$14.65			$10.15			$ 7.35	
(25-99)			$11.70			$ 8.10			$ 5.85	
(100+)			$ 9.75			$ 6.50			$ 4.55	

NOTES:

1) Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.
2) Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — Parameter is not 100% tested: 90% of units meet this specification.
3) Parameter is not 100% tested; 90% of units meet this specification.
4) The AD OP-07A and AD OP-07 are available fully processed to MIL-STD-883, Class B. Order AD OP-07-AH-883B or AD OP-07-H-883B.

Specifications subject to change without notice.

AD OP-07AH (AD OP-07-AH-883B)[4]			AD OP-07H (AD OP-07-H-883B)[4]				
MIN	TYP	MAX	MIN	TYP	MAX	TEST CONDITIONS	UNITS
3,000	5,000		2,000	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		1,500	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		±12.5	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		±12.0	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		±10.5	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		±12.0	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	25		30	75	Note 1	μV
	25	60		60	200	Note 1, T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	0.6		0.3	1.3	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 2	μV/Month
	0.3	2.0		0.4	2.8		nA
	0.8	4.0		1.2	5.6	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	±2.0		±1.0	±3.0		nA
	±1.0	±4.0		±2.0	±6.0	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz, Note 3	μV p-p
	10.3	18.0		10.3	18.0	f_O = 10Hz, Note 3	nV/√Hz
	10.0	13.0		10.0	13.0	f_O = 100Hz, Note 3	nV/√Hz
	9.6	11.0		9.6	11.0	f_O = 1kHz, Note 3	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz, Note 3	pA p-p
	0.32	0.80		0.32	0.80	f_O = 10Hz, Note 3	pA/√Hz
	0.14	0.23		0.14	0.23	f_O = 100Hz, Note 3	pA/√Hz
	0.12	0.17		0.12	0.17	f_O = 1kHz, Note 3	pA/√Hz
±13.0	±14.0		±13.0	±14.0			V
±13.0	±13.5		±13.0	±13.5		T_{min} to T_{max}	V
110	126		110	126		V_{CM} = ±CMVR	dB
106	123		106	123		V_{CM} = ±CMVR, T_{min} to T_{max}	dB
	3.0	4.0		3.0	4.0	$V_S = \pm 15V$	mA
	90	120		90	120	$V_S = \pm 15V$	mW
	6.0	8.4		6.0	8.4	$V_S = \pm 3V$	mW
100	110		100	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		94	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
-55		+125	-55		+125		°C
	$68.00 ($73.00)			$29.75 ($34.75)			
	$55.00 ($59.50)			$24.00 ($28.50)			
	$45.00 ($49.00)			$19.50 ($23.50)			

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage (Note 2) . . . . . ±22V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range
OP-07A, OP-07 . . . . . -55°C to +125°C
OP-07E, OP-07C, OP-07D . . . . . 0 to +70°C
Lead Temperature Range (Soldering, 60sec) . . . . . 300°C

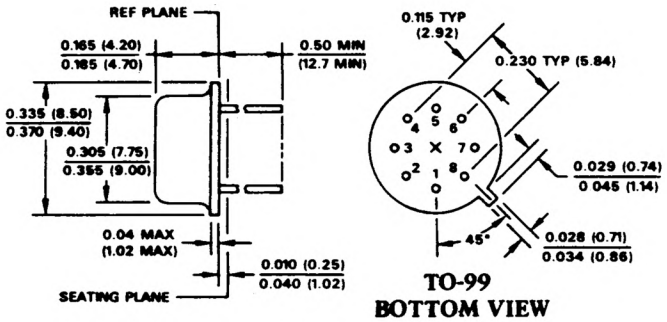
NOTES:
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

OUTLINE DIMENSIONS

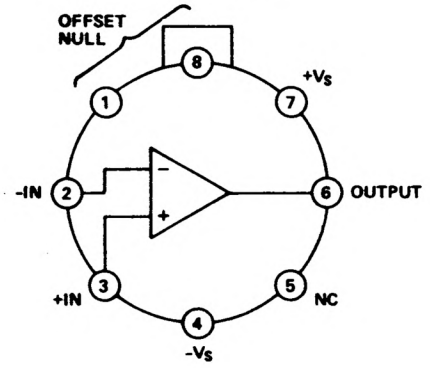
Dimensions shown in inches and (mm).

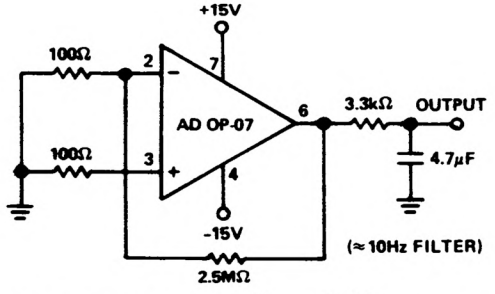


TO-99
BOTTOM VIEW

H-PACKAGE

PIN CONFIGURATION
TOP VIEW





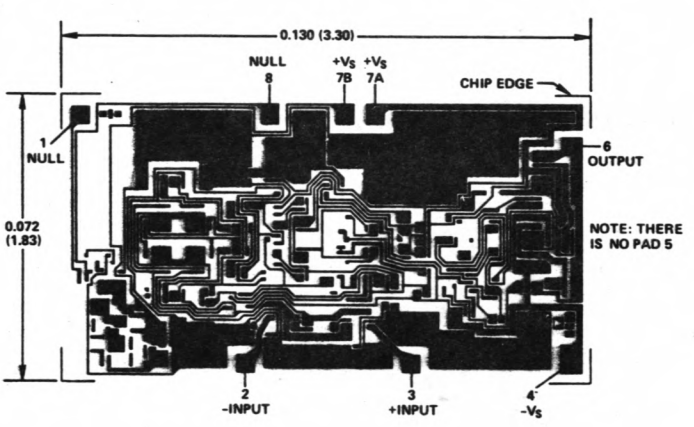
INPUT REFERRED NOISE = $\frac{V_O}{25,000} = \frac{5mV/cm}{25,000} = 200nV/cm$

SEE NOISE PHOTO-PAGE 5

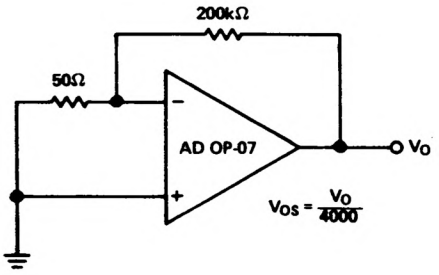
Low Frequency Noise Test Circuit

CHIP DIMENSIONS AND BONDING DIAGRAM

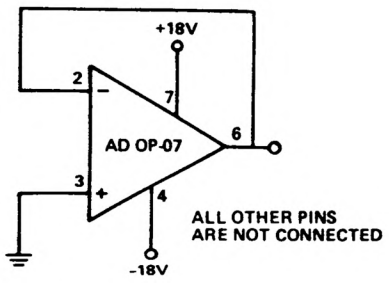
Dimensions shown in inches and (mm).



The AD OP-07 is available in wafer-trimmed chip form for precision hybrids. Consult the factory directly for details.



Offset Voltage Test Circuit



Burn-In Circuit

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/201A/301A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

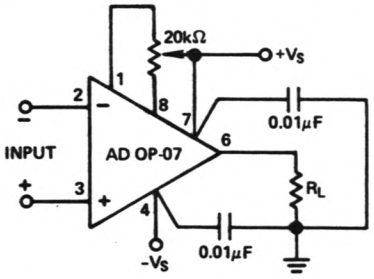


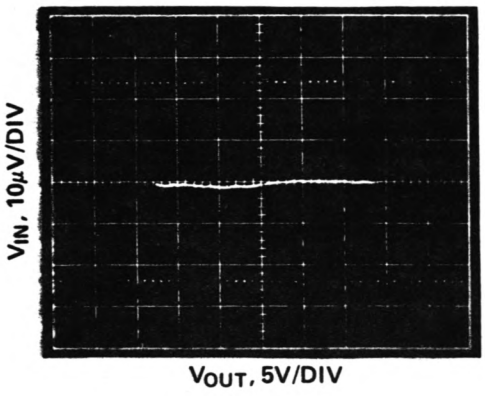
Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

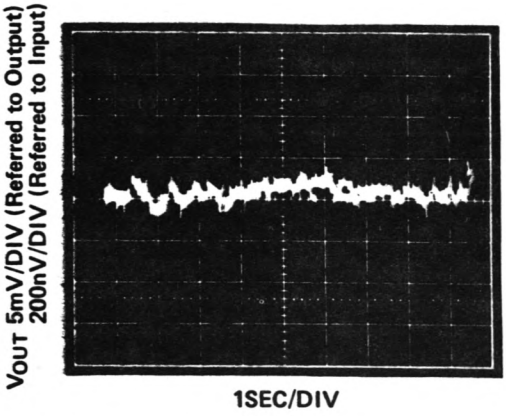
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

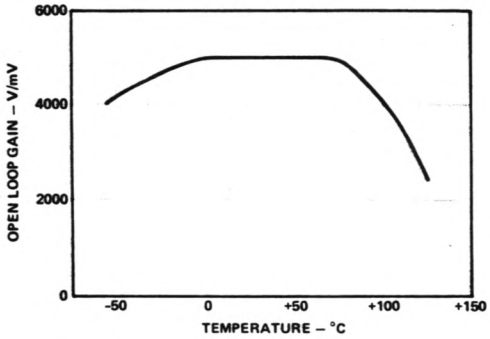
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



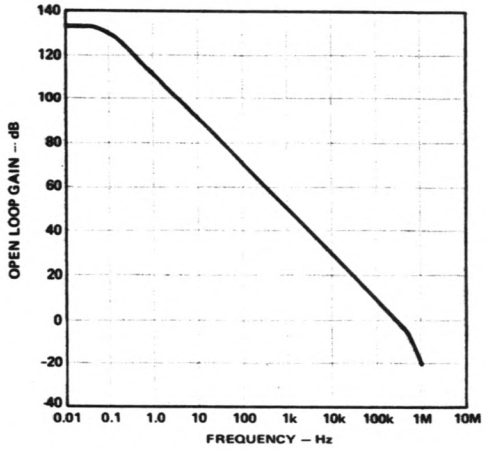
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

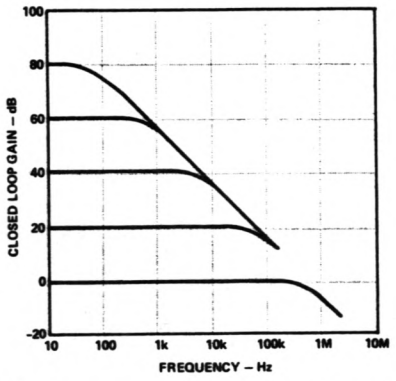


Open Loop Gain vs. Temperature

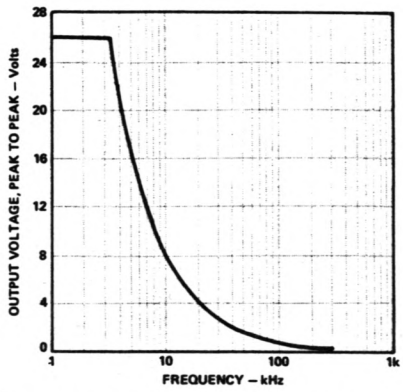


Open Loop Frequency Response

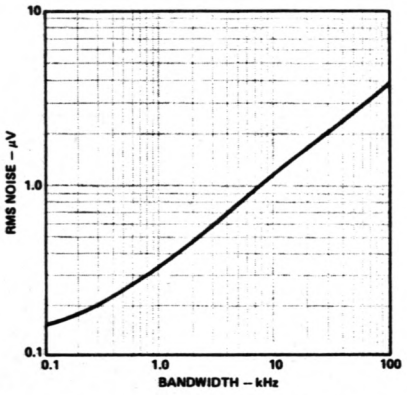
Typical Performance Curves



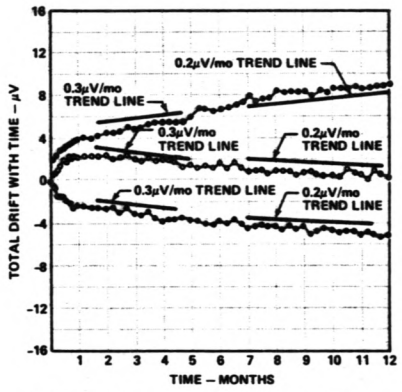
Closed Loop Response for Various Gain Configurations



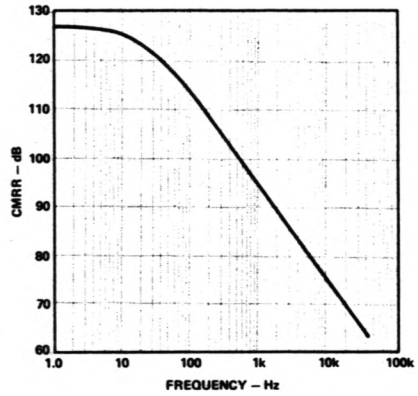
Maximum Undistorted Output vs. Frequency



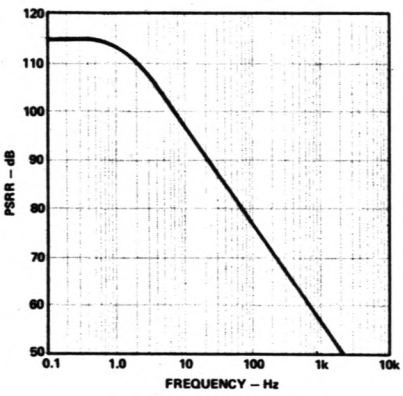
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



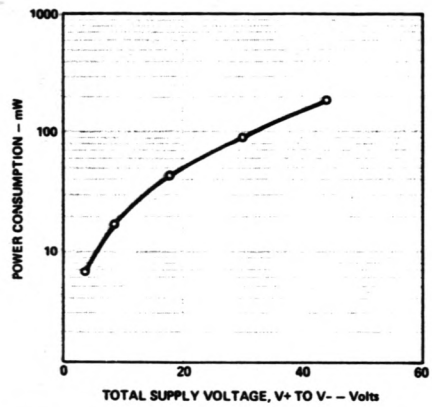
Offset Voltage Stability vs. Time



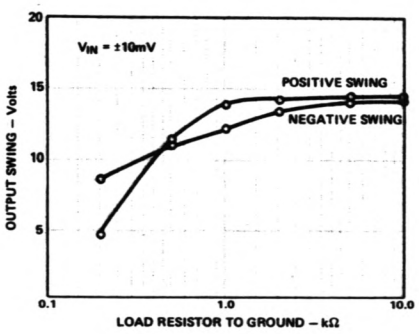
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ELECTRONIC INNOVATIONS IN ACTION — SEMICONDUCTORS

Silicon Power Pac Transistors

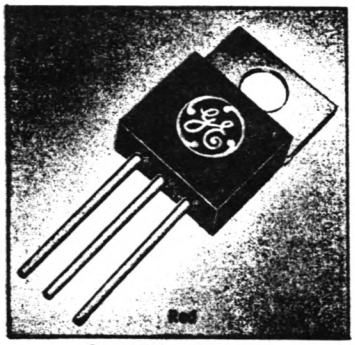
"Color Molded"

50.68 7/70
Supersedes 50.68 1/70

NPN

D44C8

The General Electric D44C is a red, silicone plastic encapsulated, power transistor designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1.0 mHz; series, shunt and switching regulators; low and high frequency inverters/converters; and many others.



Compatible with JEDEC TO-66 mounting registration

FEATURING:

- NPN complement to D45C PNP
- Red for NPN, green for PNP
- Very low collector saturation voltage (0.5V typ. @ 3.0A I_C)
- Excellent linearity
- Fast switching
- Round leads

absolute maximum ratings: (25°C) (unless otherwise specified)

		D44C1 D44C2 D44C3	D44C4 D44C5 D44C6	D44C7 D44C8	
Voltages					
Collector to Emitter	V_{CEO}	30	45	60	Volts
Emitter to Base	V_{EBO}	5	5	5	Volts
Collector to Emitter	V_{CES}	40	55	70	Volts
Current(1)					
Collector (Continuous)	I_C	←	4	→	Amps
Collector (Peak)		←	6	→	Amps
Power Dissipation(1)					
Case at 25°C	P_T	←	30	→	Watts
Case at 70°C		←	19	→	Watts
Free Air at 25°C		←	1.67	→	Watts
Free Air at 50°C		←	1.33	→	Watts
Thermal Resistance(2)					
Junction to Case	$R_{\theta JC}$	←	4.2	→	°C/W
Junction to Ambient	$R_{\theta JA}$	←	75	→	°C/W
Temperature(2)					
Operating	T_J	←	−55 to +150	→	°C
Storage	T_{STG}	←	−55 to +150	→	°C
Lead Soldering, 1/16" ± 1/32" from case for 10 seconds max.	T_L	←	+260	→	°C

Notes:
(1) Refer to the Safe Region of Operation curve for further information.
(2) Case temperature reference point is indicated on the Dimensional Outline Drawing.

electrical characteristics: (25°C) (unless otherwise specified)

		D44C3 D44C6		D44C2 D44C5 D44C8		D44C1 D44C4 D44C7
		Min.	Max.	Min.	Max.	Min.
Forward Current Transfer Ratio						
(V_{CE} = 1V, I_C = 0.2A)	h_{FE}	40	120	40	120	25
(V_{CE} = 1V, I_C = 2A)	h_{FE}	20	—	—	—	—
(V_{CE} = 1V, I_C = 1A)	h_{FE}	—	—	20	—	10

GENERAL ELECTRIC

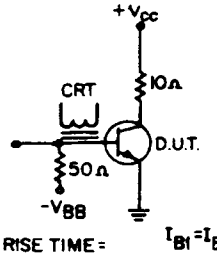
Electrical Characteristics (Continued)

		Min.	Max.	
Collector to Emitter Sustaining Voltage[3]				
(I_C = 100 mA) D44C1, 2, 3	$V_{CEO(SUS)}$	30	—	Volts
D44C4, 5, 6		45	—	Volts
D44C7, 8		60	—	Volts
Collector Saturation Voltage[3]				
(I_C = 1A, I_B = 50 mA) D44C2, 3. 5, 6, 8	$V_{CE(SAT)}$	—	0.5	Volt
(I_C = 1A, I_B = 100 mA) D44C1, 4, 7	$V_{CE(SAT)}$	—	0.5	Volt
Base Saturation Voltage[3]				
(I_C = 1A, I_B = 100 mA)	$V_{BE(SAT)}$	—	1.3	Volts
Collector Cutoff Current				
(V_{CB} = Rated V_{CES}, T_J = 25°C)	I_{CES}	—	10	μA
Emitter Cutoff Current				
(V_{EB} = 5V, T_J = 25°C)	I_{EBO}	—	100	μA
Collector Capacitance				
(V_{CB} = 10V, f = 1 mHz)	C_{CBO}	—	100	pF

		Typ.	
Gain Bandwidth Product			
(V_{CE} = 4V, I_C = 20 mA)	f_t	50	mHz
Switching Times (See Figures 1 and 2)			
Rise Time and Delay Time			
(I_C = 1A, I_{B1} = 0.1A)	$t_d + t_r$	100	nsec
Storage Time			
(I_C = 1A, $I_{B1} = I_{B2}$ = 0.1A)	t_s	500	nsec
Fall Time			
(I_C = 1A, $I_{B1} = I_{B2}$ = 0.1A)	t_f	75	nsec

Note:
(3) Pulsed measurement, 300 μsec pulse, duty cycle ≤2%.

SWITCHING CIRCUIT TO MEASURE SWITCHING TIMES



RISE TIME = 1 NANOSECONDS MAX
FALL TIME = 1 NANOSECONDS MAX
$I_{B1} = I_{B2}$ = 0.1 AMPS
PULSE = 10 μ SEC
P.R.T. = 10m SEC
CRT = TEKTRONIX CURRENT TRANSFORMER

FIGURE 1

OSCILLOSCOPE DISPLAY OF INPUT AND OUTPUT PULSE WAVEFORM IS OF SWITCHING CIRCUIT SHOWN IN FIGURE 1

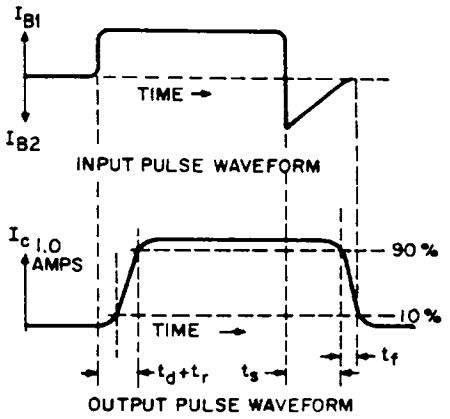
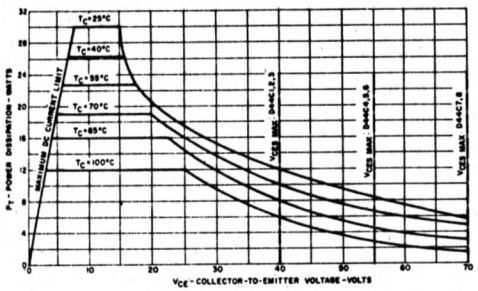
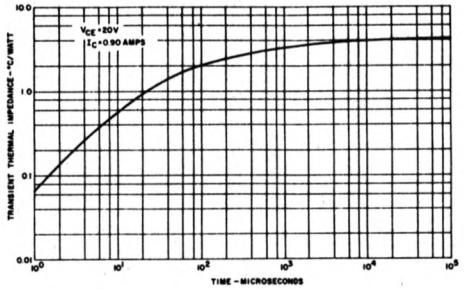


FIGURE 2

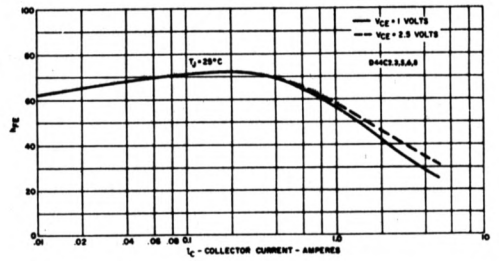
MAXIMUM PERMISSIBLE DC POWER DISSIPATION



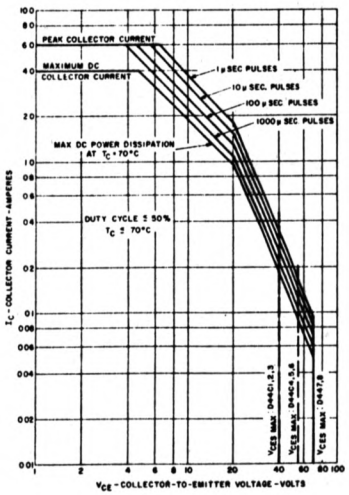
NORMALIZED TRANSIENT THERMAL IMPEDANCE
Junction to Case



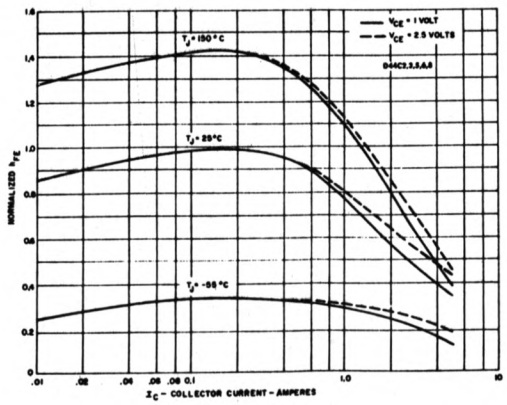
TYPICAL h_{FE} VS. I_C



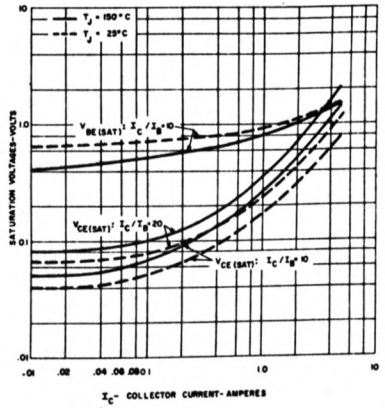
SAFE REGION OF OPERATION



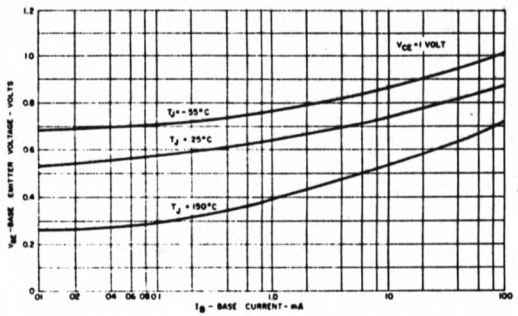
NORMALIZED h_{FE} VS. I_C



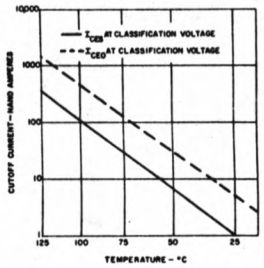
TYPICAL SATURATION VOLTAGE CHARACTERISTICS



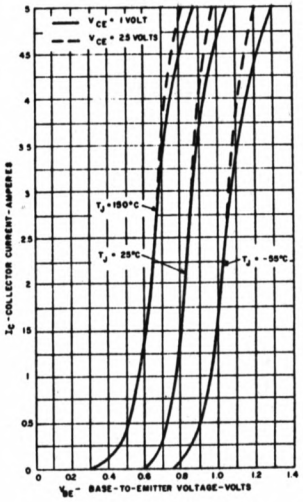
TYPICAL INPUT CHARACTERISTICS



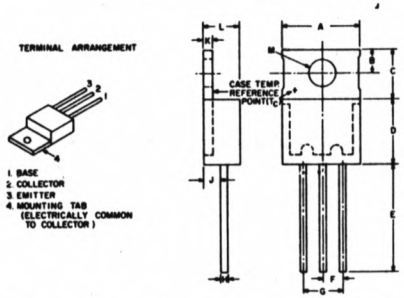
TYPICAL I_{CEO}, I_{CES} VS. TEMPERATURE



TYPICAL TRANSCONDUCTANCE CHARACTERISTICS

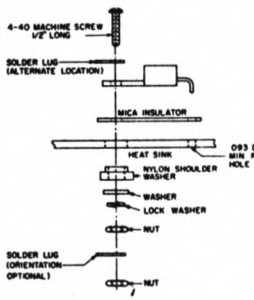


DIMENSIONAL OUTLINES



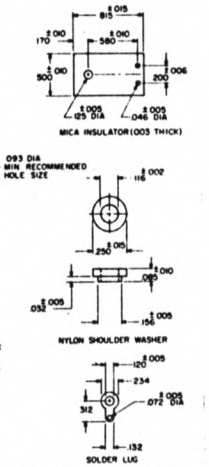
Sym.	Min.	Max.	Min.	Max.
A	.395	.405	10.03	10.29
B	.110	.120	2.79	3.05
C	.250	.260	6.35	6.61
D	.340	.350	8.64	8.89
E	.500	——	12.7	——
F	.095	1.05	2.41	2.67
G	.190	.210	4.82	5.34
H	.029	.035	.73	.89
J	.085	.115	2.16	2.92
K	.050	.060	1.27	1.52
L	.170	.190	4.32	4.83
M	.141	.145	3.58	3.68
N	——	.065	——	1.65

TYPICAL INSULATING MOUNTING



NOTE. THE THERMAL RESISTANCE TAB TO HEAT SINK WITH THE MICA WASHER IS APPROXIMATELY 4.3°C/W WITHOUT ANY THERMAL CONDUCTING COMPOUND AND ABOUT 1.25°C/W WITH A THERMAL GREASE.

INSULATING KIT



THE ABOVE PARTS WILL BE AVAILABLE UPON REQUEST AS A SEPARATE KIT AT AN ADDITIONAL COST. KIT # 130B108P5

Codes: 50, 52, 54, 55, 56; 41, 42, 45

PRINTED IN U.S.A.

GENERAL ELECTRIC

LOW-NOISE PRECISION OPERATIONAL AMPLIFIER

OP-27

FEATURES

- **Low Noise** ..... { ... **80nV$_{p-p}$ (0.1Hz to 10Hz)** ... **3nV/$\sqrt{Hz}$**
- **Low Drift** ..... **0.2μV/°C**
- **High Speed** ..... { ... **2.8V/μs Slew Rate** ... **8MHz Gain Bandwidth**
- **Low V_{OS}** **10μV**
- **Excellent CMRR** ..... **126dB at V_{CM} of ±11V**
- **High Open-Loop Gain** ..... **1.8 Million**
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**

GENERAL DESCRIPTION

The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5nV/$\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

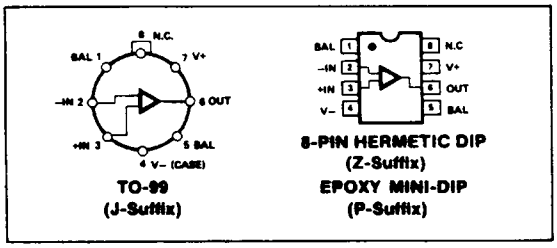
The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ORDERING INFORMATION†

V_{OS} @ 25°C MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
	OP27AJ*	OP27AZ*		MIL
	OP27EJ	OP27EZ	OP27EP	IND/COM
	OP27BJ*	OP27BZ*		MIL
	OP27FJ	OP27FZ	OP27FP	IND/COM
	OP27CJ*	OP27CZ*		MIL
	OP27GJ	OP27GZ	OP27GP	IND/COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.
†Commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

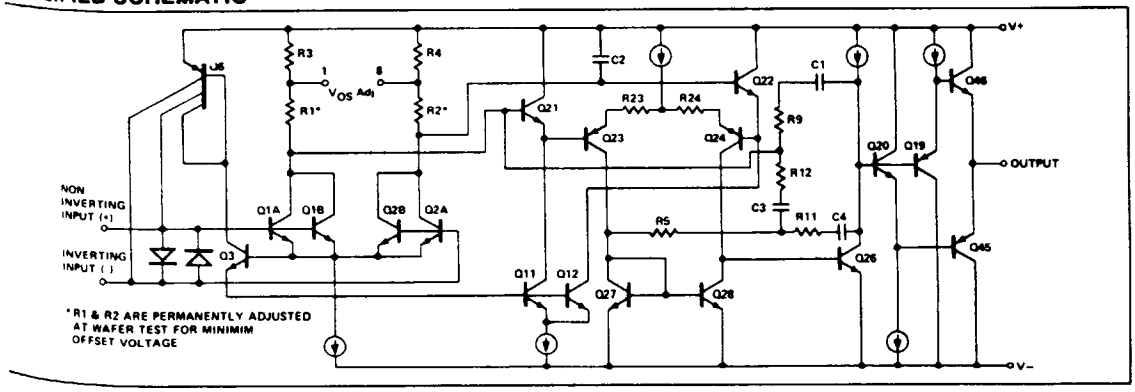
PIN CONNECTIONS



TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)
EPOXY MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



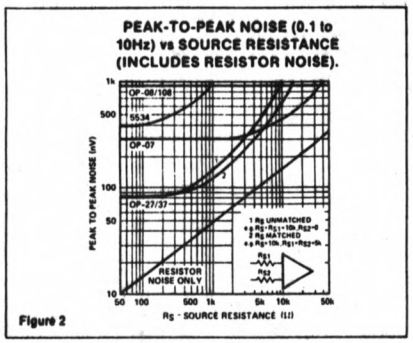


Figure 2

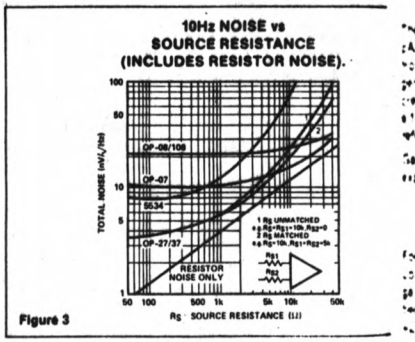


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption. (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

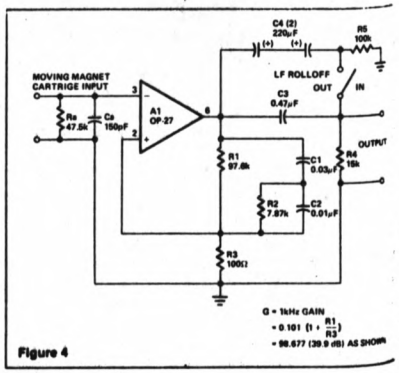


Figure 4

The OP-27 brings a $3.2nV/\sqrt{Hz}$ voltage noise and 0.45 $pA/\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of $1.3nV/\sqrt{Hz}$. The noise increases the $3.2nV/\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

The gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

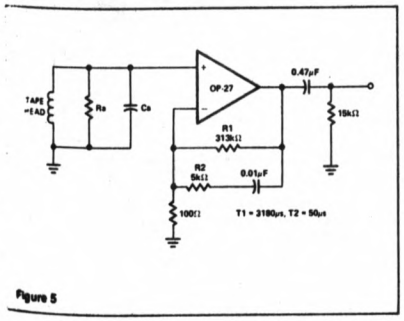


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz (T_2 = 50μs), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4nV/\sqrt{Hz}$ noise, while the op amp generates a $3.2nV/\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about $6nV/\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

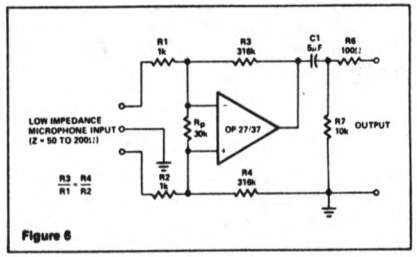
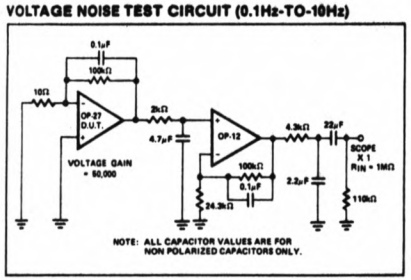


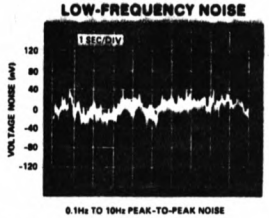
Figure 6

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)



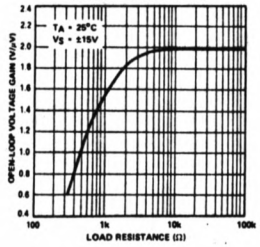
LOW-FREQUENCY NOISE



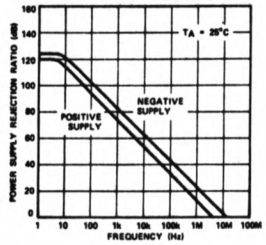
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

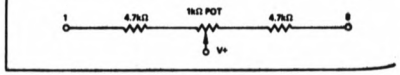
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

The OP-27 provides stable operation with load capacitances of up to 2000pF and ± 10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33μV/°C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, the network below will have a ±260μV adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

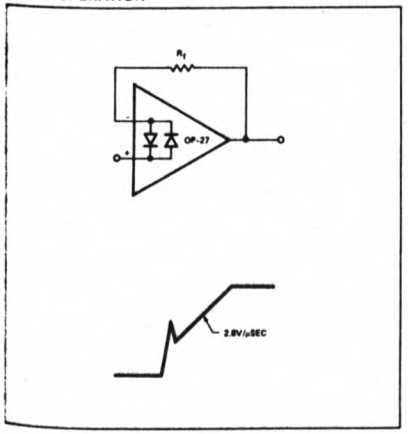
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20$mA at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25°C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $\sqrt{[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

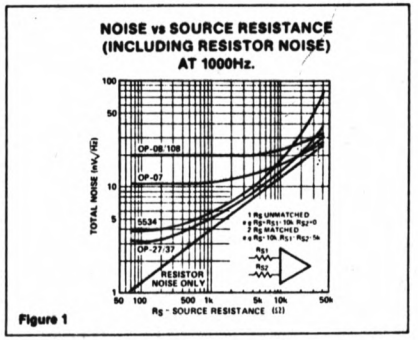


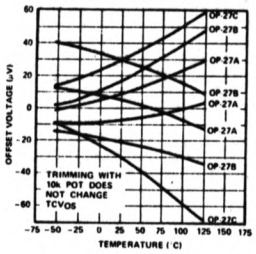
Figure 1

At $R_S < 1k\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

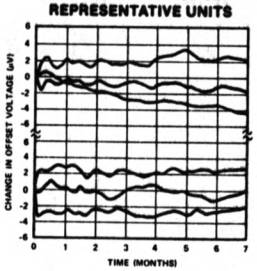
Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

TYPICAL PERFORMANCE CHARACTERISTICS

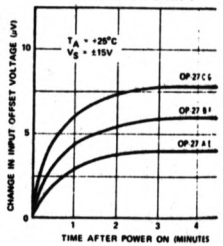
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



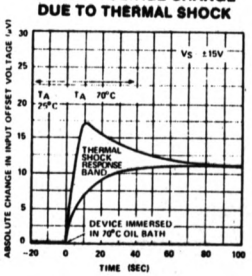
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



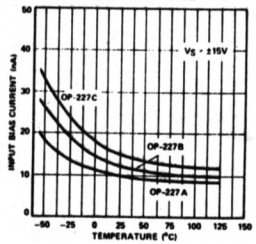
WARM-UP OFFSET VOLTAGE DRIFT



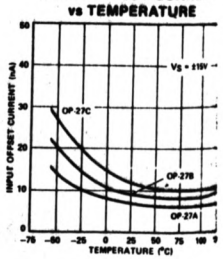
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



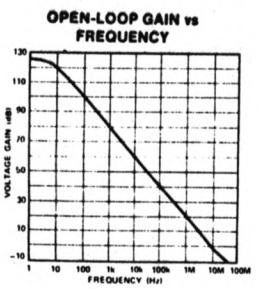
INPUT BIAS CURRENT vs TEMPERATURE



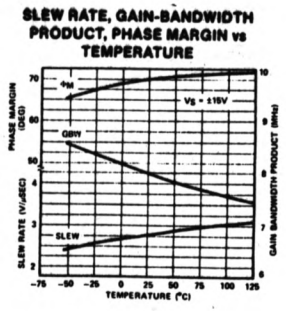
INPUT OFFSET CURRENT vs TEMPERATURE



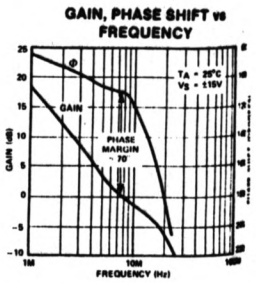
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



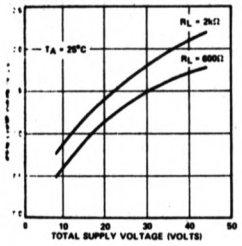
GAIN, PHASE SHIFT vs FREQUENCY



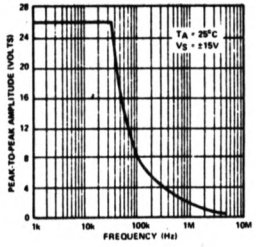
OP-27 LOW-NOISE PRECISION OPERATIONAL AMPLIFIER

TYPICAL PERFORMANCE CHARACTERISTICS

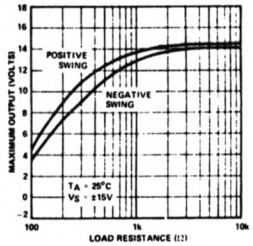
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



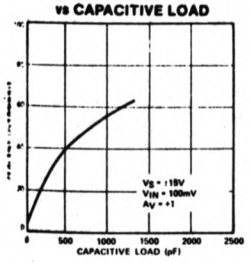
MAXIMUM OUTPUT SWING vs FREQUENCY



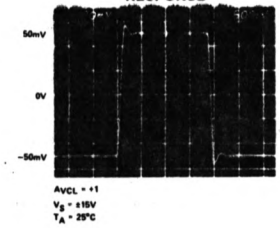
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



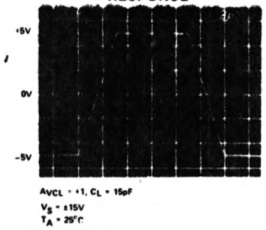
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



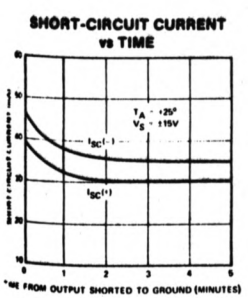
SMALL-SIGNAL TRANSIENT RESPONSE



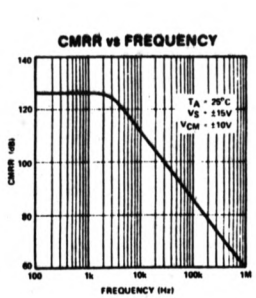
LARGE-SIGNAL TRANSIENT RESPONSE



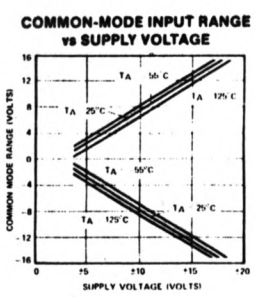
SHORT-CIRCUIT CURRENT vs TIME



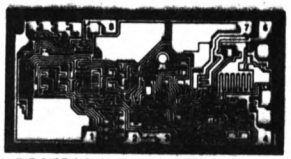
CMRR vs FREQUENCY



COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



DICE CHARACTERISTICS



DIE SIZE 0.054 × 0.108 inch, 5832 sq. mils
(1.37 × 2.74mm, 3.76 sq. mm)

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125°C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = IVR	106	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 600	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±11.5 —	±12.0 ±10.0	±11.0 —	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

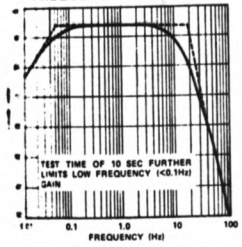
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled R_P = 8kΩ to 20kΩ	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 30Hz f_O = 1000Hz	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	nV/√Hz
Input Noise Current Density	i_n	f_O = 10Hz f_O = 30Hz f_O = 1000Hz	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	pA/√Hz
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8	8	8	MHz

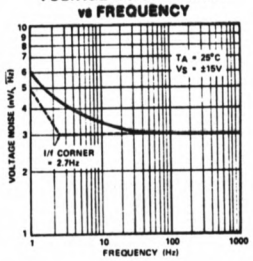
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

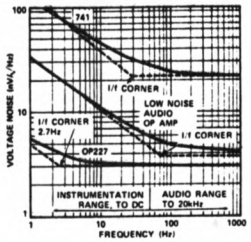
0.1Hz TO 10Hz$_{p-p}$ NOISE TESTER FREQUENCY RESPONSE



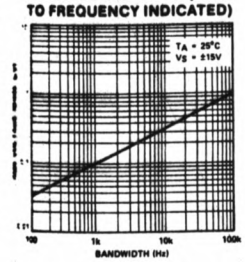
VOLTAGE NOISE DENSITY vs FREQUENCY



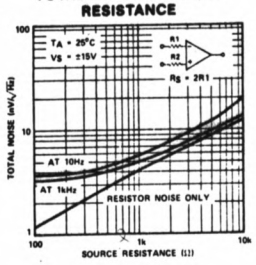
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



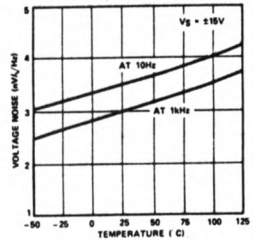
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



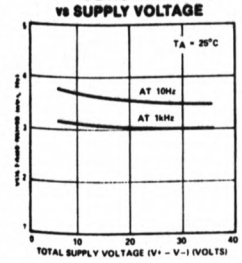
TOTAL NOISE vs SOURCE RESISTANCE



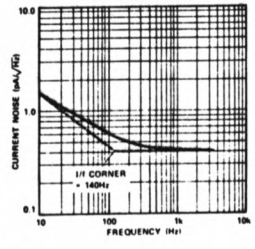
VOLTAGE NOISE DENSITY vs TEMPERATURE



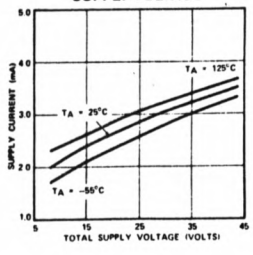
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY



SUPPLY CURRENT vs SUPPLY VOLTAGE



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 3) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-27A, OP-27B, OP-27C (J, Z) ..... −55°C to +125°C
OP-27E, OP-27F, OP-27G (J, Z) ..... −25°C to +85°C
OP-27E, OP-27F, OP-27G (P) ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating fac

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.8mW/°C

2. The OP-27's inputs are protected by back-to-back diodes. Current lim resistors are not used in order to achieve low noise. If differential i voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input volta equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, un otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	µ
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	µV/
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	n
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	n
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	µVp
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	nV/√Hz
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	
		f_O = 30Hz (Notes 3,6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	pA/√Hz
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	1.5	6	—	1.2	5	—	0.8	4	—	M
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	d
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	µV/
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/m
		R_L ≥ 600Ω, V_O = ±10V	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	
		R_L ≥ 600Ω	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	R_L ≥ 2kΩ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/µ
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MH
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	70	—	—	70	—	—	70	—	
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	m
Offset Adjustment Range		R_P = 10kΩ	—	±4.0	—	—	±4.0	—	—	±4.0	—	m

NOTES:
1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

ELECTRICAL CHARACTERISTICS for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A MIN	OP-27A TYP	OP-27A MAX	OP-27B MIN	OP-27B TYP	OP-27B MAX	OP-27C MIN	OP-27C TYP	OP-27C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	µV
Average Input Offset Drift	TCV_{OS} / TCV_{OSn}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	µV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	2	16	—	2	20	—	4	51	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

ELECTRICAL CHARACTERISTICS for V_S = ±15V, −25°C ≤ T_A ≤ +85°C for OP-27J and OP-27Z, 0°C ≤ T_A ≤ +70°C for OP-27P, unless otherwise noted.

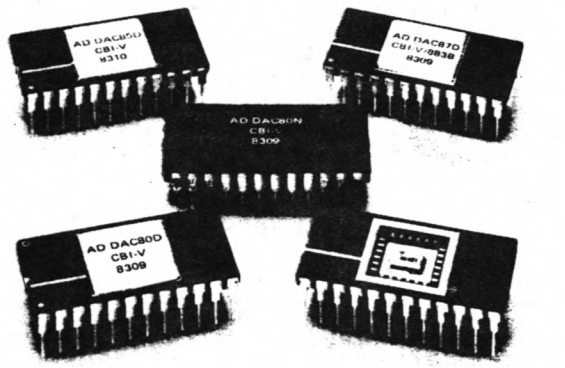
PARAMETER	SYMBOL	CONDITIONS	OP-27E MIN	OP-27E TYP	OP-27E MAX	OP-27F MIN	OP-27F TYP	OP-27F MAX	OP-27G MIN	OP-27G TYP	OP-27G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	µV
Average Input Offset Drift	TCV_{OS} / TCV_{OSn}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	µV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	2	15	—	2	16	—	2	32	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1 Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2 The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8kΩ to 20kΩ.

Complete Low Cost 12-Bit Monolithic D/A Converter

AD DAC80, AD DAC85, AD DAC87

FEATURES
- **Single Chip Construction**
- **On-Board Output Amplifier**
- **Low Power Dissipation: 300mW**
- **Monotonicity Guaranteed over Temperature**
- **Guaranteed for Operation with ±12V Supplies**
- **Improved Replacement for Standard DAC80, DAC800 HI-5680**
- **High Stability, High Current Output Buried Zener Reference**
- **Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity**
- **Low Cost Plastic Packaging**



PRODUCT DESCRIPTION

The AD DAC80 Series is a family of low cost 12-bit digital-to-analog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The AD DAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300mW which not only improves reliability but also improves long term stability.

The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete zener references.

The AD DAC80 Series is available in three performance grades and two package types. The AD DAC80 is specified for use over the 0 to +70°C temperature range and is available in both plastic and ceramic DIP packages. The AD DAC85 and AD DAC87 are available in hermetically sealed ceramic packages and are specified for the −25°C to +85°C and −55°C to +125°C temperature ranges.

PRODUCT HIGHLIGHTS

1. The AD DAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
3. The high speed output amplifier has been designed to settle within 1/2LSB for a 10V full scale transition in 2.0μs, when properly compensated.
4. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
6. System performance upgrading is possible without redesign.

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Tel: 617/329-4700 **Twx: 710/394-6577**
Telex: 924491 **Cables: ANALOG NORWOODMASS**

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC80 Min	AD DAC80 Typ	AD DAC80 Max	AD DAC85 Min	AD DAC85 Typ	AD DAC85 Max	AD DAC87 Min	AD DAC87 Typ	AD DAC87 Max	Units
TECHNOLOGY		Monolithic			Monolithic			Monolithic		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			250			250			250	μA
I_{IL} (V_{IL} = 0.8V)			100			100			100	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C			±1/2			±1/2			±1/2	LSB[1]
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C			±3/4			±3/4			±3/4	LSB
T_A @ T_{min} to T_{max}			±3/4			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.2		±0.1	±0.2	% FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05	±0.1		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	−25		+85	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20			±20			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15		±0.12	±0.2		±0.18	±0.3	% of FSR
Bipolar		±0.06	±0.10		±0.08	±0.12		±0.14	±0.24	% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±4	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ/500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Current Models										
Ranges – Unipolar	−1.96	−2.0	−2.04	−1.96	−2.0	−2.04	−1.96	−2.0	−2.04	mA
– Bipolar	±0.96	±1.0	±1.04	±0.96	±1.0	±1.04	±0.96	±1.0	±1.04	mA
Output Impedance – Bipolar	2.5	3.2	4.1	2.5	3.2	4.1	2.5	3.2	4.1	kΩ
– Unipolar	5.0	6.6	8.2	5.0	6.6	8.2	5.0	6.6	8.2	kΩ
Compliance	−2.5		+10	−2.5		+10	−2.5		+10	V
Internal Reference Voltage (V_R)	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable			±0.002			±0.002			±0.002	% of FSR/%V_S
±12V ±5%			±0.002			±0.002			±0.002	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range										
Analog Supplies	±11.4[7]		±16.5	±11.4[7]		±16.5	±11.4[7]		±16.5	V
Logic Supplies									V	
Supply Drain										
+12, +15V		5	10		5	10		5	10	mA
−12, −15V		14	20		14	20		14	20	mA
+5V										mA
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+125	−65		+150	−65		+150	°C

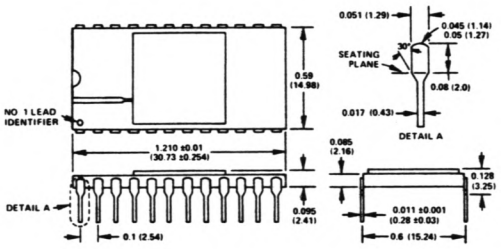
NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

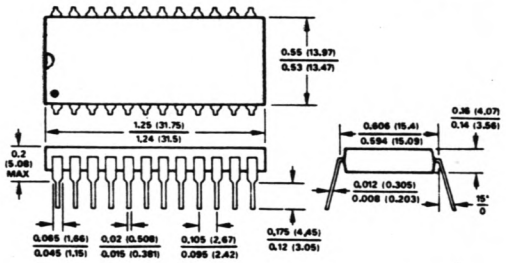
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

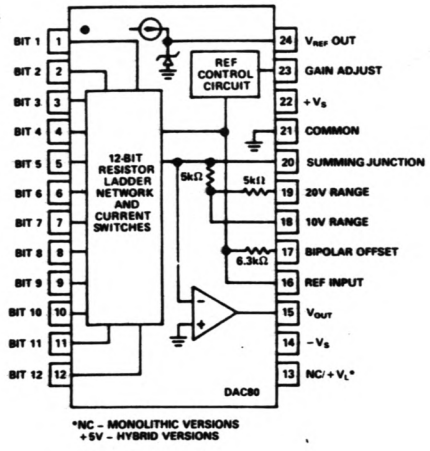
$+V_S$ to Power Ground . . . . . 0V to +18V
$-V_S$ to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 1 to 12) to Power Ground . . . −1.0V to +7V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite short to power ground or $+V_S$



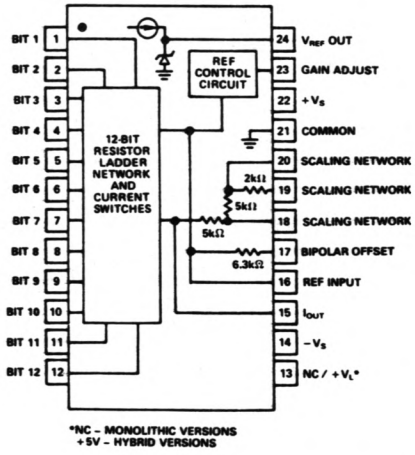
Hermetically-Sealed Ceramic Side Brazed Package (Type D) 24-Lead Dual In Line (Dimensions Shown in Inches and (mm))



Molded Plastic Package (Type N) 24-Lead Dual In Line (Dimensions Shown in Inches and (mm))



Voltage Model Functional Diagram and Pin Configuration



Current Model Functional Diagram and Pin Configuration

ORDERING GUIDE

Model	Package	Temperature Range	Linearity Error at +25°C
AD DAC80N-CBI-V	Plastic	0 to +70°C	±1/2LSB
AD DAC80D-CBI-V	Ceramic	0 to +70°C	±1/2LSB
AD DAC80D-CBI-I	Ceramic	0 to +70°C	±1/2LSB
AD DAC85D-CBI-V	Ceramic	−25°C to +85°C	±1/2LSB
AD DAC87D-CBI-V	Ceramic	−55°C to +125°C	±1/2LSB

DIGITAL INPUT CODES

The AD DAC80 Series accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for anyone of three complementary codes: CSB, COB or CTC.

Digital Input		Analog Output		
MSB	LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
0 0 0 0 0 0 0 0 0 0 0 0		+ Full Scale	+ Full Scale	− 1LSB
0 1 1 1 1 1 1 1 1 1 1 1		+ 1/2 Full Scale	Zero	− Full Scale
1 0 0 0 0 0 0 0 0 0 0 0		Mid-Scale	− 1LSB	+ Full Scale
1 1 1 1 1 1 1 1 1 1 1 1		Zero	− Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 1 1/2LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at the lowest operating temperature, +25°C and the highest operating temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 . . . 1 1 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25pF as shown in Figure 1a.

Current Output Models. Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage ranges of ±1V and 0 to −2V.

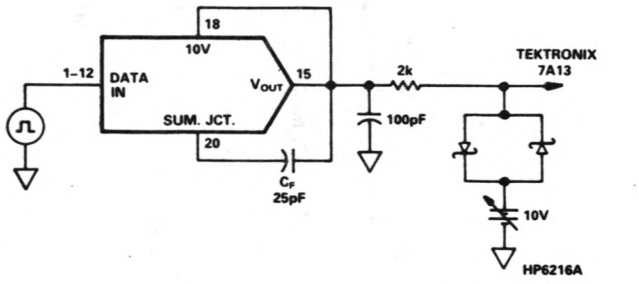


Figure 1a. Voltage Model Settling Time Circuit

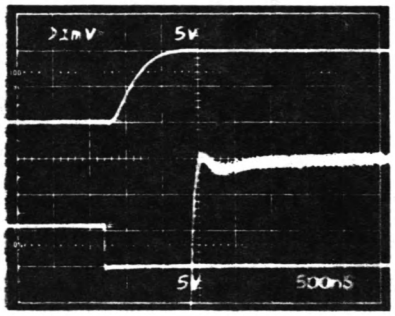


Figure 1b. Voltage Model Settling Time C_F = 25pF

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 2. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input codes, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

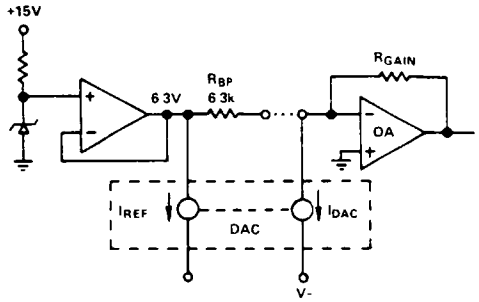


Figure 2. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ± 1/2LSB max and the differential linearity error of ± 3/4LSB max guarantee monotonic performance over the specified range. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 3. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 2) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 3. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to 10ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to 10ppm °C max.

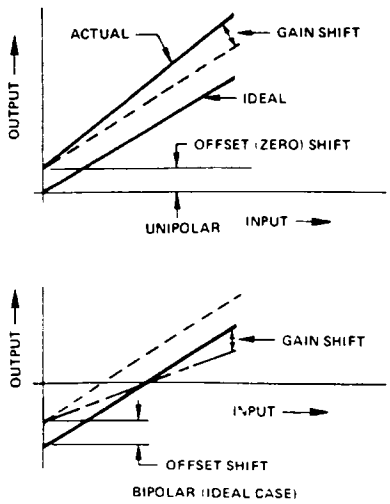


Figure 3. Unipolar and Bipolar Drifts

Using the AD DAC80 Series

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1μF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the AD DAC80 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 6 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

Offset Adjustment. For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is −10V. See Table II for corresponding codes.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

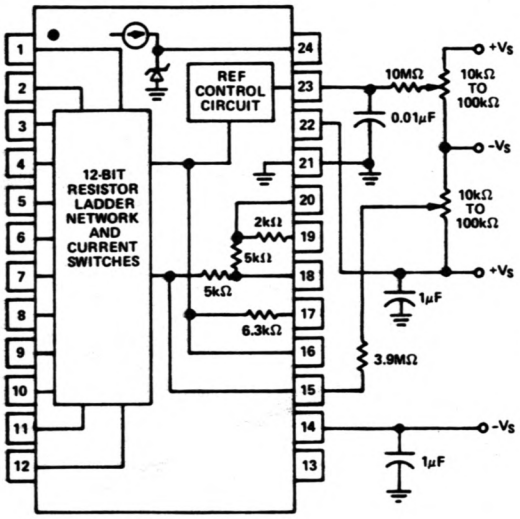


Figure 4. External Adjustment and Voltage Supply Connection Diagram, Current Model

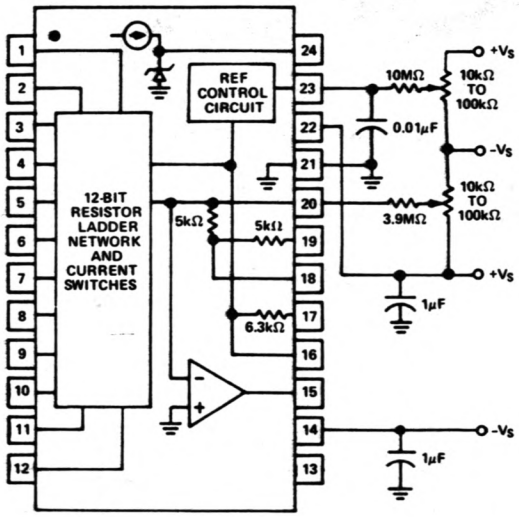


Figure 5. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

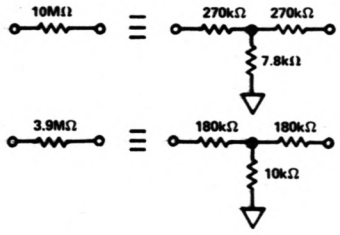


Figure 6. Equivalent Resistances

Digital Input			Analog Output			
	12 Bit Resolution		Voltage*		Current	
	MSB	LSB	0 to +10V	±10V	0 to −2mA	±1mA
CBI Model	0 0 0 0 0 0 0 0 0 0 0 0		+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
	0 1 1 1 1 1 1 1 1 1 1 1		+5.0000V	00000V	−1.0000mA	0.0000mA
	1 0 0 0 0 0 0 0 0 0 0 0		+4.9976V	−0.0049V	0.488mA	+1.000mA
	1 1 1 1 1 1 1 1 1 1 1 1		0.0000V	−10.0000V	0.0000mA	0.488μA
	1LSB		2.44mV	4.88mV	−0.9995mA	+0.0005mA

*To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

Table II. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC80 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 7).

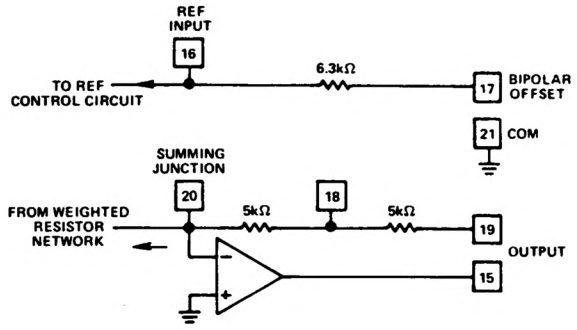


Figure 7. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 4 microseconds for a 10kΩ feedback resistor; 3 microseconds for a 5kΩ feedback resistor when using the compensation capacitor shown in Figure 1.

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 8 and 9. External R_{LS} resistors are required to produce exactly 0 to −2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

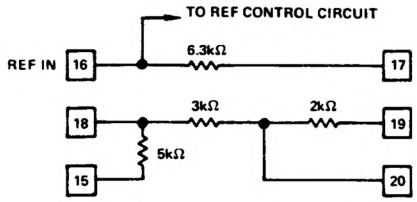


Figure 8. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to −2V. These resistors (R_{LI}: TCR = 20ppm/°C) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

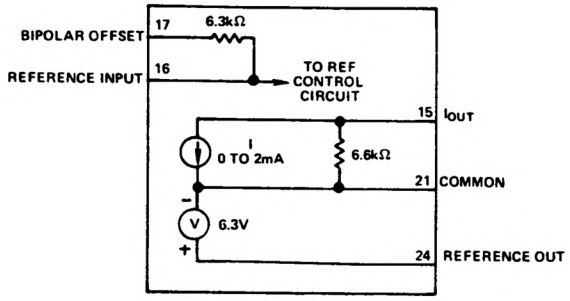


Figure 9. AD DAC80 Current Model Equivalent Output Circuit

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LI} Connections: Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	R_{LS}
CSB	0 to −2V	0.968kΩ	210Ω	20	19 & R_{LS}	15	24	Com 21	Between Pin 18 & Com 21
COB or CTC	±1V	1.2kΩ	249Ω	18	19	R_{LS}	24	15	Between Pin 20 & Com 21
CCD	0 to ±2V	3kΩ	N/A	N.C.	21	N.C.	24	N.C.	N/A

Table IV. Current Model Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 10 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = −2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to −2V. With $R_{LS} = 0$, $V_{OUT} = -1.69V$.

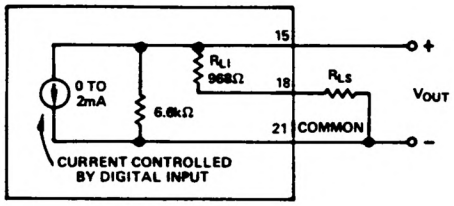


Figure 10. Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k}\right)$$

Where R_L max = 11.18kΩ

and V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 12,

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the AD DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 12.

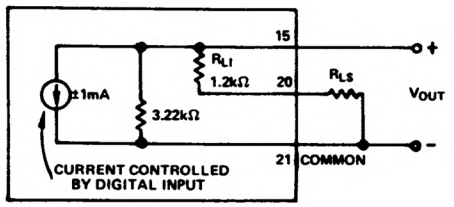


Figure 11. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

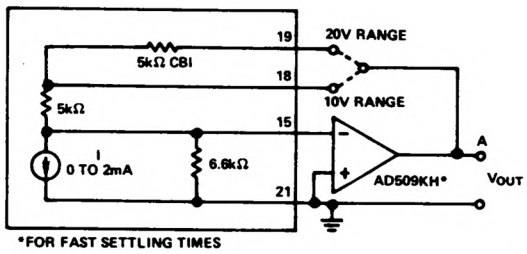


Figure 12. External Op Amp–Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

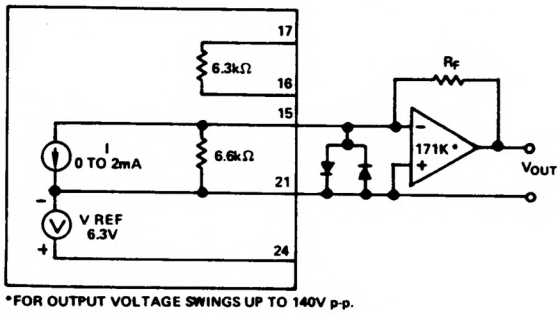


Figure 13. External Op Amp–Using External Feedback Resistors

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24

Table V. External Op Amp Voltage Mode Connections

Avantek

MONOLITHIC MICROWAVE INTEGRATED CIRCUIT DATA SHEET

MSA-0104
Cascadable Monolithic Silicon Integrated Circuit Amplifier
January, 1985
Summary

FEATURES

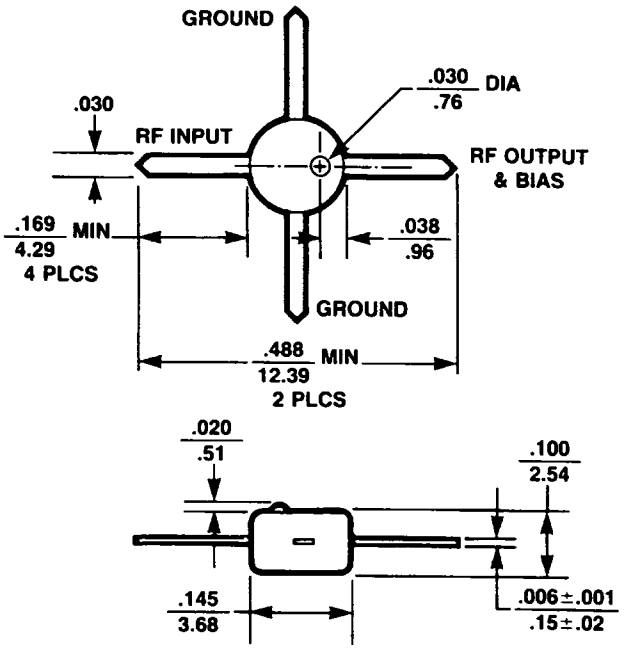
- **Plastic Package**
- **Fully Cascadable (VSWR<2:1)**
- **14 dB Gain at 1000 MHz**
- **+5V Bias (External Bias Resistor Required)**
- **+1.5 dBm P_{1dB} @ 500 MHz**
- **Short Group Delay**

DESCRIPTION

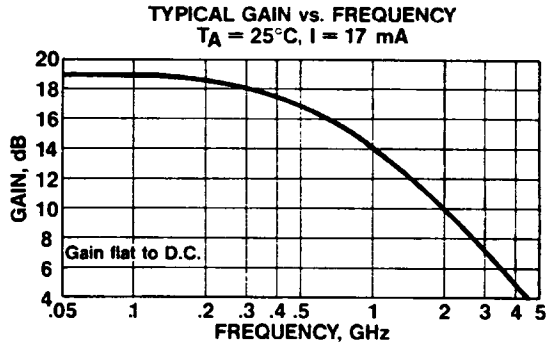
The MSA (Monolithic Silicon Amplifier) series is a family of silicon bipolar Monolithic Microwave Integrated circuits (MMICs) using nitride self-alignment, ion implantation for precise control of doping and nitride passivation for high reliability.

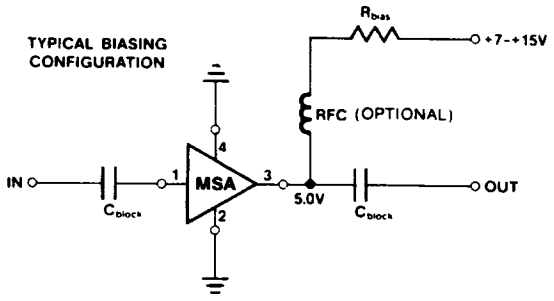
These MMICs use series and shunt feedback and exhibit very high uniformity from amplifer to amplifier. External blocking capacitors are required. Typical applications include narrow or broadband IF and RF amplifiers in industrial and commercial systems.

AVANTEK 04 PLASTIC PACKAGE



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. DIMENSIONS ARE IN IN / MM
2. TOLERANCES: XXX / XX ± .010 / .25





ELECTRICAL SPECIFICATIONS, T_A = 25°C

Symbol	Parameters/Test Conditions	Typical Volts	Current (mA)	Freq. (GHz)	Units	Min.	Typ.	Max.
$\|S_{21}\|^2$	Insertion Power Gain	5.0	17.0	0.1	dB	17.0	19.0	
$\|S_{21}\|^2$	Insertion Power Gain	5.0	17.0	1.0	dB		14.0	
VSWR	Freq. at VSWR=2:1	5.0	17.0		GHz		5	
P_{1dB}	Output Power at 1 dB Gain Compression	5.0	17.0	0.5	dBm		1.5	
NF_{50}	50Ω Noise Figure	5.0	17.0	0.5	dB		5	
IP_3	Third Order Intercept Point	5.0	17.0	0.5	dBm		15	
IP_2	Second Harmonic Intercept Point	5.0	17.0	0.5	dBm		31.0	
f_{1dB}	Frequency at −1dB Gain Point[1]	5.0	17.0		GHz		0.35	

Note 1 Frequency at which gain is 1 dB less than at 100 MHz.

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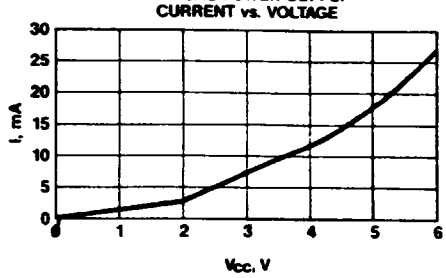
RECOMMENDED MAXIMUM RATINGS

Parameter	Cont. Oper	Abs. Max.
Power Supply Voltage	5.0 V	6.0 V
Power Supply Current	20 mA	40 mA
Case Temperature, Storage	—	150°C
Continuous RF Input Power	+16 dBm	+20 dBm
M.T.T.F. (Projected), Hrs.	$1x10^6$	$1x10^4$

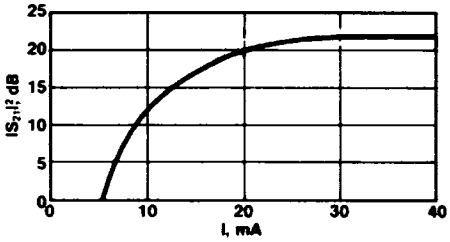
NOTES:
1. Operation of this device above any one of these parameters may shorten the MTTF from the design goals.
2. Operation of this device above any one of these parameters may cause permanent damage.

TYPICAL PERFORMANCE, $T_A = 25°C$

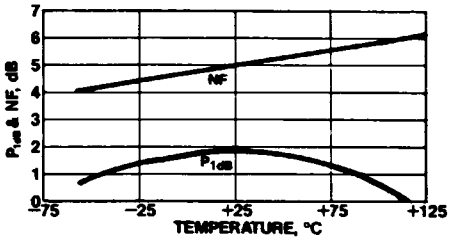
TYPICAL POWER SUPPLY CURRENT vs. VOLTAGE



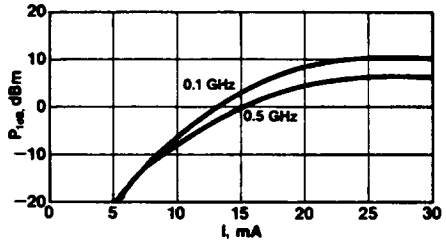
INSERTION POWER GAIN AT 0.1 GHz ($|S_{21}|^2$) vs. CURRENT



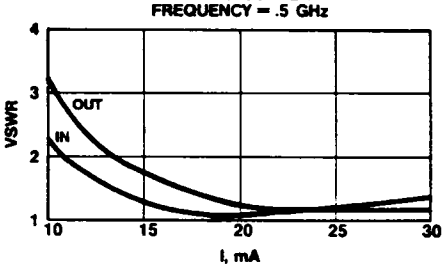
OUTPUT POWER AT 1dB GAIN COMPRESSION AND NOISE FIGURE vs. CASE TEMPERATURE
I = 17 mA, FREQ. = .5 GHz



OUTPUT POWER AT 1dB GAIN COMPRESSION vs. CURRENT AND FREQUENCY



VSWR vs. CURRENT
FREQUENCY = .5 GHz



TYPICAL SCATTERING PARAMETERS

V_{CE} = 5.0V, I_C = 17 mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	Mag	Ang	Mag	Ang
100.00	.045	131.6	18.8	8.775	170.3	.072	7.1	.046	-4.9
200.00	.068	112.5	18.7	8.583	160.8	.073	14.0	.051	-14.4
300.00	.086	94.1	18.4	8.282	152.4	.077	19.3	.046	-20.6
400.00	.106	82.1	18.0	7.943	146.1	.080	24.3	.046	-24.0
500.00	.120	72.5	17.4	7.383	138.6	.084	29.2	.043	-42.7
600.00	.128	66.4	16.9	7.029	131.5	.089	32.6	.043	-41.5
700.00	.132	59.3	16.5	6.676	125.7	.095	36.0	.041	-62.8
800.00	.140	55.1	15.7	6.089	120.4	.100	39.1	.036	-63.9
900.00	.142	52.1	15.3	5.836	115.1	.106	41.2	.039	-81.0
1000.00	.141	46.2	14.8	5.530	112.3	.113	43.0	.033	-93.2
1100.00	.142	46.0	14.2	5.121	107.2	.120	44.6	.040	-97.4
1200.00	.135	42.3	13.8	4.881	103.7	.127	46.3	.040	-120.8
1300.00	.135	41.3	13.3	4.631	99.7	.133	47.5	.041	-117.6
1400.00	.125	40.8	12.8	4.374	96.3	.141	48.2	.047	-132.8
1500.00	.117	39.7	12.4	4.166	93.1	.146	49.7	.047	-140.1
1600.00	.112	40.1	11.9	3.964	90.2	.153	49.0	.056	-142.6
1700.00	.102	39.6	11.6	3.803	87.2	.163	49.9	.061	-153.1
1800.00	.094	37.9	11.2	3.631	83.9	.168	50.9	.065	-156.0
1900.00	.087	39.2	10.8	3.473	81.4	.174	51.1	.073	-162.3
2000.00	.085	43.1	10.3	3.273	82.1	.173	53.6	.072	-159.8
2100.00	.064	39.7	10.0	3.167	76.8	.187	51.2	.083	-170.5
2200.00	.045	52.6	9.5	2.982	71.8	.195	47.3	.069	-171.8
2300.00	.050	63.9	9.8	3.076	69.6	.209	48.0	.081	-155.9
2400.00	.050	69.3	9.4	2.971	69.4	.209	50.1	.105	-168.5
2500.00	.044	89.0	9.3	2.908	69.1	.218	51.4	.109	-168.5
2600.00	.055	98.0	8.6	2.693	70.0	.211	53.5	.123	-176.1
2700.00	.058	102.9	8.3	2.591	64.2	.219	49.5	.131	-172.5
2800.00	.059	113.6	7.7	2.442	57.9	.221	46.3	.139	-176.0
2900.00	.090	126.3	8.3	2.589	52.8	.237	42.2	.159	-172.7
3000.00	.084	125.8	8.1	2.529	54.8	.251	45.7	.151	-174.7

Printed in U.S.A.

Avantek

MONOLITHIC MICROWAVE INTEGRATED CIRCUIT DATA SHEET

MSA-0204
Cascadable Monolithic Silicon Integrated Circuit Amplifier
February, 1985
Summary

FEATURES

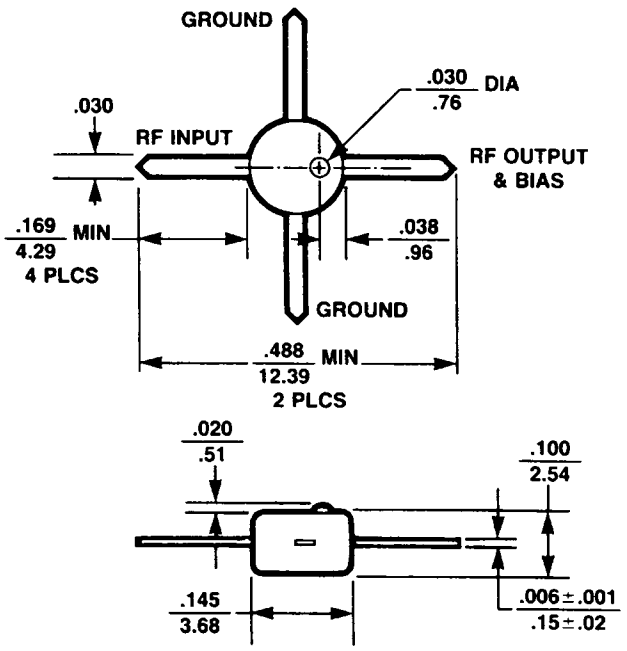
- **Plastic Package**
- **Fully Cascadable (VSWR <2:1)**
- **12.0 dB Gain at 500 MHz**
- **+5V Bias (External Bias Resistor Required)**
- **+4.0 dBm P_{1dB} @ 500 MHz**
- **Short Group Delay**

DESCRIPTION

The MSA (Monolithic Silicon Amplifier) series is a family of silicon bipolar Monolithic Microwave Integrated circuits (MMICs) using nitride self-alignment, ion implantation for precise control of doping and nitride passivation for high reliability.

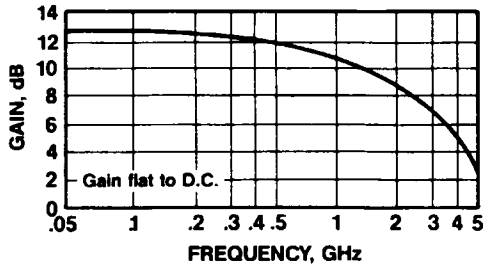
These MMICs use series and shunt feedback and exhibit very high uniformity from amplifier to amplifier. External blocking capacitors are required. Typical applications include narrow or broadband IF and RF amplifiers in industrial and commercial systems.

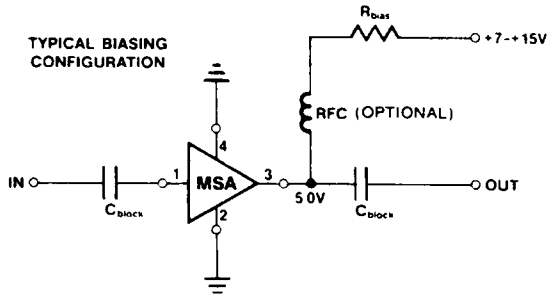
AVANTEK 04 PLASTIC PACKAGE



NOTES: (UNLESS OTHERWISE SPECIFIED)
1 DIMENSIONS ARE IN $\frac{IN}{MM}$
2 TOLERANCES $\frac{XXX}{XX} \pm \frac{010}{25}$

TYPICAL GAIN vs. FREQUENCY
T_A = 25°C, I = 25 mA





ELECTRICAL SPECIFICATIONS, T_A = 25°C

Symbol	Parameters/Test Conditions	Typical Volts	Current (mA)	Freq. (GHz)	Units	Min.	Typ.	Max
$\|S_{21}\|^2$	Insertion Power Gain	5.0	25.0	0.5	dB	10.0	12.0	—
$\|S_{21}\|^2$	Insertion Power Gain	5.0	25.0	1.0	dB	—	11.0	—
VSWR	Freq. at VSWR = 2:1	5.0	25.0	—	GHz	—	3.0	—
P_{1dB}	Output Power at 1 dB Gain Compression	5.0	25.0	0.5	dBm	—	4.0	—
NF_{50}	50Ω Noise Figure	5.0	25.0	0.5	dB	—	6.0	—
IP_3	Third Order Intercept Point	5.0	25.0	0.5	dBm	—	16.0	—
HP_2	Second Harmonic Intercept Point	5.0	25.0	0.5	dBm	—	31.0	—
f_{1dB}	Frequency at -1dB Gain Point[1]	5.0	25.0	—	GHz	—	0.8	—

Note 1 Frequency at which gain is 1 dB less than at 100 MHz

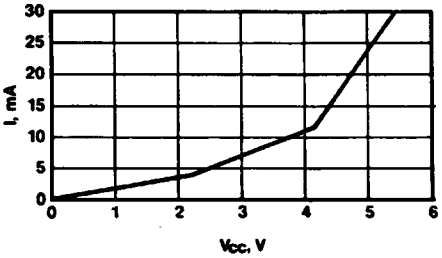
RECOMMENDED MAXIMUM RATINGS

Parameter	Cont.[1] Oper.	Abs.[2] Max.
Power Supply Voltage	5.0V	6.0V
Power Supply Current	30 mA	60 mA
Continuous RF Input Power	+16 dBm	+20 dBm
Storage Temperature	—	150° C
M.T.T.F. (Projected)	$1x10^6$ Hrs.	$1x10^4$ Hrs.
Thermal Resistance, Θjc	—	150° C/W

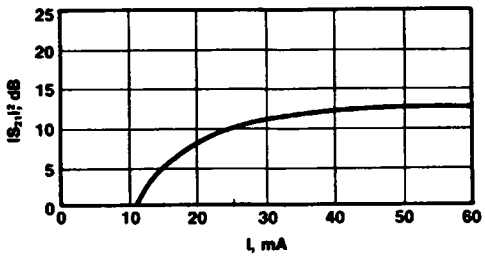
Notes:
1. Operation of this device above any one of these parameters may shorten the MTTF from the design goals.
2. Operation of this device above any one of these parameters may cause permanent damage.

TYPICAL PERFORMANCE, $T_A = 25°$ C

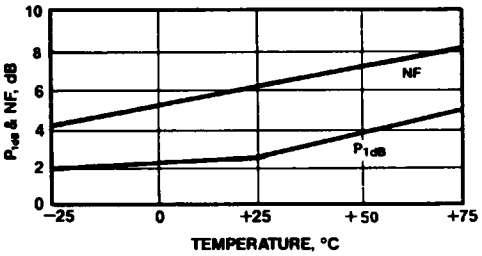
TYPICAL POWER SUPPLY CURRENT vs. VOLTAGE



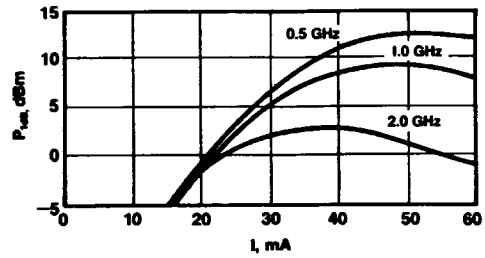
INSERTION POWER GAIN AT 0.5 GHz ($|S_{21}|^2$) vs. CURRENT



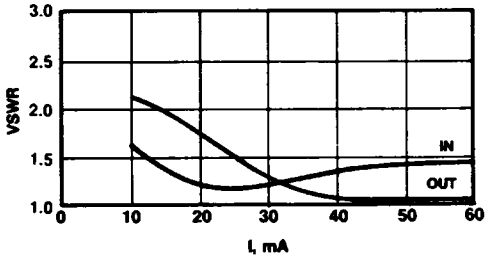
OUTPUT POWER AT 1dB GAIN COMPRESSION AND NOISE FIGURE vs. CASE TEMPERATURE I = 25 mA, FREQ. = 500 MHz



OUTPUT POWER AT 1dB GAIN COMPRESSION vs. CURRENT AND FREQUENCY



VSWR vs. CURRENT FREQUENCY = 1.0 GHz



TYPICAL SCATTERING PARAMETERS*

V_{CE} = 5 V, I_C = 25 mA

Freq.	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	Mag	Ang	dB	Ang	dB	Ang	Mag	Ang
100.00	.040	151.5	11.111	173.4	17.968	2.0	.184	-6.2
500.00	.077	96.9	10.611	149.0	17.686	7.4	.174	-29.0
1000.00	.117	66.4	10.028	120.2	16.736	11.7	.159	-57.6
1200.00	.127	59.3	9.496	109.1	16.340	13.5	.150	-68.4
1400.00	.132	52.4	9.091	100.6	15.763	13.9	.144	-81.3
1600.00	.136	48.4	8.616	90.7	15.337	14.9	.137	-93.2
1800.00	.134	44.7	8.347	81.1	14.822	13.7	.133	-105.8
2000.00	.129	45.1	7.886	72.0	14.399	13.4	.132	-118.4
2200.00	.121	42.5	7.601	63.4	13.848	11.6	.134	-131.5
2400.00	.120	46.5	7.171	56.0	13.565	11.0	.135	-141.5
2600.00	.115	48.4	6.859	47.5	13.025	8.6	.139	-152.6
2800.00	.116	56.4	6.363	40.7	12.880	6.8	.146	-162.8
3000.00	.117	62.6	6.089	33.0	12.340	5.1	.154	171.4

Printed in U.S.A.

MSA-0304
Cascadable Monolithic Silicon Integrated Circuit Amplifier
February, 1985
Summary

FEATURES

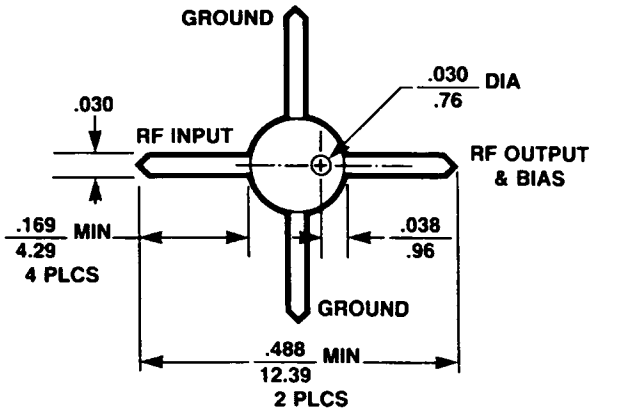
- **Plastic Package**
- **Fully Cascadable (VSWR <2:1)**
- **12.0 dB Gain at 500 MHz**
- **+5V Bias (External Bias Resistor Required)**
- **+10.0 dBm P_{1dB} @ 500 MHz**
- **Short Group Delay**

DESCRIPTION

The MSA (Monolithic Silicon Amplifier) series is a family of silicon bipolar Monolithic Microwave Integrated circuits (MMICs) using nitride self-alignment, ion implantation for precise control of doping and nitride passivation for high reliability.

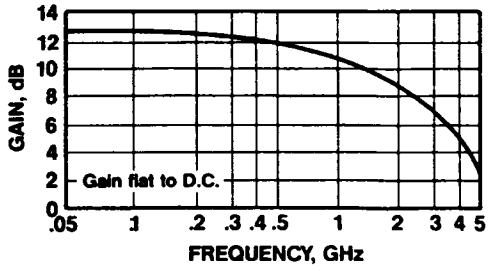
These MMICs use series and shunt feedback and exhibit very high uniformity from amplifier to amplifier. External blocking capacitors are required. Typical applications include narrow or broadband IF and RF amplifiers in industrial and commercial systems.

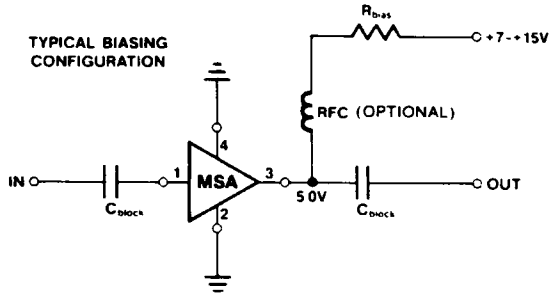
AVANTEK 04 PLASTIC PACKAGE



NOTES (UNLESS OTHERWISE SPECIFIED)
1. DIMENSIONS ARE IN IN / MM
2. TOLERANCES XXX / XX ± 010 / 25

TYPICAL GAIN vs. FREQUENCY
T_A = 25°C, I = 35 mA





ELECTRICAL SPECIFICATIONS, T_A = 25° C

Symbol	Parameters/Test Conditions	Typical Volts	Current (mA)	Freq. (GHz)	Units	Min.	Typ.	Max.
$\|S_{21}\|^2$	Insertion Power Gain	5.0	35.0	0.5	dB	10.0	12.0	—
$\|S_{21}\|^2$	Insertion Power Gain	5.0	35.0	1.0	dB	—	11.0	—
VSWR	Freq. at VSWR = 2:1	5.0	35.0	—	GHz	—	3.0	—
P_{1dB}	Output Power at 1 dB Gain Compression	5.0	35.0	0.5	dBm	—	10.0	—
NF_{50}	50Ω Noise Figure	5.0	35.0	0.5	dB	—	6.0	—
IP_3	Third Order Intercept Point	5.0	35.0	0.5	dBm	—	23.0	—
HP_2	Second Harmonic Intercept Point	5.0	35.0	0.5	dBm	—	39.0	—
f_{1dB}	Frequency at -1dB Gain Point[1]	5.0	35.0	—	GHz	—	0.9	—

Note 1. Frequency at which gain is 1 dB less than at 100 MHz

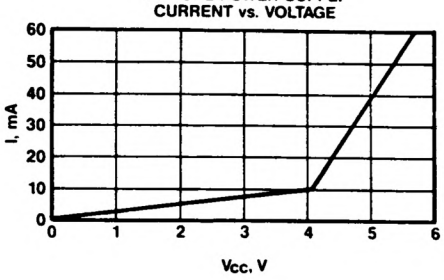
RECOMMENDED MAXIMUM RATINGS

Parameter	Cont.[1] Oper.	Abs.[2] Max.
Power Supply Voltage	5.0V	6.0V
Power Supply Current	40 mA	80 mA
Continuous RF Input Power	+16 dBm	+20 dBm
Storage Temperature	—	150° C
M.T.T.F. (Projected)	$1x10^6$ Hrs.	$1x10^4$ Hrs.
Thermal Resistance, Θjc =	—	150° C/W

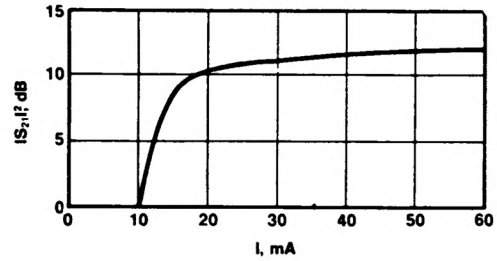
Notes:
1. Operation of this device above any one of these parameters may shorten the MTTF from the design goals.
2. Operation of this device above any one of these parameters may cause permanent damage.

TYPICAL PERFORMANCE, $T_A = 25°C$

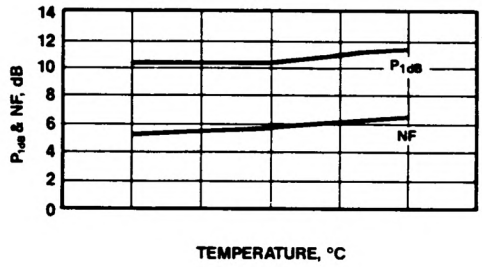
TYPICAL POWER SUPPLY CURRENT vs. VOLTAGE



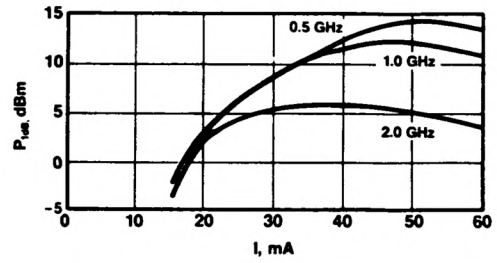
INSERTION POWER GAIN AT 0.5 GHz (S_{21}^2) vs. CURRENT



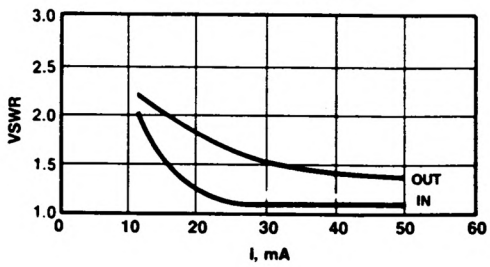
OUTPUT POWER AT 1dB GAIN COMPRESSION AND NOISE FIGURE vs. CASE TEMPERATURE I = 35 mA, FREQ. = 500 MHz



OUTPUT POWER AT 1dB GAIN COMPRESSION vs. CURRENT AND FREQUENCY



VSWR vs. CURRENT FREQUENCY = 1.0 GHz



TYPICAL SCATTERING PARAMETERS*

V_{CE} = 5 V, I_C = 35 mA

Freq.	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	Mag	Ang	dB	Ang	dB	Ang	Mag	Ang
100.00	.086	166.1	12.754	174.0	18.572	3.1	.141	-15.0
500.00	.081	135.0	12.329	148.9	18.156	8.9	.139	-55.7
1000.00	.077	106.4	11.724	119.6	17.075	14.1	.165	-100.3
1200.00	.075	101.9	11.193	108.1	16.615	15.9	.176	-116.4
1400.00	.070	99.9	10.737	99.3	15.966	16.5	.190	-129.5
1600.00	.069	102.1	10.262	89.1	15.482	17.3	.204	-142.5
1800.00	.068	108.7	9.921	79.4	14.914	16.1	.219	-152.8
2000.00	.075	119.0	9.471	69.8	14.455	15.3	.233	-164.0
2200.00	.088	123.8	9.137	60.8	13.848	13.1	.248	-173.4
2400.00	.108	127.4	8.617	53.3	13.606	12.2	.261	178.0
2600.00	.130	128.2	8.281	44.5	13.021	9.6	.273	169.4
2800.00	.159	126.9	7.685	37.6	12.923	7.3	.285	162.7
3000.00	.191	126.0	7.364	29.6	12.402	4.9	.302	155.8

Printed in U.S.A.

LM117
LM217
LM317

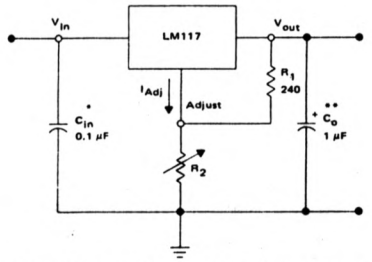
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in TO-3 and TO-220 Packages
- Output Current in Excess of 0.5 Ampere in TO-39 Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

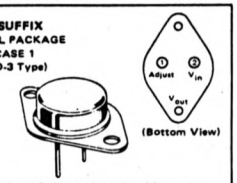
$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

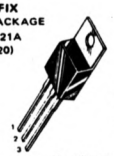
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 Type)



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO-220)



Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79
(TO-39)

Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

ORDERING INFORMATION

Device	Temperature Range	Package
LM117H	T_J = -55°C to +150°C	Metal Can
LM117K	T_J = -55°C to +150°C	Metal Power
LM217H	T_J = -25°C to +150°C	Metal Can
LM217K	T_J = -25°C to +150°C	Metal Power
LM317H	T_J = 0°C to +125°C	Metal Can
LM317K	T_J = 0°C to +125°C	Metal Power
LM317T	T_J = 0°C to +125°C	Plastic Power

4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range LM117 LM217 LM317	T_J	 -55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_I - V_O$ = 5 V; I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; $T_J = T_{low}$ to T_{high} (see Note 1); I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117/217 Min	LM117/217 Typ	LM117/217 Max	LM317 Min	LM317 Typ	LM317 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.02	–	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5 V V_O ≥ 5 V	2	Reg_{load}	 – –	 5 0.1	 15 0.3	 – –	 5 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	 –	 0.2	 5	 –	 0.2	 5	μA
Reference Voltage (Note 4) 3 V ≤ $V_I - V_O$ ≤ 40 V 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	 1.20	 1.25	 1.30	 1.20	 1.25	 1.30	V
Line Regulation (Note 3) 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.05	–	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5 V V_O ≥ 5 V	2	Reg_{load}	 – –	 20 0.3	 50 1	 – –	 20 0.3	 70 1.5	 mV %V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	–	0.7	–	%V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	3	I_{Lmin}	–	3.5	5	–	3.5	10	mA
Maximum Output Current $V_I - V_O$ ≤ 15 V, P_D ≤ P_{max} K and T Packages H Package $V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C K and T Packages H Package	3	I_{max}	 1.5 0.5 0.25 –	 2.2 0.8 0.4 0.07	 – – – –	 1.5 0.5 0.15 –	 2.2 0.8 0.4 0.07	 – – – –	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 KHz	–	N	–	0.003	–	–	0.003	–	%V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5) Without C_{ADJ} C_{ADJ} = 10 μF	4	RR	 66	 65 80	 – –	 66	 65 80	 – –	dB
Long Term Stability, $T_J = T_{high}$ (Note 6) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1	–	0.3	1	%/1.0k Hrs
Thermal Resistance Junction to Case H Package (TO-39) K Package (TO-3) T Package (TO-220)	–	$R_{\theta JC}$	 – –	 12 2.3 –	 15 3 –	 – –	 12 2.3 5	 15 3 –	°C/W

NOTES: (1) T_{low} = -55°C for LM117 T_{high} = +150°C for LM117
= -25°C for LM217 = +150°C for LM217
= 0°C for LM317 = +125°C for LM317

(2) I_{max} = 1.5 A for K (TO-3) and T (TO-220) Packages
= 0.5 A for H (TO-39) Package
P_{max} = 20 W for K (TO-3) and T (TO-220) Packages
= 2 W for H (TO-39) Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

FIGURE 5 – LOAD REGULATION

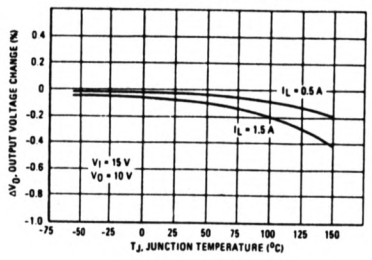


FIGURE 6 – CURRENT LIMIT

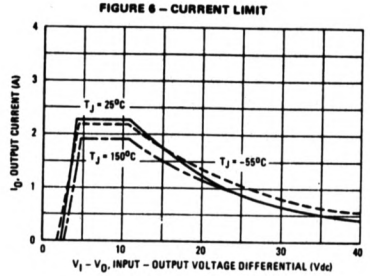


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FIGURE 7 – ADJUSTMENT PIN CURRENT

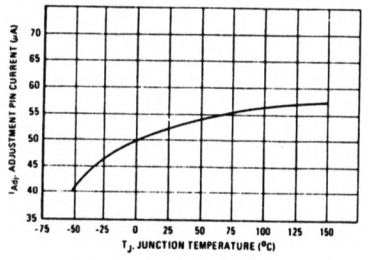

FIGURE 8 – DROPOUT VOLTAGE

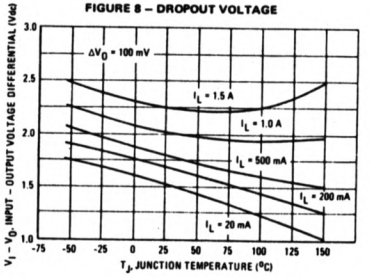

FIGURE 9 – TEMPERATURE STABILITY

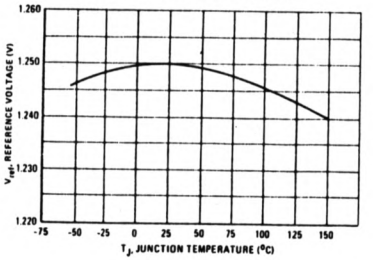

FIGURE 10 – MINIMUM OPERATING CURRENT

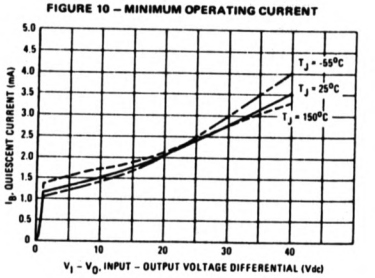

FIGURE 11 – RIPPLE REJECTION VS OUTPUT VOLTAGE

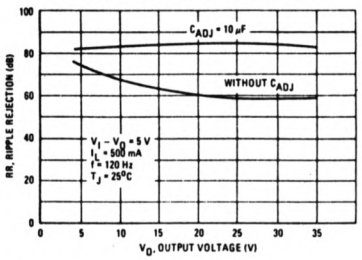

FIGURE 12 – RIPPLE REJECTION VS. OUTPUT CURRENT

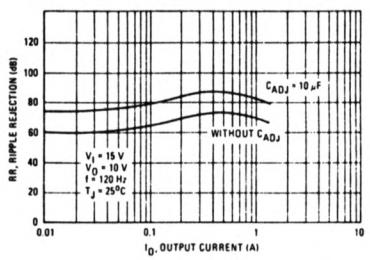

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FIGURE 13 – RIPPLE REJECTION VS. FREQUENCY

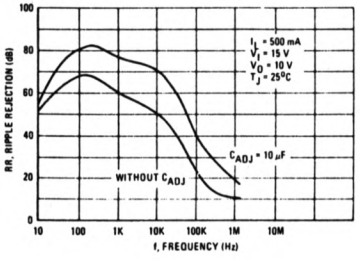


FIGURE 14 – OUTPUT IMPEDANCE

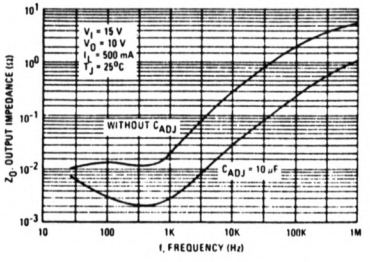


FIGURE 15 – LINE TRANSIENT RESPONSE

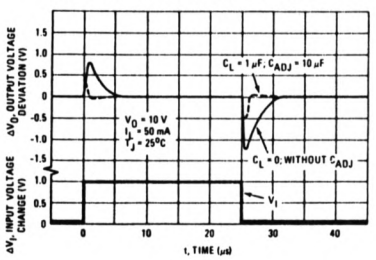
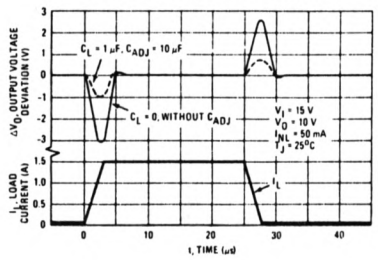


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

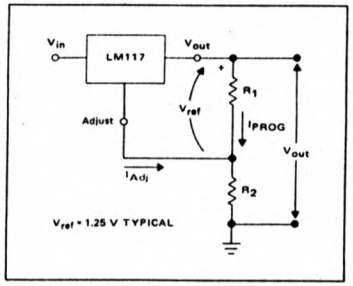
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{ADJ} > 10$ μF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

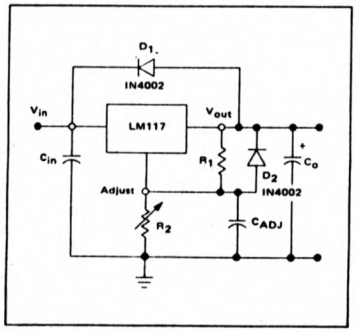


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

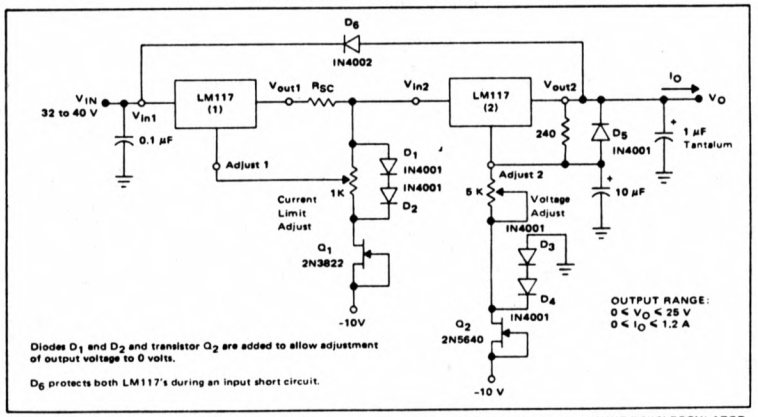


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

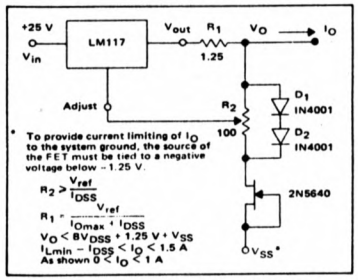


FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

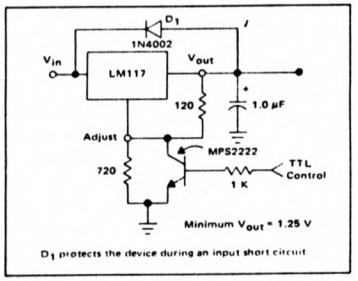


FIGURE 22 – SLOW TURN-ON REGULATOR

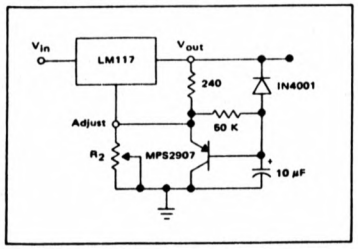
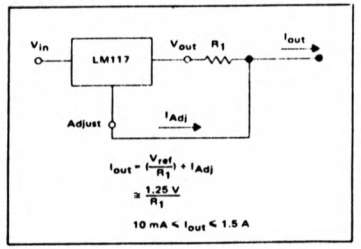


FIGURE 23 – CURRENT REGULATOR



LM117L
LM217L
LM317L

Advance Information

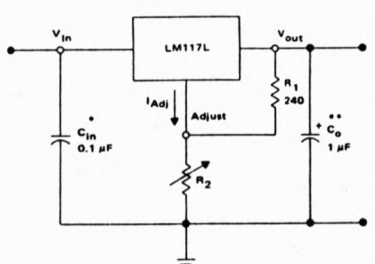
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

This is advance information and specifications are subject to change without notice.

LOW-CURRENT 3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

Z SUFFIX
CASE 29
TO-92
PLASTIC PACKAGE
(LM317L only)

Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

H SUFFIX
METAL PACKAGE
CASE 79
(TO-39)

(Bottom View)

(Case is output)

Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

ORDERING INFORMATION

Device	Temperature Range	Package
LM117LH	T_J = -55°C to +150°C	Metal Can
LM217LH	T_J = -25°C to +150°C	Metal Can
LM317LH	T_J = 0°C to +125°C	Metal Can
LM317LZ	T_J = 0°C to +125°C	Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range LM117L LM217L LM317L	T_J	 -55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_I - V_O$ = 5 V; I_O = 40 mA; $T_J = T_{low}$ to T_{high} (see Note 1); I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117L/217L Min	LM117L/217L Typ	LM117L/217L Max	LM317L Min	LM317L Typ	LM317L Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.02	–	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 5 mA ≤ I_O ≤ I_{max} V_O ≤ 5 V V_O ≥ 5 V	2	Reg_{load}	 – –	 5 0.1	 15 0.3	 – –	 5 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V 5 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	 –	 0.2	 5	 –	 0.2	 5	μA
Reference Voltage (Note 4) 3 V ≤ $V_I - V_O$ ≤ 40 V 5 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	 1.20	 1.25	 1.30	 1.20	 1.25	 1.30	V
Line Regulation (Note 3) 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.05	–	0.02	0.07	%/V
Load Regulation (Note 3) 5 mA ≤ I_O ≤ I_{max} V_O ≤ 5 V V_O ≥ 5 V	2	Reg_{load}	 – –	 20 0.3	 50 1	 – –	 20 0.3	 70 1.5	 mV %V_O
Temperature Stability ($T_{low} \le T_J \le T_{high}$)	3	T_S	–	0.7	–	–	0.7	–	%V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	3	I_{Lmin}	–	3.5	5	–	3.5	5	mA
Maximum Output Current $V_I - V_O$ ≤ 20 V, P_D ≤ P_{max} H Package $V_I - V_O$ ≤ 6.25 V, P_D ≤ P_{max} Z Package $V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C H Package Z Package	3	I_{max}	 100 100 – –	 200 200 50 20	 – – – –	 100 100 – –	 200 200 50 20	 – – – –	 mA nA
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 KHz	–	N	–	0.003	–	–	0.003	–	%V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5) Without C_{ADJ} C_{ADJ} = 10 μF	4	RR	 – –	 65 80	 – –	 – –	 65 80	 – –	dB
Long Term Stability, $T_J = T_{high}$ (Note 6) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1	–	0.3	1	%/1.0k Hrs
Thermal Resistance Junction to Case H Package (TO-39) Z Package (TO-92)	–	$R_{\theta JC}$	 – –	 40 –	 – –	 – –	 40 160	 – –	°C/W

NOTES: (1) T_{low} = -55°C for LM117L T_{high} = +150°C for LM117L
= -25°C for LM217L = +150°C for LM217L
= 0°C for LM317L = +125°C for LM317L

(2) I_{max} = 100 mA
P_{max} = 2 W for H (TO-39) Package
= 625 mW for Z (TO-92) Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

FIGURE 5 – LOAD REGULATION

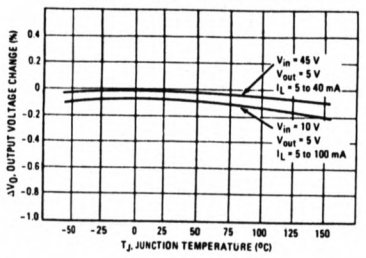


FIGURE 6 – RIPPLE REJECTION

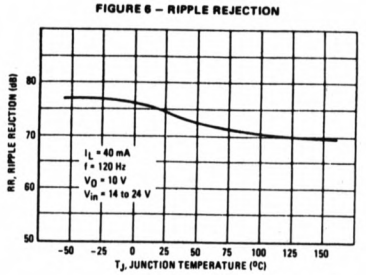


FIGURE 7 – CURRENT LIMIT

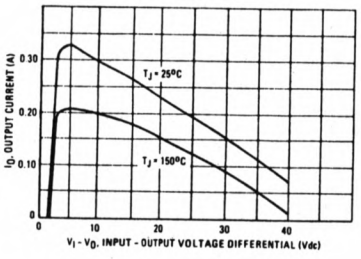


FIGURE 8 – DROPOUT VOLTAGE

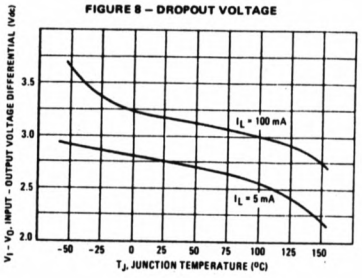


FIGURE 9 – TEMPERATURE STABILITY

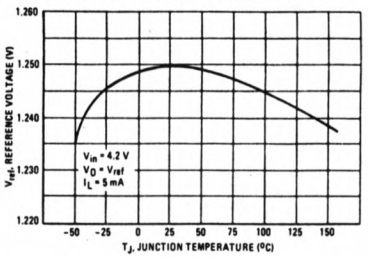


FIGURE 10 – ADJUSTMENT PIN CURRENT

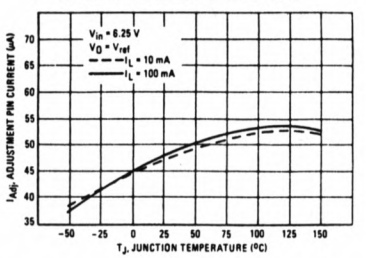


FIGURE 11 – LINE REGULATION

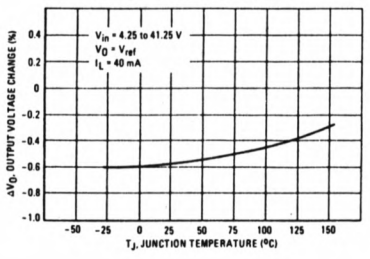
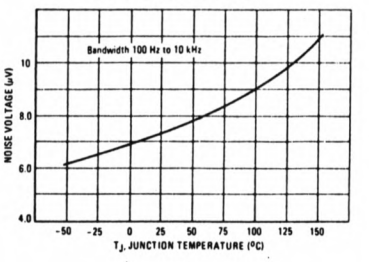


FIGURE 12 – OUTPUT NOISE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

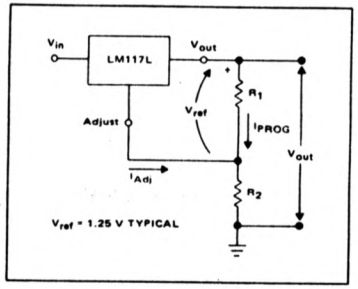
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 13 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 10 μF, C_{ADJ} > 5 μF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 14 – VOLTAGE REGULATOR WITH PROTECTION DIODES

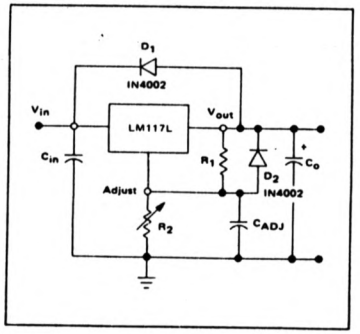


FIGURE 15 – ADJUSTABLE CURRENT LIMITER

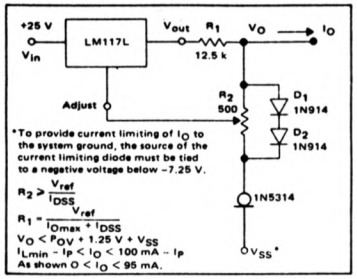


FIGURE 16 – 5 V ELECTRONIC SHUTDOWN REGULATOR

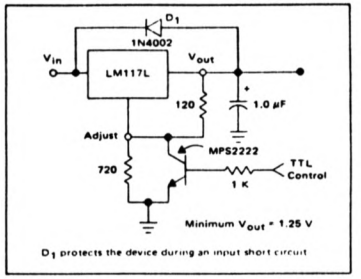


FIGURE 17 – SLOW TURN-ON REGULATOR

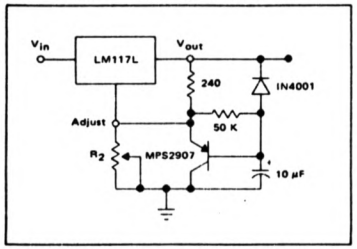
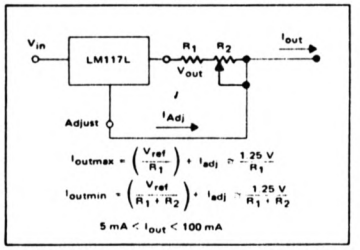


FIGURE 18 – CURRENT REGULATOR



National Semiconductor

Voltage Regulators

LM137/LM237/LM337 3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM237/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM237/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM237/LM337 are ideal complements to the LM117/LM217/LM317 adjustable positive regulators.

Features

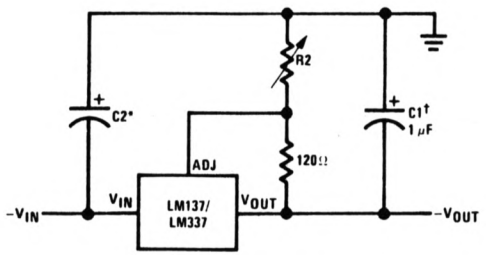
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

LM137 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM137	TO-3	20W	1.5A
LM237 LM337	TO-39	2W	0.5A
LM337T	TO-220	15W	1.5A
LM337M	TO-202	7.5W	0.5A
LM337LZ	TO-92	0.62W	0.1A

Typical Applications

Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Absolute Maximum Ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	−55°C to +150°C
LM237	−25°C to +150°C
LM337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit — **100% All Devices**

Electrical Characteristics (Note 1)

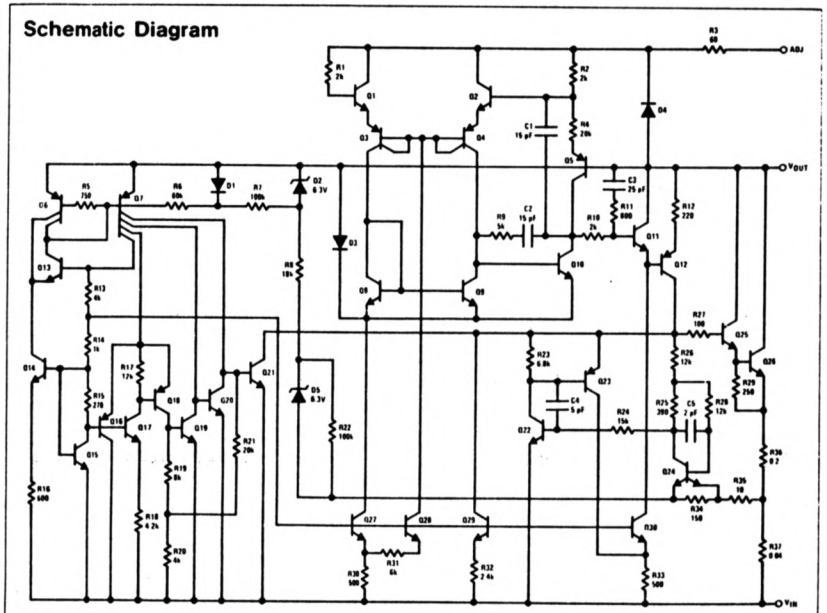
PARAMETER	CONDITIONS	LM137/LM237 MIN	LM137/LM237 TYP	LM137/LM237 MAX	LM337 MIN	LM337 TYP	LM337 MAX	UNITS
Line Regulation	$T_A = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \le I_{OUT} \le I_{MAX}$							
	$\lvert V_{OUT} \rvert \le 5V$, (Note 2)		15	25		15	50	mV
	$\lvert V_{OUT} \rvert \ge 5V$, (Note 2)		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_A = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\ mA \le I_L \le I_{MAX}$		2	5		2	5	μA
	$3.0V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $T_A = 25°C$							
Reference Voltage	$T_A = 25°C$ (Note 3)	1.225	1.250	1.275	1.213	1.250	1.287	V
	$3 \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3)	1.200	1.250	1.300	1.200	1.250	1.300	V
	$10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$							
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)							
	$\lvert V_{OUT} \rvert \le 5V$		20	50		20	70	mV
	$\lvert V_{OUT} \rvert \ge 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 40V$		2.5	5		2.5	10	mA
	$\lvert V_{IN} - V_{OUT} \rvert \le 10V$		1.2	3		1.5	6	mA
Current Limit	$\lvert V_{IN} - V_{OUT} \rvert \le 15V$							
	K and T Package	1.5	2.2		1.5	2.2		A
	H and P Package	0.5	0.8		0.5	0.8		A
	$\lvert V_{IN} - V_{OUT} \rvert = 40V$, $T_j = 25°C$							
	K and T Package	0.24	0.4		0.15	0.4		A
	H and P Package	0.15	0.17		0.10	0.17		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, $f = 120\ Hz$		60			60		dB
	$C_{ADJ} = 10\ \mu F$	66	77		66	77		dB
Long-Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
	T Package					4		°C/W
	P Package					12		°C/W

Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $-25°C \le T_j \le +150°C$ for the LM237, $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and TO-202 packages and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and TO-202 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages, and 0.5A for the TO-202 package and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8" below the base of the TO-3 and TO-39 packages.

Note 3: Selected devices with tightened tolerance reference voltage available

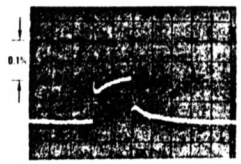
Schematic Diagram



Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of V_{OUT} = −10V) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step as the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



LM137, V_{OUT} = −10V
V_{IN}−V_{OUT} = −40V
I_L = 0A → 0.25A → 0A
Vertical sensitivity, 5 mV/div

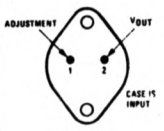
FIGURE 1

LM137, V_{OUT} = −10V
V_{IN}−V_{OUT} = 40V
I_L = 0A → 0.25A → 0A
Horizontal sensitivity, 20 ms/div

FIGURE 2

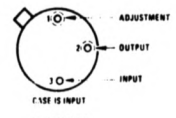
Connection Diagrams

TO-3 Metal Can Package



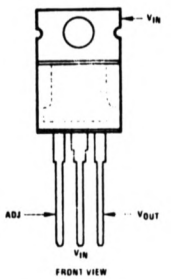
Order Number:
LM137K STEEL
LM237K STEEL
LM337K STEEL
See Package K02A

TO-39 Metal Can Package



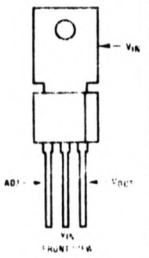
Order Number:
LM137H
LM237H
LM337H
See Package H03B

TO-220 Plastic Package



Order Number:
LM337T
See Package T03B

TO-202 Plastic Package

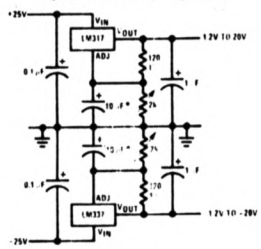


Order Number:
LM337MP
See Package P03A

For Tab Bend TO-202
Order Number
LM337MP
See Package P03E

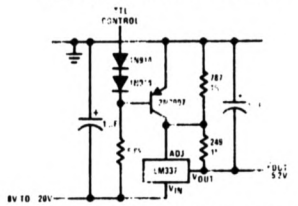
Typical Applications (Continued)

Adjustable Lab Voltage Regulator



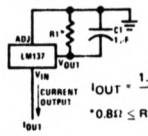
*The 10 µF capacitors are optional to improve ripple rejection

−5.2V Regulator with Electronic Shutdown*



*Minimum output = −1.3V when control input is low

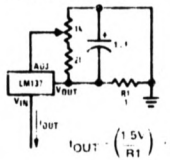
Current Regulator



$$I_{OUT} = \frac{1.250V}{R1}$$

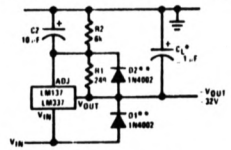
*0.8Ω ≤ R1 ≤ 120Ω

Adjustable Current Regulator



$$I_{OUT} = \left(\frac{1.5V}{R1}\right) + 15\text{% adjustable}$$

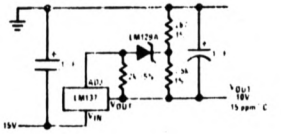
Negative Regulator with Protection Diodes



*When C_L is larger than 20 µF, D1 protects the LM137 in case the input supply is shorted

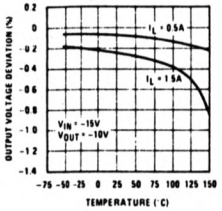
**When C2 is larger than 10 µF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

High Stability −10V Regulator

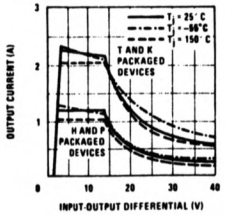


Typical Performance Characteristics (K Steel and T Packages)

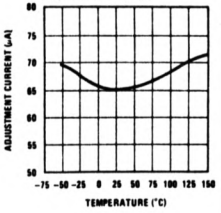
Load Regulation



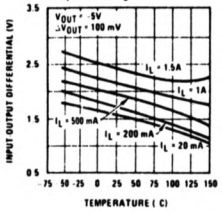
Current Limit



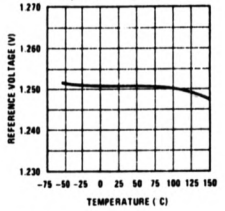
Adjustment Current



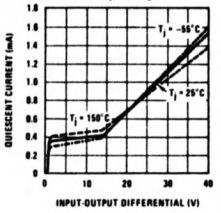
Dropout Voltage



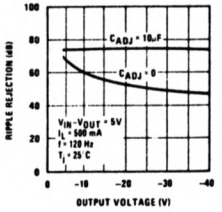
Temperature Stability



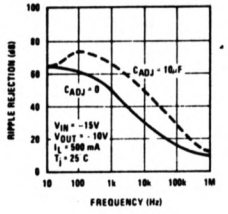
Minimum Operating Current



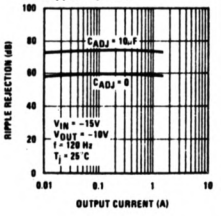
Ripple Rejection



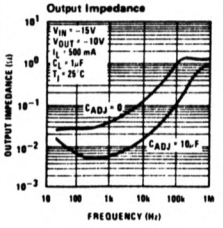
Ripple Rejection



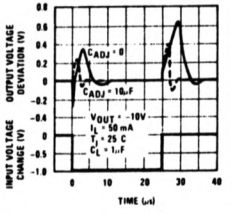
Ripple Rejection



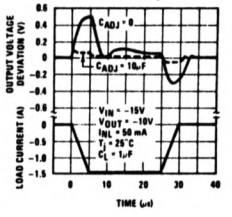
Output Impedance



Line Transient Response



Load Transient Response



National Semiconductor

LM137HV/LM237HV/LM337HV
3-Terminal Adjustable Negative Regulators (High Voltage)

General Description

The LM137HV/LM237HV/LM337HV are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −47V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137HV series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

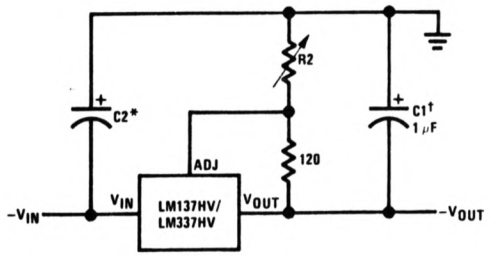
The LM137HV/LM237HV/LM337HV serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137HV/LM237HV/LM337HV are ideal complements to the LM117HV/LM217HV/LM317HV adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −47V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

Typical Applications

Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

National Semiconductor

Voltage Regulators
PRELIMINARY

LM337L 3-Terminal Adjustable Regulator

General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, only a single 1 μF solid tantalum output capacitor is needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

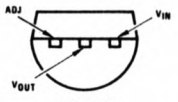
Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM337L is packaged in a standard TO-92 transistor package. The LM337L is rated for operation over a −25°C to +125°C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

Connection Diagram

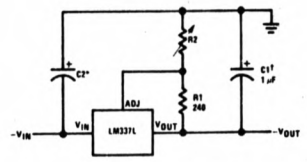


BOTTOM VIEW

Order Number LM337LZ
See NS Package Z03A

Typical Applications

1.2V-25V Adjustable Regulator

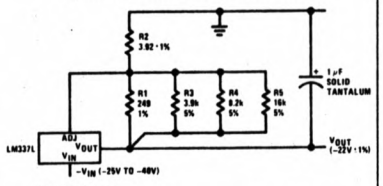


$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{240\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power supply filter capacitor

Regulator with Trimmable Output Voltage



Trim Procedure:

—If V_{OUT} is −23.08V or bigger, cut out R3 (if smaller, don't cut it out).

—Then if V_{OUT} is −22.47V or bigger, cut out R4 (if smaller, don't).

—Then if V_{OUT} is −22.16V or bigger, cut out R5 (if smaller, don't).

This will trim the output to well within 1% of −22.00 V_{DC}, without any of the expense or trouble of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

Absolute Maximum Ratings

Power Dissipation	Internally Limited	Operating Junction Temperature Range	−25°C to +125°C
Input-Output Voltage Differential	40V	Storage Temperature	−55°C to +150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	T_A = 25°C, 3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 40V, (Note 2)		0.01	0.04	%/V
Load Regulation	T_A = 25°C, 5 mA ≤ I_{OUT} ≤ I_{MAX}, (Note 2)		0.1	0.5	%
Thermal Regulation	T_A = 25°C, 10 ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	5 mA ≤ I_L ≤ 100 mA 3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 40V		0.2	5	μA
Reference Voltage	3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 40V, (Note 3) 10 mA ≤ I_{OUT} ≤ 100 mA, P ≤ 625 mW	1.20	1.25	1.30	V
Line Regulation	3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 40V, (Note 2)		0.02	0.07	%/V
Load Regulation	5 mA ≤ I_{OUT} ≤ 100 mA, (Note 2)		0.3	1.5	%
Temperature Stability	T_{MIN} ≤ T_j ≤ T_{MAX}		0.65		%
Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert$ ≤ 40V 3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 15V		3.5 2.2	5 3.5	mA mA
Current Limit	3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 13V $\lvert V_{IN}-V_{OUT}\rvert$ = 40V	100 25	200 50	320 120	mA mA
Rms Output Noise, % of V_{OUT}	T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz		0.003		%
Ripple Rejection Ratio	V_{OUT} = −10V, f = 120 Hz, C_{ADJ} = 0 C_{ADJ} = 10 μF	66	65 80		dB dB
Long-Term Stability	T_A = 125°C		0.3	1	%

Note 1: Unless otherwise specified, these specifications apply −25°C ≤ T_j ≤ +125°C for the LM337L; $V_{IN}-V_{OUT}$ = 5V and I_{OUT} = 40 mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100 mA.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to PC board.

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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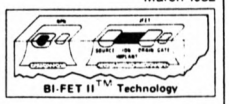
March 1982

National Semiconductor



LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

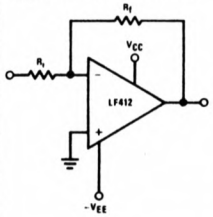
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	1 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA/Amplifier
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	< 0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



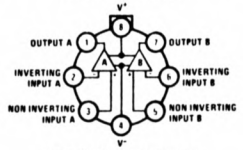
Ordering Information

LF412XYZ

X indicates electrical grade
Y indicates temperature range
"M" for military
"C" for commercial
Z indicates package type
"H" or "N"

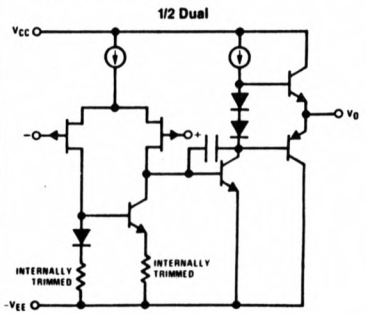
Connection Diagrams

LF412AMH/LF412MH, LF412ACH/LF412CH
Metal Can Package

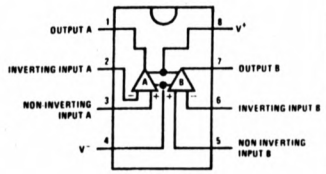


Note: Pin 4 connected to case.
TOP VIEW

Simplified Schematic



LF412ACN, LF412CN
Dual-In-Line Package



TOP VIEW

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IM B20M32 Printed in U.S.A.

LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

Absolute Maximum Ratings

	LF412A	LF412
Supply Voltage	± 22V	± 18V
Differential Input Voltage	± 38V	± 30V
Input Voltage Range (Note 1)	± 19V	± 15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 3)	670 mW	500 mW
T_j max	150°C	115°C
θ_{jA}	150°C/W	160°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A Min	LF412A Typ	LF412A Max	LF412 Min	LF412 Typ	LF412 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 6)			7	10		7	20 (Note 6)	$\mu V/°C$
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		± 12	± 13.5		± 12	± 13.5		V
V_{CM}	Input Common-Mode Voltage Range			± 16	+ 19.5		± 11	+ 14.5		V
					− 16.5			− 11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				3.6	5.6		3.6	6.8	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A Min	LF412A Typ	LF412A Max	LF412 Min	LF412 Typ	LF412 Max	Units
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz–20 kHz (Input Referred)		− 120			− 120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Notes

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

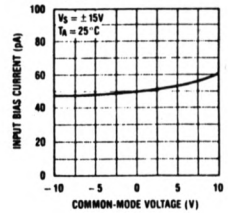
Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 90% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature. T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

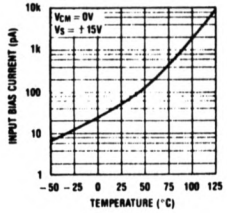
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

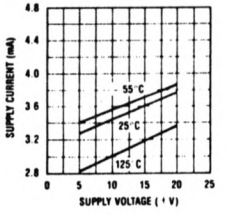
Input Bias Current



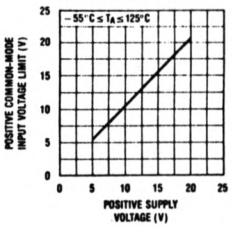
Input Bias Current



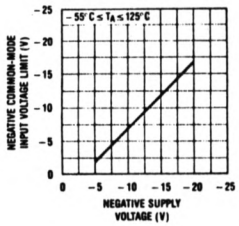
Supply Current



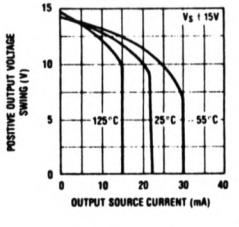
Positive Common-Mode Input Voltage Limit



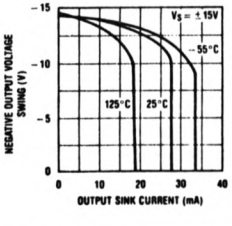
Negative Common-Mode Input Voltage Limit



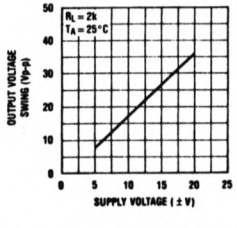
Positive Current Limit



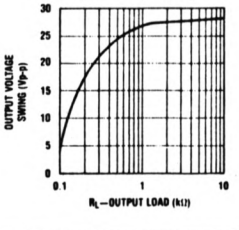
Negative Current Limit



Output Voltage Swing

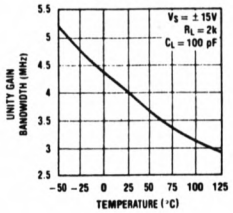


Output Voltage Swing

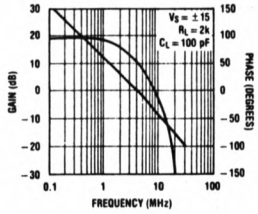


Typical Performance Characteristics (Continued)

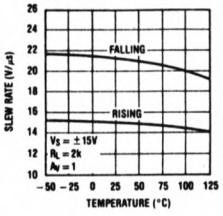
Gain Bandwidth



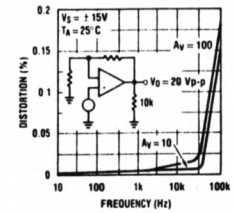
Bode Plot



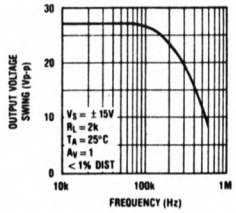
Slew Rate



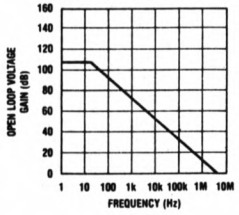
Distortion vs Frequency



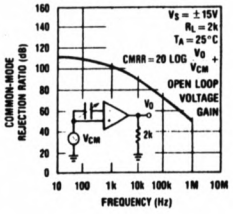
Undistorted Output Voltage Swing



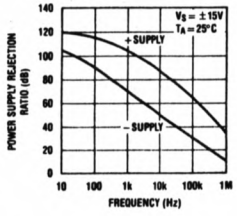
Open Loop Frequency Response



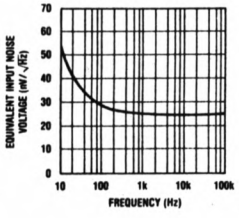
Common-Mode Rejection Ratio



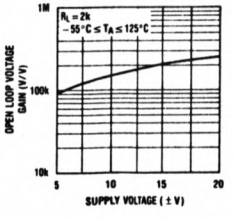
Power Supply Rejection Ratio



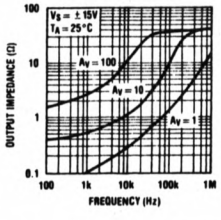
Equivalent Input Noise Voltage



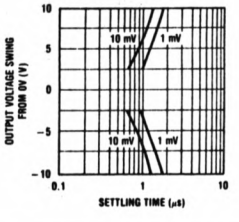
Open Loop Voltage Gain



Output Impedance

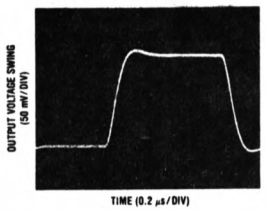


Inverter Settling Time

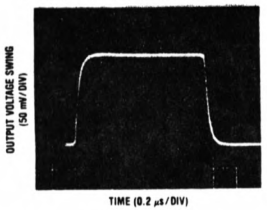


Pulse Response $R_L = 2$ kΩ, $C_L = 10$ pF

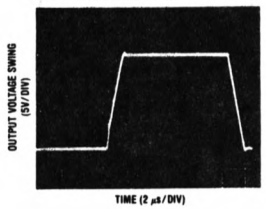
Small Signal Inverting



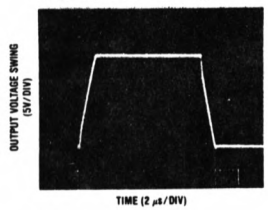
Small Signal Non-Inverting



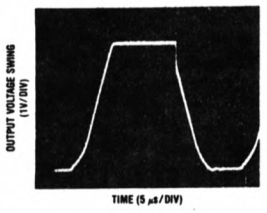
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ± 4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ± 10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Application Hints (Continued)

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

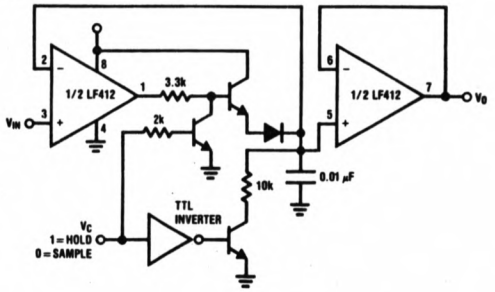
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

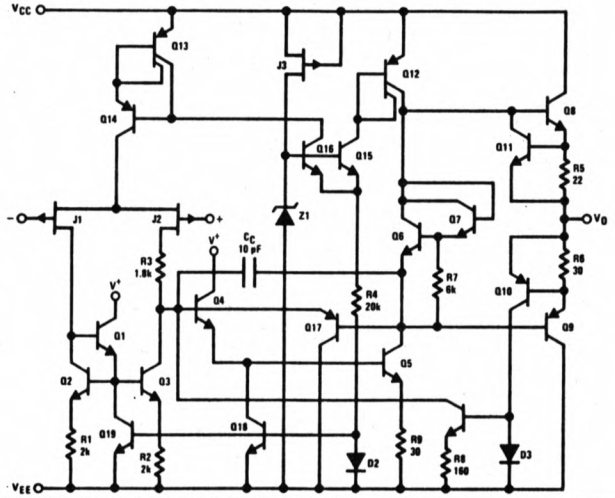
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

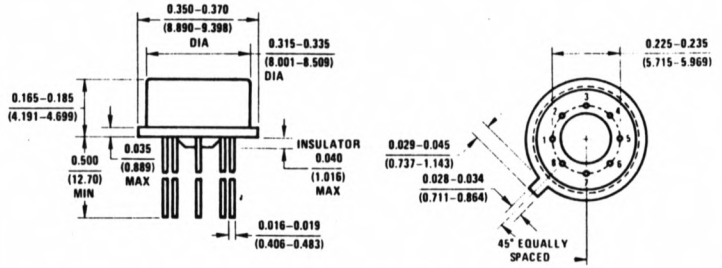
Single Supply Sample and Hold



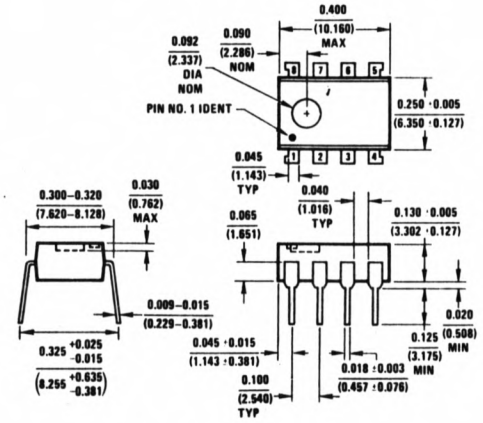
Detailed Schematic



Physical Dimensions inches (millimeters)

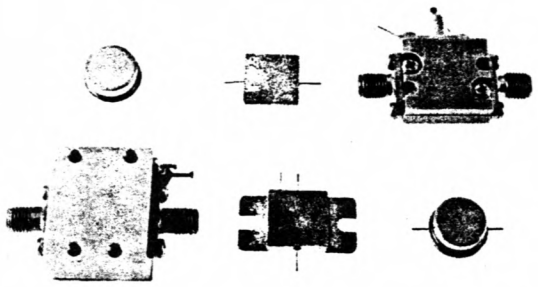


TO-5 Metal Can Package (H)
Order Number LF412AMH, LF412MH, LF412ACH, LF412CH
NS Package Number H08B



Molded Dual-In-Line Package (N)
Order Number LF412ACN, LF412CN
NS Package Number N08A

AH-507



10 to 500 MHz TO-8 Cascadable Amplifier

- High Power Output: +24.0dBm
- Medium Gain: +15.0dB
- Low Noise Figure: 4.5dB
- **Various Package Options (see photo)**
  Surface Mounted (SMTO-8), Flatpack with flange (FPF), Connectorized (CAH), Connectorized Flatpack (CFP), Flatpack (FP), and TO-8 (AH)

Electrical Specifications

Measured in a 50-ohm system at +15 Vdc nominal

Characteristic	Typical 25°C	Guaranteed 0°C to +50°C	Specifications −54°C to +85°C
Frequency (MHz Min.)	10-500	10-500	10-500
Small Signal Gain (dB Min.)	+15.0	+14.0	+14.0
Gain Flatness (dB Max.)	±0.5	±1.0	±1.0
Noise Figure (dB Max.)	+4.5	+7.0	+9.0
Power Output @ 1 dB Compression (dBm Min.)	+24.0	+20.0	+20.0
Two Tone 3rd Order Intercept Point (dBm Min.)	+37.0	+32.0	+30.0
Two Tone 2nd Order Intercept Point (dBm Min.)	+40.0	+38.0	+36.0
One Tone 2nd Harmonic Intercept Point (dBm Min.)	+46.0	+44.0	+40.0
Input/Output VSWR (Max.)	4.5:1	2.0:1	2.0:1
DC Current at 15 V (mA Max.)	+76.0	+80.0	+90.0

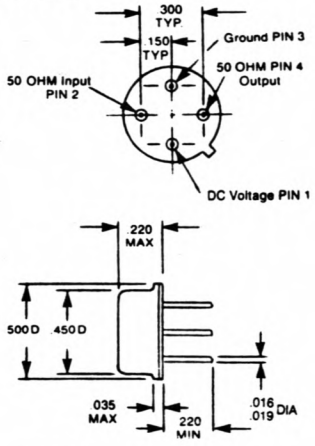
Maximum Ratings

Ambient Operating Temperature ..... −54°C to +100°C
Storage Temperature ... −62°C to +125°C
Maximum Case Temperature ..... +100°C
Maximum DC Voltage ..... +18.0V
Maximum Continuous RF Input Power ..... +17.0dBm
Maximum Short Term RF Input Power ..... +50.0 mW (1 minute Max.)
Maximum Peak Power ..... +0.5W (3µseconds Max.)
"X" Series Burn-In Temperature ..... +100°C
Weight ..... +2.5 grams Max.

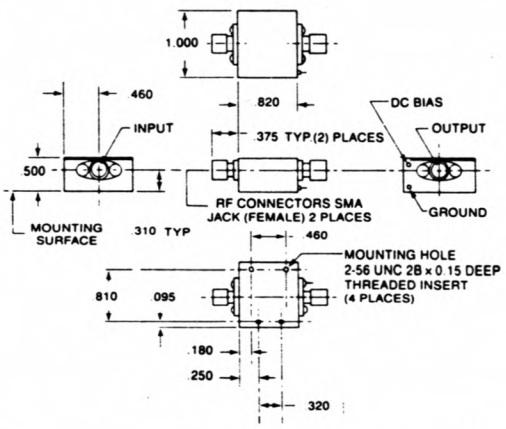
Outline Drawings

(For additional package configurations, see Section 9)

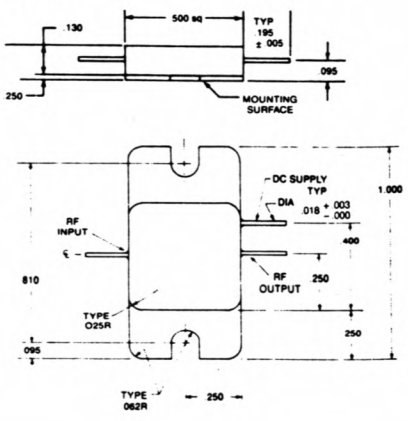
AH-507



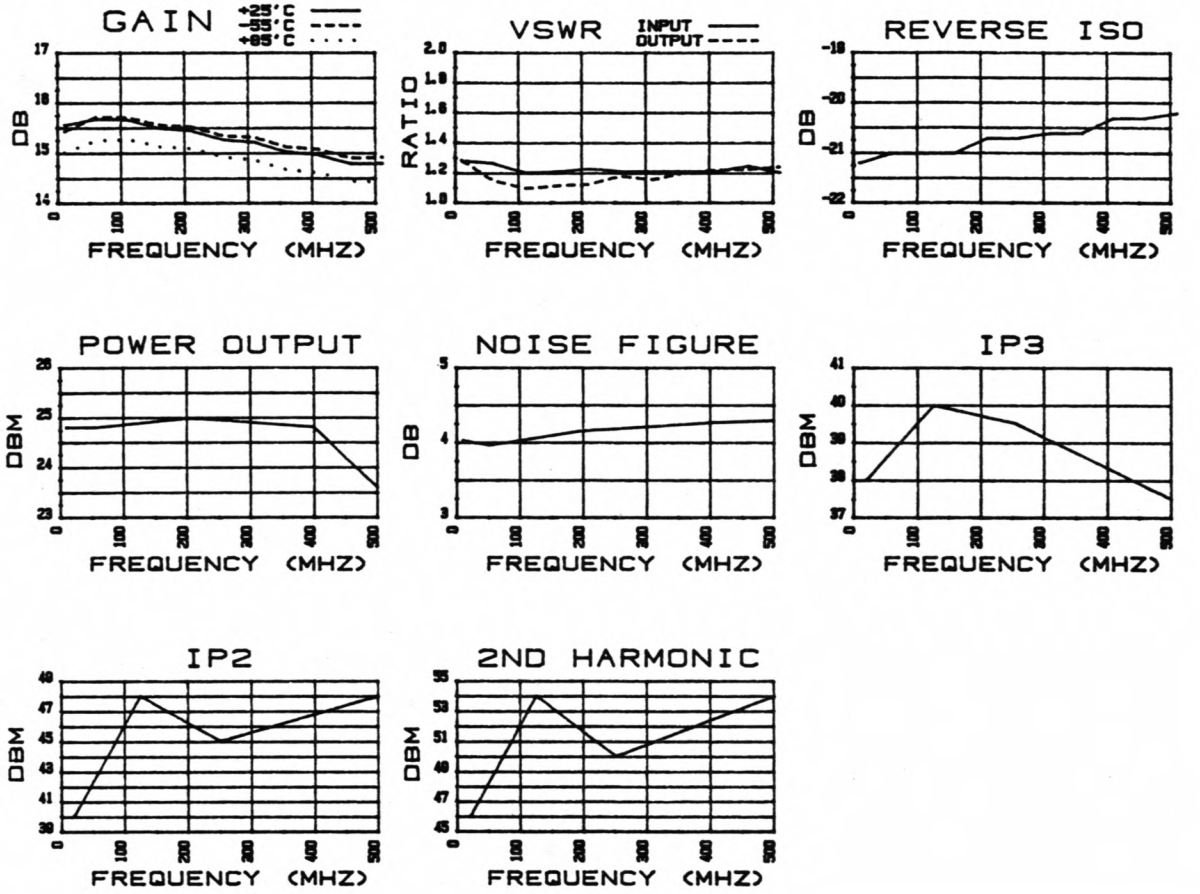
CAH-507



FPF-507



Typical Performance



AH-507 *76 mA* @15.0Vdc

Linear S-Parameters

FREQUENCY	RETURN LOSS INPUT (S11)		TRANS. GAIN FORWARD (S21)		TRANS. GAIN REVERSE (S12)		RETURN LOSS OUTPUT (S22)	
MHz	dB	ANG	dB	ANG	dB	ANG	dB	ANG
10.000	-18.2	-128.7	15.55	-169.8	-21.20	12.0	-18.1	130.5
60.000	-18.7	164.8	15.68	172.5	-21.00	1.0	-23.2	162.0
110.000	-20.8	145.3	15.65	162.5	-21.00	-0.8	-26.5	-147.5
160.000	-20.3	138.0	15.48	154.5	-21.00	-2.0	-25.0	-147.8
210.000	-19.7	123.5	15.43	147.3	-20.70	-2.5	-24.5	-144.8
260.000	-20.5	110.8	15.25	139.3	-20.70	-4.0	-21.6	-139.5
310.000	-20.3	99.3	15.20	131.5	-20.60	-5.7	-22.8	-133.8
360.000	-20.5	86.5	15.01	124.8	-20.60	-6.5	-20.6	-147.8
410.000	-20.4	65.3	14.95	117.5	-20.30	-8.2	-19.9	-137.0
460.000	-19.1	47.3	14.78	109.8	-20.30	-10.0	-19.8	-142.0
510.000	-20.8	28.3	14.80	102.8	-20.20	-13.0	-19.2	-143.6

Deviation from Linear Phase, Gain, Group Delay, and VSWR

FREQUENCY (MHz)	VSWR INPUT	DEV. LIN. 0 (DEG.)	GAIN DEV. (dB)	GROUP DELAY (n-SEC)	VSWR OUTPUT
10.000	1.281	8.261	0.297	0.000	1.284
60.000	1.263	-1.318	0.427	0.986	1.149
110.000	1.201	-3.148	0.397	0.556	1.099
160.000	1.214	-2.977	0.227	0.444	1.119
210.000	1.231	-2.057	0.177	0.403	1.127
260.000	1.208	-1.886	-0.003	0.444	1.181
310.000	1.214	-1.466	-0.053	0.431	1.156
360.000	1.208	-0.045	-0.243	0.375	1.206
410.000	1.211	0.875	-0.303	0.403	1.225
460.000	1.250	1.295	-0.473	0.431	1.228
510.000	1.201	2.466	-0.453	0.389	1.246

HEWLETT hp PACKARD

COMPONENTS

STEP RECOVERY DIODES

5082-0100 SERIES
5082-0200 SERIES
5082-0300 SERIES
5082-0800 SERIES

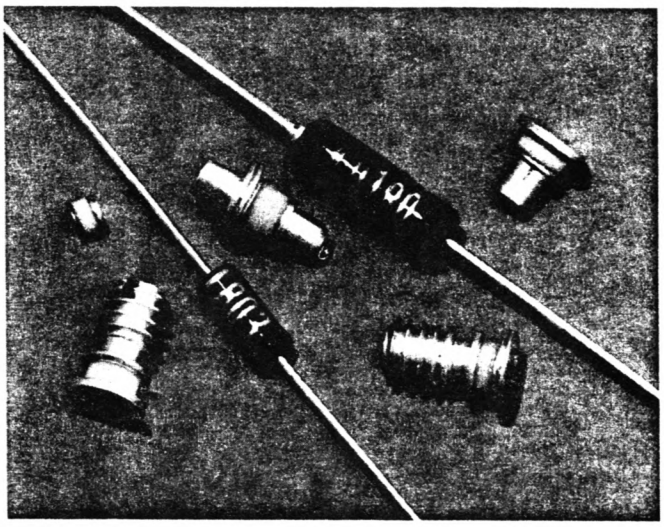
Features

OPTIMIZED FOR BOTH LOW AND HIGH ORDER MULTIPLIER DESIGNS FROM UHF THROUGH Ku BAND

PASSIVATED CHIP FOR MAXIMUM STABILITY AND RELIABILITY

AVAILABLE IN A VARIETY OF PACKAGES

SPECIAL ELECTRICAL SELECTIONS AVAILABLE UPON REQUEST



Description/Applications

These diodes are manufactured using modern epitaxial growth techniques. The diodes are passivated with a thermal oxide for maximum stability. The result is a family of devices offering highly repeatable, efficient and reliable performance. These diodes are designed to meet the general requirements of MIL-S-19500.

The 5082-0800 Series diode is designed to maximize cut-off frequency while maintaining a fast transition time. This characteristic leads to excellent performance in either low or high order multipliers and in comb generators. All ceramic package diodes in the 5082-0800 Series are supplied with measured data.

Maximum Ratings at $T_{CASE} = 25°C$

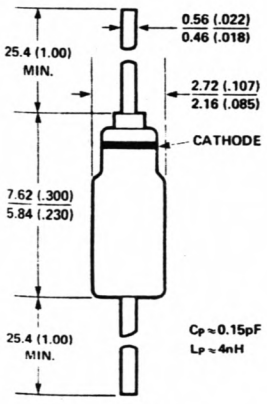
Junction Operating and
Storage Temperature . . . . . -65°C to 200°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

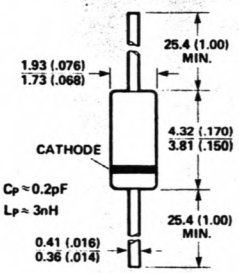
DC Power Dissipation . . . . . $\frac{200°C - T_{case}}{\theta_{jc}}$

Soldering Temperature . . . . . 230°C for 5 sec.

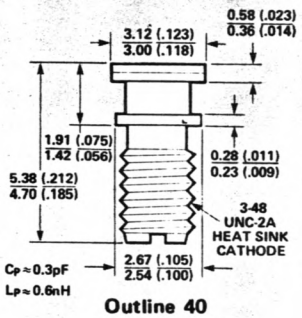
Package Dimensions



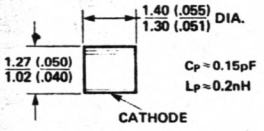
Outline 11



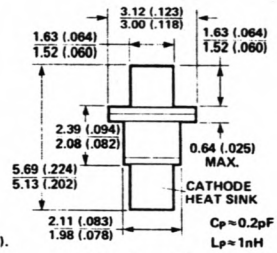
Outline 15



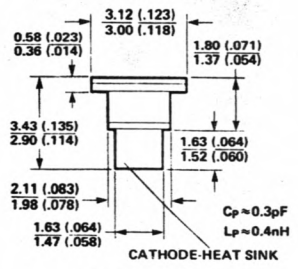
Outline 40



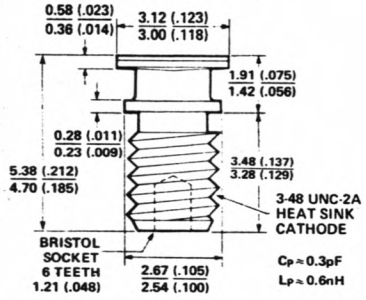
Outline 56



Outline 31



Outline 41



Outline 65

DIMENSIONS IN MILLIMETERS AND (INCHES).

Mechanical Specifications

Hewlett-Packard's step recovery diodes are available in a variety of packages. Special package configuration is available upon request. Contact your local HP Field Office for additional information.

The metal-ceramic packages are hermetically sealed. The anode studs and flanges are gold-plated Kovar. The cathode studs are gold-plated copper. The maximum soldering temperature is 230°C for 5 seconds.

The HP outline 15 and 11 packages have glass hermetic seals with dumet leads. The maximum soldering temperature is 230°C for 5 seconds. The leads on outline 15 should be restricted so that any bend starts at least 1.6 mm (.063 in.) from the glass body.

Diodes for High Efficiency Multipliers (All Specifications at T_A = 25°C)

Ceramic Packaged Diodes

ELECTRICAL SPECIFICATIONS

TYPICAL PARAMETERS

Part Number 5082-	Junction Capacitance at -6V, $C_{j(-6)}$ *[1] [pF]		Minimum Breakdown Voltage, V_{BR} * at I_R = 10μA [V]	Minimum Cutoff Frequency, f_c[2] [GHz]	Package Outline	Output Frequency Range [GHz]	Output Power, P_o[3] [W]	Lifetime, τ [ns]	Transition Time		Thermal Resistance, Θ_{jc} [°C/W]
	Min.	Max.							t_t [ps]	Charge Level [pC]	
0800 0801 0802	3.5	5.0	75	100	40 31 41	1-3	10	250	350	1500	15
0805 0806 0807	2.5	3.5	60	140	31 40 41	3-5	6	100	250	1500	20
0810 0811 0812	1.5	2.5	60	140	31 40 41	5-8	4	100	200	1000	25
0820 0821 0822	0.7	1.5	45	160	31 41 40	7-10	2.5	50	100	300	30
0830 0831	0.35	1.2	25	200	31 41	8-12	1.0	20	75	300	45
0835 0836 0885	0.1	0.5	15	350	31 41 56	10-20	0.3	10	50	100	60

*Data supplied with each diode includes measured V_{BR} and $C_{T(-6)}$

Glass Packaged Diodes (Outline 15)[4]

ELECTRICAL SPECIFICATIONS

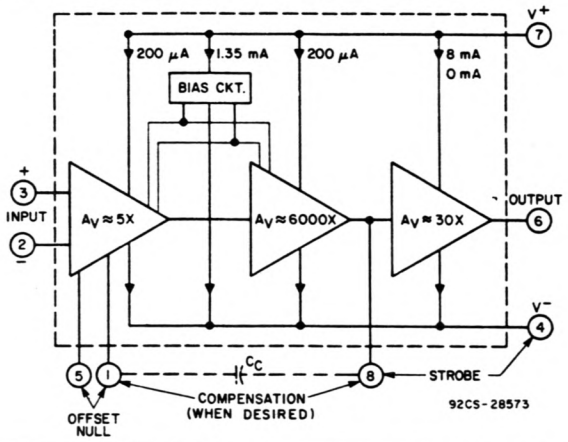
TYPICAL PARAMETERS

Part Number 5082-	Maximum Junction Capacitance at -6V, $C_{j(-6)}$[1] [pF]	Minimum Breakdown Voltage, V_{BR} at I_R = 10μA [V]	Minimum Cutoff Frequency, f_c [2] [GHz]	Lifetime, τ [ns]	Transition Time	
					t_t [ps]	Charge Level [pC]
0803	6.0	70	100	250	350	1500
0815	4.0	50	140	60	250	1500
0825	2.0	45	160	50	95*	300
0833	1.6	25	175	30	75*	300
0840	0.6	15	300	10	50*	100

*The transition times shown for the package 15 devices are limited by the package inductance to a minimum of 100 ps. The lower transition times shown for the -0825, -0833 and -0840 are based on the performance of the chip.

BiMOS Operational Amplifiers

CA3130, CA3130A, CA3130B | MOS/FET Input, CMOS Output
CA3160, CA3160A, CA3160B | Frequency Compensated Version of CA3130
CA3260, CA3260A, CA3260B | Dual Version of CA3160



Type No.	Package	Operating Temp. Range
CA3130S, AS, BS CA3160S, AS, BS CA3260S, AS, BS	8-Lead DIL-CAN	−55 to +125° C
CA3130T, AT, BT CA3160T, AT, BT CA3260T, AT, BT	8-Lead TO-5	
CA3130E, AE CA3160E, AE CA3260E, AE	8-Lead Mini-DIP	
CA3130H CA3160H CA3260H	Chip	

Gate-protected p-channel MOS/FET (PMOS) transistors in the input circuit provide very-high-input impedance, very-low-input current, exceptional speed performance, and common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails
- Wide BW: 15 MHz typ. (unity-gain bandwidth) - CA3130
  4 MHz typ. (unity-gain bandwidth) - CA3160, CA3260
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor - CA3130
- Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired) - CA3160
- Low V_{IO}: 2 mV max. (CA3160, CA3260)

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
- High-input-impedance wideband amplifiers
- Voltage followers
- Voltage regulators
- Peak detectors - CA3130
- Single-supply full-wave precision rectifiers - CA3130
- Photo-diode sensor amplifiers
- Wien-Bridge oscillators
- Voltage-controlled oscillators
- Ideal interface with digital COS/MOS

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

Electrical Characteristics: T_A = 25°C, V^+ = 7.5V, V^- = − 7.5V

Type	R_I (Typ) TΩ	I_I (Max) pA	I_{IO} (Max) pA	V_{IO} (Max) mV	SR (Typ) V/μs	f_T (Typ) MHz	Output Swing (Typ)-V	Compensation	A_{OL} (min.) V/V	A_{OL} (min.) dB	Supply Voltage Range V
CA3130	1.5	50	30	15	10	4	−0.002 to + 13	External	50K	94	4.5 to 16
CA3130A	1.5	30	20	5	10	4	−0.002 to + 13	External	50K	94	4.5 to 16
CA3130B	1.5	20	10	2	10	4	−0.002 to + 13	External	100K	100	4.5 to 16
CA3160	1.5	50	30	15	10	4	−0.002 to + 13	Internal	50K	94	4.5 to 16
CA3160A	1.5	30	20	5	10	4	−0.002 to + 13	Internal	50K	94	4.5 to 16
CA3160B	1.5	20	10	2	10	4	−0.002 to + 13	Internal	100K	100	4.5 to 16
CA3260*	1.5	50	30	15	10	4	−0.002 to + 13	Internal	50K	94	4 to 16
CA3260A*	1.5	30	20	5	10	4	−0.002 to + 13	Internal	50K	94	4 to 16
CA3260B*	1.5	20	10	2	10	4	−0.002 to + 13	Internal	100K	100	4 to 16

*Characteristics are for each amplifier.

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC34071, MC34072
MC35071, MC35072
MC33071, MC33072

Advance Information

HIGH PERFORMANCE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

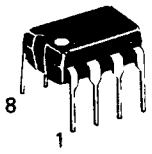
SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY OPERATIONAL AMPLIFIERS

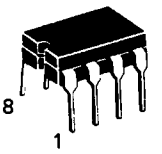
A standard low-cost Bipolar technology with innovative design concepts are employed for the MC34071/MC34072 series of monolithic operational amplifiers. These devices offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate, and fast settling time without the use of JFET device technology. In addition, low input offset voltage can economically be achieved. Although these devices can be operated from split supplies, they are particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, also provides high capacitive drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC34071/MC34072 series of devices are available in standard or prime performance (A Suffix) grades and specified over commercial, industrial/vehicular or military temperature ranges.

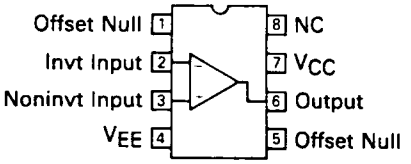
- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.10%
- Wide Single Supply Operating Range: 3.0 to 44 Volts
- Wide Input Common Mode Range Including Ground (V_{EE})
- Low Input Offset Voltage: 1.5 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14.0 V for V_S = ±15 V
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low T.H.D. Distortion: 0.02%
- Excellent Phase Margins: 60°
- Excellent Gain Margin: 12 dB



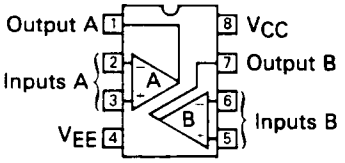
P SUFFIX
PLASTIC PACKAGE
CASE 626-04



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



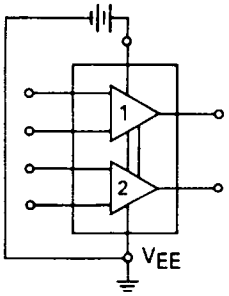
Single, Top View



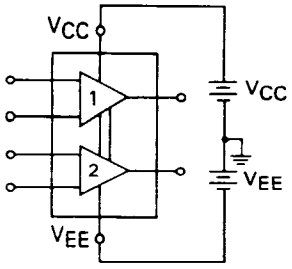
Dual, Top View

SINGLE SUPPLY

3.0 V to 44 V



SPLIT SUPPLY



ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC35071U,AU	−55 to +125°C	Ceramic DIP
	MC33071U,AU	−40 to +85°C	Ceramic DIP
	MC33071P,AP	−40 to +85°C	Plastic DIP
	MC34071U,AU	0 to +70°C	Ceramic DIP
	MC34071P,AP	0 to +70°C	Plastic DIP
Dual	MC35072U,AU	−55 to +125°C	Ceramic DIP
	MC33072U,AU	−40 to +85°C	Ceramic DIP
	MC33072P,AP	−40 to +85°C	Plastic DIP
	MC34072U,AU	0 to +70°C	Ceramic DIP
	MC34072P,AP	0 to +70°C	Plastic DIP
Quad	MC34074 Series	Refer to MC34074 Data Sheet	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	MC3507_A/MC3407_A/ MC3307_A			MC3507_/MC3407_/ MC3307_			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{CM} = 0)	V_{IO}							mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	0.5	1.5	—	1.0	3.5	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	0.5	2.0	—	1.5	4.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	3.5	—	—	5.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0)	I_{IB}							nA
T_A = +25°C		—	100	500	—	100	500	
T_A = T_{low} to T_{high}		—	—	700	—	—	700	
Input Offset Current (V_{CM} = 0)	I_{IO}							nA
T_A = +25°C		—	6.0	50	—	6.0	75	
T_A = T_{low} to T_{high}		—	—	300	—	—	300	
Large Signal Voltage Gain	A_{VOL}							V/mV
V_O = ±10 V, R_L = 2.0 k		50	100	—	25	100	—	
Output Voltage Swing	V_{OH}							V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 k, T_A = +25°C		3.7	4.0	—	3.7	4.0	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		13.7	14	—	13.7	14	—	
V_{CC} = +15 V, V_{EE} − 15 V, R_L = 2.0 k, T_A = T_{low} to T_{high}		13.5	—	—	13.5	—	—	
	V_{OL}							
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 k, T_A = +25°C		—	0.1	0.2	—	0.1	0.2	
V_{CC} = +15 V, V_{EE} + −15 V, R_L = 10 k, T_A = +25°C		—	−14.7	−14.4	—	−14.7	−14.4	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 k, T_A = T_{low} to T_{high}		—	—	−13.8	—	—	−13.8	
Output Short-Circuit Current (T_A = +25°C)	I_{SC}							mA
Input Overdrive = 1.0 V, Output to Ground								
Source		10	30	—	10	30	—	
Sink		20	47	—	20	47	—	
Input Common Mode Voltage Range	V_{ICR}							V
T_A = +25°C		V_{EE} to (V_{CC} − 1.8)			V_{EE} to (V_{CC} − 1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} − 2.2)			V_{EE} to (V_{CC} − 2.2)			
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	80	97	—	70	97	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω)	PSRR	80	97	—	70	97	—	dB
Power Supply Current (Per Amplifier)	I_D							mA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	1.6	2.0	—	1.6	2.0	
V_{CC} = −15 V, V_{EE} = −15 V, T_A = +25°C		—	1.9	2.5	—	1.9	2.5	
V_{CC} = −15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	2.8	—	—	2.8	

NOTES: (continued)

3 T_{low} = −55°C for MC35071,A MC35072,A
= −40°C for MC33071,A MC33072,A
= 0°C for MC34071,A MC34072,A

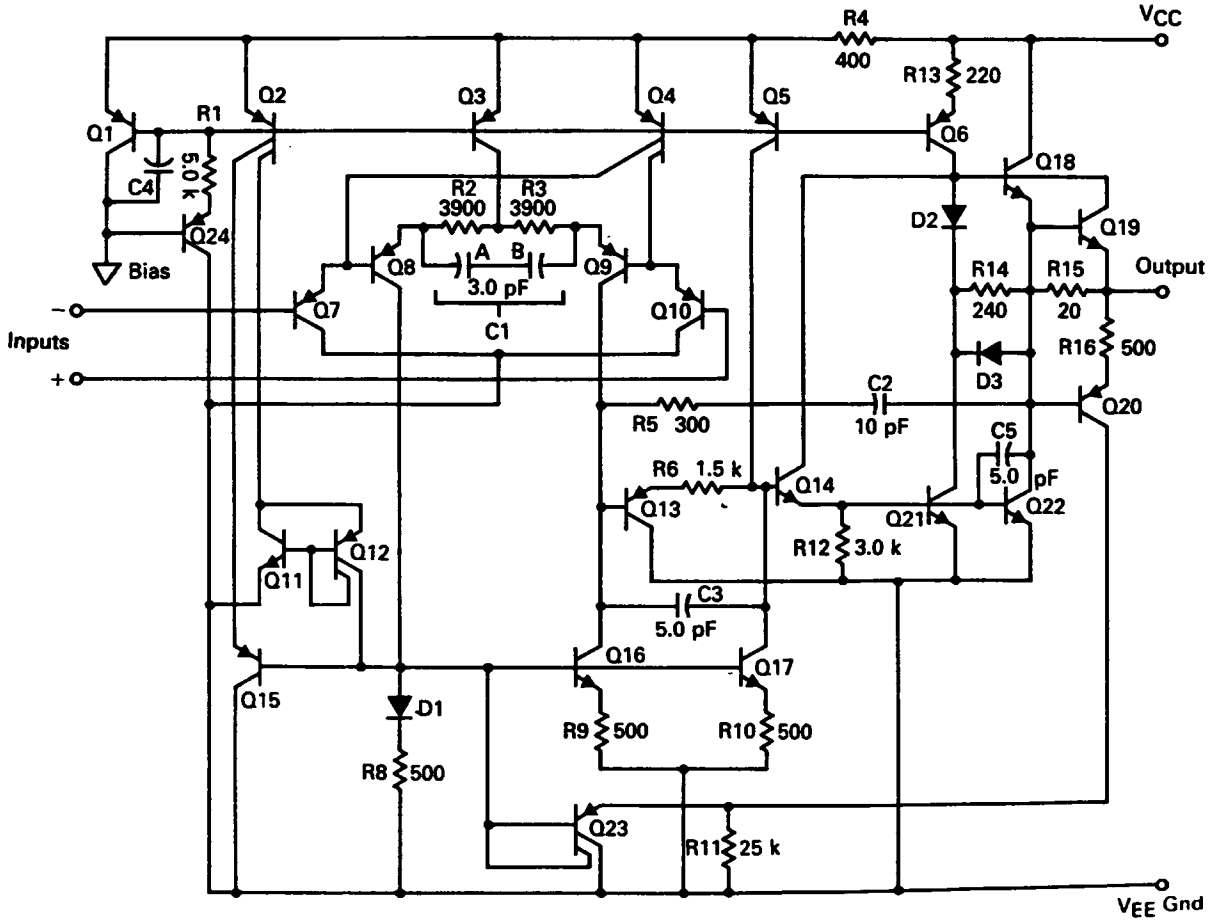
T_{high} = +125°C for MC35071,A/35072,A
= +85°C for MC33071,A/33072,A
= +70°C for MC34071,A/34072,A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Ambient Temperature Range MC35071,A/MC35072,A MC33071,A/MC33072,A MC34071,A/MC34072,A	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

NOTES:
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

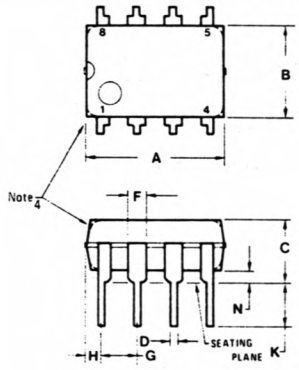
EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC3507_A/MC3407_A/ MC3307_A			MC3507_/MC3407_/ MC3307_			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 k, C_L = 500 pF)	SR							V/μs
A_V + 1.0		8.0	10	—	—	10	—	
A_V − 1.0		—	13	—	—	13	—	
Settling Time (10 V Step, A_V = −1.0)	t_s							μs
To 0.10% (±1/2 LSB of 9-Bits)		—	1.1	—	—	1.1	—	
To 0.01% (±1/2 LSB of 12-Bits)		—	2.2	—	—	2.2	—	
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	—		4.5	—	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 k, V_O = 20 V_{p-p}, THD = 5.0%	BWp	—	200	—	—	200	—	kHz
Phase Margin	ϕm							Degrees
R_L = 2.0 k		—	60	—	—	60	—	
R_L = 2.0 k, C_L = 300 pF		—	40	—	—	40	—	
Gain Margin	A_m							dB
R_L = 2.0 k		—	12	—	—	12	—	
R_L = 2.0 k, C_L = 300 pF		—	4.0	—	—	4.0	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	—	32	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.22	—	—	0.22	—	$pA/\sqrt{Hz}$
Input Capacitance	C_i	—	0.8	—	—	0.8	—	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{p-p}, f = 10 kHz	THD	—	0.02	—	—	0.02	—	%
Channel Separation (f = 10 kHz, MC34072,A Only)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	z_o	—	30	—	—	30	—	Ω

For typical performance curves and applications information refer to MC34074 series data sheet.

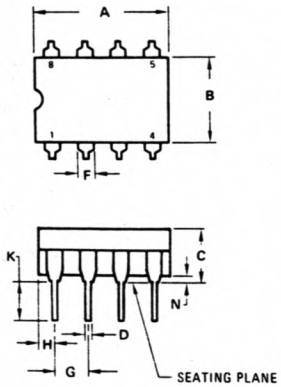


$R_{\theta JA}$ = 100°C/W (Typ)

P SUFFIX
CASE 626-04

NOTES:
1. LEAD POSITIONAL TOLERANCE: ⌀ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030



$R_{\theta JA}$ = 100°C/W (Typ)

U SUFFIX
CASE 693-02

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

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