

VLBA Technical Report No 6

THE UTILITY CONTROL-MONITOR SYSTEM

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Aug 1989

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1.0 INTRODUCTION

This manual describes the VLBA Utility Control and Monitor system which is used to interface Miscellaneous Devices to the VLBA Antenna Control Computer via the Monitor and Control Bus (MCB). The Miscellaneous Device signals are simple but important functions which must be connected to the control computer because they control vital Antenna functions and monitor important alarm conditions.

In this system the Utility Interface module (M103) is the control element and contains digital and analog circuitry to interface the Miscellaneous Device signals to the MCB. M103 command outputs and monitor data inputs are connected to the Miscellaneous Devices by a distribution box and associated cables.

The Control-Monitor signal interfaces and distribution box are given special emphasis because the required diversity of the interface types and associated connectivity considerations dominated the system design. In fact, the need for these capabilities was the impetus for the creation of the system. The signal polarities, channel addresses and distribution box connections of these interface circuits are described in the first portion of the manual. Included in the descriptions of the interface circuits are interfacing guidelines for connecting control and data signals to the system.

A description of the M103 logic and the interactions with the VLBA Standard Interface board follows the interface circuit description mentioned above.

This manual also documents the application of this system to the VLBA antenna and control building electronics. The descriptions list addresses, signal names, signal characteristics, devices serviced and function.

This manual contains data which is convenient for system installation and trouble shooting. This data includes assembly drawings, logic schematic diagrams, bin wire lists, cable and Distribution Junction Box drawings.

2.0 SYSTEM DESCRIPTION

One Utility Control - Monitor System is installed in the Antenna Pedestal Room and services antenna functions; the other system is installed in the control computer rack and services Station Building functions.

These control and monitor functions are (with two exceptions): discrete command and monitor channels, analog signal multiplexing channels and AD590 temperature sensor interface-multiplexer channels. The two exceptions are command reset channels which are described in Section 5.0.

M103 Communications with the control computer are implemented by an internal VLBA Standard Interface Board which receives serial commands and data requests from the Antenna Control computer via the Transmit line (XMT) of the Monitor and Control Bus. This board activates the M103 control logic, gathers the requested data and serially outputs it to the control computer on the Receive line (RCV) of the MCB. The Standard Interface Board controls M103 analog multiplexers and performs A/D conversion of analog signals.

Discrete commands are output via the Standard Interface Board parallel tri-state Command/Monitor bus to storage registers which drive discrete command interface circuits. Inputs from discrete monitor interface circuits are sampled and input to the board by the Standard Interface Board tri-state Command/Monitor bus. The Interface circuits are described in Section 3.0.

Figure 1 (next page) depicts the Utility Control - Monitor System block diagram.

The Distribution Box is described in Section 4.0.

The M103 logic is described in Section 5.0.

The MCB and VLBA Standard Interface Board are not described in this manual; see Specification A55001N001 for details on the MCB protocol. Specification A55001N002 describes the operation of the Standard Interface Board.

The Antenna Utility Interface Module is located in the third bin (below the Focus-Rotation bins) in the Focus-Rotation - ACU rack in the Antenna Pedestal Room. The associated Distribution Junction Box is located on the junction box mounting panel behind and to the left of the Focus-Rotation - ACU rack.

The Station Building Utility Interface Module is located in a bin below the station computer. The associated Distribution Junction Box is mounted in the Computer Room on the wall between the Computer Room and Auxiliary Room.

Drawing A55001W005 (the bin wire list) depicts the bin and connector configurations.

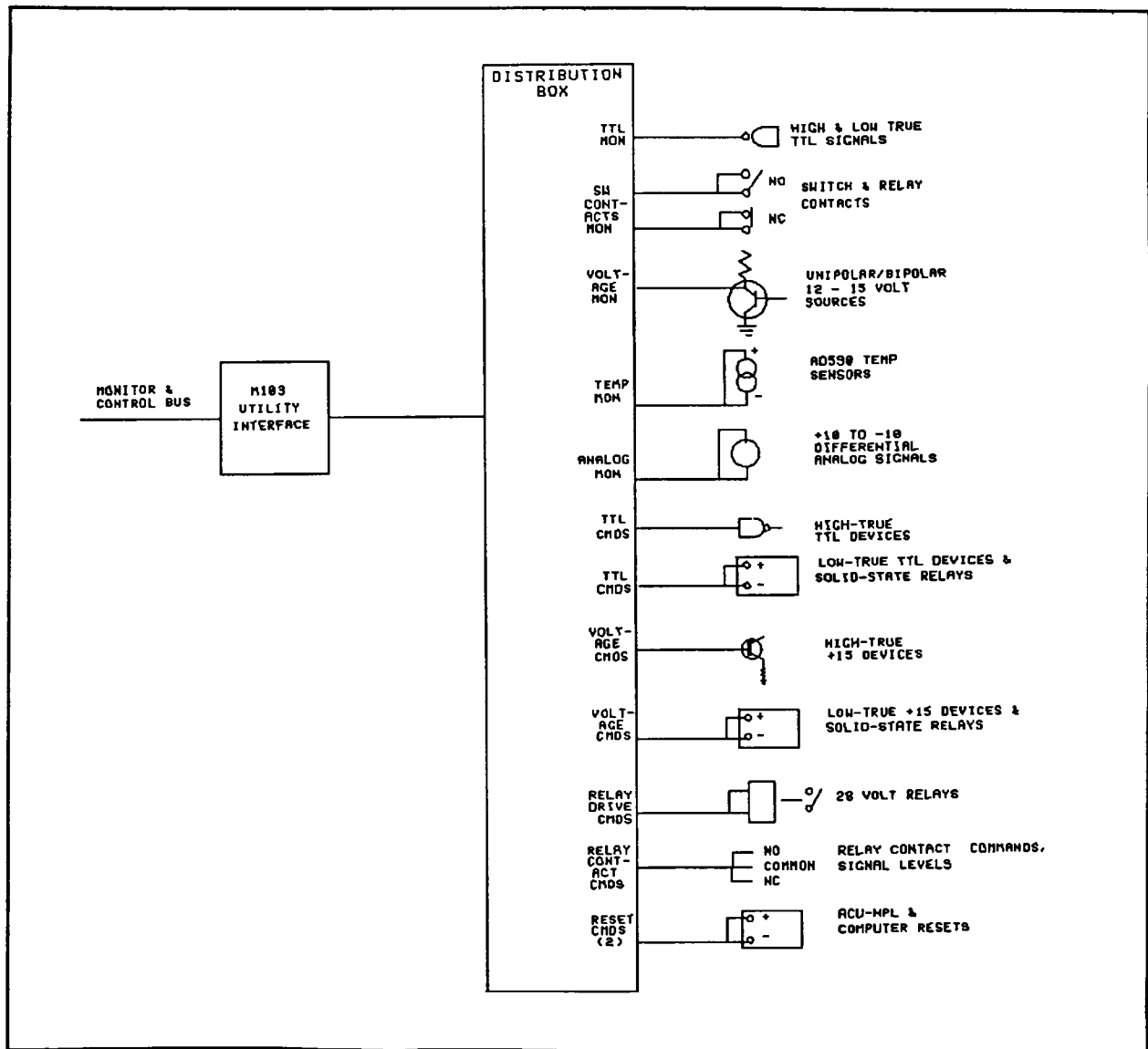


Figure 1, Utility Control & Monitor System Block Diagram

2.1 M103 MODULE DESCRIPTION

The Utility Interface module is a 3-wide module; drawing D55007A0-10 (included in this manual) depicts the configuration.

Packaging considerations made this module 3-wide; the space requirements for the PC boards mounted in the module dictated a two layer packaging scheme; see the Module Assembly Drawing in Section 9.0. The VLBA Standard Interface Board and Power supply board are mounted side-by-side in the front of the module. A consequence of this packaging scheme is that the power supply components are inaccessible with the interface board in place but these components are exposed when the interface board is removed. The module components may be accessed by removing the right (viewed from the front) cover and the wiring may be accessed by removing the left cover. The Power supply board is mounted on module rails and the interface board is mounted in card guides attached to the module screens. Digital and analog circuitry boards are mounted on the same rails as the power supply board.

In contrast to most VLBA modules which are powered by an external rack power supply, the M103 uses internal power supplies powered by 110 volt AC UPS Power. The logic (+5 V) and analog (+/- 15 V) power are provided by a modular triple output supply. A separate supply provides relay drive (+28 V) power. The power supplies, signal relays (described in Section 3.0) and relay driver chips are mounted on the power supply PC board.

An Analog Circuit Board (Board Location A) contains differential analog multiplexer chips and operational amplifiers to convert AD590 temperature sensor currents to voltages which are wired to multiplexers on the board. The digital logic is installed on wire-wrapped logic connector boards in Locations B and C.

A front panel multi-color LED array displays MCB and interface board activity.

3.0 DEVICE INTERFACE CIRCUITS

As one might expect, the character of the control-monitor signal interfaces serviced by this system is quite varied; at the time that the system was designed it was structured to service all known requirements. Additional channel capacity of all types was added to service potential future applications. The quantities and character of these reserve channels is a judgement as to future needs. In the event that it is necessary to modify channel capacity or character, the M103 module has expansion capacity in the form of spare chip space for additional discrete and/or analog channels and spare I/O pins to connect these signals to the distribution box. The distribution box also has space for additional terminals to fan these signals out to the new devices serviced.

In this manual the terms "Device" and "Device Circuit" refer to the miscellaneous components serviced by the Utility Control-Monitor system.

There are no hand-shaking provisions for the discrete command/monitor functions; they are simple on/off states. Secondly, there are no provisions for logical dependancies between channels; if these are required they must be implemented in the control computer software. The state of the discrete monitor inputs are sampled; there are no provisions to trap a transient (momentary) occurrence of a state change which might occur between sample times.

3.1 DISCRETES POLARITY PROGRAMMING - The Utility Interface was designed so that device discrete signals could be either a high or low level for a "true" condition. Thus a "1" discrete command output by the computer always turns on a device and a "0" turns it off. Similarly a "1" on a discrete monitor input to the computer always signifies a "true" or "alarm" condition, the converse follows. This feature simplifies the software in the control computer because it eliminates the need for the software to be structured to hardware interface details. The other side of the coin is that it slightly increases the bulk of the digital hardware; the task of programming signal polarity is assumed by the digital logic.

Discretess command and monitor logic polarity adaption is accomplished by routing inputs and outputs through an exclusive- or gate which has one gate input wired to a polarity control pin on the module I/O connectors. Programming is accomplished on the bin backplane socket contacts. If the polarity control socket contact is allowed to float, the input or output sense is inverted. If the polarity control socket is grounded the sense of the input or output is not inverted. Polarity control is applied to discretess in sets of one, two or three bits. Signal polarity control wiring on the bin backplane is particularized for the two implementations of the system.

The bin backplane wire list is partitioned into four sections: the first section is wiring common to both implementations of the system; the second section is wiring peculiar to the Antenna Pedestal Room system; the third section is wiring peculiar to the Station Building system and the fourth section is wiring peculiar to module M101, the VLBA Inclinometer Interface. The discretes command and monitor signal polarity control wiring is contained in sections two and three. The M101 wiring is only installed in the Antenna Pedestal Room system.

Because some discretes command outputs and monitor inputs are combined into sets of two or more bits with a common polarity control pin, it is necessary to assign channels into sets with common polarity programming.

Unassigned discrete monitor inputs should be configured so that a "0" is input to the computer. This is conveniently implemented by either installing a wire jumper in the Distribution Box or by permitting the input to float; the choice depends upon the sense of the polarity programming. Details of this jumpering are described in the Discrete Monitor Interface circuit discussion.

Discrete commands are formatted as a single address per discrete channel and a single bit argument; a "1" in the least significant bit of the command word argument will turn on the address-designated line and a "0" will turn it off.

3.2 DISCRETE COMMAND CHANNEL INTERFACE CIRCUITS - Command Interface circuit descriptions and typical circuits are as follows:

TTL COMMANDS, TCMD0 - TCMD5: These channels use a 74LS367 driver which will source 2.6 ma and sink 24 ma. Logic common and +5 Volt busses in the Distribution Box enable logic signal drive or current sink drive. (see the Distribution Box description in Section 4.0.)

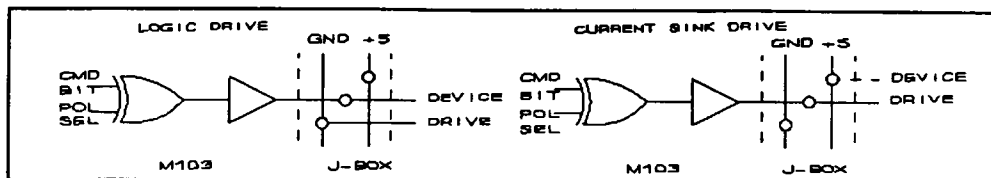


Figure 2, TTL Command Circuit

VOLTAGE COMMANDS, VCMD6 & VCMD7: These channels use a 7407 open-collector driver with a 1.5 Kohm pull-up to +15 Volts. A 7407 buffer will sink 16 ma; 10 ma will flow through the pull-up resistor; the balance of 6 ma can be sunk through the device circuit. A logic common bus and +15 Volt bus in the Distribution Box enable logic signal drive or current sink drive. The circuit schematic is shown below.

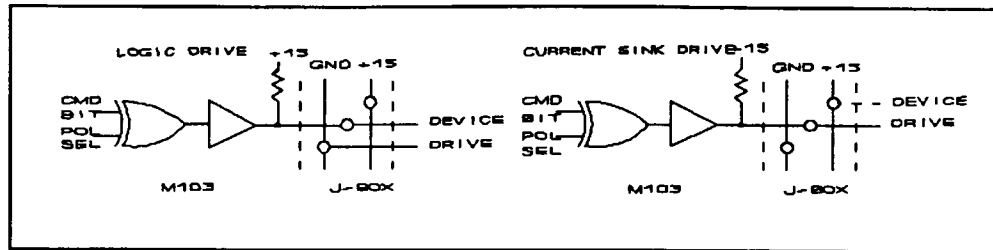


Figure 3, Voltage Command Circuit

28 VOLT RELAY DRIVER COMMANDS, RDCMD8 & RDCMD9: A 28 volt current sinking ULN2068 Darlington relay driver provides drive for Device 28 volt relays. A +28 Volt bus in the Distribution Box provides a current source for these relays.

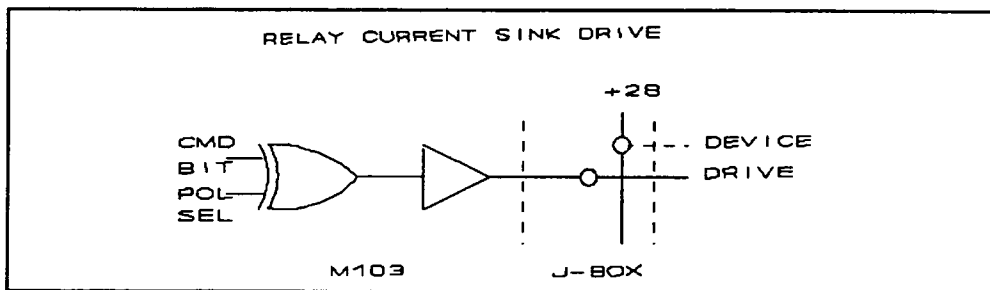


Figure 4, Relay Driver Command Circuit

RELAY CONTACT COMMANDS, RCMD10 & RCMD11: A pair of SPDT signal relays service these channels. Normally open (NO), Common (C) and Normally closed (NC) contacts are available in the Distribution Box so that both states of the relay may be used. These contacts are limited to low-level signalling applications. The relay contacts and module wiring do not permit these relays to be wired into 110 Volt circuits. Note that the NO and NC contact designations refer to the unenergized condition (i.e. a "0" in the command register); a "1" in the command register will cause the NC-C contacts to open and the NO-C contacts to close.

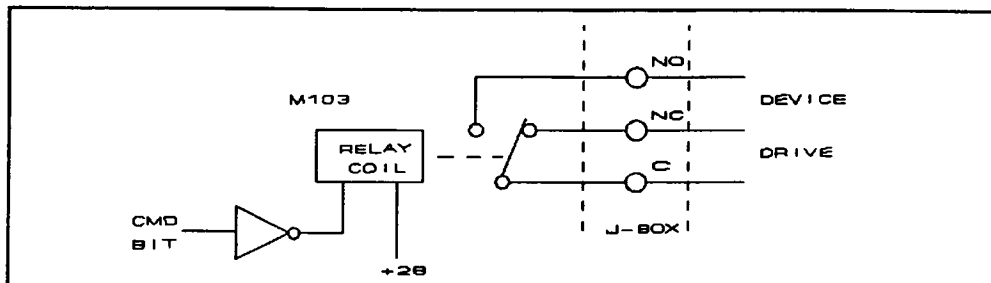


Figure 5, Relay Contact Commands

3.3 TABLE OF DISCRETES COMMAND CHANNELS

The table below describes the discrettes command channel addresses, signal names, signal levels and circuit applications: (XX denotes Block ID)

Command Address	Signal Name	Circuit Type	Logic Levels	Application
XX28H	TCMD0	TTL	0/+3.5	TTL logic-driven devices, solid state relay control via current sinking.
XX29H	TCMD1	"	"	"
XX2AH	TCMD2	"	"	"
XX2BH	TCMD3	"	"	"
XX2CH	TCMD4	"	"	"
XX2DH	TCMD5	"	"	"
XX2EH	VCMD6	Voltage	0/+15	Voltage driven devices, Driver is an open-collector buffer with a 1.5 K pull-up to +15 V
XX2FH	VCMD7	"	"	"
XX30H	RDCMD8	Relay driver	0/+28	28 volt relay driver, current sink output
XX31H	RDCMD9	"	"	"
XX32H	RCMD10	Relay	NO-C-NC	Relay contact drive, NO, C & NC contacts available (not to be used in 110 Volt AC circuits)
XX33H	RCMD11	"	"	"
XX37H	ACU/NPL Reset	28 V relay drive	0/+28V	ACU and NPL AC power is interrupted for 2 seconds
XX37H	Comp Reset	SSR drive	0/+5V	Computer AC power is interrupted for 10 seconds

The two discrete command exceptions (mentioned in 2.0 above) are reset functions. The first reset channel induces a power reset of the ACU and NPL circuitry by turning off the AC power to these units for two seconds. The second reset channel resets the antenna control computer by turning off the computer AC power for ten seconds when it appears that the program execution is not correct. This logic is described in Section 4.0.

3.4 DISCRETES COMMAND CHANNELS POLARITY CONTROL - Command signal polarity control bits are grouped as follows;

TCMD0 & TCMD1:	common polarity control pin	-	Bin J1	-	c
TCMD2 & TCMD3:	"	"	"	"	- " J1 - t
TCMD4 & TCMD5:	"	"	"	"	- " J1 - FF
VCMD6:	private polarity control pin	-	"	J1	- X
VCMD7:	"	"	"	"	- " J1 - f

3.5 DISCRETE MONITOR INTERFACE CIRCUITS

TTL LEVEL-CONTACT CLOSURE CIRCUITS, TDMONO - TDMOM11: A 470 ohm pull-up resistor permits these channels to be driven by a TTL gate or isolated or ground-referenced NC-C or NO-C switch or relay contacts. The Device TTL driver must be capable of sinking 10 ma. A logic common bus in the Distribution Box provides a logic common reference connection for the Device signal.

A Device TTL logic gate connected to a TDMONX input may be either a high or low for an off or non-alarm state. The state of the associated polarity control pin determines the polarity of the signal input to the discrettes monitor register so that the computer is always provided a "1" for "On" or an "Alarm" state irrespective of the actual Device signal polarity. Grounding the associated Polarity Control pin will cause the computer to read a "1" for a high-true "on" or "Alarm" sense. The converse follows.

If a TDMONX input is wired to a Device NO-C (Normally Open-Common) contact set (i.e. the NO-C contacts are open in the off or non-alarm state), the associated Polarity Control Pin should be left floating; the computer will read a "0" for the state of this bit. When the contacts close the computer will read a "1" state for this contact set.

If a TDMONX input is wired to a Device NC-C contact set the associated Polarity Control Pin should be grounded; the computer reads a "0" for the off or non-alarm state. When the NO-C contacts open the computer will read a "1".

Unassigned TDMONX inputs should be jumpered in the Distribution Box so that the computer reads a "0" state from unassigned channels. Unassigned inputs which have been polarity-programmed to produce a "1" state for a high-true input should have the input jumpered to

ground in the Distribution Box. Unassigned inputs which have been polarity-programmed to produce a "1" state for a low-true input should be left floating.

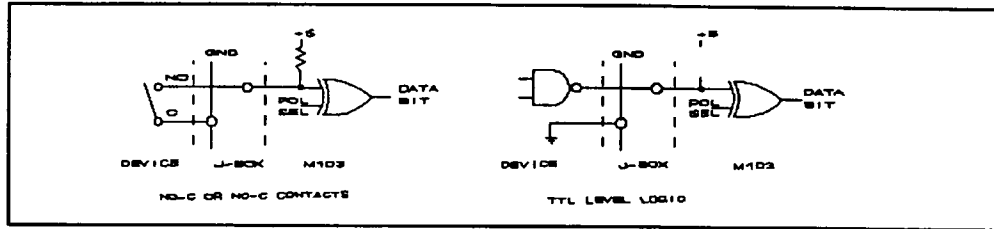


Figure 6, TTL Monitor Circuit

VOLTAGE INPUT CHANNELS, VDMON12 & VDMON13: An optical isolator detector permits these channels to be driven by +12 to +15 Device circuits. These circuits do not have to be ground referenced. The Device driver must be capable of sourcing 5 ma.

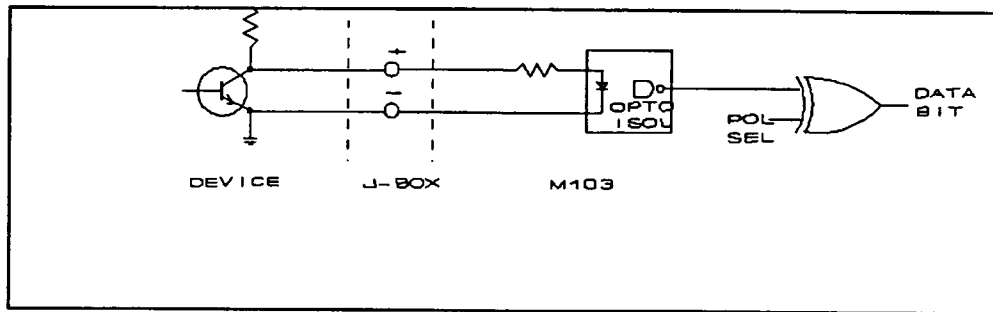


Figure 7, Voltage Monitor Circuit

3.6 TABLE OF DISCRETE MONITOR INTERFACE CHANNELS

Discrete monitor inputs are grouped into a 16-bit parallel input word which is sampled by a single address; the bit assignments, signal names, signal levels and circuit applications are described in the table below. (XX denotes Block ID, bit 0 is the least significant bit.)

Monitor Address	Signal Name	Circuit Type	Logic Levels	Application
-----	-----	-----	-----	-----
XX20H, bit 0	TDMON0	TTL logic, or switch contacts	0/+3.5 V	Device TTL or NO-C-NC contact outputs
XX20H, bit 1	TDMON1	"	"	"
XX20H, bit 2	TDMON2	"	"	"
XX20H, bit 3	TDMON3	"	"	"
XX20H, bit 4	TDMON4	"	"	"
XX20H, bit 5	TDMON5	"	"	"
XX20H, bit 6	TDMON6	"	"	"
XX20H, bit 7	TDMON7	"	"	"
XX20H, bit 8	TDMON8	"	"	"
XX20H, bit 9	TDMON9	"	"	"
XX20H, bit 10	TDMON10	"	"	"
XX20H, bit 11	TDMON11	"	"	"
XX20H, bit 12	VDMON12	12/15 Voltage levels	0/15 V	Device 12 or 15 volt outputs

XX20H, VDMON13 " " "
bit 13

XX20H, VDMON14 " " "
bit 14

3.7 DISCRETES MONITOR CHANNELS POLARITY CONTROL - Discretess

Monitor polarity control bits are grouped as follows:

TDMON0, TDMON1 & TDMON2:	common polarity control pin - J2 - m
TDMON3, TDMON4 & TDMON5:	" " " " - J2 - EE
TDMON6, TDMON7 & TDMON8:	" " " " - J2 - j
TDMON9, TDMON10 & TDMON11:	" " " " - J2 - CC
VMON12:	private polarity control pin - J1 - a
VMON13:	" " " " - J1 - r
VMON14:	" " " " - J1 - DD

3.8 ANALOG SIGNAL MONITORING

Analog monitoring involves multiplexers on the Analog Signal board and the Standard Interface Board multiplexers, Sample and Hold and A/D Converter. The Analog Signal board and Standard Interface Board multiplexers are capable of operation with signal levels up to +/- 35 volts (i.e. common mode + normal mode). The differential input Instrumentation Amplifier provides a common-mode rejection ratio of about 80 db (with a 1 Kohm source impedance) at 60 Hz and can tolerate signal levels up to +/- 15 volts (i.e. common mode + normal mode). The M103 and Standard Interface multiplexers use make-before-break switches to eliminate momentary channel-to-channel connections during switching transitions.

ANALOG SIGNAL CHANNELS, AN1 - AN12: Twelve Miscellaneous Devices analog signals are multiplexed, sampled and converted to 12 bit digital values. Scaling is the standard +10 - 0 - -10 volts analog signal span. Eight channels are multiplexed by HI508A multiplexers on the Analog Board and four channels are multiplexed by the Standard Interface Board multiplexer.

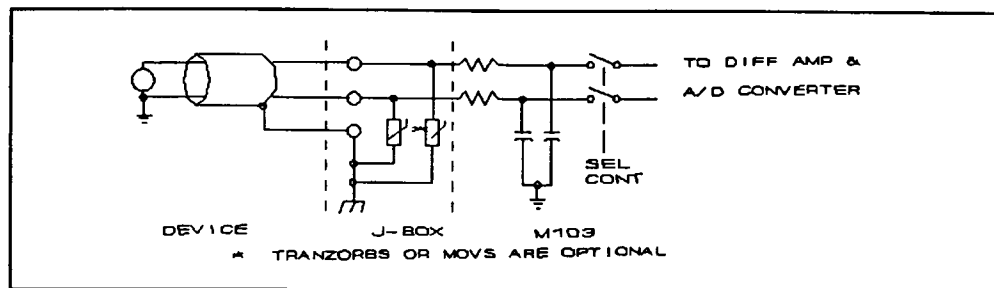


Figure 8, Analog Multiplexer Circuit

M103 INTERNAL ANALOG CHANNELS, AN13 - AN20: Eight channels of M103 internal signals are multiplexed to monitor the performance of the module. These signals are M103 power supplies and reference voltages. Voltage divider-filters and HI508A multiplexers on the Analog Board perform this function.

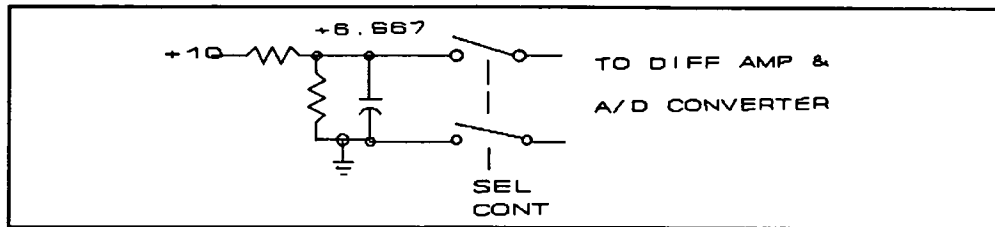


Figure 9, Internal Analog Multiplexer Circuit

AD590 TEMPERATURE SENSOR INTERFACES, TEMP1 - TEMP8: Rack, room and structure temperature measurements are important VLBA parameters. The Analog Board has eight channels of operational amplifier current to voltage converter circuits for AD590 temperature sensors. The amplifier outputs are sampled by multiplexers on the Analog Board and converted to digital values by the Standard Interface Board. An LM324 operational amplifier transforms the AD590 temperature sensor current to a voltage which is scaled at 100 mv/deg C. An 8-channel analog multiplexer routes the amplifier outputs to the Standard Interface Board for A/D conversion. The -15 Volt AD590 excitation and cable shield ground are bussed in the Distribution Box.

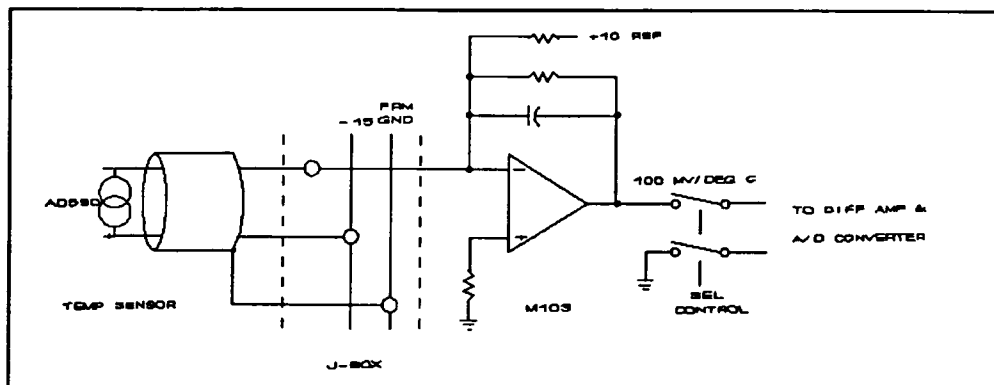


Figure 10, Temperature Sensor Interface Circuit

3.9 TABLE OF ANALOG MONITOR CHANNELS

The table below describes the analog monitor channel addresses, signal names and circuit applications.

Monitor Address	Signal Name	Circuit Type	Signal Levels	Application
XX08H	AN1	Diff Input analog mux	+10 to -10 V	General analog signal multiplexing, inputs protected by RC filter
XX09H	AN2	"	"	"
XX0AH	AN3	"	"	"
XX0BH	AN4	"	"	"
XX0CH	AN5	"	"	"
XX0DH	AN6	"	"	"
XX0EH	AN7	"	"	"
XX0FH	AN8	"	"	"
XX00H	AN9	"	"	"
XX04H	AN10	"	"	"
XX05H	AN11	"	"	"
XX06H	AN12	"	"	"
XX10H	AN13	-15V/2	M103 internal -15 volt PS Voltage	
XX11H	AN14	+10V*.667	Internal +10 Volt reference, monitored to sense A/D gain errors	
XX12H	AN15	0V	M103 Analog ground, monitored to sense A/D zero drift	
XX13H	AN16	+15V/2	M103 internal +15 volt PS voltage	
XX14H	AN17	+5V	M103 internal +5 volt PS voltage	
XX15H	AN18	+28V/4	M103 internal +28 volt PS voltage	
XX16H	AN19	0V	M103 analog ground	

XX17H	AN20	0V	M103 analog ground	
XX18H	TEMP1	op amp & mux	.100V/ degC	Rack, room & structure temperatures using AD590 temp probes
XX19H	TEMP2	"	"	"
XX1AH	TEMP3	"	"	"
XX1BH	TEMP4	"	"	"
XX1CH	TEMP5	"	"	"
XX1DH	TEMP6	"	"	"
XX1EH	TEMP7	"	"	"
XX1FH	TEMP8	"	"	"

4.0 DISTRIBUTION BOX AND CABLING

A requisite for a system of this character is convenience in wiring to Miscellaneous Devices; it should be easy to connect additional Device Channels to the system without retrofitting existing cables, connectors and junction boxes. The cables to Device Channels are typically single, twisted-pair shielded cables which are most conveniently terminated on screw terminals. For these reasons the Distribution Box uses modular three-tier screw termination terminal blocks and the cables are fed through insulating bushings. The three-tier terminal scheme simplifies device signal connections because all wires from a device terminate on one block.

Bussing strips bridge bus signals over one or two terminals as required by the interface circuits; this simplifies cable connections to signals such as logic common, voltage sources, AD590 temperature sensor excitation, frame ground for analog signal cable shields, etc. These bus signals and circuits were described in Section 3.0. A cable connects the two device signal wires and shield to the M103 module bin backplane.

Figure 11 depicts the Distribution Box terminal layout and associated channel signal names. Figure 12 depicts the Station Building Distribution Box and Figure 13 depicts the Pedestal Room Distribution Box. These figures follow the text in this section.

DISTRIBUTION BOX BUSSING - The table below shows the bussing configuration:

SIGNAL	BUSSED TERMINALS	BUS SIGNAL	FUNCTION
-----	-----	-----	-----
Temp1	128 - 135	-15 Volts	AD590 sensor excitation
Temp8	228 - 235	Frame Gnd	Cable shield gnd bus
TDMON0	116 - 127	Digital Gnd	Logic Gnd reference
TDMON8	216 - 227	Frame Gnd	Cable shield gnd bus
AN1	204 - 215	Frame Gnd	Cable shield gnd bus
AN8			
VDMON11	201 - 203	Frame Gnd	Cable shield gnd bus
VDMON12			
TCMD0	236 - 241	Digital Gnd	Logic gnd reference
TCMD5	136 - 141	+5 Volts	+5 volt bus for current sink control circuits

VCMD6	242 - 243	Digital Gnd	Logic gnd reference
VCMD7	142 - 143	+15 Volts	+15 volt bus for current sink control circuits
RDCMD8	146 - 148	+28 Volts	+28 volt bus for 28 volt relays, current sink
ACU RES	246 - 248	Frame Gnd	Cable shield gnd bus

Frame Ground bus terminals are wired to the Distribution Box ground bus which is tied to Antenna frame or Station Building ground; the Distribution Box case is also grounded to frame Ground.

The signal cable from the M103 module provides Digital Ground, +5 Volts, -15 Volts, +15 Volts and +28 Volts to the busses tabulated above.

TRANSIENT SPIKE PROTECTION - Transient spike protection for command and monitor channels is provided in the Distribution boxes by MOV Varistors or Tranzorb avalanche protection diodes which may be installed on the terminals to shunt these spikes to the grounding bus-bar. Transient spikes can be induced on signal distribution cables by lightning discharges to or near the Antenna structure.

Tranzorbs or MOVs need only be installed for long wire runs or for wire runs that reach far up the antenna structure.

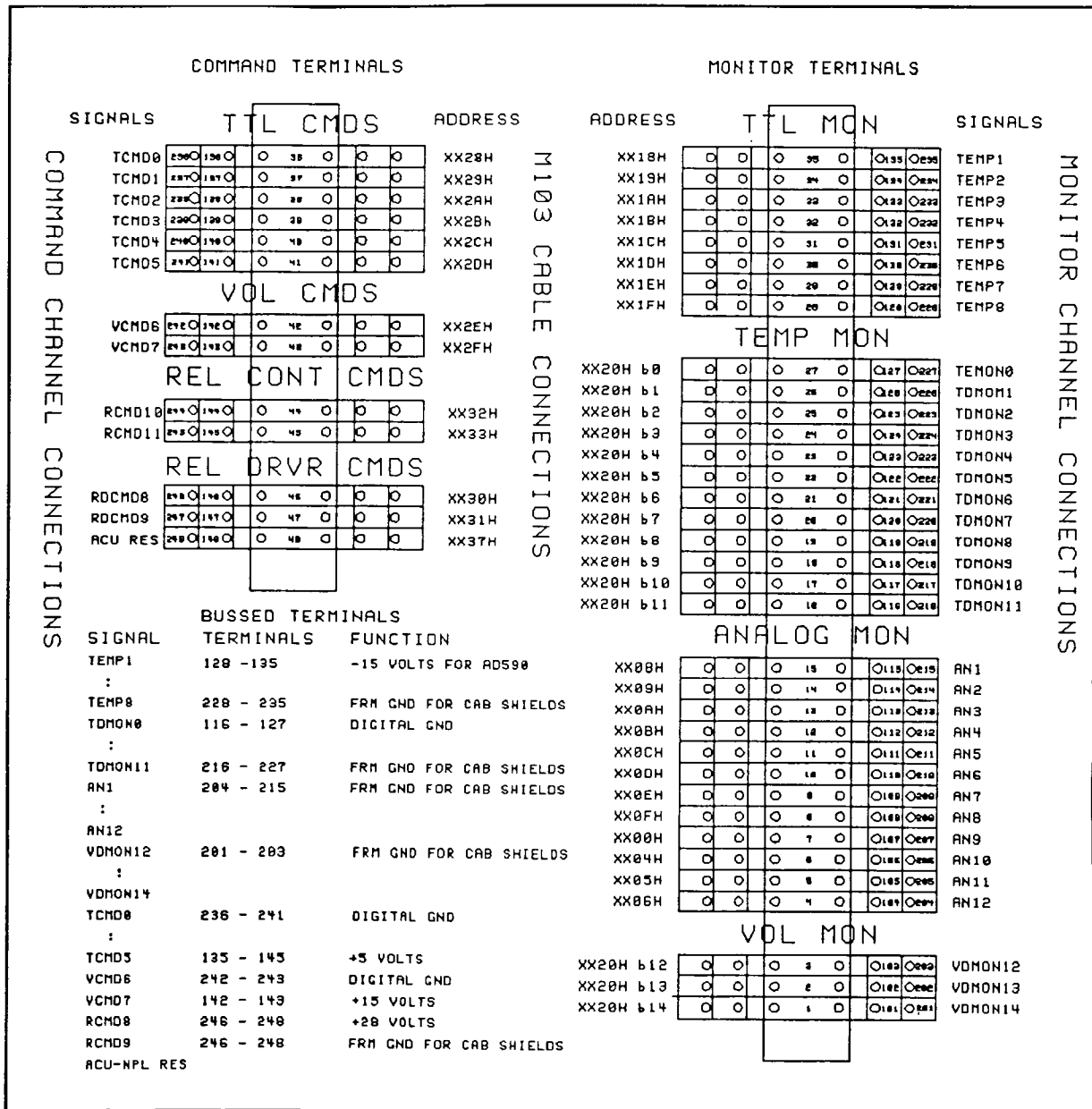


Figure 11, Distribution Box Terminal Assignments

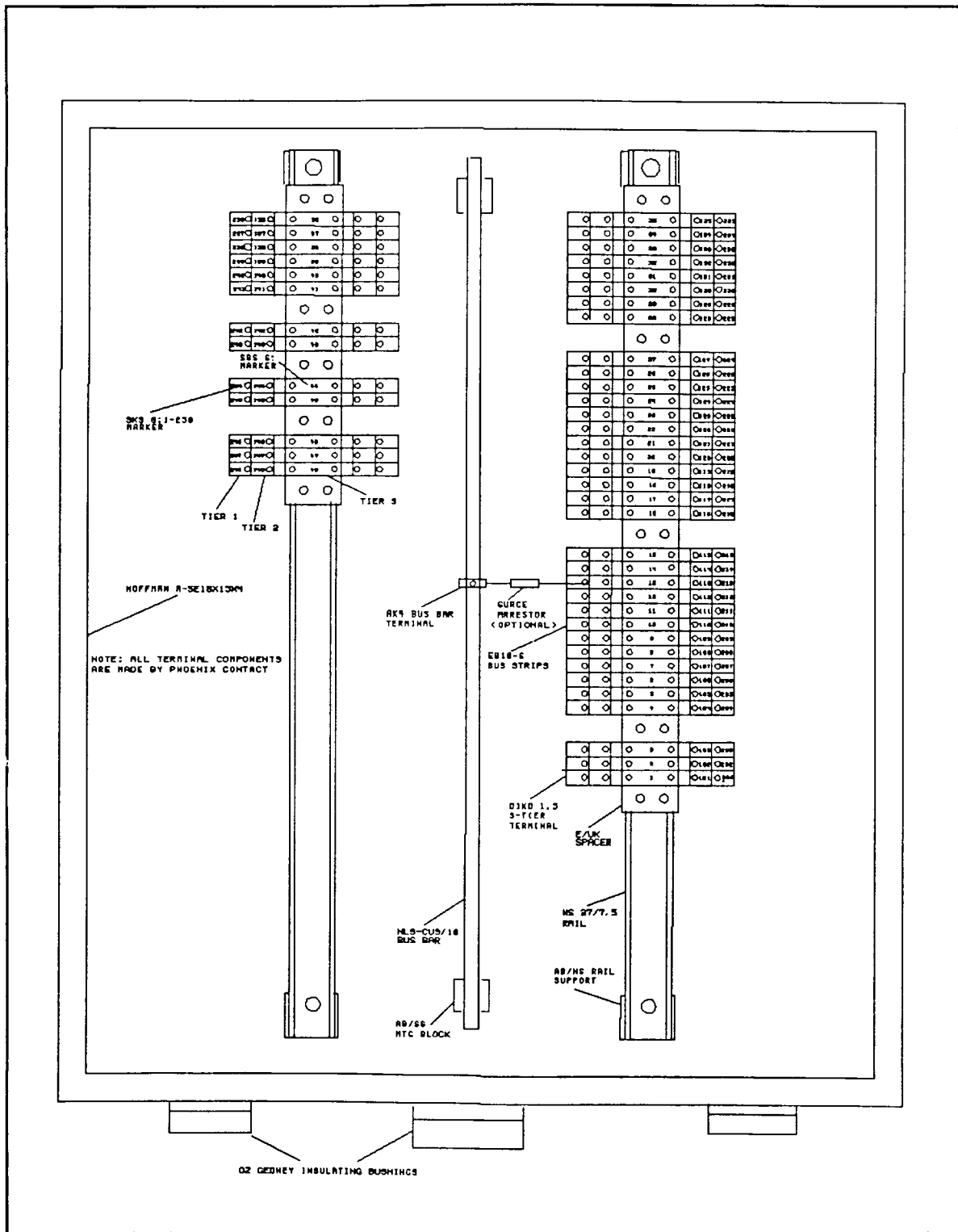


Figure 12, Station Building Distribution Box

5.0 UTILITY INTERFACE THEORY OF OPERATION

The VLBA Standard Interface Board is the control element of the Utility Control-Monitor System; it controls channel selection, reads discrete monitor data, loads the discretized command register and converts analog signals to digital values. Since this module is a plug-in replaceable unit and is described elsewhere, its characteristics will be discussed only in the context of its interactions with the M103 logic. For details on the operation of this module the reader is referred to the VLBA Standard Interface and Bus Protocol specifications, the logic drawings and the Intel 8032 microcontroller program.

Sheet 1 of the M103 logic drawings depicts the Address Decode & Enable Logic which interacts with the Standard Interface. This logic is driven by the Address bus, Read/Write-bar and Device Request terms from the Standard Interface. Device Request is the activating control term and enables the address decode logic which controls the M103 logic. In response to a Device Request, the M103 logic is expected to reply with either a Device Acknowledge term which indicates a digital interaction with the Standard Interface or with an Analog Enable term which indicates that an analog signal is to be multiplexed and converted.

When Read/Write-bar is high, monitor data is input to the Standard Interface. The two monitor data responses are conditioned by the address decode logic of Sheet 1. If the decoded addresses are in the analog address set (XX04H - XX1FH) and if Read/Write-bar is high, the Analog Enable (ANEN) goes true. The Analog Board multiplexers and Standard Interface Board analog multiplexers-A/D convert the address-designated analog signal to a digital value which is impressed upon the tri-state Command-Monitor bus lines.

If the decoded address is XX20H, the Device Acknowledge term goes true which indicates a discrete monitor data read operation; this permits the Standard Interface to sample the discrete monitor data.

If Read/Write-bar is low, a command operation is to be performed. If the decoded addresses fall into the command address range (XX28H to XX37H), Device Acknowledge goes true and the discrete command bit is stored in the address-designated command storage register.

The Standard Interface board parallel tri-state CMD/Mon bus is the avenue for data I/O. Under control of the address logic and ANEN described above, the A/D converter digital output is tri-stated onto the bus and the A/D converter End-of-Conversion strobe causes this data to be read by the interface board.

If discrete monitor data is to be read, the discrete monitor data register is tri-stated onto the Cmd/Mon bus; the Device

Acknowledge term causes the data to be read by the interface board.

If a command is to be output to the command register, the discrete command is tri-stated onto the Cmd/Mon bus and stored in the address-designated register bit.

The command register consists of two 74LS259 eight-bit addressable latches (B5 and B10); register bit selection is controlled by the three least significant address bits. The two Enable Command terms (28H-2FH and 30H-37H) enable these two registers to sample and store the state of the least significant bit (C/M0) of the tri-state Cmd/Mon bus. The command register outputs drive the command interface circuits described in Section 3.0.

The Discrete Monitor Data Register consists of four 4-bit latches (B2, B7, B12 and B22) which are driven by the discrete monitor data interface circuits described in Section 3.0. The state of these interface circuits is sampled by the Discrete Load Clock from the Address Decode & Enable logic discussed above.

The analog multiplexers used on the M103 Analog Interface Board (board location C) use Harris HI508A chips which require address inputs greater than +4.5 volts for a "1" state; this is greater than the 3.5 volt standard LSTTL totem-pole output level. To supply this level the Address Buffer Logic uses open-collector 7407 buffers with a pull-up resistor to +5 volts.

The Standard Interface Board requires an initialization to tell it which addresses it must respond to; on power up (and at convenient intervals) the board issues an ID (Identification Request) to the Device ID Logic. This term enables tri-state drivers to tri-state a Device ID code onto the least significant 8 bits of the Cmd/Mon bus. The board reads this code and it becomes the upper 8 bits of the channel addresses. The inputs to these 74LS368 buffers are hard-wired in the bin backplane. The ID code for the Antenna Pedestal room Utility Command - Monitor System is 41H; the Station Building system ID code is 42H.

Eight channels of LM324 operational amplifiers on the Analog Board (board A) convert the AD590 temperature sensor current outputs to a 100 mv/deg C voltage. The AD590 output is one microamp per deg C + 273 microamps. A 273 microamp current from a precision +10 volt reference voltage offsets the AD590 offset current. The amplifier outputs are wire-wrap jumpered to a HI508A differential analog multiplexer on the analog board. The -15 volt excitation for the AD590 sensors is provided by a bus in the Distribution Box.

Board A contains eight channels of HI508A differential multiplexers to sample external analog data. These multiplexers can tolerate input signal levels as high as +/- 35 volts without damage. The multiplexer inputs are protected by a 1 Kohm/.1 ufd RC filter

which filters voltage spikes on the analog signal lines and isolates the signal sources from the multiplexer switching charge transfers.

An additional four channels of external analog data is multiplexed by four multiplexer channels on the Standard Interface Board (XX04H through XX06H). A logic term, Hi/Lo Select controls these multiplexer channels. If the analog data address is in the XX00-XX07H set, Hi/Lo Select is low true which causes the Standard Interface Board analog multiplexers to respond to the three least-significant address bits. These analog channels are also protected by RC filters and can also tolerate an input signal level of +/- 35 volts without damage.

Eight channels of differential multiplexers sample internal M103 power supplies and reference voltages; these channels provide a measure of performance of the M103 module. One percent resistor voltage dividers scale the +10, +/- 15 and +28 volts to the standard analog signal span.

The ACU-NPL reset circuit uses a control flip-flop and a 14 stage HCT4060 counter-oscillator to generate a two second time delay. This signal term drives a ULN2068 current sinking relay driver which drives a 28 volt relay in the Pedestal Room. Prior to activation, the flip-flop (C18) is reset which inhibits the counter. The flip-flop is set by the address 4137H command; the Q output turns on the relay driver which activates the relay thus interrupting power to these units. At the count of 8192 Q14 rises and clocks off the control flip-flop. The time-out period is determined by the period of the clock oscillator which is determined by the resistors and capacitor on dip header C12.

The computer reset circuit employs two concatenated counter circuits similar to the ACU-NPL reset. The Antenna Control Computer is expected to output an alternating "1" and "0" at intervals of 10 minutes to address 4237H. The rising edge of the "1" in the command register bit B10-12 triggers one-shot C2-12 which strobe-resets HCT4060 counter C28. If Q14 (count of 8192) rises, flip-flop C18-11 is set; this turns off the computer power (via an SSR in a box in the rear of the computer rack). When C18 is set, HCT4060 counter C26 begins counting and the rise of Q14 in C26 clocks off flip-flop C18-11 which restores power to the computer. Resistors and a capacitor on dip header C27 determine the time-out periods of 21 minutes for C28 and 20 seconds for C26.

The 28 volt relay power load imposes a system constraint because the 28 volt power supply is rated at 400 ma. This is adequate capacity for driving several light duty relays. The 28 volt relay drivers are capable of sinking 1.5 Anps but the total 28 volt relay drive load (including ACU-NPL reset) should not exceed 400 ma.

6.0 PEDASTAL ROOM SYSTEM CHANNELS

Block ID code = 41H

COMMAND CHANNELS

Command Address	Signal Name	Circuit Type	Function Assignment
-----	-----	-----	-----
4128H	TCMD0	TTL	Feed Heater SSR Control *
4129H	TCMD1	"	Not Assigned
412AH	TCMD2	"	" "
412BH	TCMD3	"	" "
412CH	TCMD4	"	" "
412DH	TCMD5	"	" "
412EH	VCMD6	Voltage	" "
412FH	VCMD7	"	" "
4130H	RDCMD8	Relay driver	" "
4131H	RDCMD9	"	" "
4132H	RCMD10	Relay	UPS Panic Shutdown. 1 = UPS shutdown.
4133H	RCMD11	"	Not Assigned
4137H	ACU/NPL Reset	28 V relay	" " ACU & NPL Power Reset

* Tranzorb protected in the Pedestal Room Distribution Box.

DISCRETE MONITOR CHANNELS

Monitor Address	Signal Name	Circuit Type	Function Assignment
-----	-----	-----	-----
4120H, bit 0	TDMON0	TTL level, or contacts	Ant Smoke Detector Trouble NO-C contact set
4120H, bit 1	TDMON1	"	UPS Battery Alarm. High = low battery.

4120H, bit 2	TDMON2	"		UPS Inverter Alarm. High = inverter on.
4120H, bit 3 Bus.	TDMON3	"		Not assigned. Input jumpered to Distribution Box Gnd
4120H, bit 4	TDMON4	"	"	"
4120H, bit 5	TDMON5	"	"	"
4120H, bit 6	TDMON6	"	"	"
4120H, bit 7	TDMON7	"	"	"
4120H, bit 8	TDMON8	"	"	"
4120H, bit 9	TDMON9	"	"	"
4120H, bit 10	TDMON10	"	"	"
4120H, bit 11	TDMON11	"	"	"
4120H, bit 12	VDMON12	12/15 Voltage		Not Assigned
4120H, bit 13	VDMON13	"	"	"
4120H, bit 14	VDMON14	"	"	"

ANALOG MONITOR CHANNELS

Monitor Address	Signal Name	Circuit Type	Value	Function Assignment
-----	-----	-----	-----	-----
4108H	AN1	Diff an mux	.5V/Amp	Feed Heater Current *
4109H	AN2	"		Not Assigned
410AH	AN3	"		" "
410BH	AN4	"		" "

410CH	AN5	"		" "
410DH	AN6	"		" "
410EH	AN7	"		" "
410FH	AN8	"		" "
4100H	AN9	"		" "
4104H	AN10	"		" "
4105H	AN11	"		" "
4106H	AN12	"		" "
4110H	AN13	"	-15V/2	M103 internal -15 volt PS Voltage
4111H	AN14	"	+10V*.667	M103 Internal +10 Volt reference
4112H	AN15	"	0V	M103 Analog ground
4113H	AN16	"	+15V/2	M103 internal +15 V PS
4114H	AN17	"	+5V	M103 internal +5 volt PS
4115H	AN18	"	+28V/4	M103 internal 28 volt PS
4116H	AN19	"	0V	M103 analog ground
4117H	AN20	"	0V	M103 analog ground

* Tranzorb protected in the Pedestal Room Distribution Box.

TEMPERATURE MONITOR CHANNELS

(Scaling = .100 volts/deg C)

Monitor Address	Signal Name	Function Assignment
-----	-----	-----
4118H	TEMP1	Pedestal Room Air Temperature
4119H	TEMP2	ACU Rack Temperature
411AH	TEMP3	Servo Drive Cabinet Temperature.
411BH	TEMP4	Outsid Air Temperature.

411CH	TEMP5	"	"
411DH	TEMP6	"	"
411EH	TEMP7	"	"
411FH	TEMP8	"	"

7.0 STATION BUILDING SYSTEM CHANNELS

Block ID Code = 42H

COMMAND CHANNELS

Command Address	Signal Name	Circuit Type	Function Assignment
-----	-----	-----	-----
4228H	TCMD0	TTL	Not Assigned
4229H	TCMD1	"	" "
422AH	TCMD2	"	" "
422BH	TCMD3	"	" "
422CH	TCMD4	"	" "
422DH	TCMD5	"	" "
422EH	VCMD6	Voltage	" "
422FH	VCMD7	"	" "
4230H	RDCMD8	Relay driver	" "
4231H	RDCMD9	"	" "
4232H	RCMD10	Relay contacts	NO-C contact set closure causes UPS Panic Shutdown
4233H	RCMD11	"	Not Assigned
4237H	Comp	SSR drive	Computer power reset

DISCRETE MONITOR CHANNELS

Monitor Address	Signal Name	Circuit Type	Function Assignment
-----	-----	-----	-----
4220H,	TDMON0	TTL logic, or switch contacts	NO-C closure indicates UPS alarm, low batteries

4220H, bit 1	TDMON1	"		NO-C, closure indicates UPS inverter on
4220H, bit 2	TDMON2	"		NO-C, closure indicates Power Transfer Switch on Generator.
4220H, bit 3	TDMON3	"		logic common bus Antenna non-critical CB, NO-C indicates tripped
4220H, bit 4	TDMON4	"		Antenna critical CB, NO-C indicates tripped
4220H, bit 5	TDMON5	"		Not Assigned, input jumpered to Dist Box logic common bus
4220H, bit 6	TDMON6	"		Antenna Fire Alarm, NC-C indicates Alarm
4220H, bit 7	TDMON7	"		Air Handler #2 NC-C indicates Fault
4220H, bit 8	TDMON8	"		Air Handler #1 NC-C indicates Fault
4220H, bit 9	TDMON9	"		ACU Fault NC-C indicates Fault
4220H, bit 10	TDMON10	"		Bldg Fire Alarm Trouble NC-C indicates Trouble
4220H, bit 11	TDMON11	"		Not Assigned, input jumpered to Dist Box logic common bus
4220H, bit 12	VDMON12	12/15 Voltage levels		"
4220H, bit 13	VDMON13	"		"
4220H, bit 14	VDMON14	"		"

ANALOG MONITOR CHANNELS

Monitor Address	Signal Name	Circuit Type	Value	Function Assignment
-----	-----	-----	-----	-----
4210H	AN1	Diff an mux		N/A

4211H	AN2	"		N/A
4212H	AN3	"		N/A
4213H	AN4	"		N/A
4214H	AN5	"		N/A
4215H	AN6	"		N/A
4216H	AN7	"		N/A
4217H	AN8	"		N/A
4200H	AN9	"		N/A
4204H	AN10	"		N/A
4205H	AN11	"		N/A
4206H	AN12	"		N/A
4210H	AN13	"	-15V/2	M103 internal -15 volt PS Voltage
4211H	AN14	"	+10V*.667	M103 Internal +10 Volt reference
4212H	AN15	"	0V	M103 Analog ground
4213H	AN16	"	+15V/2	M103 internal +15 V PS
4214H	AN17	"	+5V	M103 internal +5 volt PS
4215H	AN18	"	+28V/4	M103 internal 28 volt PS
4216H	AN19	"	0V	M103 analog ground
4217H	AN20	"	0V	M103 analog ground

TEMPERATURE MONITOR CHANNELS

(Scaling = .100 volts/deg C)

Monitor Address	Signal Name	Function Assignment
-----	-----	-----
4218H	TEMP1	"C" Rack Temperature
4219H	TEMP2	"D" Rack Temperature

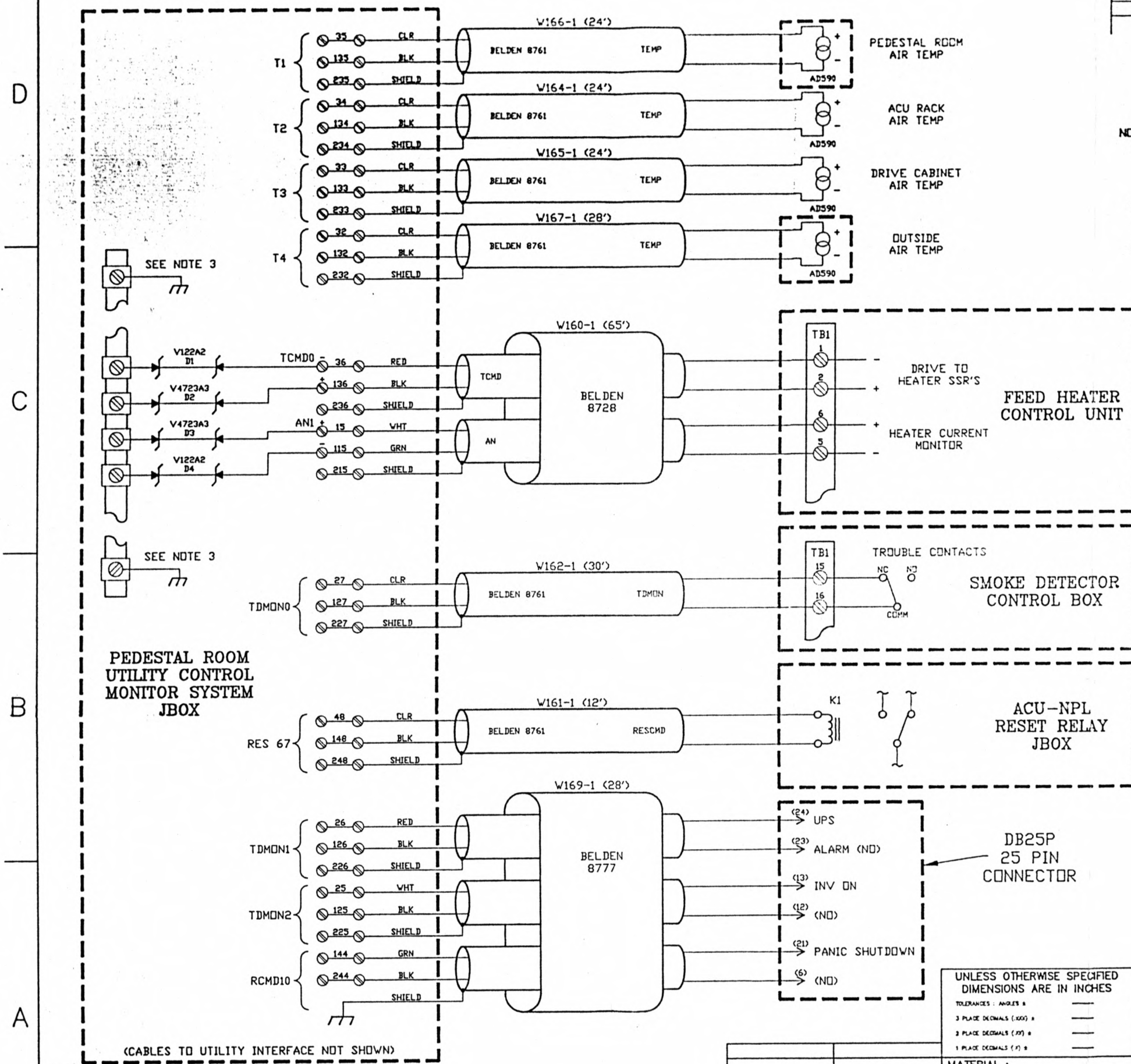
421AH	TEMP3	Electronics Room air temperature
421BH	TEMP4	Computer Rack temperature
421CH	TEMP5	Tape Recorder Rack temperature
421DH	TEMP6	Computer Room air temperature
421EH	TEMP7	Auxiliary Room air temperature
412FH	TEMP8	N/A

8.0 UTILITY CONTROL - MONITOR SYSTEM DRAWING LIST

ANTENNA PEDASTAL ROOM SIGNAL DISTRIBUTION SCHEMATIC	C55001W004
STATION BUILDING SIGNAL DISTRIBUTION SEMATIC	C55001W003
M103 LOGIC SCHEMATIC	D55001S005
M103 ASSEMBLY DRAWING	D55001A010
M103 BIN WIRE LIST, (REV D)	A55001W005
M103 BIN TO DISTRIBUTION BOX CABLE WIRE LIST	A55001W002
UTILITY CONTROL-MONITOR SYSTEM JUNCTION BOX ASSY	C55001A003
UTILITY INTERFACE LOGIC CHIP LOCATIONS	A55001A009
STANDARD INTERFACE CARD, MODEL D	C55002S004

9.0 UTILITY CONTROL - MONITOR SYSTEM DRAWINGS

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	5-89	ANDREATA		REDRAWN WITH ACAD
B	3-90	ANDREATA		REVISED TO AS BUILT



- NOTES:
- CABLE:
 - 2 COND - BELDEN 8761, TV PAIR WITH DRAIN/SHIELD
 - 4 COND - BELDEN 8728, 2 TV PAIR WITH DRAIN/SHIELD
 - 6 COND - BELDEN 8777, 3 TV PAIR WITH DRAIN/SHIELD
 - CABLES FROM UTILITY CONTROL/MONITOR JBOX TO ** CONTROL INTERFACE NOT SHOWN (SEE NRAD DVG. #C55001A003 AND #A55001V002)
 - TIE TO JBOX GND AND RUN #10 AVG (OR LARGER) LINE FROM BUS BAR TO ANTENNA FRAME GND.

LOCATED OUTSIDE VERTEX ROOM

MAR 15 1990

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES

TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.000) ±
2 PLACE DECIMALS (.00) ±
1 PLACE DECIMALS (.1) ±

UTILITY CONTROL/MONITOR SYSTEM	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
PEDESTAL ROOM UTILITY CON/MON SYSTEM DEVICE CABLES	DRAWN BY ANDREATA DATE 5-89 DESIGNED BY WEBER DATE 4-88 APPROVED BY DATE
SHEET NUMBER 1 of 1	DRAWING NUMBER C55001V004

NEXT ASSEMBLY	DWG. TYPE
---------------	-----------

ACAD: PEDRCABL

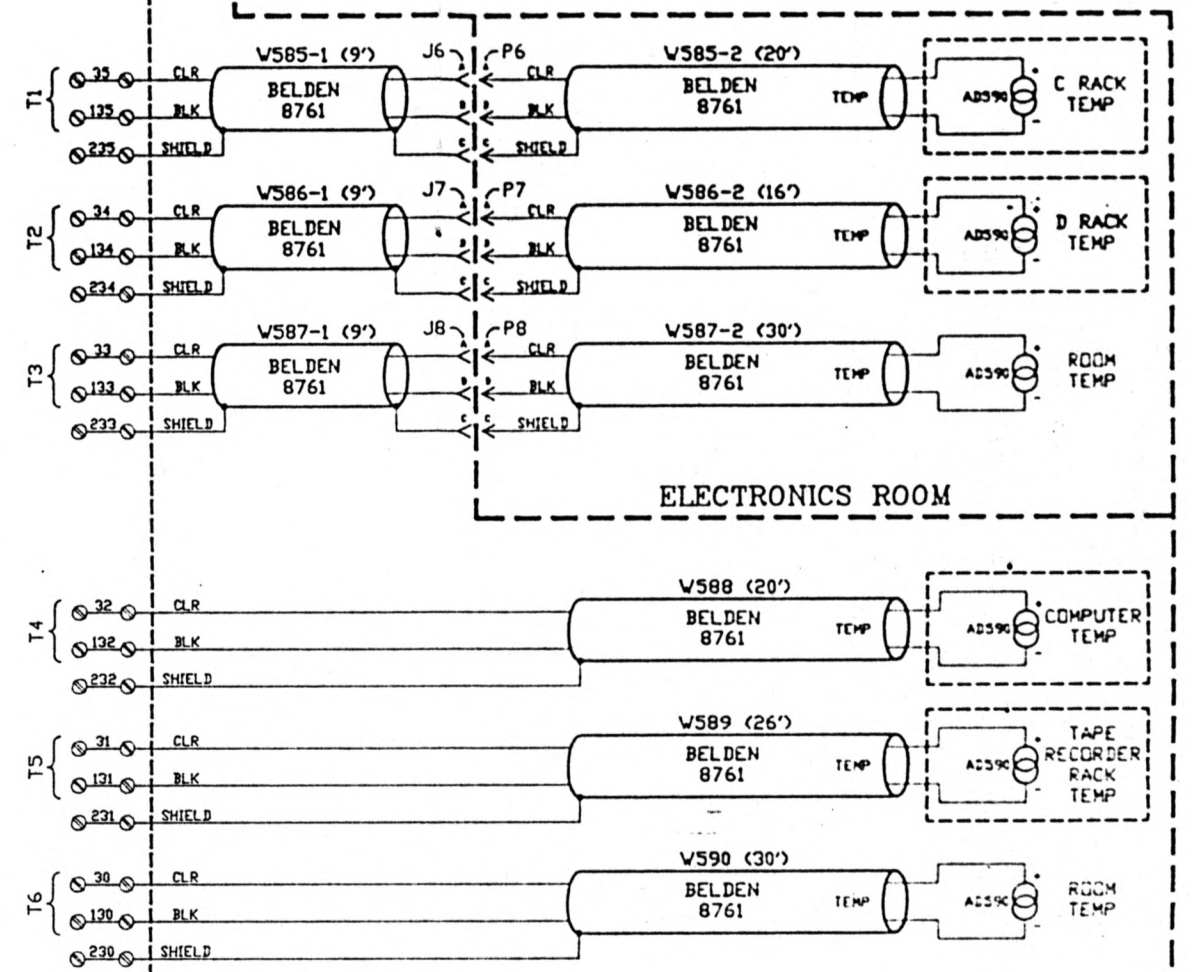
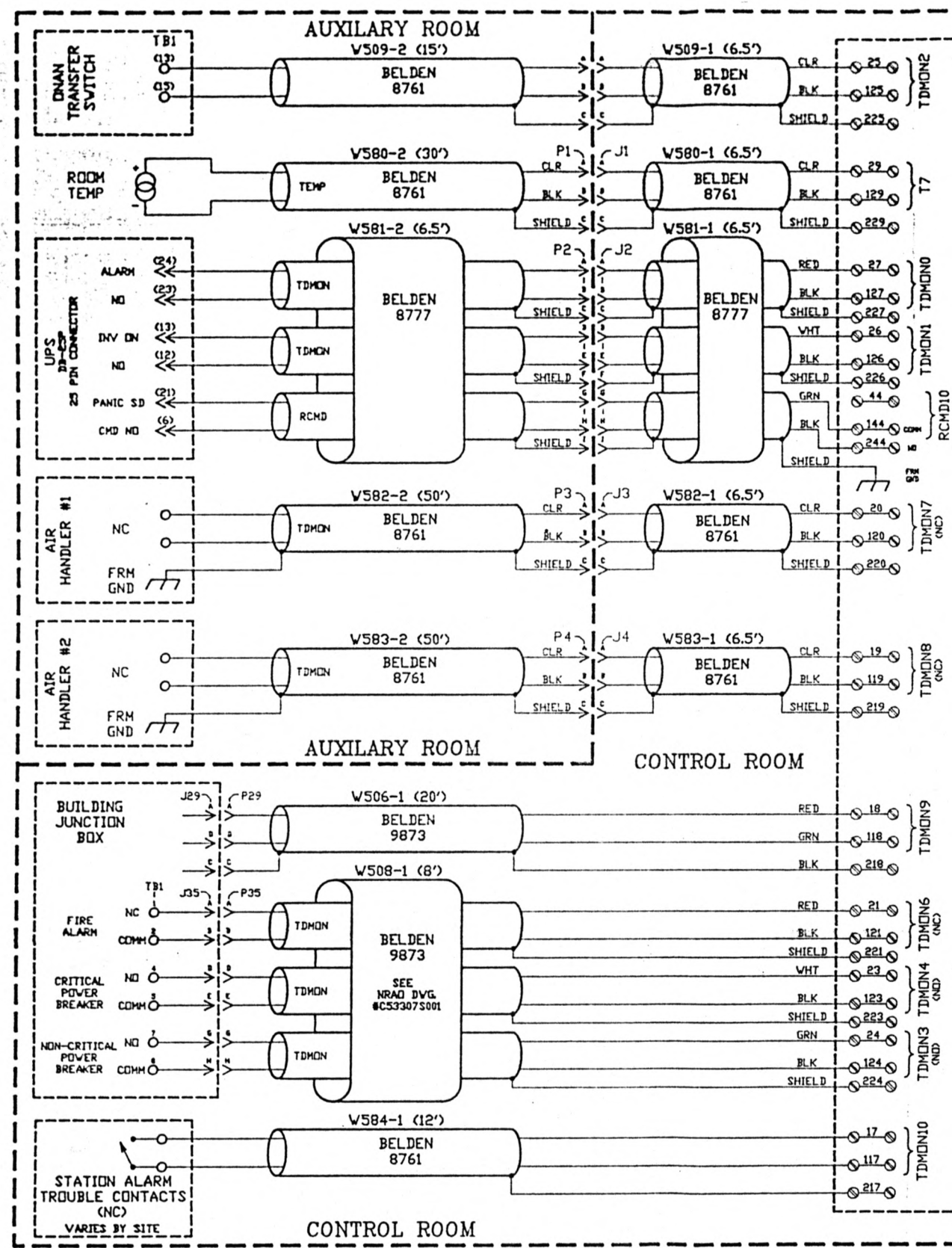
REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
A	4-89	ANDREATA		MINOR CORRECTIONS
B	3-90	ANDREATA		REVISED TO AS BUILT

D

C

B

A



CONTROL BUILDING
UTILITY CON/MON SYSTEM
JUNCTION BOX
CABLES TO UTILITY INTERFACE
NOT SHOWN
(SEE NOTE #2)

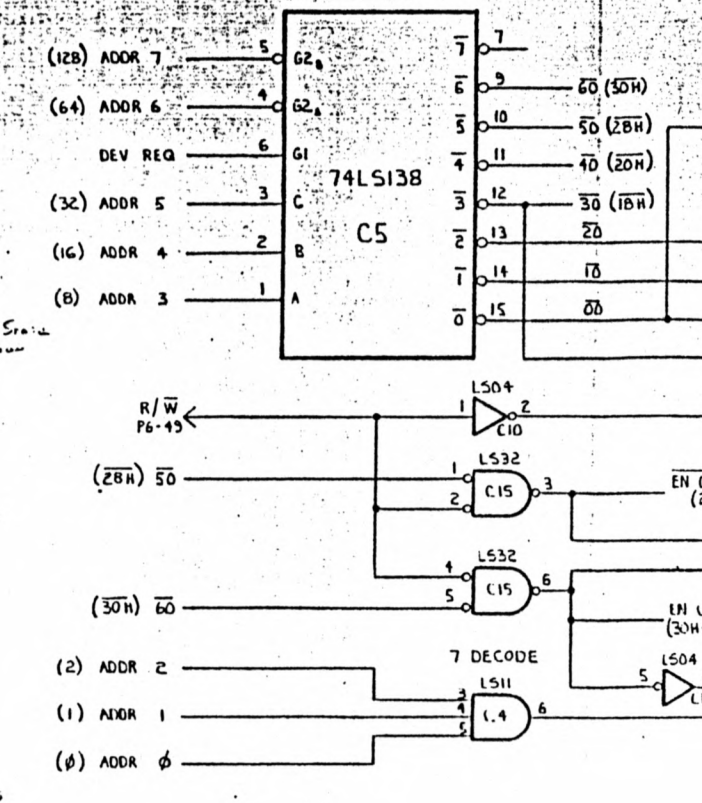
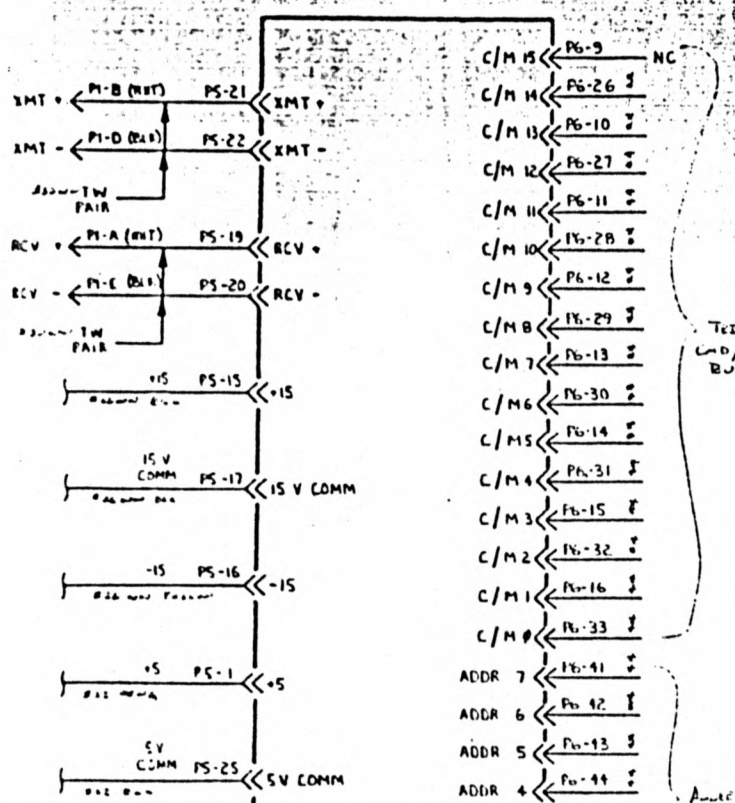
- NOTES:
- CONNECTORS:
 - TEMP CHANNELS = BULKHEAD - MS3100A14S-1S
CABLE PLUG - MS3106A14S-1P
CABLE STRAIN RELIEF - MS3057A-14
 - TDMON CHANNELS = BULKHEAD - MS3100A14S-1S
CABLE PLUG - MS3106A14S-1P
CABLE STRAIN RELIEF - MS3057A-14
 - UPS CABLE = BULKHEAD - MS3100A18-1S
CABLE PLUG - MS3106A18-1P
 - BUILDING JBOX = CABLE PLUG - MS3126F12-10S
 - FOR CABLES FROM UTILITY CON/MON TO CONTROL INTERFACE SEE NRAD DWG #C55002A005 AND #A55002V003.
 - CABLES: BELDEN #8761 = 2 CONDUCTOR
BELDEN #8777 = 3 PAIR
BELDEN #9873 = 3 PAIR

MAR 15 1990

ACAD: CNTRLCBL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		V L B A Y		UTILITY CONTROL/MONITOR SYSTEM		NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801	
TOLERANCES: ANGLES: —		T I T L E		CONTROL BUILDING UTILITY CON/MON SYSTEM DEVICE CABLES		DRAWN BY VEBER	
3 PLACE DECIMALS (.003) ± —		MATERIAL: —		DESIGNED BY VEBER		DATE 4-88	
3 PLACE DECIMALS (.001) ± —		FINISH: —		APPROVED BY		DATE 4-88	
1 PLACE DECIMALS (.1) ± —		NEXT ASSEMBLY		SHEET NUMBER		SCALE	
		DWG. TYPE		1 of 1		DRAWING NUMBER	
				C55001V003		REV. 8	

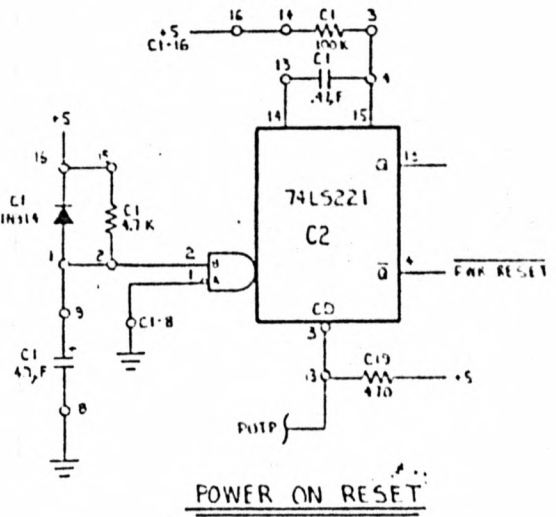
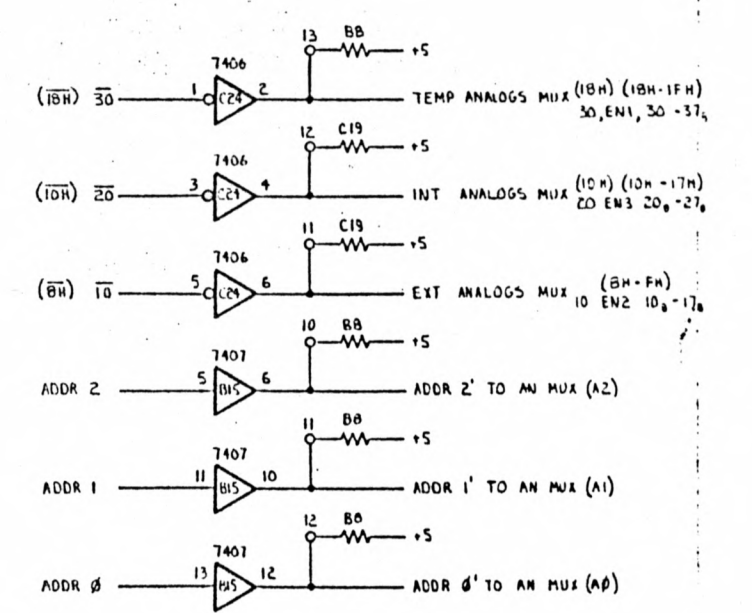
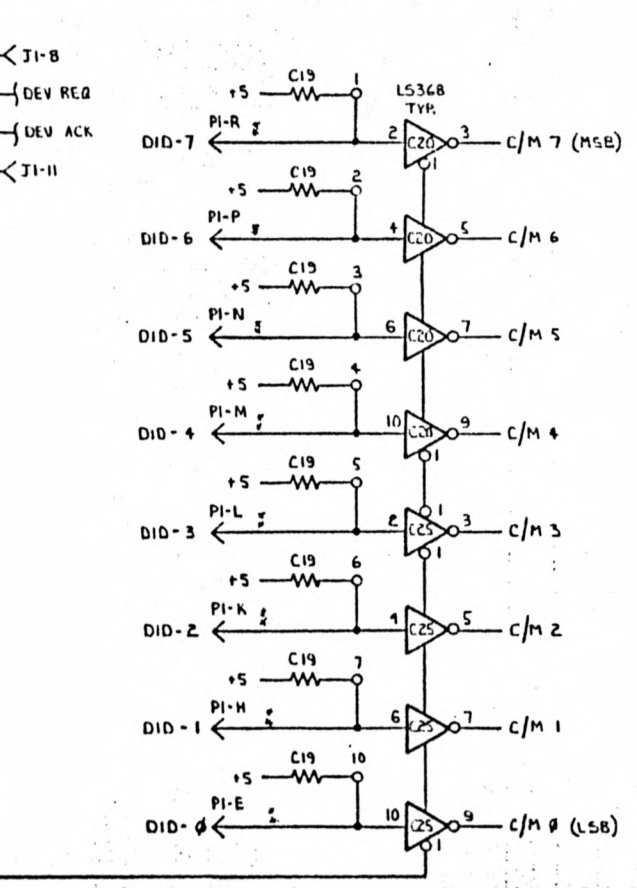
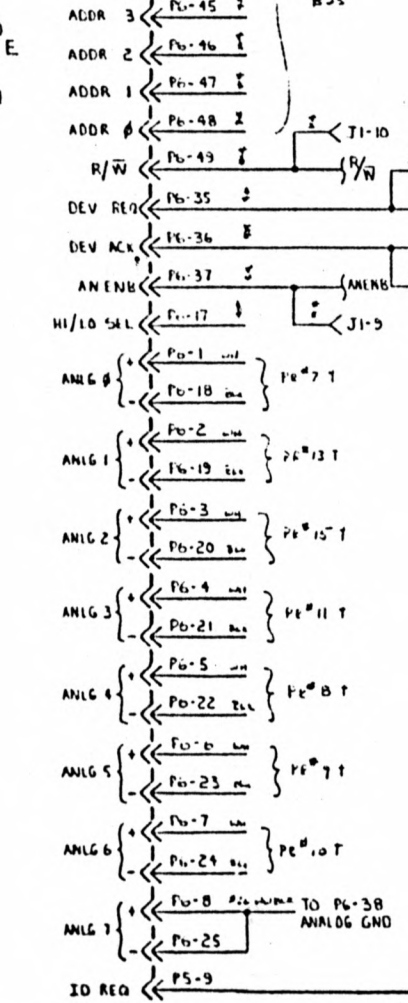
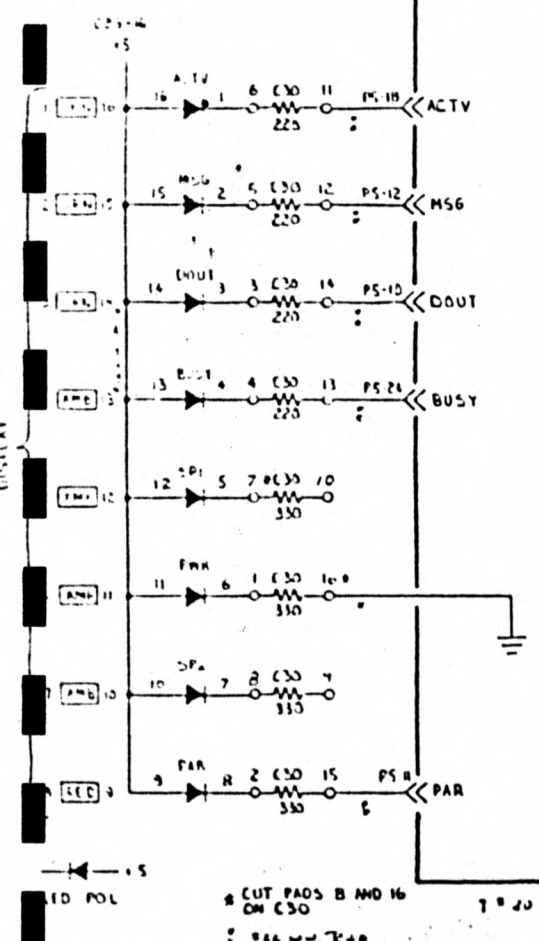
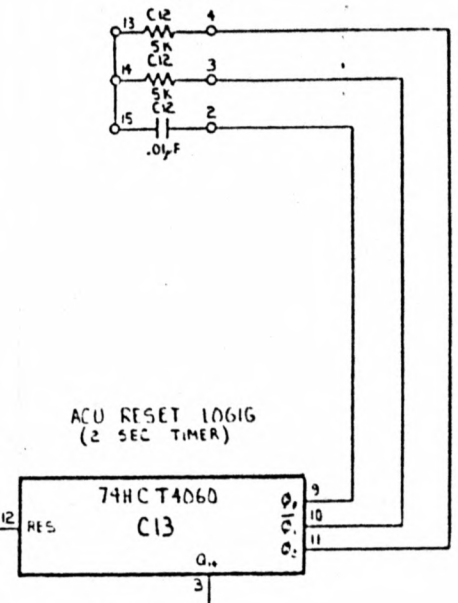
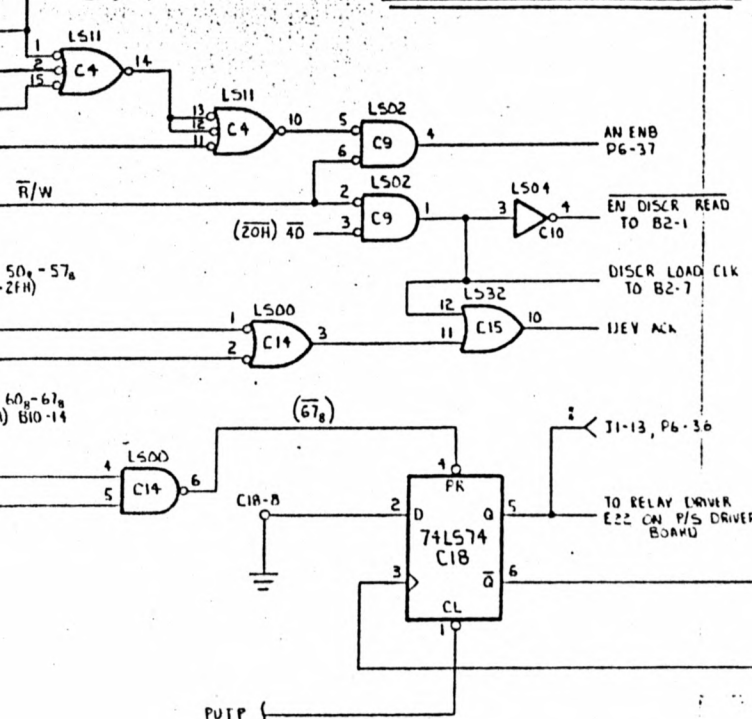
REV	DATE	BY	APP'D	DESCRIPTION
A				REV 30 3 8 1968



ADDR ASSIGNMENTS

30₈-37₈ - TEMP ANALOGS (18H-1FH)
 10₈-17₈ - EXT ANALOGS (0H-7H)
 20₈-27₈ - INT ANALOGS (5₈-15₈, 15₈-10₈, GND) (10H-17H)
 04₈, 05₈, 06₈, 07₈ - EXT ANALOGS
 40₈ - DISCR MON (20H)
 50₈-67₈ - DISCR CMDS (28H)

ADDR DECODE ENABLE LOGIC

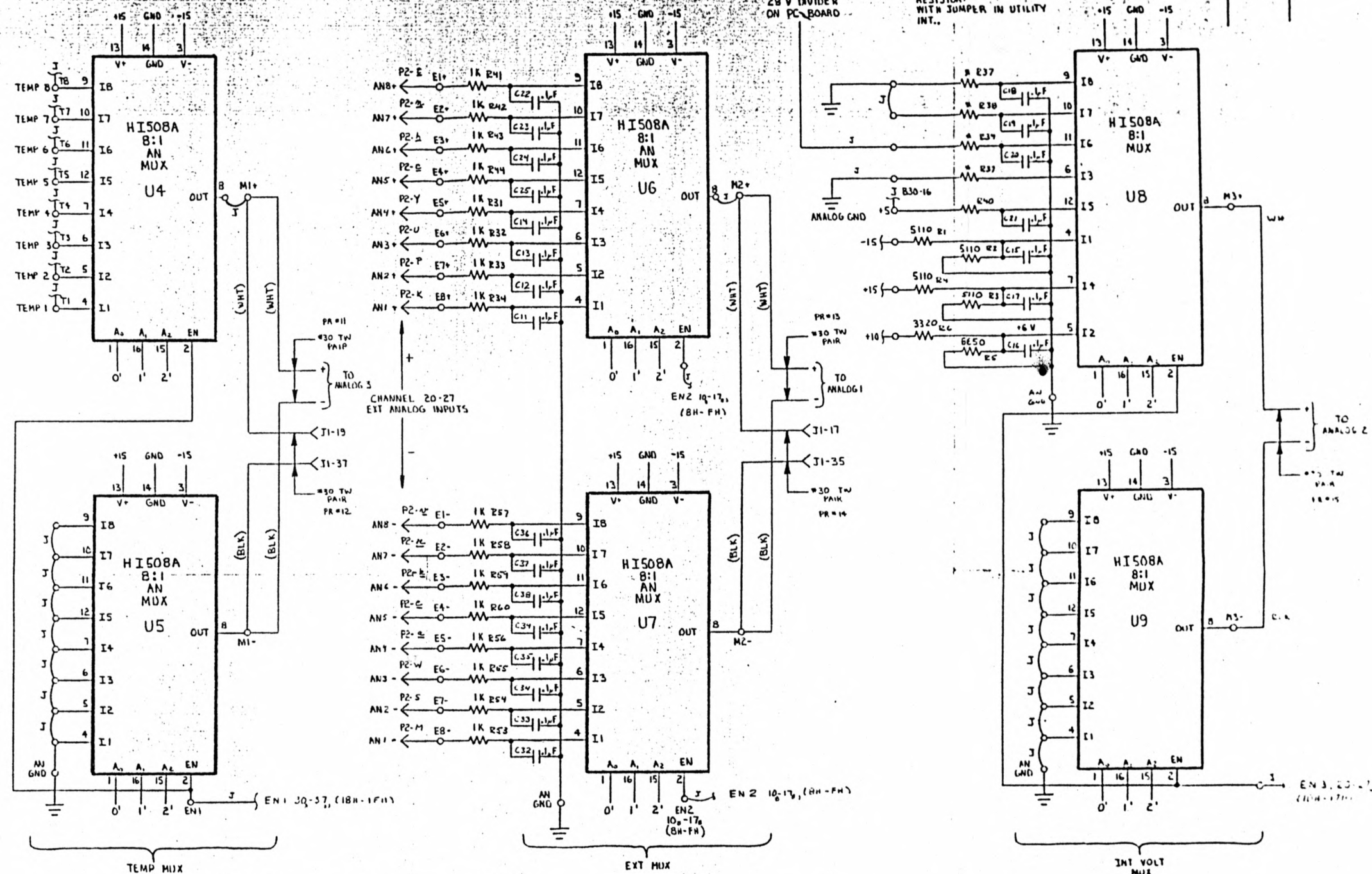
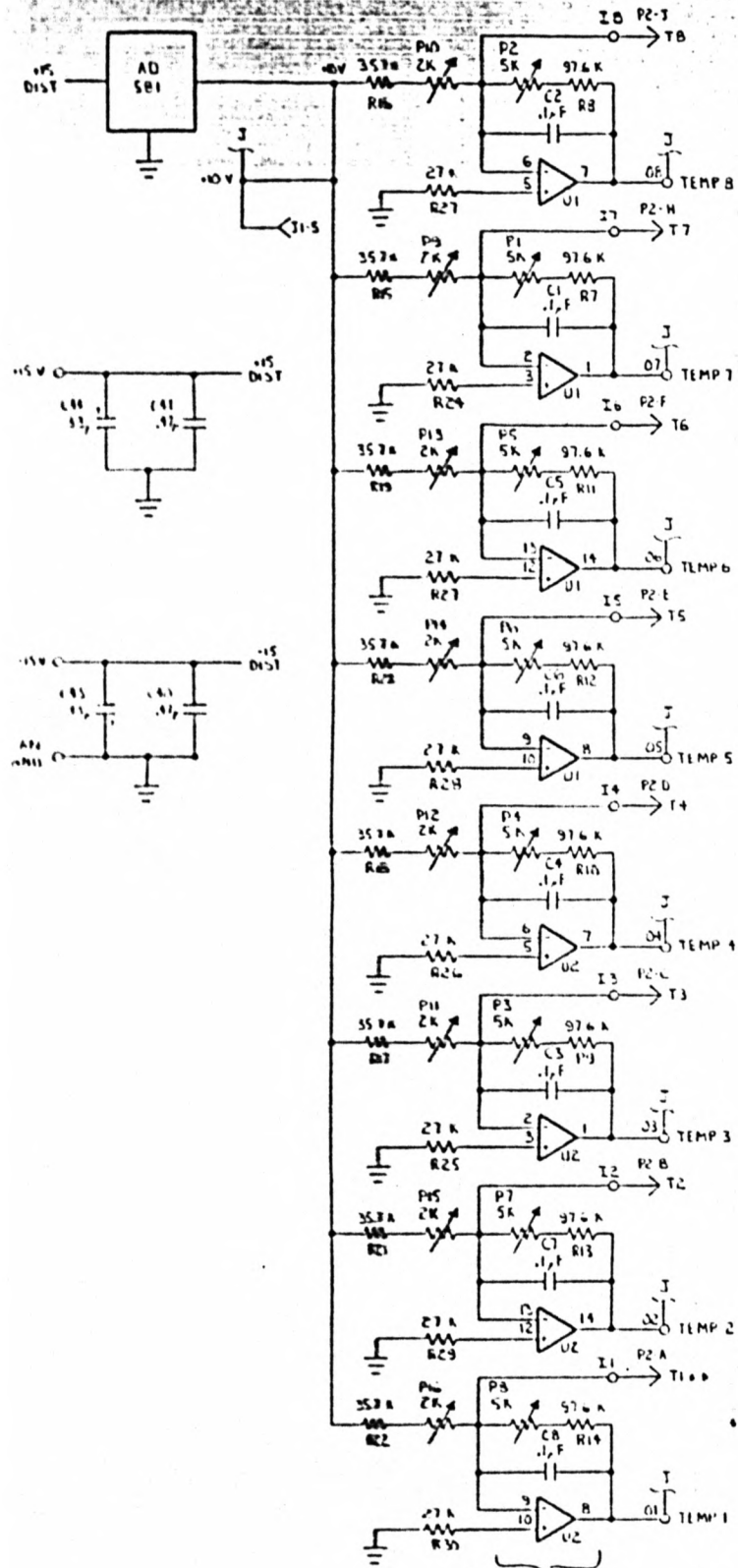


STD. INT. AND ADDRESS LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		V MIO3		NATIONAL RADIO ASTRONOMY OBSERVATORY	
TOLERANCES: ANGLES ±		B UTILITY INTERFACE		DATE 10-88	
3 PLACE DECIMALS: ±		A MIO3		BY ANBERTTA	
2 PLACE DECIMALS: ±		UTILITY INTERFACE MODULE SCHEMATIC		CHECKED BY WEFER	
1 PLACE DECIMALS: ±				APPROVED BY	
				DATE	
MATERIAL:				SHEET NUMBER 1 OF 4	
FINISH:				DRAWING NUMBER D550015005	
NEXT ASSY		USED ON		REV A	

CONTROL BLOC MIO3 ID = 42H ANTENNA MIO3 ID = 41H

AD590 TEMP PROBE INTERFACE



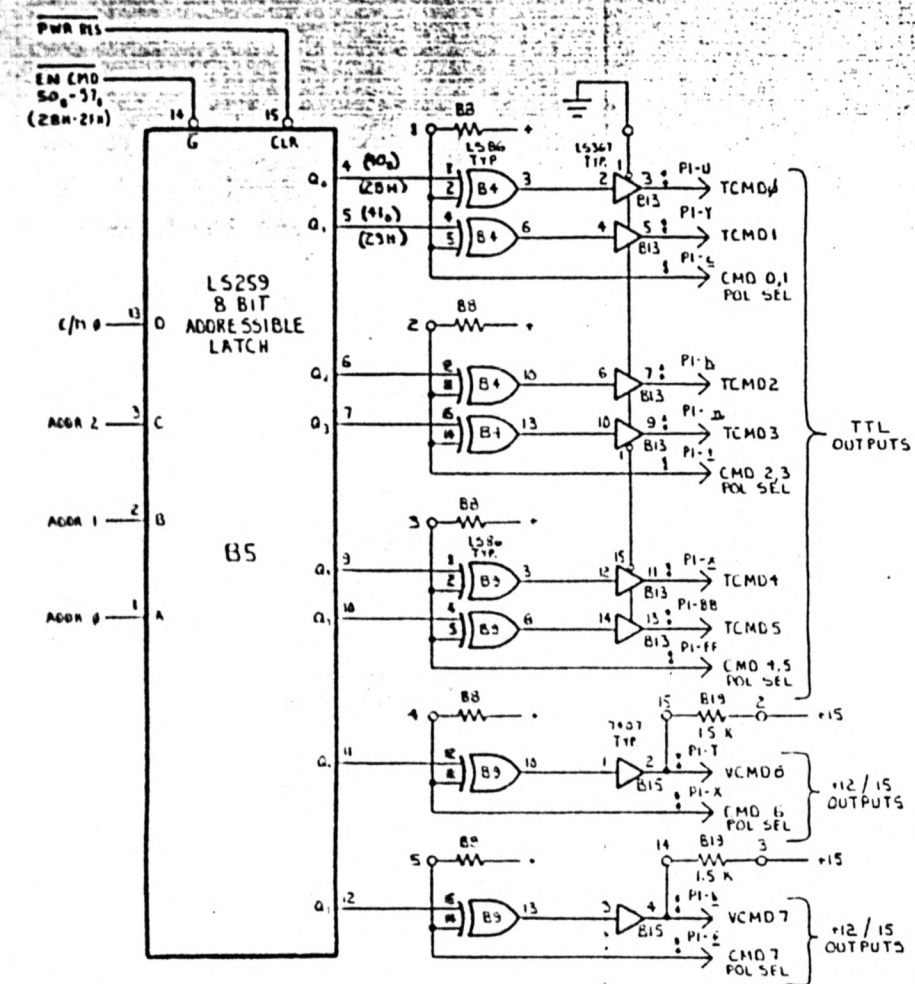
15V EXCITATION FOR AD590 TEMP PROBES IS DISTRIBUTED IN JUNCTION BOX.

- NOTES:
- ALL CIRCUITRY ON THIS SHEET IS IN LOG A, M103
 - WIRE WRAP PIN SYMBOL DENOTES A WIRE WRAP PIN; J DENOTES A WIRE WRAP WIRE JUMPER.
 - A₀ = A₀ DIST
A₁ = A₁ DIST
A₂ = A₂ DIST

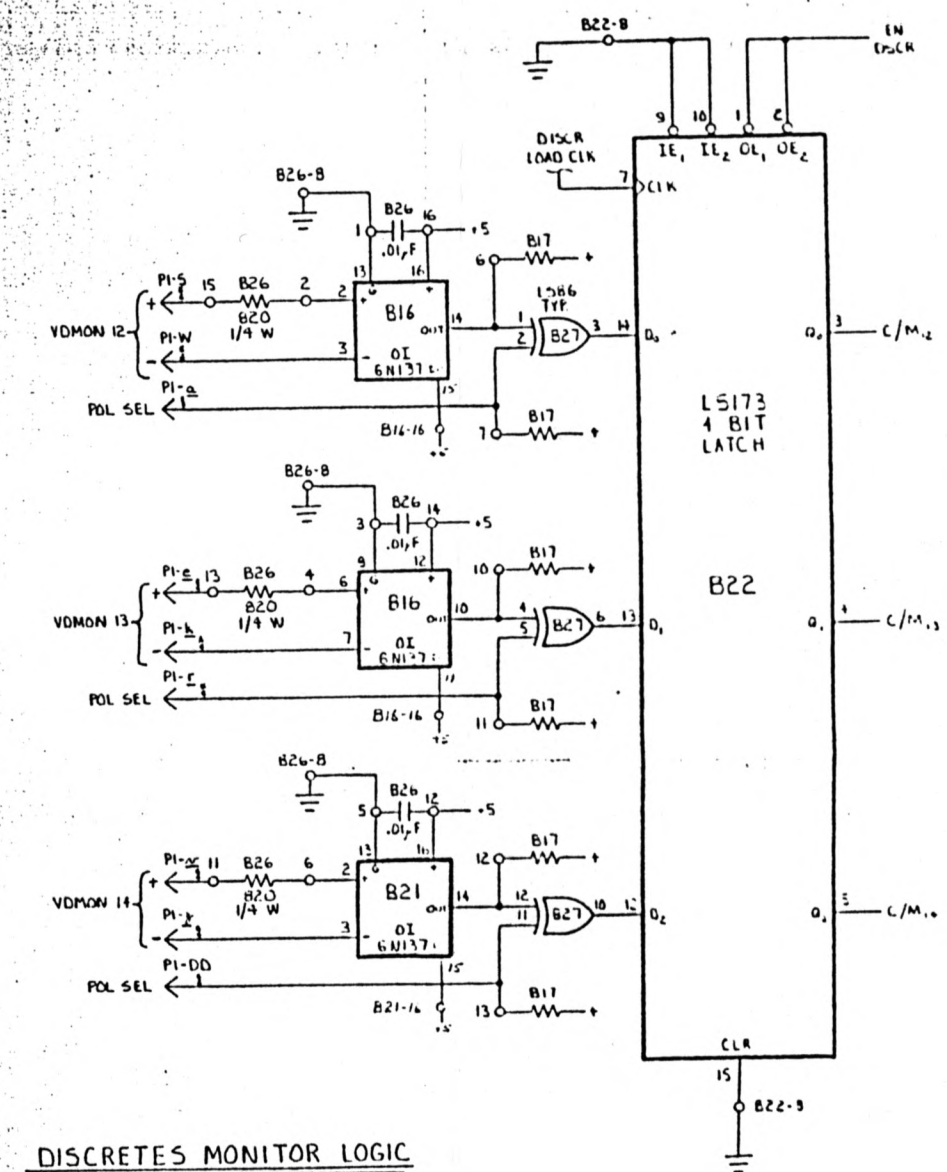
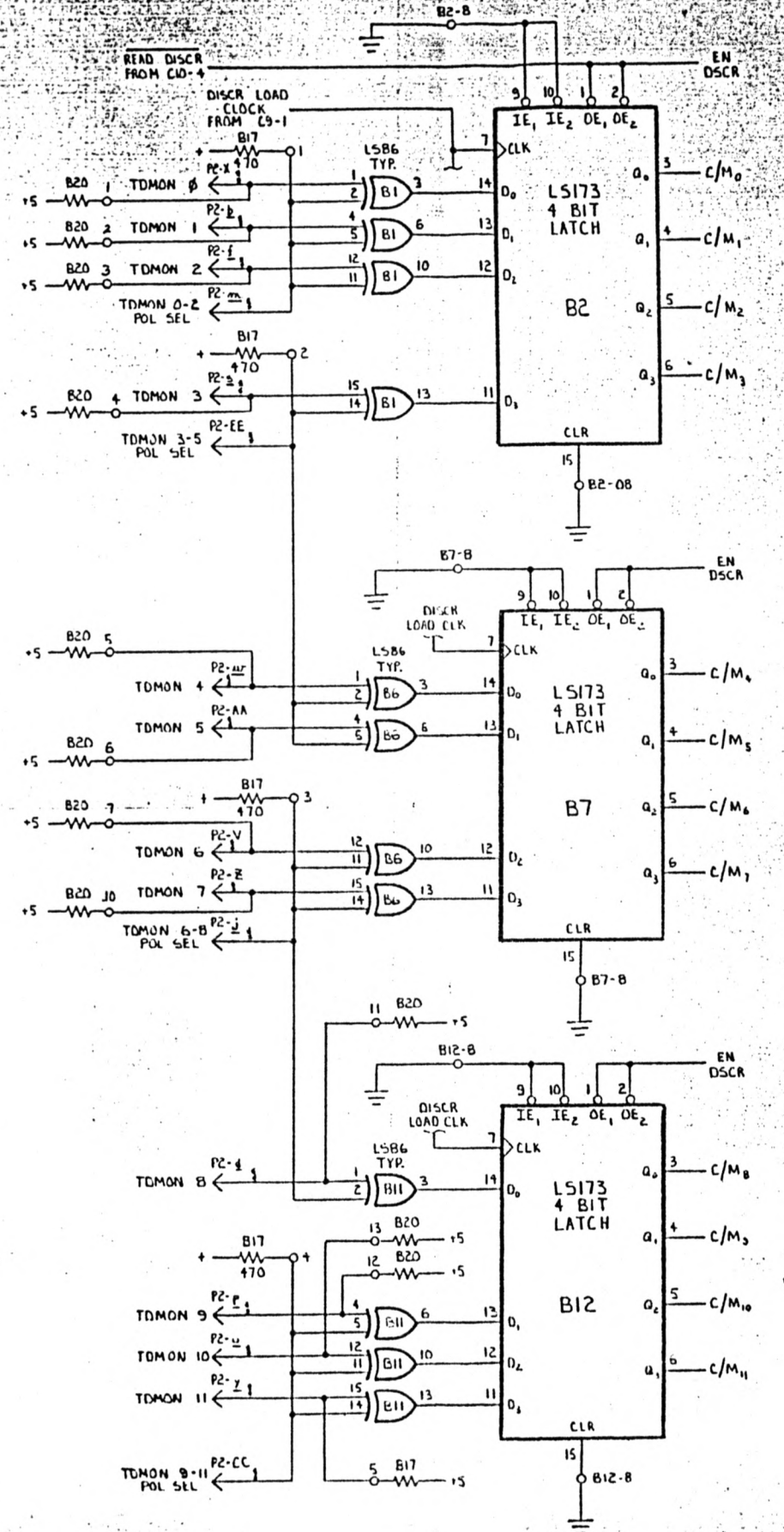
ANALOG CIRCUITRY BOARD

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		V M103		NATIONAL RADIO ASTRONOMY OBSERVATORY	
TOLERANCES: ANGLES ±	—	B UTILITY INTERFACE		DATE	10-87
1 PLACE DECIMALS: ±	—	A UTILITY INTERFACE		APPROVED BY	WELER
2 PLACE DECIMALS: ±	—	MODULE SCHEMATIC		DATE	10-87
3 PLACE DECIMALS: ±	—	MATERIAL:		SHEET	2 OF 9
4 PLACE DECIMALS: ±	—	FINISH:		DRAWING	055001-0005
NEXT ASSY		USED ON		REV	1

REV	DATE	DESIGNED BY	APPROVED BY	DESCRIPTION
A	1-88	WEEER		MINI-A REVISIONS



DISCRETES CMD REGISTER



DISCRETES MONITOR LOGIC

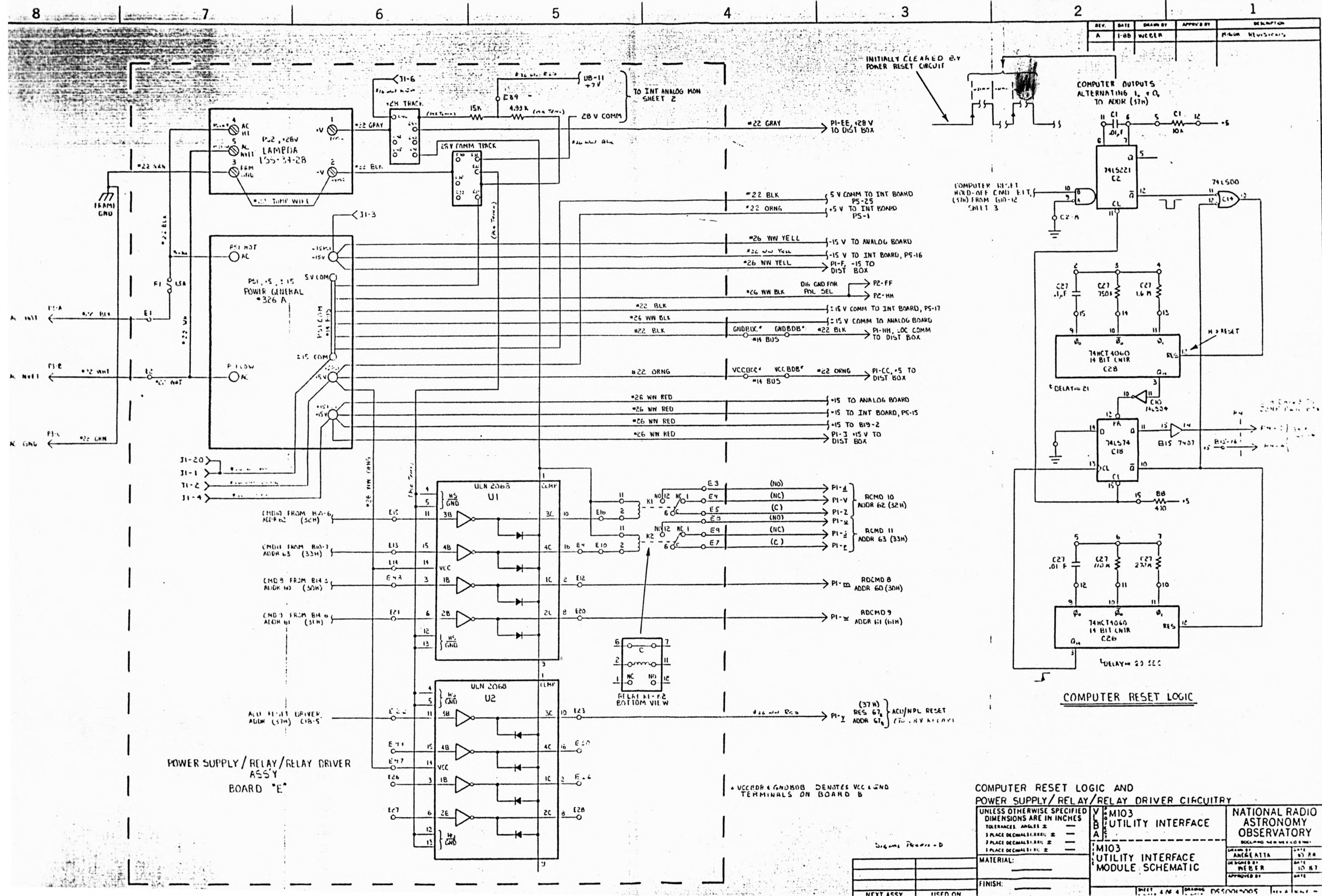
DISCRETE COMMAND AND MONITOR LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES: ± 1 PLACE DECIMALS: ± 2 PLACE DECIMALS: ± 3 PLACE DECIMALS: ±	MIO3 UTILITY INTERFACE MIO3 UTILITY INTERFACE MODULE SCHEMATIC	NATIONAL RADIO ASTRONOMY OBSERVATORY DESIGNED BY: ANDRE BTTA CHECKED BY: W. P. B. APPROVED BY: DATE:
MATERIAL: _____	FINISH: _____	SHEET 3 OF 4 DRAWING NO. D55001-2-005

Signal Profile - C

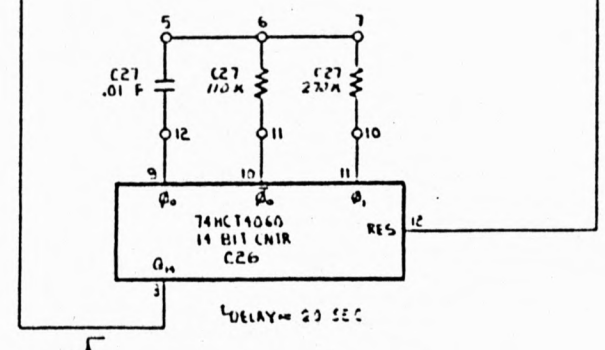
NEXT ASSY	USED ON

2, #26 W/W, RED



REV.	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	1-88	WEBER		POWER SUPPLY/RELAY/RELAY DRIVER ASSY BOARD 'E'

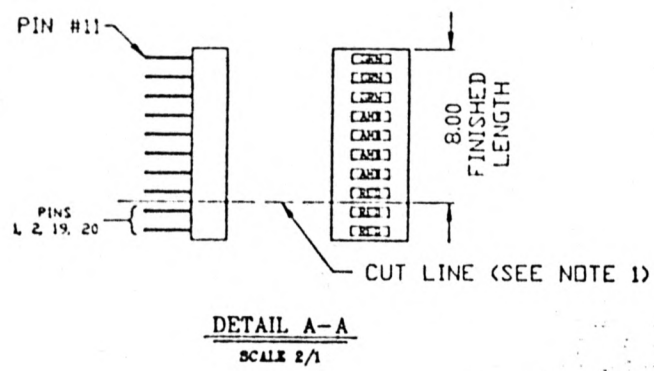
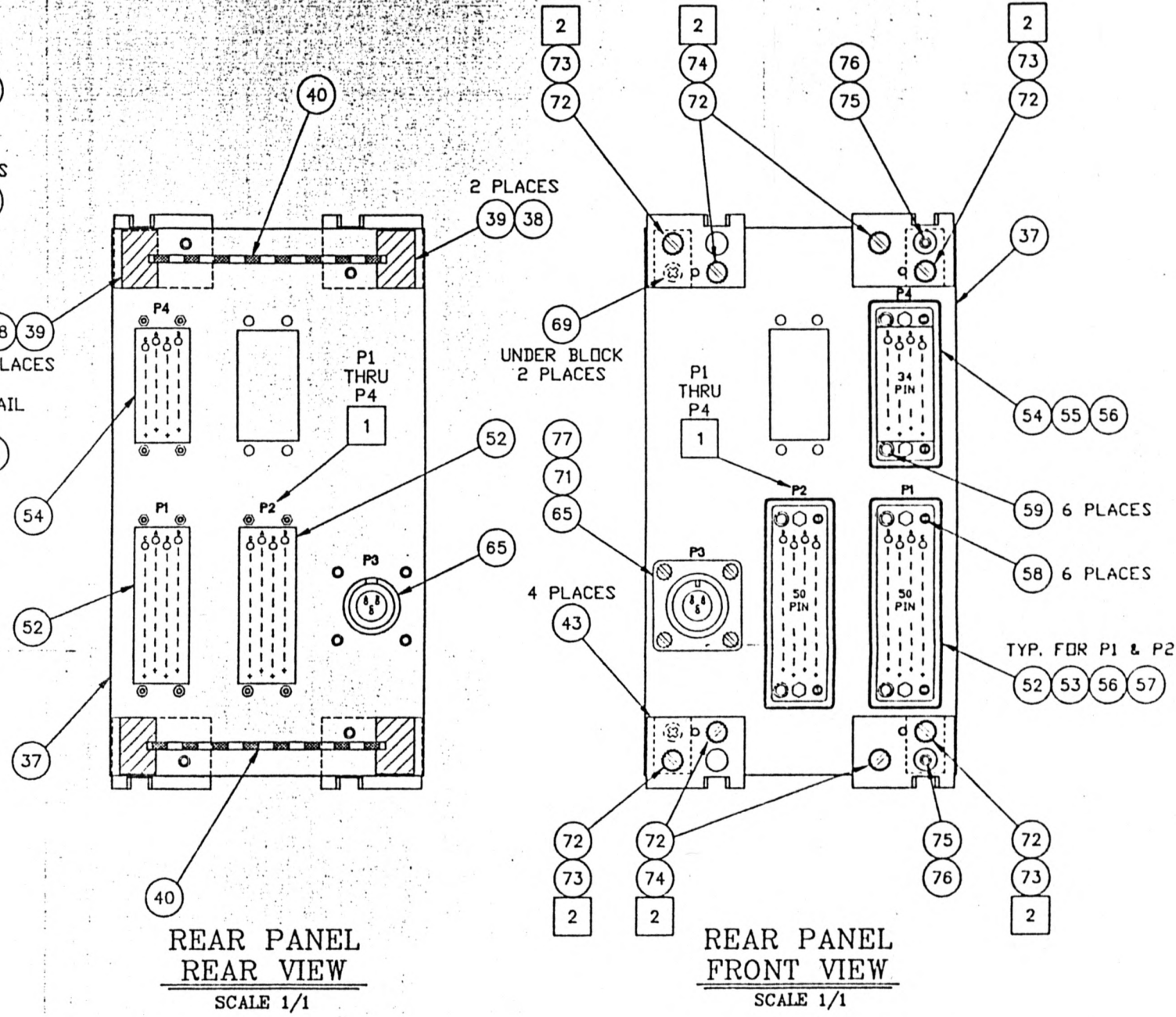
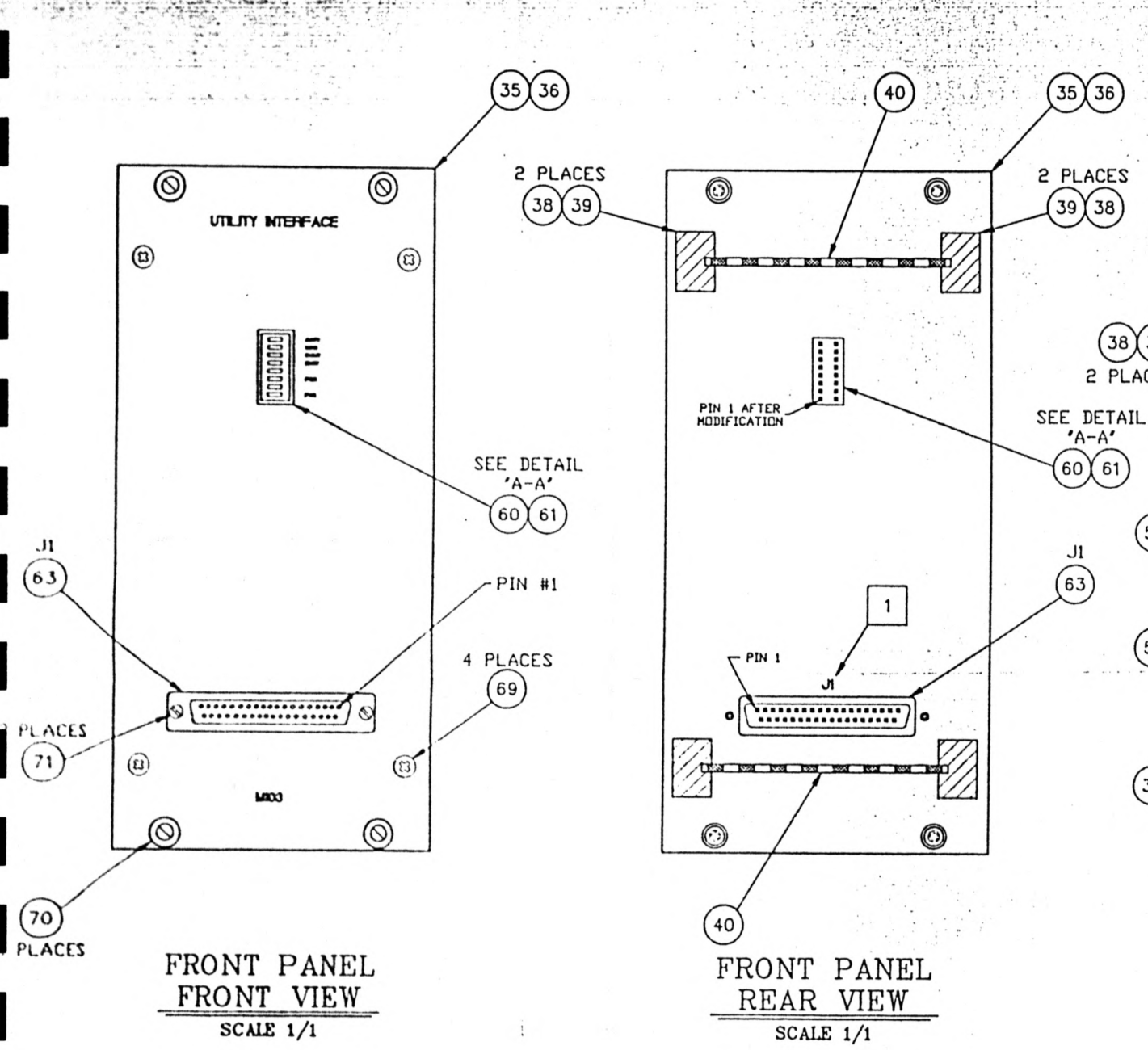
COMPUTER RESET LOGIC



COMPUTER RESET LOGIC AND POWER SUPPLY/RELAY/RELAY DRIVER CIRCUITRY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS: ± 2 PLACE DECIMALS: ± 1 PLACE DECIMALS: ±	MATERIAL:	FINISH:
NATIONAL RADIO ASTRONOMY OBSERVATORY Boulder, Colorado 80506 DRAWN BY: ANGELO DESIGNED BY: WEBER APPROVED BY: [Signature] DATE: 10-87		

DATE: 10-87	DATE: 10-87
DATE: 10-87	DATE: 10-87
DATE: 10-87	DATE: 10-87

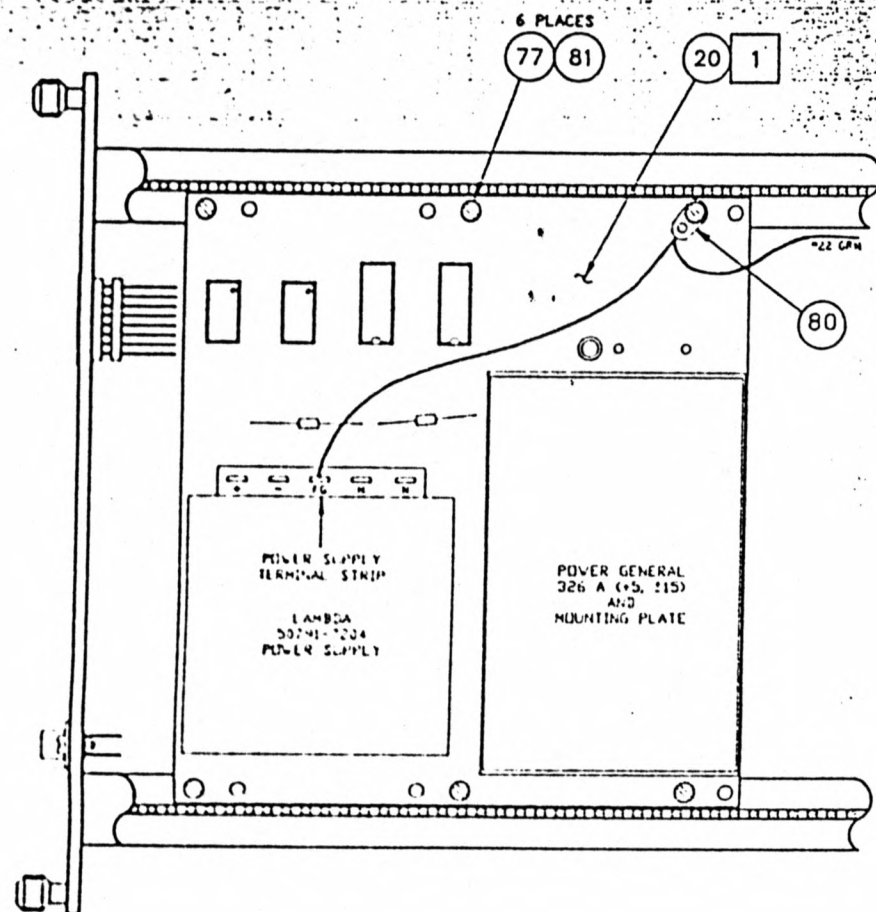


- NOTES:
- 1 MARKING SHALL BE .125 HIGH, LEDGIBLE, AND PERMANENT, LOCATED APPROXIMATELY AS SHOWN.
 - 2 WHERE TWO WASHERS (ITEM #72) ARE REQUIRED, PLACE ONE UNDER THE SCREW HEAD AND THE OTHER BETWEEN THE GUIDE BLOCK (ITEM #43) AND THE REAR PANEL.

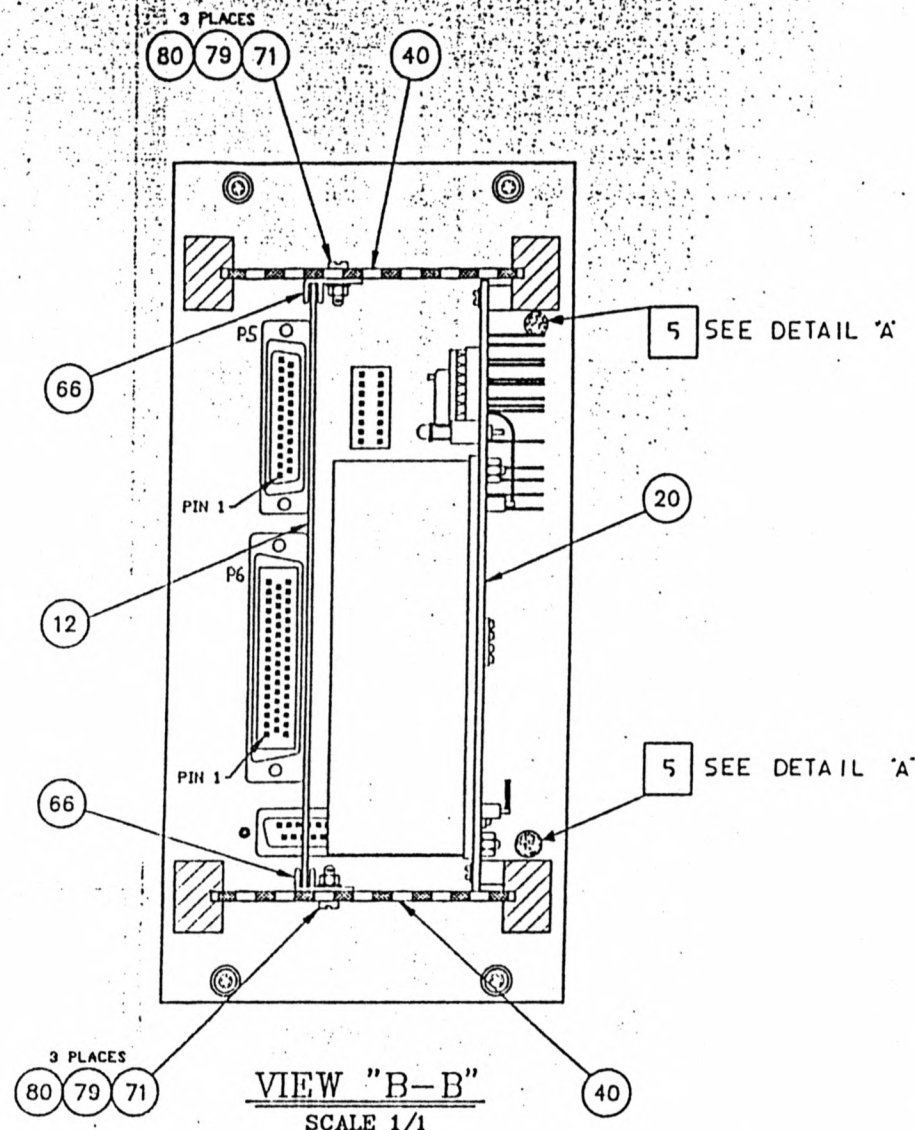
ACAD - M103ASY1

B.O.M.-A55001B004

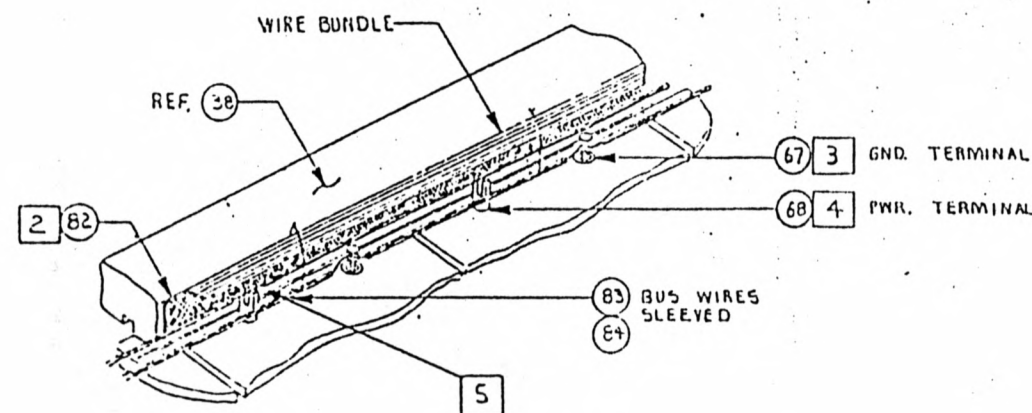
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS; HOLE: ± .005 2 PLACE DECIMALS; HOLE: ± 1 PLACE DECIMALS; HOLE: ±		Y B A M103 UTILITY INTERFACE		NATIONAL RADIO ASTRONOMY OBSERVATORY	
MATERIAL:		M103 UTILITY INTERFACE MODULE		DRAWN BY: ANDREA ATTA DATE: 12-27-27	
FINISH:		ASSEMBLY		DESIGNED BY: W. J. R. DATE: 12-27-27	
NEXT ASSY:		USED ON:		APPROVED BY: DATE:	
SHEET 1 OF 3		DRAWING NUMBER: 055001A010		REV: 1	



VIEW "A-A"
SCALE 1/1



VIEW "B-B"
SCALE 1/1



DETAIL "A"
NO SCALE

NOTES :

- 1 SEE DWG. #C55001A011 FOR LOCATIONS AND DESIGNATIONS OF TERMINALS TO BE WIRED.
- 2 KAPTON TAPE (ITEM #82) SHALL RUN FULL LENGTH OF TOP AND BOTTOM RAILS ON BOARD MOUNTING SIDE OF MODULE.
- 3 SOLDER GND TERMINAL (ITEM #67) TO LOGIC CONNECTOR BOARD GND PLANE.
- 4 SOLDER POWER TERMINAL (ITEM #68) TO LOGIC CONNECTOR BOARD VCC PLANE.
- 5 POWER AND LOGIC WIRING SHALL BE ON THE WIRE WRAP SIDE OF ITEMS #20, #24, AND #43.

B.O.M. - *A55001B004

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMAL: DIA. ± .005 3 PLACE DECIMAL: DIA. ± 3 PLACE DECIMAL: DIA. ±	V MIO3 B UTILITY A INTERFACE	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL:	MIO3 UTILITY INTERFACE MODULE ASSEMBLY	DATE: 12-84 BY: J. B. J.
FINISH:		DATE: 12-84 BY: J. B. J.
NEXT ASSY	USED ON	DATE: 12-84 BY: J. B. J.

BIN WIRE LIST,
UTILITY
CONTROL-MONITOR
SYSTEM

A55001W005

COVER SHEET	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST	PAGE 1 OF 42

WIRE LIST DESCRIPTION

THIS WIRE LIST DEFINES THE BIN WIRING FOR THE VLBA UTILITY CONTROL-MONITOR SYSTEM. THE DATA IN THIS WIRE LIST IS A DERIVATIVE OF DRAWING A55001W005. THE FIRST PART OF THE WIRE LIST CONSISTS OF A BIN BACK PANEL CONNECTOR LAYOUT DIAGRAM TO SHOW CONNECTOR PLACEMENT AND THE ASSOCIATED SIGNAL SETS. FOLLOWING THIS LAYOUT ARE MODULE PINOUT SCHEMATICS WHICH SHOW CONNECTOR LOCATIONS, CONTACT PATTERNS AND SIGNAL ASSIGNMENTS.

TWO UTILITY CONTROL-MONITOR SYSTEMS ARE USED AT THE VLBA ANTENNA SITES: ONE SYSTEM IS INSTALLED IN THE STATION BUILDING AND SERVICES STATION BUILDING DEVICES; THE SECOND SYSTEM IS INSTALLED IN THE ANTENNA PEDESTAL ROOM AND SERVICES ANTENNA DEVICES.

THE BULK OF THE WIRING IS COMMON TO THE TWO APPLICATIONS BUT THERE ARE A FEW SMALL APPLICATION-DEPENDENT DIFFERENCES BETWEEN THE TWO SYSTEMS. TO SIMPLIFY THE BIN WIRE LIST, THE WIRING DATA IS PARTITIONED INTO FOUR SECTIONS; THE FIRST SECTION IS COMMON TO BOTH APPLICATIONS AND THE FOLLOWING THREE DEFINE THE APPLICATION-DEPENDENT DIFFERENCES. THESE THREE ARE USED AS REQUIRED FOR BIN CONSTRUCTION AND MAINTENANCE-CHECKOUT. THE SECTIONS ARE IDENTIFIED IN THE FOOTER OF EACH WIRE LIST SHEET.

UNIQUE ELEMENTS ARE WIRING THAT IS PARTICULARIZED FOR DISCRETES POLARITY SELECTION, DEVICE ID CODING AND MCB SIGNAL WIRING. A SECOND UNIQUE ELEMENT IS THE WIRING FOR THE M101 INCLINOMETER-TEMPERATURE SENSOR INTERFACE WHICH IS USED IN THE PEDESTAL ROOM SYSTEM. SINCE ANTENNA INCLINOMETERS ARE EXPERIMENTAL DEVICES WHICH MAY NOT BE USED ON ALL VLBA ANTENNAS, THE M101 BIN WIRING IS A SEPARATE SECTION WHICH MAY BE OMITTED IN THE EVENT THAT INCLINOMETERS ARE NOT USED.

SECTION 1 IS WIRING COMMON TO THE TWO SYSTEM APPLICATIONS.

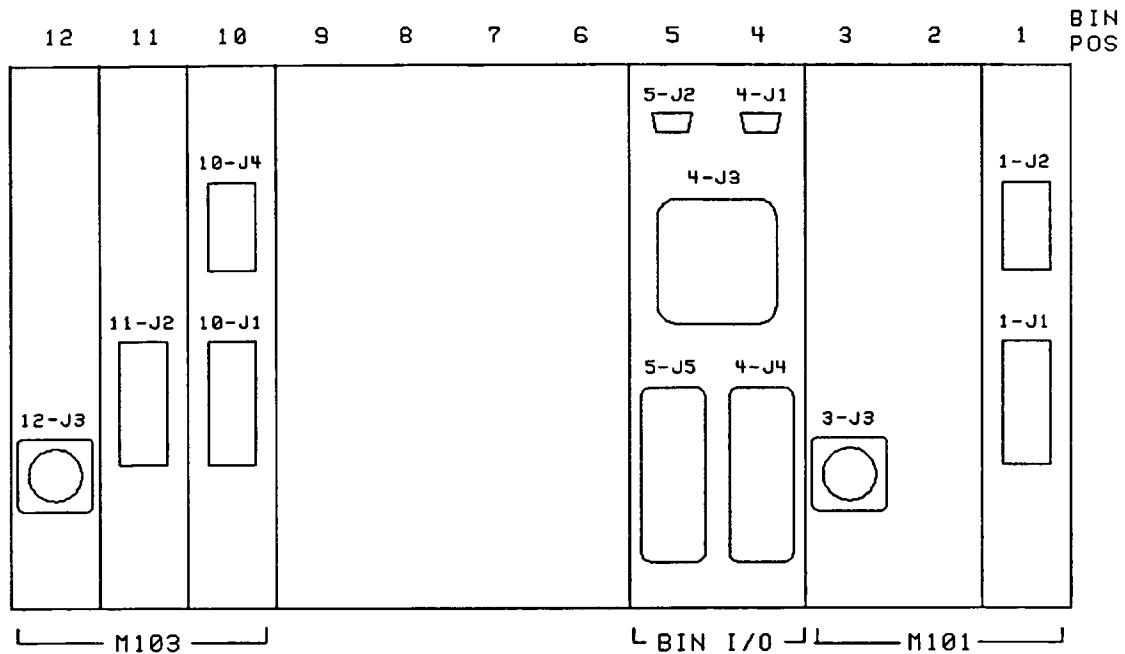
SECTION 2 DEFINES THE WIRING PECULIAR TO THE ANTENNA PEDESTAL ROOM APPLICATION.

SECTION 3 DEFINES THE WIRING PECULIAR TO THE STATION BUILDING APPLICATION.

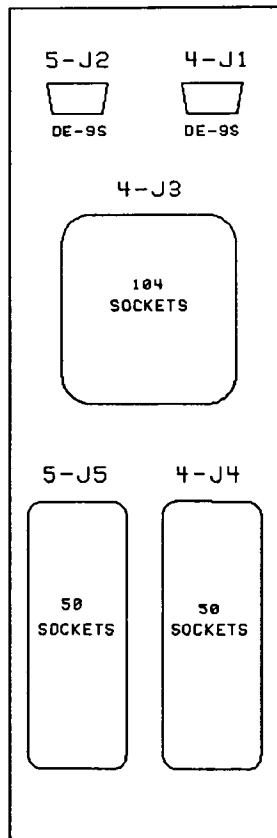
SECTION 4 DEFINES THE M101 WIRING.

WIRE LIST DESCRIPTION	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST	PAGE 2 OF 42

BIN REAR VIEW

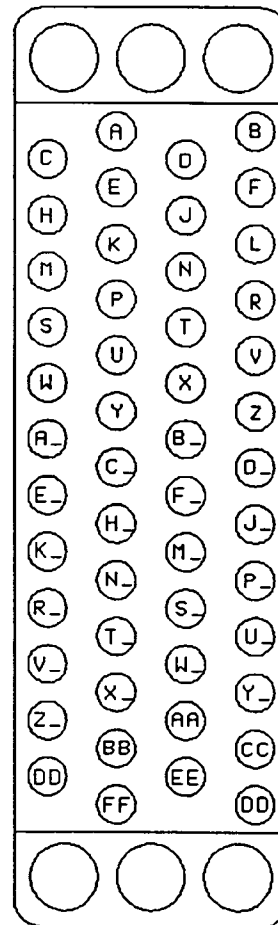


CONNECTOR	MODULE	FUNCTION
1-J1	M101	ANTENNA & INCLINOMETER TEMP SIGNALS
1-J2	M101	INCLINOMETER SIGNALS, MCB SIGNALS & DEVICE ID
3-J3	M101	M101 110 VAC POWER
10-J1	M103	CMD5: TTL, VOLTAGE, RELAY, RELAY DRIVE, RESET, CMD POL SEL. MON: VOLTAGE, DEV ID, MCB SIGNALS
11-J2	M103	MON: TEMP SIGNALS, TTL, ANALOG, MON POL SEL
10-J4	M103	COMPUTER RESET SSR DRIVE
12-J3	M103	M103 110 VAC POWER
4-J1	BIN I/O	MCB INPUT
5-J2	BIN I/O	MCB OUTPUT
4-J3	BIN I/O	ANT & INCL TEMP SIGNALS, INCLINOMETER SIGNALS
4-J4	BIN I/O	CMD5: TTL, VOLTAGE, RELAY, RELAY DRIVE, RESET MON: VOLTAGE
5-J5	BIN I/O	MON: TEMP SIGNALS, TTL, ANALOG



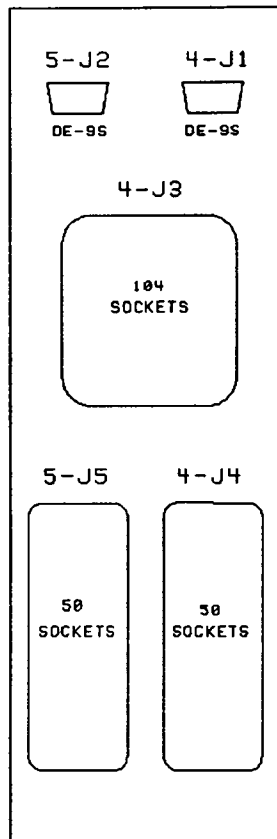
BIN I/O PANEL

NOTE: X_ DESIGNATES LOWER CASE X, ETC

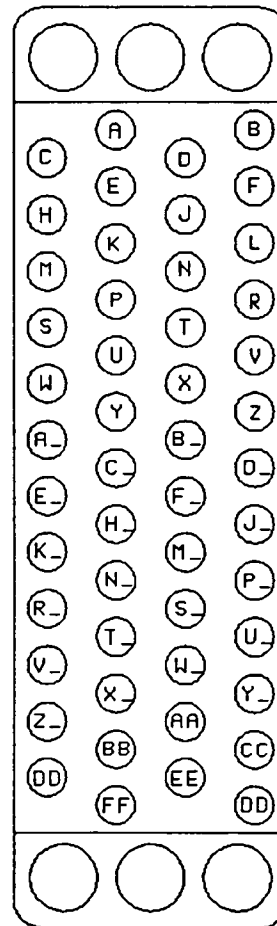


4-J4, MATING VIEW

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A		S	VDMON12+	H_	TCMD2	Z_	VDMON14-
B		T	VCMD6	J_	RCMD11-NC	AA	
C		U	TCMD0	K_	VDMON13-	BB	TCMD5
D		V	RCMD10-NC	M_	RDCMD8	CC	+5 TO DIST BOX
E		W	VDMON12-	N_	TCMD3	DD	
F	-15 TO DIST BOX	X		P_	RCMD11-COMM	EE	+28 TO DIST BOX
H		Y	TCMD1	R_		FF	
J	+15 TO DIST BOX	Z	RCMD10 COMM	S_		HH	COMM TO D-BOX
K		A_		T_			
L		B_	VCMD7	U_	RCMD11-NO		
M		C_		V_	VDMON14+		
N		D_	RCMD10-NO	W_	RCMD9		
P		E_	VDMON13+	X_	TCMD4		
R		F_		Y_	RES67 (ACU)		
BIN I/O, 4-J4 PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 4 OF 42	



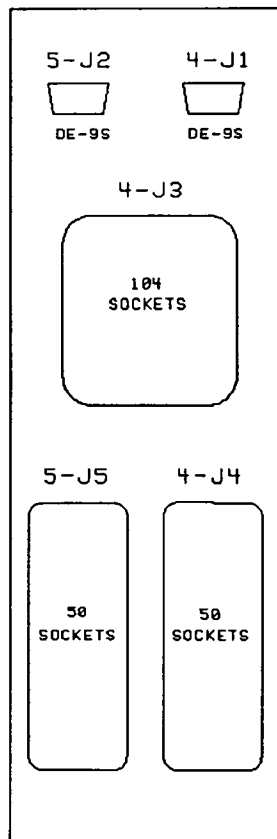
BIN I/O PANEL



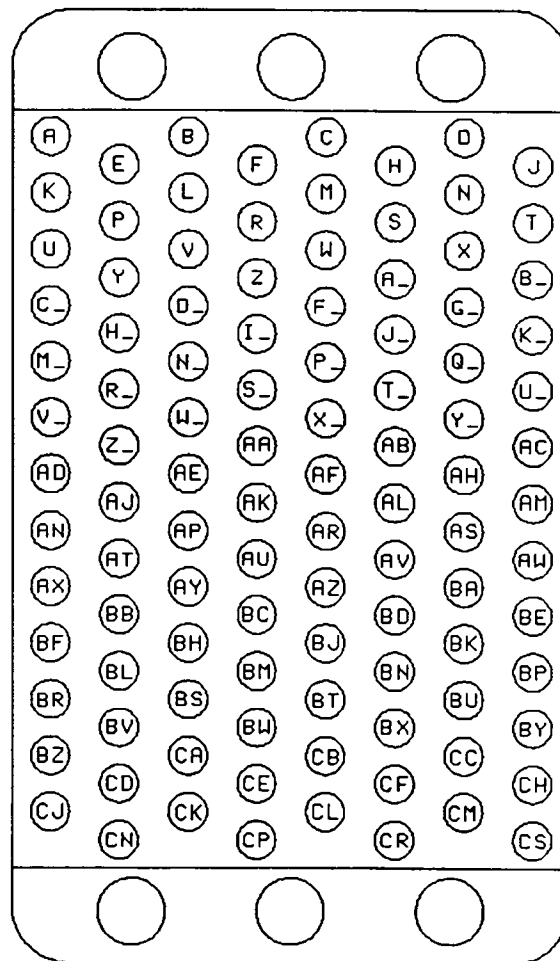
5-J5, MATING VIEW

NOTE: X₋ DESIGNATES LOWER CASE X, ETC

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	TEMP1	S	AN2-	H ₋	AN6+	Z ₋	AN9-
B	TEMP2	T	AN12-	J ₋		AA	TDMON5
C	TEMP3	U	AN3+	K ₋	AN6-	BB	AN10+
D	TEMP4	V	TDMON6	M ₋		CC	
E	TEMP5	W	AN3-	N ₋	AN7+	DD	AN10-
F	TEMP6	X	TDMON0	P ₋	TDMON9	EE	
H	TEMP7	Y	AN4+	R ₋	AN7-	FF	
J	TEMP8	Z	TDMON7	S ₋	TDMON3	HH	
K	AN1+	A ₋	AN4-	T ₋	AN8+		
L	AN11+	B ₋	TDMON1	U ₋	TDMON10		
M	AN1-	C ₋	AN5+	V ₋	AN8-		
N	AN11-	D ₋	TDMON8	W ₋	TDMON4		
P	AN2+	E ₋	AN5-	X ₋	AN9+		
R	AN12+	F ₋	TDMON2	Y ₋	TDMON11		
BIN I/O, 5-J5 PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 5 OF 42	



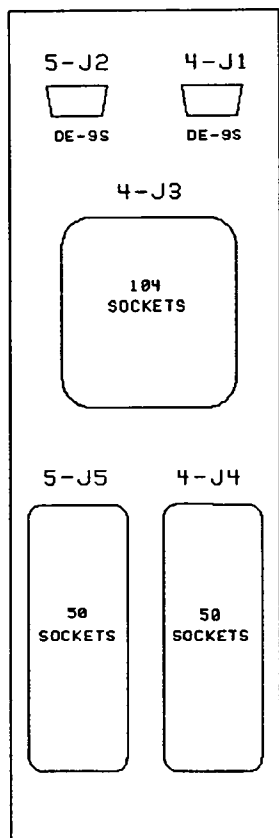
BIN I/O PANEL



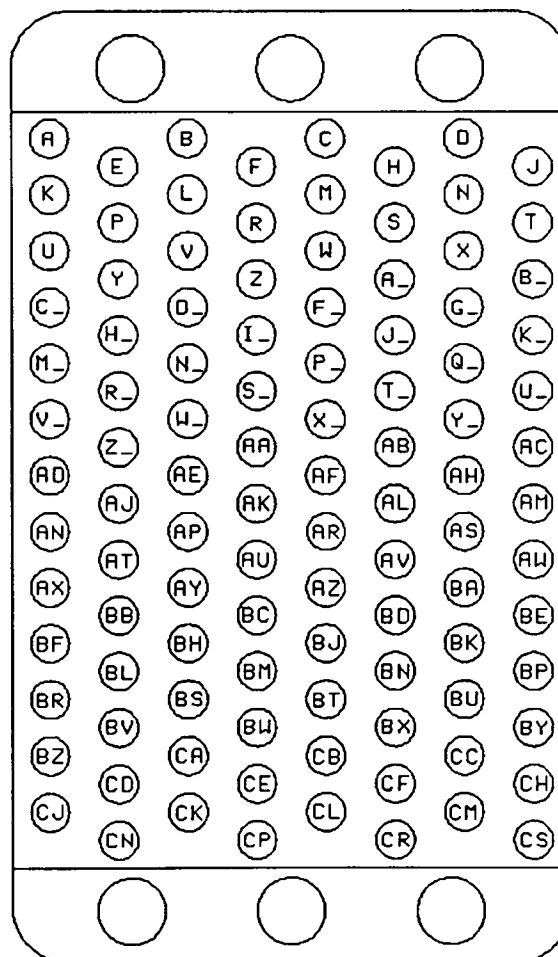
4-J3 MATING VIEW

NOTE: X₋ DESIGNATES LOWER CASE X, ETC

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	TEMP 1-S	S		H ₋		X ₋	
B	TEMP 14-S	T	+ - 15 COMM	I ₋		Y ₋	
C		U	TEMP 3-S	J ₋		Z ₋	
D	+15 TO INCL	V	TEMP 16-S	K ₋	EPARE (IN1-)	AA	
E	-15 TEMP EXC	W		M ₋	TEMP 5-S	AB	
F		X		N ₋		AC	
H		Y		P ₋		AD	TEMP 7-S
J		Z		Q ₋	ENORME (IN4+)	AE	TEMP 20-S
K	TEMP 2-S	A ₋		R ₋		AF	
L	TEMP 15-S	B ₋		S ₋	-15 TEMP EXC	AH	WPARE (IN2+)
M		C ₋	TEMP 4-S	T ₋		AJ	
N	-15 TO INCL	D ₋	TEMP 17-S	U ₋	ENORME (IN4-)	AK	
P		F ₋		V ₋	TEMP 6-S	AL	
R		G ₋	EPARE (IN1+)	W ₋	TEMP 19-S	AM	WPARE (IN2-)
BIN I/O, 4-J3 PINOUT						DATE 4-89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 6 OF 42	



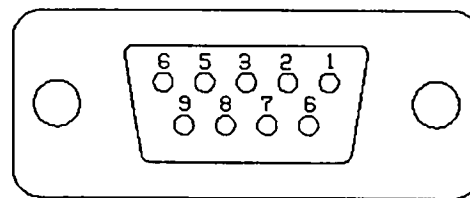
BIN I/O PANEL



4-J3 MATING VIEW

NOTE: X_ DESIGNATES LOWER CASE X, ETC

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
AN	TEMP 8-S	BD		BV		CL	
AP	TEMP 21-S	BE		BW		CM	
AR		BF	TEMP 10-S	BX		CN	
AS	WNORME (IN5+)	BH	TEMP 23-S	BY	ANORME (IN6-)	CP	
AT		BJ		BZ	TEMP 12-S	CR	
AU		BK	APARE (IN3+)	CA		CS	
AV		BL		CB			
AW	WNORME (IN5-)	BM		CC			
AX	TEMP 9-S	BN		CD			
AY	TEMP 22-S	BP	APARE (IN3-)	CE			
AZ		BR	TEMP 11-S	CF			
BA		BS	TEMP 24-S	CH			
BB		BT		CJ	TEMP 13-S		
BC		BU	ANORME (IN6+)	CK			
BIN I/O, 4-J3 PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 7 OF 42	



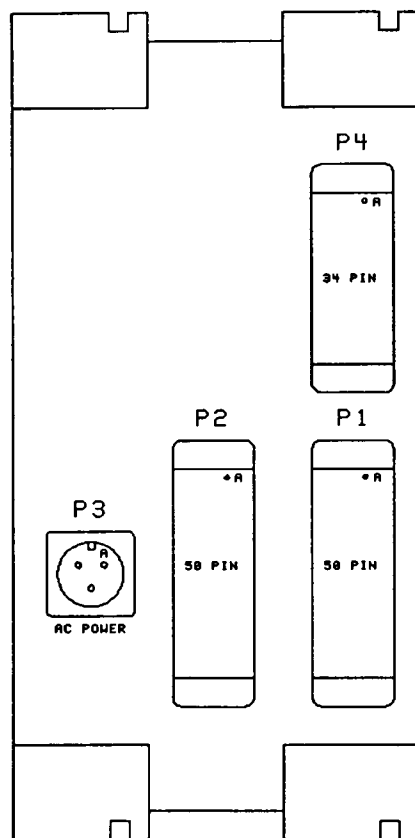
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4-J1  -- MCB INPUT
5-J2  -- MCB OUTPUT

```

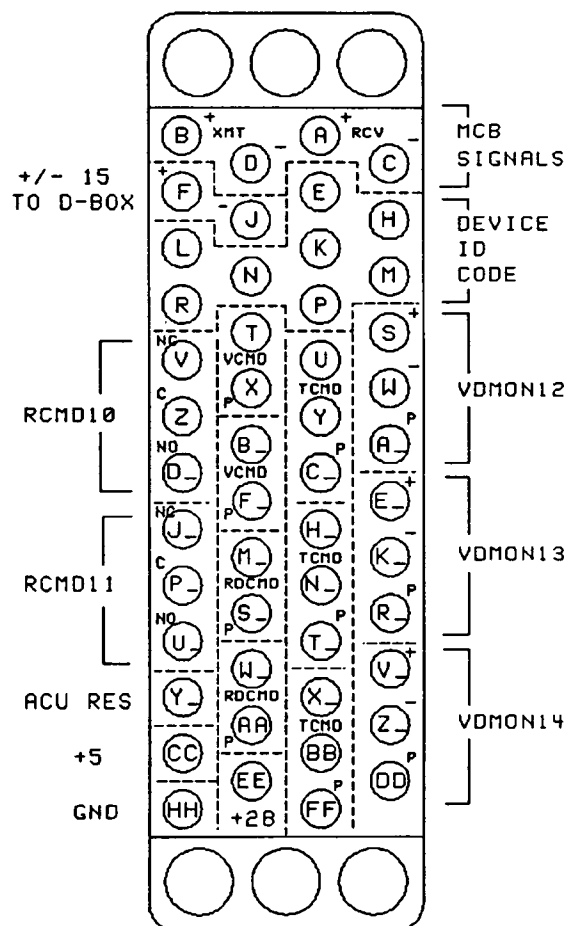
BIN I/O PANEL

PIN	FUNCTION					
1	XMT+					
2	XMT-					
3						
4						
5	SHIELDS (2 PR)					
6						
7						
8	RCV+					
9	RCV-					
BIN I/O, 4-J1 & 5-J2 PINOUTS						DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 8 OF 42



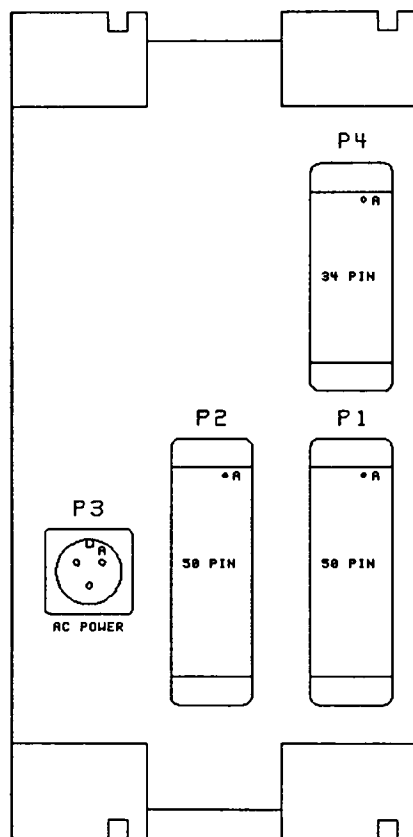
MODULE REAR VIEW

NOTE: PINS WITH _ SUFFIX ARE LOWER CASE



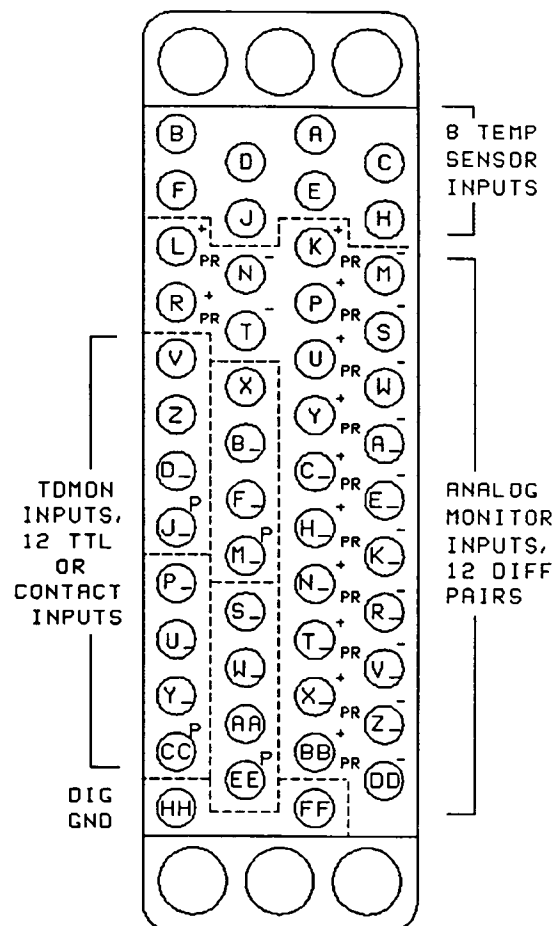
P1 PIN LAYOUT

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	RCV+	S	VDMON12+	H ₋	TCMD2	Z ₋	VDMON14-
B	XMT+	T	VCMD6	J ₋	RCMD11-NC	AA	RDCMD9 POL SEL
C	RCV-	U	TCMD0	K ₋	VDMON13-	BB	TCMD5
D	XMT-	V	RCMD10-NC	M ₋	RDCMD8	CC	+5 TO DIST BOX
E	DID 0	W	VDMON12-	N ₋	TCMD3	DD	VDMON14 POL SEL
F	-15 TO DIST BOX	X	VCMD6 POL SEL	P ₋	RCMD11-COMM	EE	+28 TO DIST BOX
H	DID 1	Y	TCMD1	R ₋	VDMON13 POL SEL	FF	TCMD4,5 POL SEL
J	+15 TO DIST BOX	Z	RCMD10-COMM	S ₋	RDCMD8 POL SEL	HH	COMM TO D-BOX
K	DID 2	A ₋	VDMON12 POL SEL	T ₋	TCMD2,3 POL SEL		
L	DID 3	B ₋	VCMD7	U ₋	RCMD11-NO		
M	DID 4	C ₋	TCMD0,1 POL SEL	V ₋	VDMON14+		
N	DID 5	D ₋	RCMD10-NO	W ₋	RDCMD9		
P	DID 6	E ₋	VDMON13+	X ₋	TCMD4		
R	DID 7	F ₋	VCMD7 POL SEL	Y ₋	ACU RESET DRV		
M103 P1 SIGNAL PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 9 OF 42	



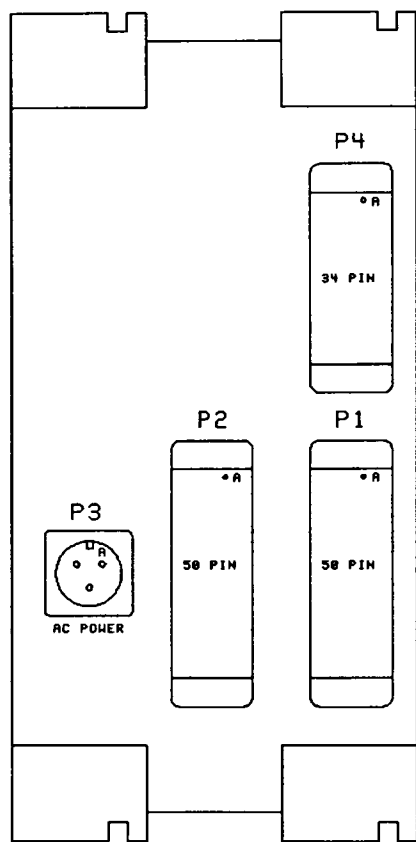
MODULE REAR VIEW

NOTE: PINS WITH _ SUFFIX ARE LOWER CASE

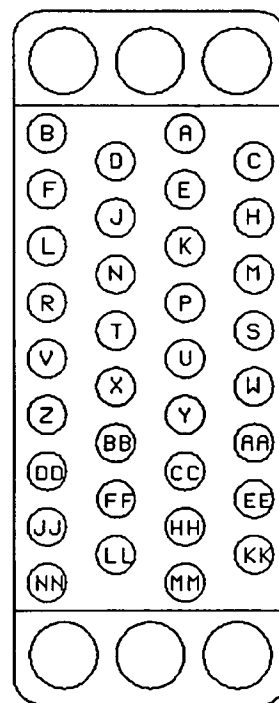


P2 PIN LAYOUT

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	TEMP1	S	AN2_	H_	AN6+	Z_	AN9-
B	TEMP2	T	AN12-	J_	TDMON6-8 P-SEL	AA	TDMON5
C	TEMP3	U	AN3+	K_	AN6-	BB	AN10+
D	TEMP4	V	TDMON6	M_	TDMON0-2 P-SEL	CC	TDMON9-11 P-SEL
E	TEMP5	W	AN3-	N_	AN7+	DD	AN10-
F	TEMP6	X	TDMON0	P_	TDMON9	EE	TDMON3-5 P-SEL
H	TEMP7	Y	AN4+	R_	AN7-	FF	DIG GND, P-SEL
J	TEMP8	Z	TDMON7	S_	TDMON3	HH	DIG GND, P-SEL
K	AN1+	A_	AN4-	T_	AN8+		
L	AN11+	B_	TDMON1	U_	TDMON10		
M	AN1-	C_	AN5+	V_	AN8-		
N	AN11-	D_	TDMON8	W_	TDMON4		
P	AN2+	E_	AN5-	X_	AN9+		
R	AN12+	F_	TDMON2	Y_	TDMON11		
M103 P2 SIGNAL PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 10 OF 42	

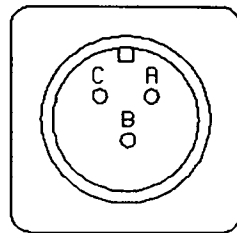


MODULE REAR VIEW



P4 PIN LAYOUT

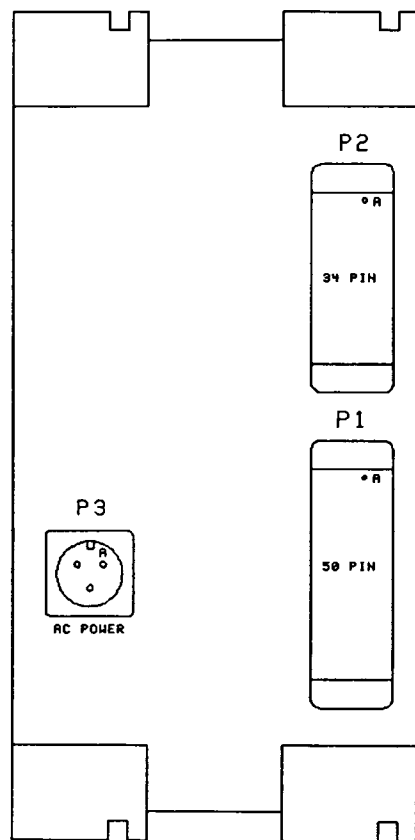
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	+5, CMP RES BOX	S		HH			
B		T		JJ			
C	CMP RES SSR DRV	U		KK			
D		V		LL			
E		W		MM			
F		X		NN			
H		Y					
J		Z					
K		AA					
L		BB					
M		CC					
N		DD					
P		EE					
R		FF					
M103 P4 SIGNAL PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 11 OF 42	

[illegible]

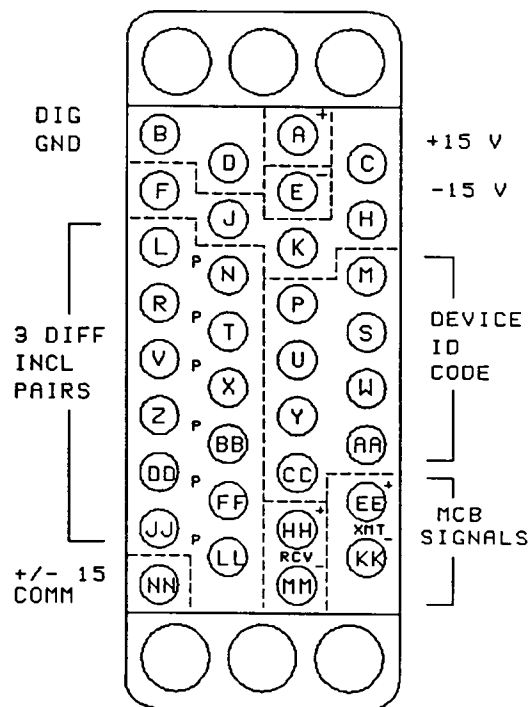


NOTE: PINS WITH _ SUFFIX ARE LOWER CASE

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	TEMP13	S		H_	TEMP20	Z_	
B	TEMP1	T		J_	TEMP8	AA	
C		U		K_		BB	TEMP24
D	-15 EXC	V	TEMP17	M_		CC	TEMP12
E	TEMP14	W	TEMP5	N_		DD	
F	TEMP2	X		P_	TEMP9	EE	
H		Y	TEMP18	R_		FF	
J		Z	TEMP6	S_		HH	
K	TEMP15	A_	-15 EXC	T_	TEMP22		
L	TEMP3	B_		U_	TEMP10		
M		C_	TEMP19	V_			
N		D_	TEMP7	W_			
P	TEMP16	E_		X_	TEMP23		
R	TEMP4	F_		Y_	TEMP11		
M101 P1 SIGNAL PINOUT							DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST							PAGE 13 OF 42

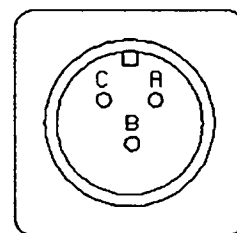


MODULE REAR VIEW



P2 PIN LAYOUT

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A	+15 V TO INCL	S	DID-2	HH	RCV+		
B	DIG GND	T	ENDORME-LO	JJ	WNORME-HI		
C		U	DID 3	KK	XMT-		
D	DIG GND	V	WPARE-HI	LL	WNORME-LO		
E	-15 V TO INCL	W	DID 4	MM	RCV-		
F		X	WPARE-LO	NN	+/- 15 COMM		
H		Y	DID 5				
J		Z	WNORME-HI				
K		AA	DID 6				
L	EPARE-HI	BB	WNORME-LO				
M	DID 0	CC	DID PARITY				
N	EPARE-LO	DD	APARE-HI				
P	DID 1	EE	XMT+				
R	ENDORME-HI	FF	APARE-LO				
M101 P2 SIGNAL PINOUT						DATE 4/89	
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 14 OF 42	



PIN	FUNCTION					
A	110 VAC					
B	AC NUETRAL					
C	FRAME GND					
M101 P3 PINOUT						DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST						PAGE 15 OF 42

PIN	FUNCTION	TYPE	FROM	TO
A				
B				
C				
D				
E				
F	-15 TO DIST BOX	RED, #22	10-J1-F	
H				
J	+15 TO DIST BOX	YELL, #22	10-J1-J	
K				
L				
M				
N				
P				
R				
S	VDMON12+			10-J1-S
T	VCMD6		10-J1-T	
U	TCMD0		10-J1-U	
V	RCMD10 NC		10-J1-V	
W	VDMON12-			10-J1-W
X				
Y	TCMD1		10-J1-Y	
Z	RCMD10 COMM		10-J1-Z	
A_				
B_	VCMD7		10-J1-B_	
C_				
D_	RCMD10 NO		10-J1-D_	
E_	VCMD13+		10-J1-E_	
F_				
H_	TCMD2		10-J1-H_	
J_	RCMD11 NC		10-J1-J_	
K_	VDMON13-			10-J1-K_
M_	RCMD8		10-J1-M_	
N_	TCMD3		10-J1-N_	
P_	RCMD11 COMM		10-J1-P_	
R_				
S_				
T_				
U_	RCMD11 NO		10-J1-U_	
V_	VDMON14+			10-J1-V_
W_	RCMD9		10-J1-W_	
X_	TCMD4		10-J1-X_	
Y_	RES 67 (ACU-NPL RESET)		10-J1-Y_	
MODULE M103 BIN I/O		CONN 4-J4	SECTION 1	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 16 OF 42

[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A	TEMP1			11-J2-A
B	TEMP2			11-J2-B
C	TEMP3			11-J2-C
D	TEMP4			11-J2-D
E	TEMP5			11-J2-E
F	TEMP6			11-J2-F
H	TEMP7			11-J2-H
J	TEMP8			11-J2-J
K	AN1+	WH, TP1		11-J2-K
L	AN11+	WH, TP2		11-J2-L
M	AN1-	BLK, TP1		11-J2-M
N	AN11-	BLK, TP2		11-J2-N
P	AN2+	WH, TP3		11-J2-P
R	AN12+	WH, TP4		11-J2-R
S	AN2-	BLK, TP3		11-J2-S
T	AN12-	BLK, TP4		11-J2-T
U	AN3+	WH, TP5		11-J2-U
V	TDMON6			11-J2-V
W	AN3-	BLK, TP5		11-J2-W
X	TDMON0			11-J2-X
Y	AN4+	WH, TP6		11-J2-Y
Z	TDMON7			11-J2-Z
A_	AN4-	BLK, TP6		11-J2-A_
B_	TDMON1			11-J2-B_
C_	AN5+	WH, TP7		11-J2-C_
D_	TDMON8			11-J2-D_
E_	AN5-	BLK, TP7		11-J2-E_
F_	TDMON2			11-J2-F_
H_	AN6+	WH, TP8		11-J2-H_
J_				
K_	AN6-	BLK, TP8		11-J2-K_
M_				
N_	AN7+	WH, TP9		11-J2-N_
P_	TDMON9			11-J2-P_
R_	AN7-	BLK, TP9		11-J2-R_
S_	TDMON3			11-J2-S_
T_	AN8+	WH, TP10		11-J2-T_
U_	TDMON10			11-J2-U_
V_	AN8-	BLK, TP10		11-J2-V_
W_	TDMON4			11-J2-W_
X_	AN9+	WH, TP11		11-J2-X_
Y_	TDMON11			11-J2-Y_
MODULE M103 BIN I/O		CONN 5-J5	SECTION 1	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 18 OF 42

[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A				
B				
C				
D				
E				
F	-15 TO DIST BOX	RED, #22		4-J4-F
H				
J	+15 TO DIST BOX	YELL, #22		4-J4-J
K				
L				
M				
N				
P				
R				
S	VDMON12+		4-J4-S	
T	VCMD6			4-J4-T
U	TCMD0			4-J4-U
V	RCMD10 NC			4-J4-V
W	VDMON12-		4-J4-W	
X				
Y	TCMD1			4-J4-Y
Z	RCMD10 COMM			4-J4-Z
A_				
B_	VCMD7			4-J4-B_
C_				
D_	RCMD10 NO			4-J4-D_
E_	VDMON13+		4-J4-E_	
F_				
H_	TCMD2			4-J4-H_
J_	RCMD11 NC			4-J4-J_
K_	VDMON13-		4-J4-K_	
M_	RDCMD8			4-J4-M_
N_	TCMD3			4-J4-N_
P_	RCMD11 COMM			4-J4-P_
R_				
S_				
T_				
U_	RCMD11 NO			4-J4-U_
V_	VDMON14+		4-J4-V_	
W_	RDCMD9			4-J4-W_
X_	TCMD4			4-J4-X_
Y_	RES 67 (ACU-NPL RESET)			4-J4-Y_
MODULE M103		CONN 10-J1	SECTION 1	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 20 OF 42

[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A	TEMP1		5-J5-A	
B	TEMP2		5-J5-B	
C	TEMP3		5-J5-C	
D	TEMP4		5-J5-D	
E	TEMP5		5-J5-E	
F	TEMP6		5-J5-F	
H	TEMP7		5-J5-H	
J	TEMP8		5-J5-J	
K	AN1+	WH, TP1	5-J5-K	
L	AN11+	WH, TP2	5-J5-L	
M	AN1-	BLK, TP1	5-J5-M	
N	AN11-	BLK, TP2	5-J5-N	
P	AN2+	WH, TP3	5-J5-P	
R	AN12+	WH, TP4	5-J5-R	
S	AN2-	BLK, TP3	5-J5-S	
T	AN12-	BLK, TP4	5-J5-T	
U	AN3+	WH, TP5	5-J5-U	
V	TDMON6		5-J5-V	
W	AN3-	BLK, TP5	5-J5-W	
X	TDMON0		5-J5-X	
Y	AN4+	WH, TP6	5-J5-Y	
Z	TDMON7		5-J5-Z	
A_	AN4-	BLK, TP6	5-J5-A_	
B_	TDMON1		5-J5-B_	
C_	AN5+	WH, TP7	5-J5-C_	
D_	TDMON8		5-J5-D_	
E_	AN5-	BLK, TP7	5-J5-E_	
F_	TDMON2		5-J5-F_	
H_	AN6+	WH, TP8	5-J5-H_	
J_	TDMON 6-8 POL SEL			
K_	AN6-	BLK, TP8	5-J5-K_	
M_				
N_	AN7+	WH, TP9	5-J5-N_	
P_	TDMON9		5-J5-P_	
R_	AN7-	BLK, TP9	5-J5-R_	
S_	TDMON3		5-J5-S_	
T_	AN8+	WH, TP10	5-J5-T_	
U_	TDMON10		5-J5-U_	
V_	AN8-	BLK, TP10	5-J5-V_	
W_	TDMON4		5-J5-W_	
X_	AN9+	WH, TP11	5-J5-X_	
Y_	TDMON11		5-J5-Y_	
MODULE M103		CONN 11-J2	SECTION 1	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 22 OF 42

[illegible]

[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A	RCV+	WH, TP2	5-J2-8	1-J1-HH
B	XMT+	WH, TP1	5-J2-1	1-J1-EE
C	RCV-	BLK, TP2	5-J2-9	1-J1-MM
D	XMT-	BLK, TP1	5-J2-2	1-J1-KK
E	DID0		11-J2-FF	10-J1-P
F				
H	DID1			
J				
K	DID2			
L	DIS3			
M	DID4			
N	DID5			
P	DID6		10-J1-E	10-J1-R
R	DID7		10-J1-P	
S				
T				
U				
V				
W				
X	TCMD6 POL SEL			
Y				
Z				
A_	VDMON12 POL SEL			
B_				
C_	TCMD0,1 POL SEL			
D_				
E_				
F_	VCMD7 POL SEL			
H_				
J_				
K_				
M_				
N_				
P_				
R_	VDMON 13 POL SEL			
S_	RDCMD8 POL SEL			
T_	TCMD2,3 POL SEL			
U_				
V_				
W_				
X_				
Y_				
MODULE M103		CONN 10-J1	SECTION 2	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 26 OF 42

[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A				
B				
C				
D				
E				
F				
H				
J				
K				
L				
M				
N				
P				
R				
S				
T				
U				
V				
W				
X				
Y				
Z				
A_				
B_				
C_				
D_				
E_				
F_				
H_				
J_	TDMON6-8 POL SEL			
K_				
M_	TDMON0-2 POL SEL			
N_				
P_				
R_				
S_				
T_				
U_				
V_				
W_				
X_				
Y_				
MODULE M103		CONN 11-J2	SECTION 2	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 28 OF 42

[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A	+5 TO COMP RESET BOX			
B				
C	SSR DRV TO CMP RES BOX			
D				
E				
F				
H				
J				
K				
L				
M				
N				
P				
R				
S				
T				
U				
V				
W				
X				
Y				
Z				
AA				
BB				
CC				
DD				
EE				
FF				
HH				
JJ				
KK				
LL				
MM				
NN				
MODULE M103		CONN 10-J4	SECTION 3	DATE 4/89
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[illegible]

PIN	FUNCTION	TYPE	FROM	TO
A	RCV+	WH, TP2	5-J2-8	
B	XMT+	WH, TP1	5-J2-1	
C	RCV-	BLK, TP2	5-J2-9	
D	XMT-	BLK, TP1	5-J2-2	
E	DID0			
F				
H	DID1		11-J2-FF	10-J1-P
J				
K	DID2			
L	DID3			
M	DID4			
N	DID5			
P	DID6		10-J1-H	10-J1-R
R	DID7		10-J1-P	
S				
T				
U				
V				
W				
X	TCMD6 POL SEL			
Y				
Z				
A_	VDMON12 POL SEL			
B_				
C_	TCMD0, 1 POL SEL			
D_				
E_				
F_	VCMD7 POL SEL			
H_				
J_				
K_				
M_				
N_				
P_				
R_	VDMON13 POL SEL			
S_	RDCMD8 POL SEL			
T_	TCMD2, 3 POL SEL			
U_				
V_				
W_				
X_				
Y_				
MODULE M103		CONN 10-J1	SECTION 3	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 33 OF 42

PIN	FUNCTION	TYPE	FROM	TO
A				
B				
C				
D				
E				
F				
H				
J				
K				
L				
M				
N				
P				
R				
S				
T				
U				
V				
W				
X				
Y				
Z				
A_				
B_				
C_				
D_				
E_				
F_				
H_				
J_	TDM0N6-8 POL SEL			
K_				
M_	TDM0N0-2 POL SEL			
N_				
P_				
R_				
S_				
T_				
U_				
V_				
W_				
X_				
Y_				
MODULE M103		CONN 11-J2	SECTION 3	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 35 OF 42

[illegible]

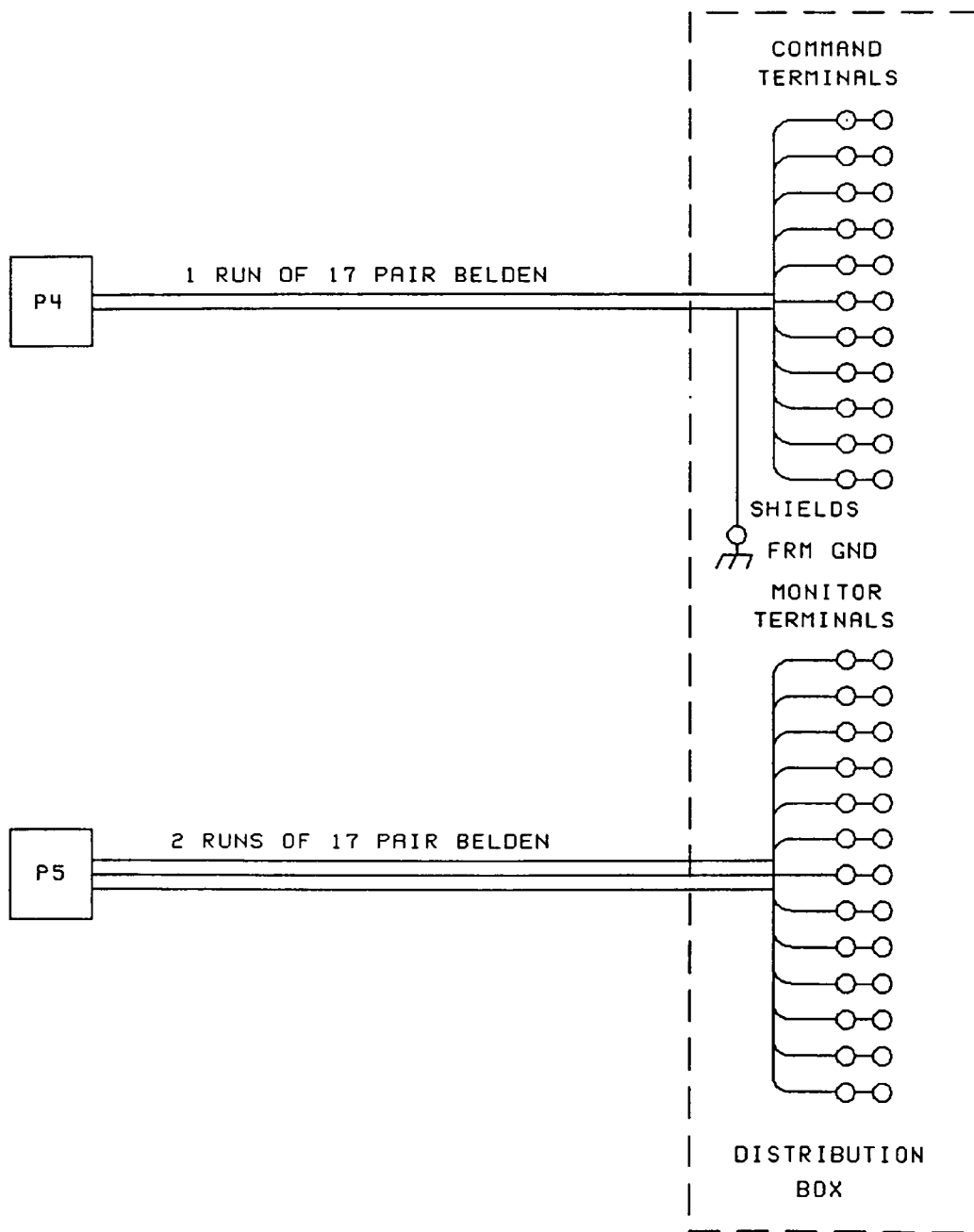
PIN	FUNCTION	TYPE	FROM	TO
A	TEMP 13-S			4-J3-CJ
B	TEMP 1-S			4-J3-A
C				
D	TEMP PROBE -15V EXC			4-J3-E
E	TEMP 14-S			4-J3-B
F	TEMP 2-S			4-J3-K
H				
J				
K	TEMP 15-S			4-J3-L
L	TEMP 3-S			4-J3-U
M				
N				
P	TEMP 16-S			4-J3-V
R	TEMP 4-S			4-J3-C_
S				
T				
U	TEMP 17-S			4-J3-D_
V	TEMP 5-S			4-J3-M_
W				
X				
Y	TEMP 18-S			4-J3-N_
Z	TEMP 6-S			4-J3-V_
A_	TEMP PROBE -15V EXC			4-J3-S_
B_				
C_	TEMP 19-S			4-J3-W_
D_	TEMP 7-S			4-J3-AD
E_				
F_				
H_	TEMP 20-S			4-J3-AE
J_	TEMP 8-S			4-J3-AN
K_				
M_				
N_	TEMP 21-S			4-J3-AP
P_	TEMP 9-S			4-J3-AX
R_				
S_				
T_	TEMP 22-S			4-J3-AY
U_	TEMP 10-S			4-J3-BF
V_				
W_				
X_	TEMP 23-S			4-J3-BH
Y_	TEMP 11-S			4-J3-BR
MODULE M101		CONN 1-J1	SECTION 4	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 37 OF 42

PIN	FUNCTION	TYPE	FROM	TO
A	+15V TO INCL	#22, RED		4-J3-D
B	DIG GND FOR ID BYTE			
C				
D	DIG GND FOR ID BYTE			
E	-15V TO INCL	#22, YELL		4-J3-N
F				
H				
J				
K				
L	EAST PAR ELEV (IN1+)	RED, TP20		4-J3-G ₋
M	ID0BAR			
N	EAST PAR ELEV (IN1-)	BLK, TP20		4-J3-K ₋
P	ID1BAR			
R	EAST NORM ELEV (IN4+)	RED, TP23		4-J3-Q ₋
S	ID2BAR			
T	EAST NORM ELEV (IN4-)	BLK, TP23		4-J3-U ₋
U	ID3BAR			
V	WEST PAR ELEV (IN2+)	RED, TP21		4-J3-AH
W	ID4BAR			
X	WEST PAR ELEV (IN2-)	BLK, TP21		4-J3-AM
Y	ID5BAR			
Z	WEST NORM ELEV (IN5+)	RED, TP24		4-J3-AS
AA	ID6BAR			
BB	WEST NORM ELEV (IN5-)	BLK, TP24		4-J3-AW
CC	IDPARBAR			
DD	APEX PAR ELEV (IN3+)	RED, TP22		4-J3-BK
EE	XMT+	WH, TP1	10-J1-B	
FF	APEX PAR ELEV (IN3-)	BLK, TP22		4-J3-BP
HH	RCV+	WH, TP2	10-J1-A	
JJ	APEX NORM ELEV (IN6+)	RED, TP25		4-J3-BU
KK	XMT-	BLK, TP1	10-J1-D	
LL	APEX NORM ELEV (IN6-)	BLK, TP25		4-J3-BY
MM	RCV-	BLK, TP2	10-J1-C	
NN	ANALOG (+-15V) COMM	#22, BLK		4-J3-T
MODULE M101		CONN 1-J2	SECTION 4	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 39 OF 42

PIN	FUNCTION	TYPE	FROM	TO
A	TEMP 1-S		1-J1-B	
B	TEMP 14-S		1-J1-E	
C				
D	+15V TO INCL	RED, #22	1-J2-A	
E	TEMP PROBE -15V EXC	BLK, TP26	1-J1-D	
F				
H				
J				
K	TEMP 2-S		1-J1-F	
L	TEMP 15-S		1-J1-K	
M				
N	-15V TO INCL	YELL, #22	1-J2-E	
P				
R				
S				
T	ANALOG (+-15v) COMM	BLK, #22		1-J2-NN
U	TEMP 3-S		1-J1-L	
V	TEMP 16-S		1-J1-P	
W				
X				
X				
Y				
Z				
A ₋				
B ₋				
C ₋	TEMP 4-S		1-J1-R	
D ₋	TEMP 17-S		1-J1-U	
F ₋				
G ₋	EAST PAR ELEV (IN1+)	WH, TP20	1-J2-L	
H ₋				
J ₋				
K ₋	EAST PAR ELEV (IN1-)	BLK, TP20	1-J2-N	
M ₋	TEMP 5-S		1-J1-V	
N ₋	TEMP 18-S		1-J1-Y	
P ₋				
Q ₋	EAST NORM ELEV (IN4+)	WH, TP23	1-J2-R	
R ₋				
S ₋	TEMP PROBE -15V EXC		1-J1-A ₋	
T ₋				
U ₋	EAST NORM ELEV (IN4-)	BLK, TP23	1-J2-T	
V ₋	TEMP 6-S		1-J1-Z	
W ₋	TEMP 19-S		1-J1-C ₋	
MODULE BIN I/O		CONN 4-J3	SECTION 4	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 40 OF 42

PIN	FUNCTION	TYPE	FROM	TO
X_				
Y_				
Z_				
AA				
AB				
AC				
AD	TEMP 7-S		1-J1-D_	
AE	TEMP 20-S		1-J1-H_	
AF				
AH	WEST PAR ELEV (IN2+)	WH, TP21	1-J2-V	
AJ				
AK				
AL				
AM	WEST PAR ELEV (IN2-)	BLK, TP21	1-J2-X	
AN	TEMP 8-S		1-J1-J_	
AP	TEMP 21-S		1-J1-N_	
AR				
AS	WEST NORM ELEV (IN5+)	WH, TP24	1-J2-Z	
AT				
AU				
AV				
AW	WEST NORM ELEV (IN5-)	BLK, TP24	1-J2-BB	
AX	TEMP 9-S		1-J1-P_	
AY	TEMP 22-S		1-J1-T_	
AZ				
BA				
BB				
BC				
BD				
BE				
BF	TEMP 10-S		1-J1-U_	
BH	TEMP 23-S		1-J1-X_	
BJ				
BK	APEX PAR ELEV (IN3+)	WH, TP22	1-J2-DD	
BL				
BM				
BN				
BP	APEX PAR ELEV (IN3-)	BLK, TP22	1-J2-FF	
BR	TEMP 11-S		1-J1-Y_	
BS	TEMP 24-S		1-J1-BB	
BT				
BU	APEX NORM ELEV (IN6+)	WH, TP25	1-J2-JJ	
MODULE BIN I/O		CONN 4-J3	SECTION 4	DATE 4/89
UTILITY CONTROL - MONITOR SYSTEM BIN WIRE LIST				PAGE 41 OF 42

[illegible]



CABLE: 17 TW-PR, SHIELDED, BELDEN #9769

A55001W002

UTILITY BIN TO DISTRIBUTION BOX CABLE

DATE 5/3/88

UTILITY CONTROL - MONITOR SYSTEM

PAGE 1 OF 4

PIN	FUNCTION	TYPE	FROM	TO
F	- 15 TO DIST BOX	PR#11, YELL		TERM 128-135
J	+ 15 TO DIST BOX	PR#11, RED		TERM 142-143
S	DMON12+	PR#1, RED		TERM 3
W	DMON12-	PR#1, BLK		TERM 103
E_	DMON13+	PR#2, WH		TERM 2
K_	DMON13-	PR#2, BLK		TERM 102
V_	DMON14+	PR#3, GRN		TERM 1
Z_	DMON14-	PR#3, BLK		TERM 101
U	TCMD0	PR#17, GRN		TERM 36
Y	TCMD1	PR#17, BRN		TERM 37
H_	TCMD2	PR#16, GRN		TERM 38
N_	TCMD3	PR#16, YELL		TERM 39
X_	TCMD4	PR#15, GRN		TERM 40
BB	TCMD5	PR#15, BLUE		TERM 41
T	VCMD6	PR#14, GRN		TERM 42
B_	VCMD7	PR#14, WH		TERM 43
M_	RDCMD8	PR#13, RED		TERM 46
W_	RDCMD9	PR#13, ORNG		TERM 47
R	SPARE WIRE	PR#9, GRN		CUC *
V	RCMD10 NC	PR#9, RED		TERM 44
Z	RCMD10 C	PR#12, BRN		TERM 144
D_	RCMD10 NO	PR#12, RED		TERM 244
F_	SPARE WIRE	PR#4, BLK		CUC *
J_	RCMD11 NC	PR#4, BLUE		TERM 45
P_	RCMD11 C	PR#10, RED		TERM 145
U_	RCMD11 NO	PR#10, BLUE		TERM 245
AA	SPARE WIRE	PR#5, BLK		CUC *
Y_	RES 67 (ACU RESET)	PR#5, YELL		TERM 48
HH	LOGIC COMMON	PR#7, BLK		TERM 236-241
CC	+ 5 VOLTS	PR#7, ORNG		TERM 136-141
FF	SPARE WIRE	PR#8, RED		CUC *
EE	+ 28 VOLTS	PR#8, WH		TERM 146-148
	NOTES			
	CUC * COIL UP IN CORNER			
	TIE ALL DRAIN WIRES TO			
	TO DIST BOX FRAME GND			
	A_ LOWER CASE, TYP			
UTILITY BIN TO D-BOX CABLE		CONN P4		DATE 5/3/88
UTILITY CONTROL - MONITOR SYSTEM				PAGE 2 OF 4

PIN	FUNCTION	TYPE	FROM	TO
A	TEMP1	B1PR#1, BLK		TERM 35
B	TEMP2	B1PR#1, RED		TERM 34
		B1PR#1, SHLD		TERM 235
C	TEMP3	B1PR#2, BLK		TERM 33
D	TEMP4	B1PR#2, WH		TERM 32
		B1PR#2, SHLD		TERM 233
E	TEMP5	B1PR#3, BLK		TERM 31
F	TEMP6	B1PR#3, GRN		TERM 30
		B1PR#3, SHLD		TERM 231
H	TEMP7	B1PR#4, BLK		TERM 29
J	TEMP8	B1PR#4, BLUE		TERM 28
		B1PR#4, SHLD		TERM 229
K	AN1+	B1PR#5, BLK		TERM 15
M	AN1-	B1PR#5, YELL		TERM 115
		B1PR#5, SHLD		TERM 215
P	AN2+	B1PR#6, BLK		TERM 14
S	AN2-	B1PR#6, BRN		TERM 114
		B1PR#6, SHLD		TERM 214
U	AN3+	B1PR#7, BLK		TERM 13
W	AN3-	B1PR#7, ORNG		TERM 113
		B1PR#7, SHLD		TERM 213
Y	AN4+	B1PR#8, RED		TERM 12
A_	AN4-	B1PR#8, WH		TERM 112
		B1PR#8, SHLD		TERM 212
C_	AN5+	B1PR#9, RED		TERM 11
E_	AN5-	B1PR#9, GRN		TERM 111
		B1PR#9, SHLD		TERM 211
H_	AN6+	B1PR#10, RED		TERM 10
K_	AN6-	B1PR#10, BLUE		TERM 110
		B1PR#10, SHLD		TERM 210
N_	AN7+	B1PR#11, RED		TERM 9
R_	AN7-	B1PR#11, YELL		TERM 109
		B1PR#11, SHLD		TERM 209
T_	AN8+	B1PR#12, RED		TERM 8
V_	AN8-	B1PR#12, BRN		TERM 108
		B1PR#12, SHLD		TERM 208
X_	AN9+	B1PR#13, RED		TERM 7
Z_	AN9-	B1PR#13, ORNG		TERM 107
		B1PR#13, SHLD		TERM 207
BB	AN10+	B1PR#14, GRN		TERM 6
DD	AN10-	B1PR#14, WH		TERM 106
		B1PR#14, SHLD		TERM 206
UTILITY BIN TO D-BOX CABLE		CONN P5		DATE 5/3/88
UTILITY CONTROL - MONITOR SYSTEM				PAGE 3 OF 4

PIN	FUNCTION	TYPE	FROM	TO
L	AN11+	B1PR#15, GRN		TERM 5
N	AN11-	B1PR#15, BLUE		TERM 105
		B1PR#15, SHLD		TERM 205
R	AN12+	B1PR#16, GRN		TERM 4
T	AN12-	B1PR#16, YELL		TERM 104
		B1PR#16, SHLD		TERM 204
FF	SPARE WIRE	B1PR#17, GRN		CUC *
HH	SPARE WIRE	B1PR#17, BRN		CUC *
X	TDMON0	B2PR#17, GRN		TERM 27
B_	TDMON1	B2PR#17, BRN		TERM 26
		B2PR#17, SHLD		TERM 227
F_	TDMON2	B2PR#16, GRN		TERM 25
S_	TDMON3	B2PR#16, YELL		TERM 24
		B2PR#16, SHLD		TERM 225
W_	TDMON4	B2PR#15, GRN		TERM 23
AA	TDMON5	B2PR#15, BLUE		TERM 22
		B2PR#15, SHLD		TERM 223
V	TDMON6	B2PR#14, GRN		TERM 21
Z	TDMON7	B2PR#14, WH		TERM 20
		B2PR#14, SHLD		TERM 221
D_	TDMON8	B2PR#12, RED		TERM 19
P_	TDMON9	B2PR#12, ORNG		TERM 18
		B2PR#12, SHLD		TERM 119
U_	TDMON10	B2PR#11, RED		TERM 17
Y_	TDMON11	B2PR#11, YELL		TERM 16
		B2PR#11, SHLD		TERM 117
	NOTES			
	* CUC, COIL UP IN CORNER			
	A_ LOWER CASE, TYP			
	B1PR#1 IS RUN #1, PAIR #1			
	B2PR#1 IS RUN #2, PAIR #1			
	STUB OFF ALL DRAIN WIRES			
	AT P5 END OF CABLE			
UTILITY BIN TO D-BOX CABLE		CONN P5		DATE 5/3/88
UTILITY CONTROL - MONITOR SYSTEM				PAGE 4 OF 4

D

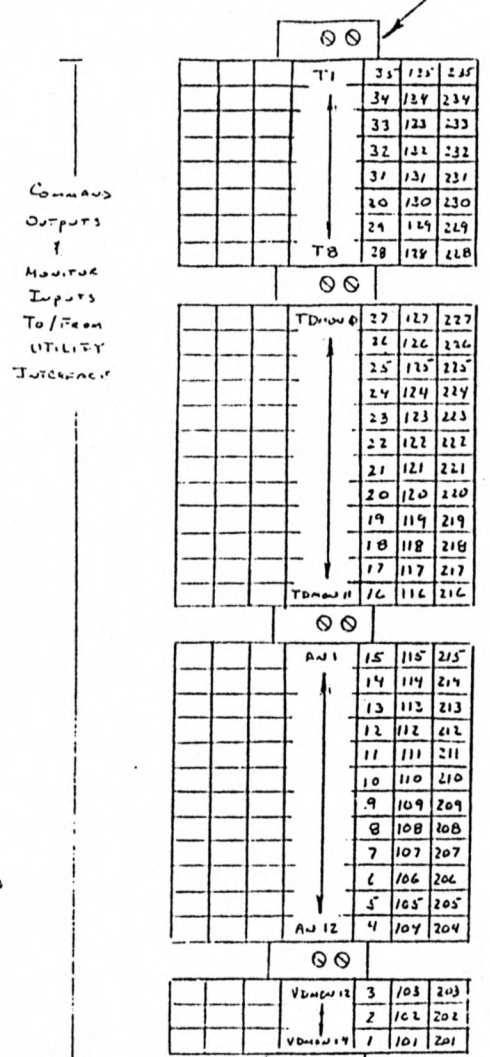
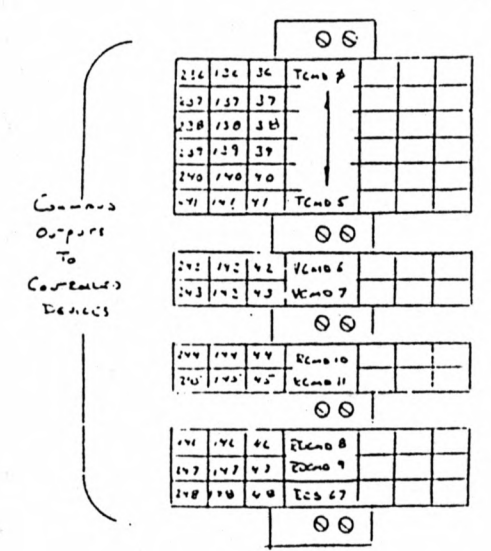
C

B

A

Junction Box Top

Space, E-UK



Bus Strip Configuration

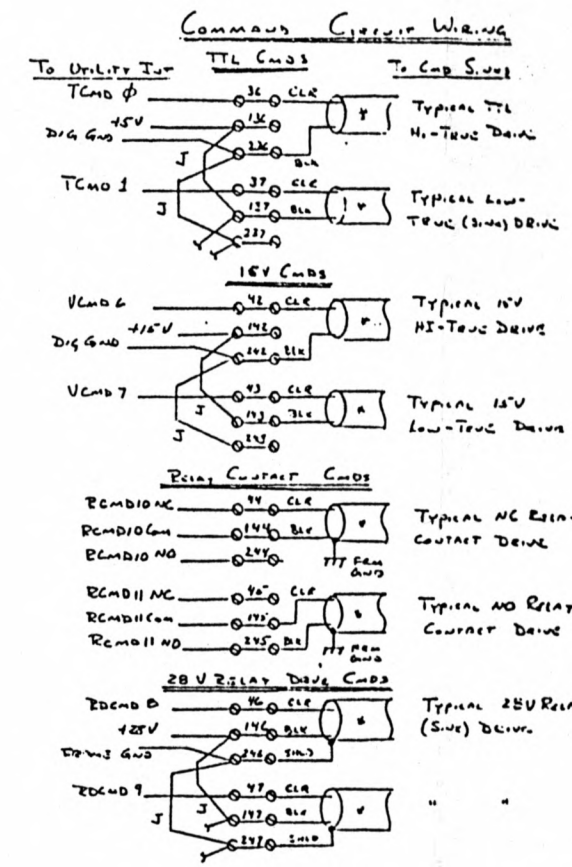
- Temp Probes : 128 - 135, -15V Bus (T1 - T8)
- TTL Mon : 116 - 127, Dig Gnd Bus (TDMON)
- Running Mon : 204 - 215, Frame Gnd, Cable Shields (AUX)
- 15V Disc Mon : 201 - 203, Frame Gnd, Cable Shields (VDMON)
- TTL Disc Cnd : 236 - 241, Dig Gnd Bus (TCMD)
- 15V Disc Cnd : 242 - 243, Dig Gnd Bus (VCMND)
- 28V Relay Drive : 146 - 148, +28V Bus (RCD)
- Cnd (RCD) : 246 - 248, Frame Gnd, Cable Shields

Utility Interface Junction Box Terminal Layout

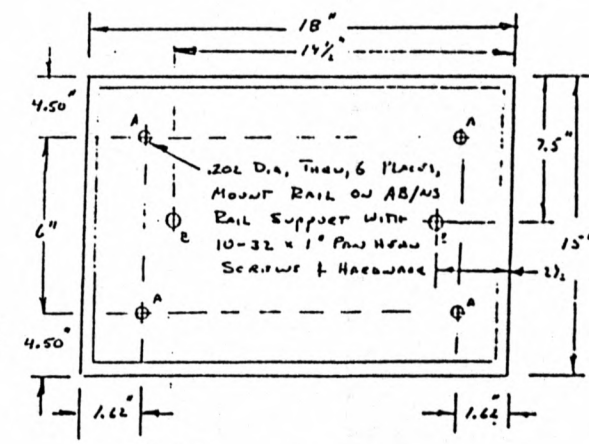
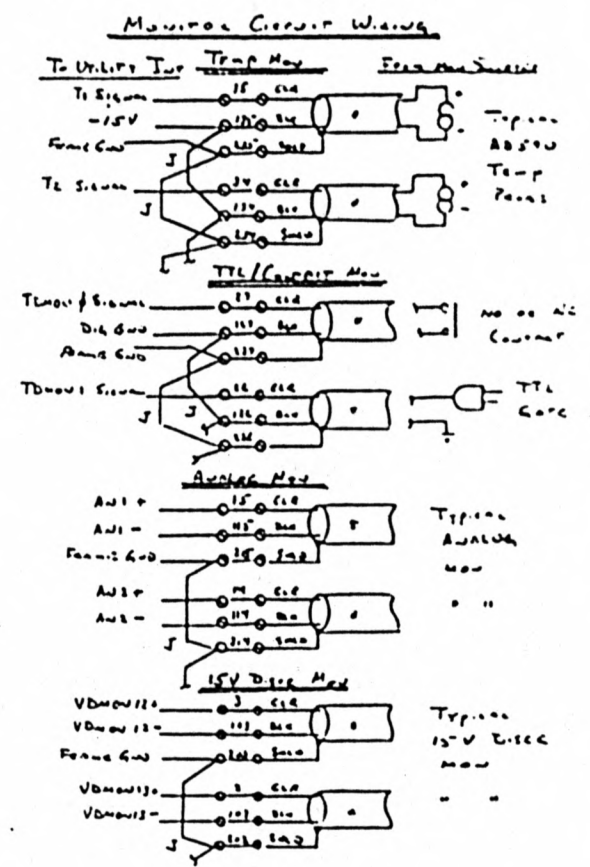
- * Typical Cable To Cnd Strips / Mon Sources is Zelen "B761"
- J-203 To Bus I/O Cable is Dorian "A55002W003"

Cable Bus Cnd: HUS-62112
Bus and wire: HUS-62112
Cnd: HUS-62112

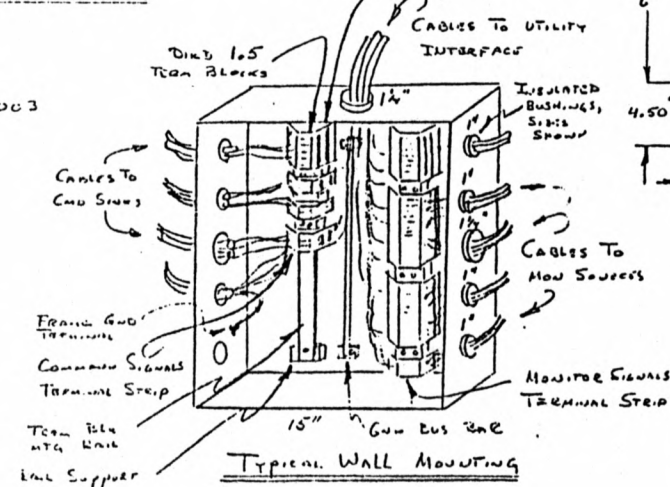
- Terminal Blocks : 3 TIE PHOSPHOR CONTACT DIKD 1.5"
- Space : PHOSPHOR CONTACT E-UK
- Rail : PHOSPHOR CONTACT NS 37/7, 5
- Jump Strips : PHOSPHOR CONTACT C810-6
- Rail Supports : PHOSPHOR CONTACT AB/NS
- Junction Box : Hardware A-SEIBK 15x4
- Insulating Bushings : 0-2/Grady AB815(14) ; AB815(17) ; AB815(18)
- Terminal Markings : PHOSPHOR CONTACT SKSC: 1-250
- Frame Gnd Terminals : 14 SWG, Type 159
- Hardware : HUS-62112



NOTE: J DENOTES JUMPER STRIPS BRIDGES ACROSS 100 & 200 TIE TERMINALS & WIRE TO -15V, Dig Gnd, +15V, +28V Frame Gnd As Required By Circuit Type, See Table At Left



* A Jumper: Mount Terminals on 1/2" dia. Rail Support with nuts to secure bus.
* B Jumper: Mount bus on 1/2" dia. Rail Support with nuts to secure bus.
* C Jumper: Mount bus on 1/2" dia. Rail Support with nuts to secure bus.
* D Jumper: Mount bus on 1/2" dia. Rail Support with nuts to secure bus.



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ± .06
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

UTILITY Control-Mon
System

UTILITY Control-Mon
System Junction Box
Notes, Layout & Wiring

NATIONAL RADIO
ASTRONOMY
OBSERVATORY

SOCORRO NEW MEXICO 87001

DRAWN BY: J. W. H. T.
DATE: 7/11/77

DESIGNED BY: J. W. H. T.
DATE: 7/11/77

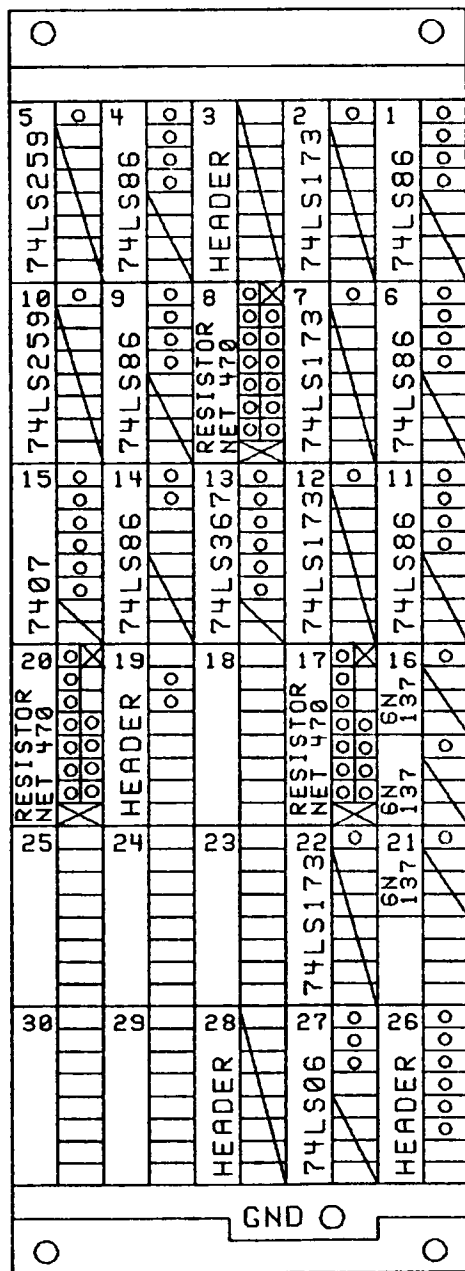
APPROVED BY: J. W. H. T.
DATE: 7/11/77

SHEET NUMBER: 1/1
DRAWING NUMBER: C55001A003

NEXT ASSY: USED ON:

LOC B

SPECIAL SUB ASSY' S



ITEM	BOM#	DWG#
B03		A55001A009 SHT 3
B08		470 OHM RES NET
B17		470 OHM RES NET
B19		A55001A009 SHT 4
B20		470 OHM RES NET
B26		A55001A009 SHT 9
B28		A55001A009 SHT 3

<DC M103IC1>

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801

V
J
D
C

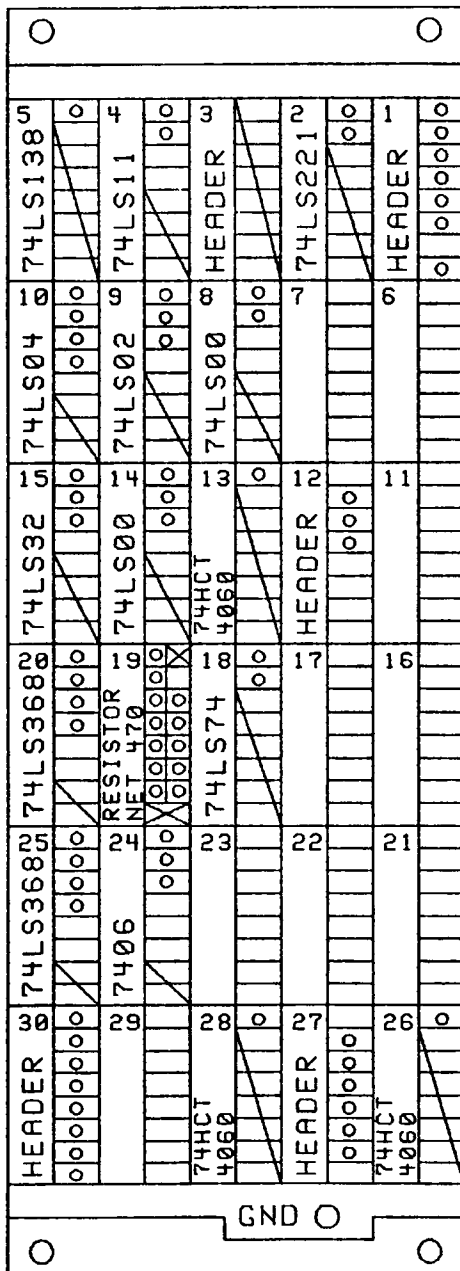
PROJECT: UTILITY CONT-MON SYSTEM
TITLE: M103, UTILITY INTERFACE
IC LAYOUT DIAGRAM

DWG NO: A55001A009

SHEET 1 of 9 REV:

LOC C

SPECIAL SUB ASSY' S



ITEM	BOM#	DWG#
C01		A55001A009 SHT 8
C03		A55001A009 SHT 3
C12		A55001A009 SHT 7
C19		470 OHM RES NET
C27		A55001A009 SHT 6
C30		A55001A009 SHT 5

<DC M103IC2>

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801

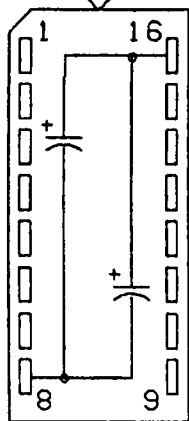
DATE

PROJECT: UTILITY CONT-MON SYSTEM
TITLE: M103, UTILITY INTERFACE
IC LAYOUT DIAGRAM

DWG NO: A55001A009

SHEET 2 of 9

REV:



DESCRIPTION	VALUE	MFG	MFG P/N
DIP HEADER			
TANTALUM CAP.	4.7 μ F 35V		
MONOLITHIC CAP.	0.1 μ F 50V		

MODULE: M103

BOARD LOCATION: B3, B28, C3

<DC M103IC3>

PROJECT: UTILITY CONT-MON SYSTEM

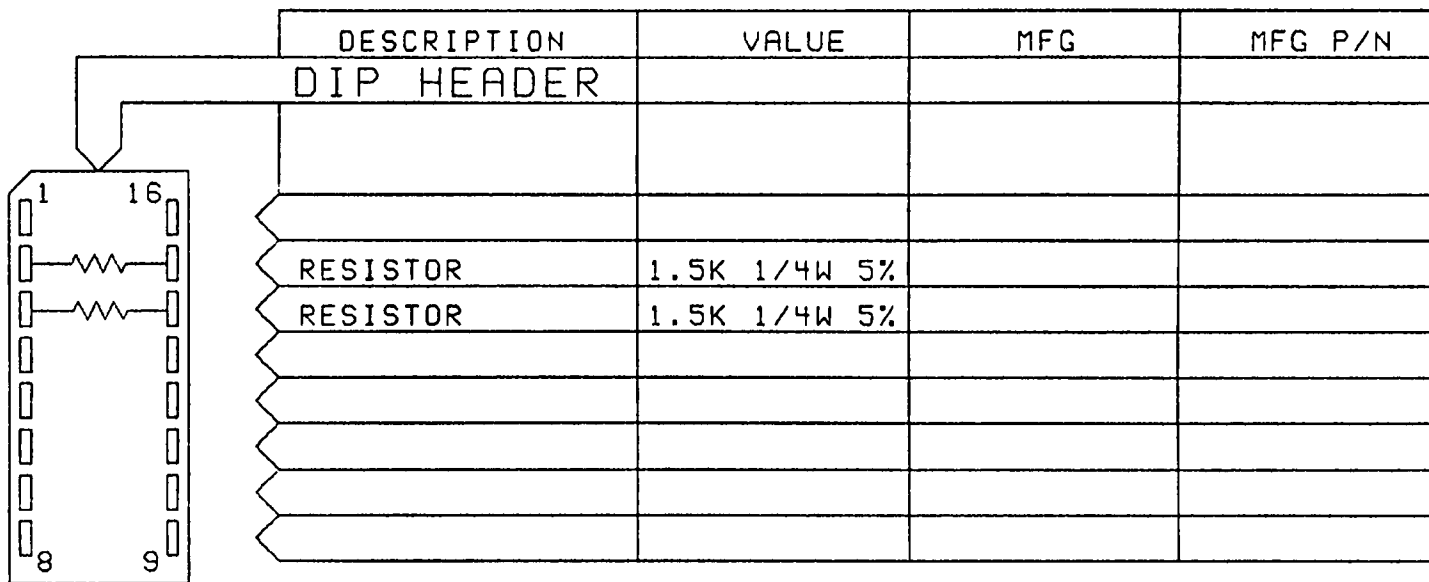
TITLE: M103, UTILITY INTERFACE

IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 3 OF 9 REV:

V LBA

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801



MODULE: M103

BOARD LOCATION: B19

<DC M103IC4>

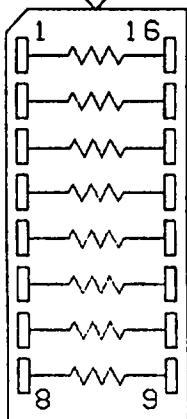
PROJECT: UTILITY CONT-MON SYSTEM

TITLE: M103, UTILITY INTERFACE
IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 4 of 9 REV:

V LBA

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801



DESCRIPTION	VALUE	MFG	MFG P/N
DIP HEADER			
RESISTOR	220 1/4W 5%		
RESISTOR	220 1/4W 5%		
RESISTOR	220 1/4W 5%		
RESISTOR	220 1/4W 5%		
RESISTOR	330 1/4W 5%		
RESISTOR	330 1/4W 5%		
RESISTOR	330 1/4W 5%		
RESISTOR	330 1/4W 5%		

NOTE: RESISTANCE IN OHMS

MODULE: M103

BOARD LOCATION: C30

<DC M103IC5>

PROJECT: UTILITY CONT-MON SYSTEM

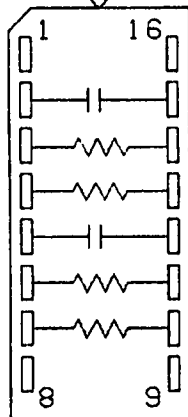
TITLE: M103, UTILITY INTERFACE

IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 5 OF 9 REV:

V LDC

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801



DESCRIPTION	VALUE	MFG	MFG P/N
DIP HEADER			
MONO CAPACITOR	0.1 μ F 50V		
RESISTOR	750K 1/4W		
RESISTOR	1.6M 1/4W		
MONO CAPACITOR	0.01 μ F 50V		
RESISTOR	110K 1/8W 1%		
RESISTOR	247K 1/8W 1%		

NOTE: RESISTANCE IN OHMS

MODULE: M103

BOARD LOCATION: C27

<DC M103IC6>

PROJECT: UTILITY CONT-MON SYSTEM

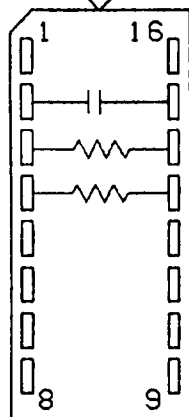
TITLE: M103, UTILITY INTERFACE

IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 6 OF 9 REV:

UTL

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801



DESCRIPTION	VALUE	MFG	MFG P/N
DIP HEADER			
MONO CAPACITOR	0.001 uF 50V		
RESISTOR	4990 1%		
RESISTOR	4990 1%		

NOTE: RESISTANCE IN OHMS

MODULE: M103

BOARD LOCATION: C12

<CDC M103IC7>

PROJECT: UTILITY CONT-MON SYSTEM

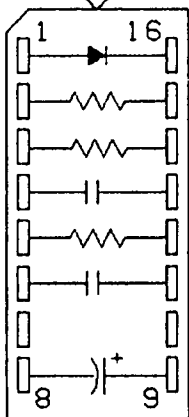
TITLE: M103, UTILITY INTERFACE

IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 7 OF 9 REV:

V LBA

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801



DESCRIPTION	VALUE	MFG	MFG P/N
DIP HEADER			
DIODE	DIODE		
RESISTOR	4.7K 1/8W 1%		
RESISTOR	100K 1/8W 1%		
MONO CAPACITOR	0.47 μ F 50V		
RESISTOR	10K 1/8W 1%		
MONO CAPACITOR	0.01 μ F 50V		
TANTILUM CAP	4.7 μ F 35V		

NOTE: RESISTANCE IN OHMS

MODULE: M103

BOARD LOCATION: C1

<DC M103IC8>

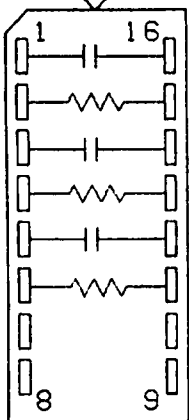
PROJECT: UTILITY CONT-MON SYSTEM

TITLE: M103, UTILITY INTERFACE
IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 8 OF 9 REV:

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801

V LBA



DESCRIPTION	VALUE	MFG	MFG P/N
DIP HEADER			
MONO CAPACITOR	0.01 μ F 50V		
RESISTOR	820 1/4W 5%		
MONO CAPACITOR	0.01 μ F 50V		
RESISTOR	820 1/4W 5%		
MONO CAPACITOR	0.01 μ F 50V		
RESISTOR	820 1/4W 5%		

NOTE: RESISTANCE IN OHMS

MODULE: M103

BOARD LOCATION: B26

<DC M103IC9>

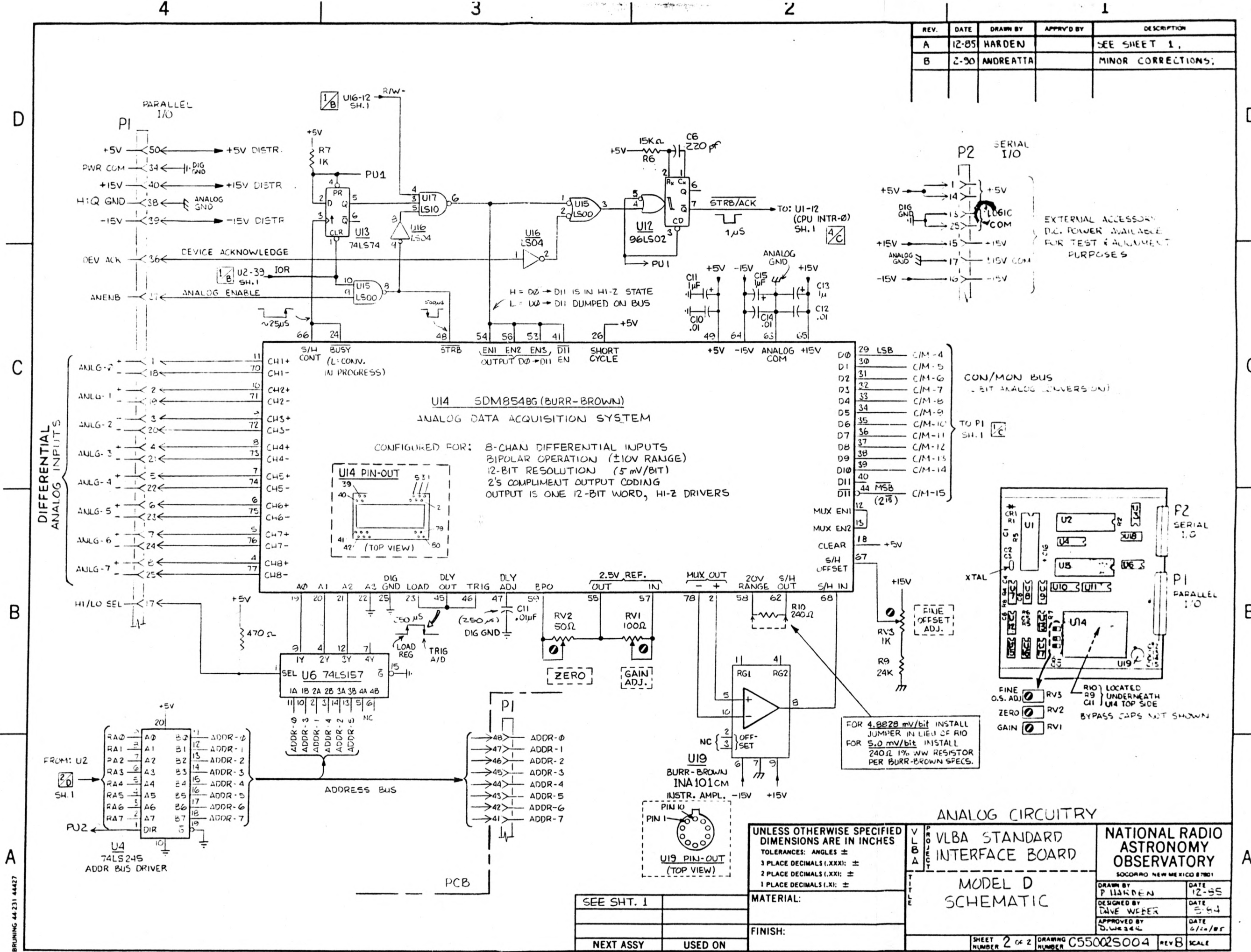
PROJECT: UTILITY CONT-MON SYSTEM

TITLE: M103, UTILITY INTERFACE
IC LAYOUT DIAGRAM

DWG NO: A55001A009 SHEET 9 OF 9 REV:

NATIONAL RADIO ASTRONOMY
OBSERVATORY
SOCORRO, NM 87801

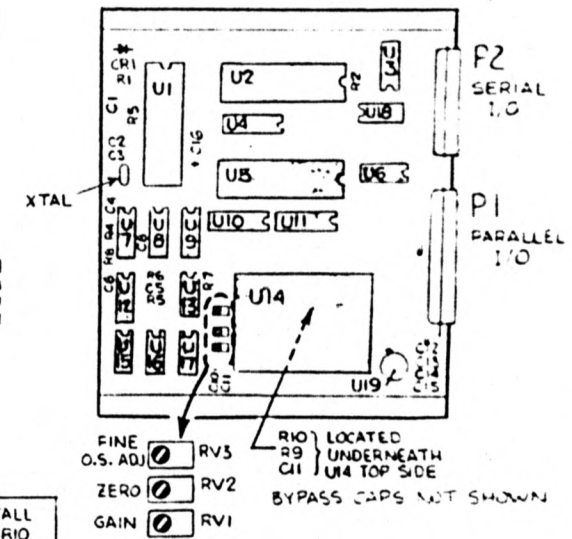
U L B T A



REV.	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	12-85	HARDEN		SEE SHEET 1.
B	2-90	ANDREATTA		MINOR CORRECTIONS:

EXTERNAL ACCESSORY
D.C. POWER AVAILABLE
FOR TEST & ALIGNMENT
PURPOSES

CON/MON BUS
- BIT ANALOG CONVERSION

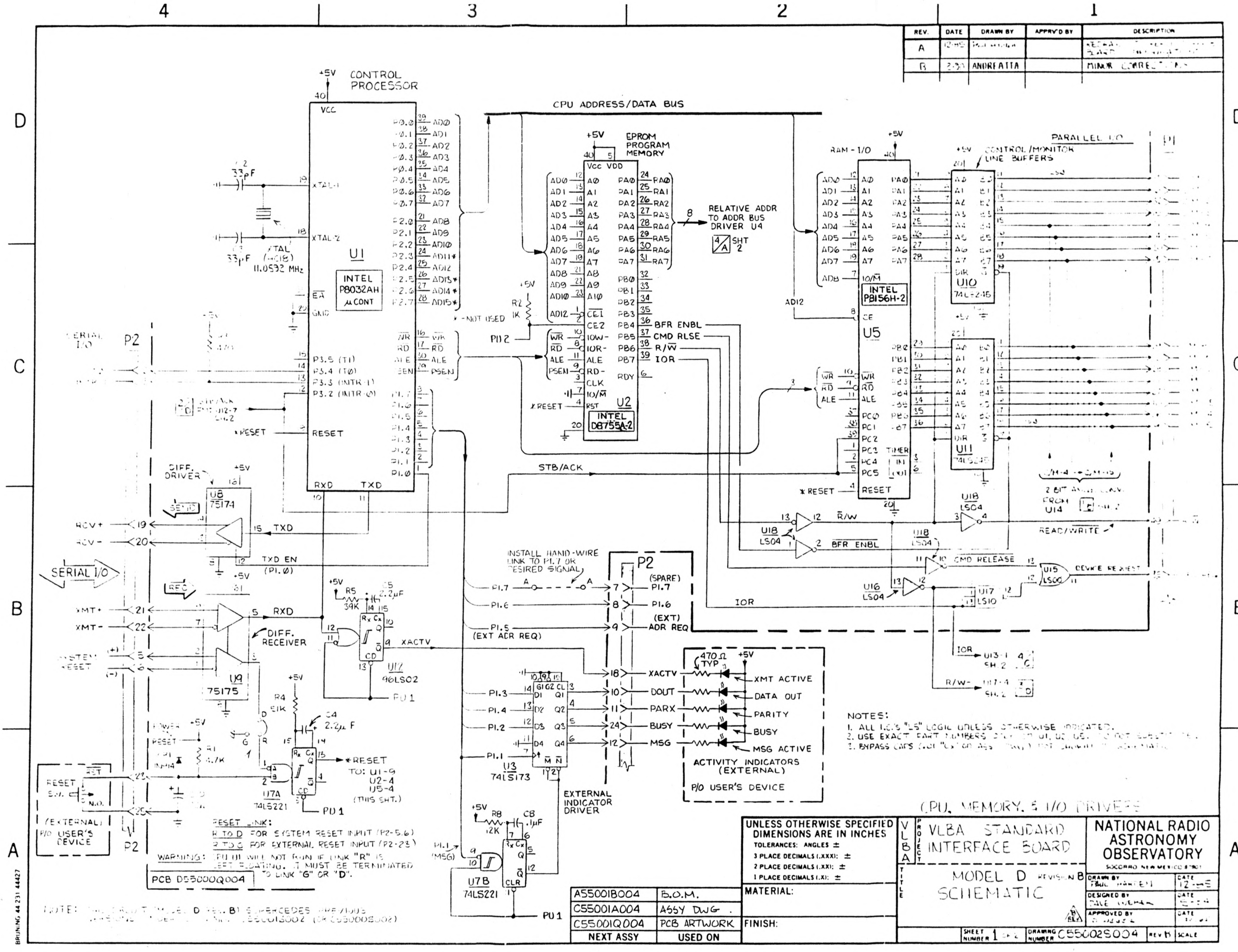


FOR 4.8828 mV/bit INSTALL
JUMPER IN LIEU OF R10
FOR 5.0 mV/bit INSTALL
240Ω 1% WW RESISTOR
PER BURR-BROWN SPECS.

ANALOG CIRCUITRY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±		VLBA STANDARD INTERFACE BOARD		NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801	
MATERIAL:		MODEL D SCHEMATIC		DRAWN BY P. HARDEN	DATE 12-85
FINISH:				DESIGNED BY DAVE WEBER	DATE 5-84
				APPROVED BY D. W. 344	DATE 6/20/85
SEE SHT. 1		SHEET 2 OF 2		DRAWING NUMBER C550025004	REV 8
NEXT ASSY		USED ON		SCALE	

BRUNING 44-231 44427



REV.	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	12-85	PAUL MONTANI		REPAIR - REVISION 1
B	2-90	ANDREAITA		MINOR CORRECTIONS

- NOTES:
1. ALL LOGIC "LS" LOGIC UNLESS OTHERWISE INDICATED.
 2. USE EXACT PART NUMBERS FOR U1, U2, U5. DO NOT SUBSTITUTE.
 3. BYPASS CAPS (NOT "X" OR "A" CAPS) NOT SHOWN IN SCHEMATIC.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (XXX): ±
2 PLACE DECIMALS (XX): ±
1 PLACE DECIMALS (X): ±

A55001B004	B.O.M.
C55001A004	ASBY DWG.
C55001Q004	PCB ARTWORK
NEXT ASSY	USED ON

CPU, MEMORY, & I/O DRIVERS	
VLBA STANDARD INTERFACE BOARD	
MODEL D REVISION B	
SCHEMATIC	
NATIONAL RADIO ASTRONOMY OBSERVATORY SACRAMENTO, CALIFORNIA 95834	
DESIGNED BY PAUL MONTANI	DATE 12-85
APPROVED BY ANDREAITA	DATE 2-90
SHEET NUMBER 1 of 2	DRAWING NUMBER C55002S004
REV 15	SCALE

BRUNING 44 231 44427

