VLBA Technical Report No. 7 (Rev. B)

LO TRANSMITTER MODULE (L102)
and
LO RECEIVER MODULE (L105).

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DESIGN CHANGES AND RETROFITS.

The LO System has undergone a number of changes since the initial design. In the version of the system described in this manual, the 500 MHz reference is sent out to the antenna at 500.000 MHz, i.e. without any frequency offset. At the antenna the VCXO is locked without an IF in the loop. In the earlier version the 500 MHz transmitted to the antenna was offset by 2.083 kHz. The VCXO at the antenna was locked with a loop IF of 2.083 kHz and the offset was thereby removed from the output of the LO Transmitter module. This arrangement offered some advantage in implementation of the pulse calibration system, but was abandoned when it was found that it was difficult to suppress residual sidebands at the offset frequency. A minor change in units seven and onwards is that the monitor detector amplifiers have a standard output of -1 volt rather than +1 volt. In the Round-Trip Monitor module, which is also part of the LO system but is described in a separate manual, the averaging time for the round trip phase measurement was 1 second in early units and has been increased to 3 seconds. Retrofitting of all units to the system described in this manual will be completed during 1992.

CONTENTS

FIGURES

(1) Basic Description of the Local Oscillator Reference System.

The purpose of the system described in this manual is to provide a high stability reference frequency at the antenna that can be multiplied as necessary to obtain the required local oscillator signals. The transmission line that caries this signal from the electronics building to the antenna vertex room is approximately 70 m long, and must be monitored by a round-trip phase measurement. In selecting the reference frequency it is important that it should be high enough that the line length can be monitored with sufficient accuracy. On the other hand it should be low enough that the discrete tuning steps in the LO frequencies are not too widely separated, that the loss in the transmission line is not too high, and that good matching can be maintained. It is also useful if the frequency is within the range for which voltage-controlled crystal oscillators are available. These considerations led to a choice of 500 MHz. The goal is to transmit this frequency to the antenna without degradation, so that the phase stability is determined mainly by the maser from which the signal is derived. A frequency of 100 MHz is also transmitted to the antennas to provide a reference for the phase-locked loop in the 2-16 GHz Synthesizer modules. Since this is not multiplied in frequency, the phase stability requirement is not so high.

A simplified block diagram of the system is shown in Fig. 1, in which the broken lines indicate the distribution into three modules. Two of these are located in the electronics building at each site, and one in the antenna vertex room. A frequency of 100 MHz is supplied by the maser, and this is frequency multiplied to 500 MHz, and transmitted to the antenna. It is also used to lock a voltage-controlled crystal oscillator (VCXO) with an offset of 2.083 kHz which is used in the round-trip phase measurement. A frequency of 100 MHz is also transmitted directly to the antenna. The signals at 100 and 500 MHz could be carried on the same cable, but separate cables have been used to avoid the need for diplexing filters.

To implement the round-trip phase measurement a small part of the 500 MHz signal at the antenna is reflected back down the cable by a diode reflector that is driven between on and off states by a squarewave at 1.953 kHz. The returned signal thus contains sidebands at (500.000000 ± 0.001953) MHz: see Fig. 1 (inset). At the maser location the returned signals are converted with the local oscillator at 500.002083 MHz, and the upper sideband then appears as a signal at 130.2 Hz from the output of the mixer. This signal is separated from other signals from the mixer by means of a lowpass filter with cutoff at 200 MHz, and its phase is compared with that of a locally generated 130.2 Hz signal to provide the round-trip phase measurement. Note that the strongest signal entering the R-port of the mixer is likely to be the 500.000 MHz reflected from mismatches in the cable, and not the component from the modulated reflector. Since the cable contains flexible sections that bend as the antennas slew and track, such a component will vary with time in both amplitude and phase. With the scheme in Fig. 1, the wanted output at 130.2 Hz is generated by the combination of two frequencies which do not include 500.000 MHz, so that a component at this last frequency on one port of the mixer has no effect on the wanted output. Thus the possibility of an unwanted reflection causing phase errors in the round trip measurement is avoided.

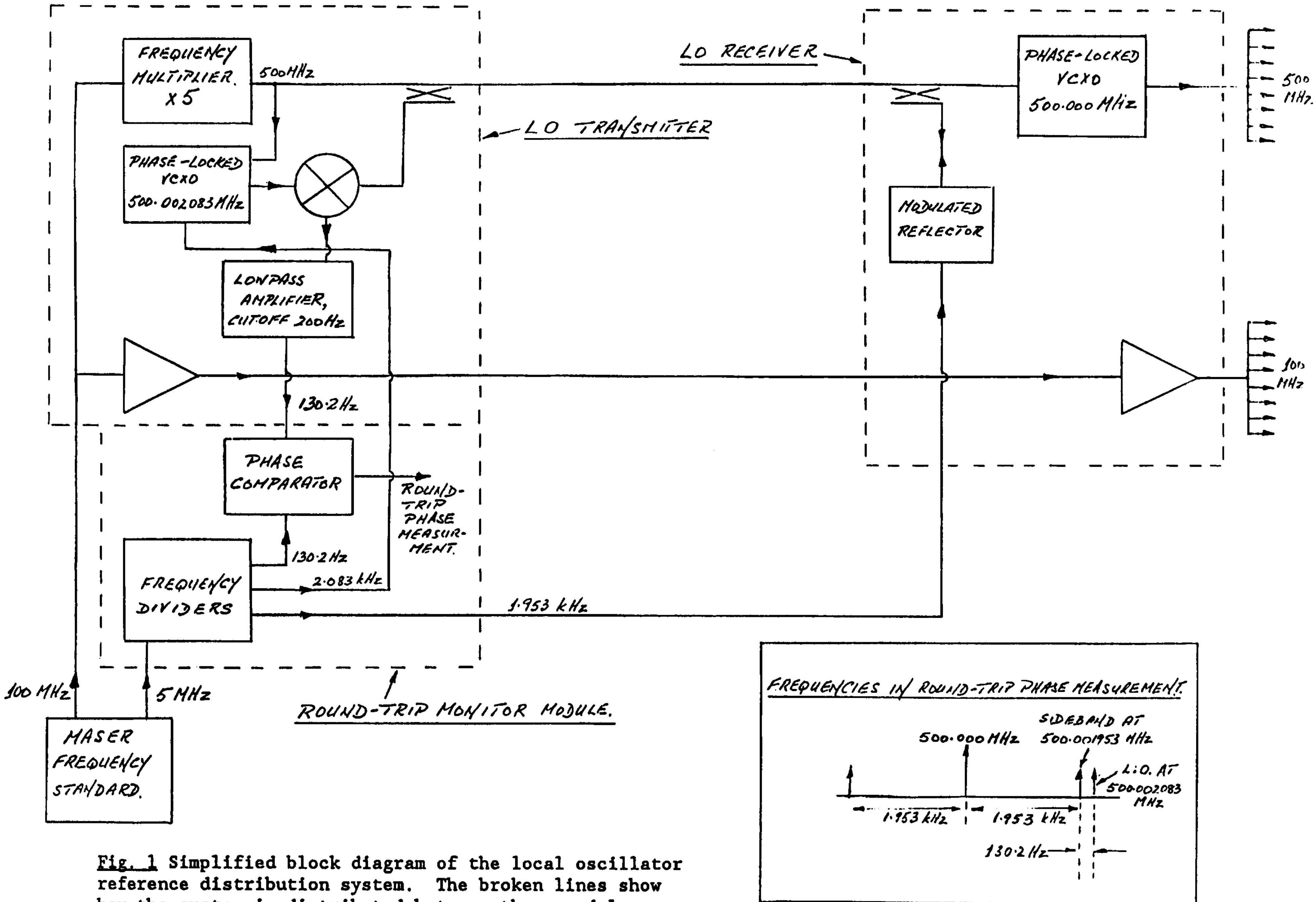

Fig. 1 Simplified block diagram of the local oscillator reference distribution system. The broken lines show how the system is distributed between three modules. The inset shows the frequencies returned from the modulated reflector, including a sideband at 500.001953 MHz which is used for the round-trip phase measurement.

Note that a VCXO is required at the antenna to remove any vestiges of the reflector modulation frequency. Although the reflected component is launched onto the transmission line in the direction of the transmitter module, reflections in the line will produce components travelling towards the receiver which appear as low level sidebands on the wanted reference frequency. The 500 MHz reference at the output of the LO transmitter must be free from noise or other sidebands to a high degree, since to provide the required LO signals it will be multiplied by factors up to 170 (for 86 GHz), resulting in enhancement of sidebands by up to 45 dB. Thus a VCXO is necessary to eliminate such sidebands.

The Round-Trip Monitor module is described in a separate report by Erich Schlecht, but it may be useful to give a few details here. The three low frequencies are generated from a 1 MHz signal derived from the 5 MHz output of the maser by frequency division as follows:

2.083 kHz = 1 MHz / 15 x 2**5
1.953 kHz = 1 MHz / 2**9
130.2 Hz = 1 MHz / 15 x 2**9

Synchronous counters are used. All three frequencies contain at least one division by two, which is necessary to obtain symmetrical squarewave outputs. In addition it is necessary that the frequency used in the phase measurement (130.2 Hz) be obtained by a division by four, since two reference waveforms in phase quadrature are used in the phase comparison. The counter chains are reset to zero every three seconds as a precaution against possible disturbance of their relative phases by, for example, a transient power failure. Three seconds[1] is the shortest integral number of seconds that contains an integral number of cycles at 2.083 kHz, and thus zeroing every three seconds avoids introducing phase jumps in the 2.083 kHz which would disturb the phase-locked loops. The phase comparison is done by gateing and counting 5 MHz pulses, and the counters used here are also read out and reset at the same three second intervals. The count data are read out through a monitor and control interface card in the module.

(2) Design of the LO Transmitter Module.

A detailed block diagram of the LO Transmitter module is shown in the top half of Fig. 2. A 100 MHz input to the module is split three ways. The first output of the splitter goes to a level monitoring detector (Omni Spectra 20090), the output of which is amplified to a standard value of -1 volt when the 100 MHz input level is correct. A circuit diagram of the amplifier is

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[1] An alternative series of frequencies that would allow readouts at any multiple of 50 milliseconds would be obtained by dividing 1 MHz by (5**3)x(2**2), (2**5)x3x5, and (2**5)x3x(5**3) to obtain 2.083 kHz, 2.000 kHz, and 83.3 Hz, respectively, and using 2.000 kHz as the offset frequency for the 500 MHz transmitted to the antenna. The divider chains would require slightly more IC's than are used in the present scheme.

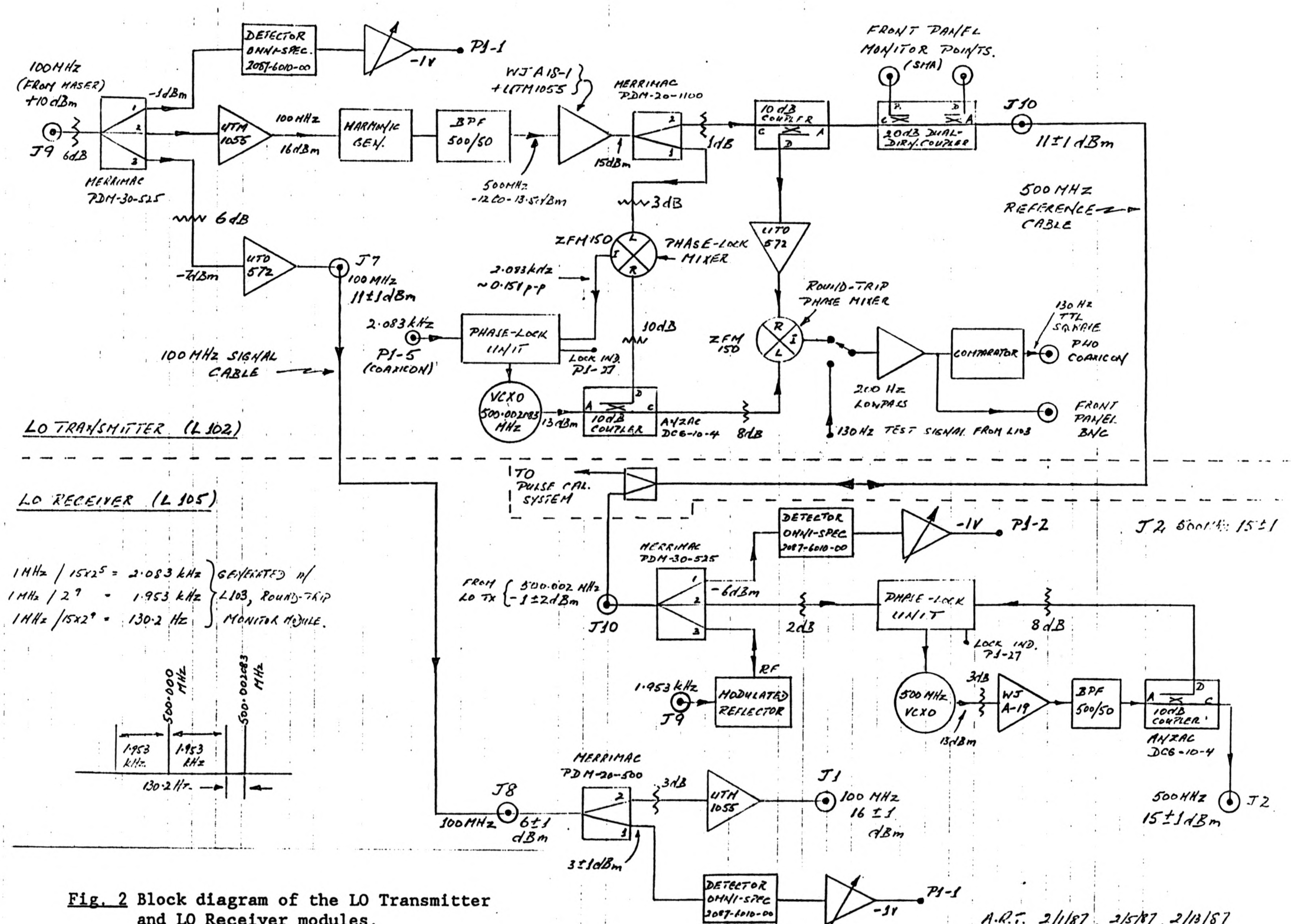


Fig. 2 Block diagram of the LO Transmitter and LO Receiver modules.

A.R.T. 2/1/87, 2/5/87, 2/13/87
2/18/87 2/27/87, 6/2/87, 7/23/87, 9/28/87
[redacted]87, [redacted]87, [redacted]/87 [redacted]10/8[redacted]

shown in Fig. 3. The amplifier circuit board includes two of these amplifiers, only one of which is used in the LO Transmitter, but both are used in the LO Receiver. The third output from the power splitter is amplified and goes to the LO Receiver.

The second output of the splitter goes to a harmonic generator to produce 500 MHz. The generator uses a design by R. Mauzy, and is shown in Fig. 4. The 500 MHz is then split and one output goes through a cable to the LO Receiver in the antenna. Before leaving the LO Transmitter it passes through a dual directional coupler with outputs on the module front panel. This coupler is included to monitor the signals on the cable. The other 500 MHz signal is used to drive the L-port of the phase-lock mixer at a nominal level of 10 dBm. Note that this level is not critical, and a range of 7 to 13 dBm is satisfactory. The phase-lock mixer is used in the phase locked loop that locks the VCXO at 500.002083 MHz. A description of the circuitry in the phase lock unit is given in the section that follows. The signals returned down the 500 MHz line from the modulated reflector are sampled by a 10-dB coupler and fed through an amplifier to the round-trip phase mixer. Note that the amplifier provides isolation to prevent signals at 500.002083 Mhz that leak through the mixer from contaminating the outgoing 500 MHz. The signal from the I-port of the mixer contains the required 130.2 Hz component which is selected out by a 200 Hz lowpass amplifier, and then turned into a TTL squarewave by a comparator. A block diagram of the amplifier and comparator is shown in Fig. 5. The squarewave from the comparator goes to the Round-Trip Monitor module (L103). A switch at the input of the lowpass amplifier allows for connection to a 130.2 Hz reference waveform from the Round-Trip Monitor module for test purposes, including checking of the phase stability of the lowpass amplifier.

(3) The LO-Transmitter Phase Lock Unit.

A circuit diagram of the unit is given in Fig. 6. A digital phase detector type MC4044, U6 in the diagram, receives inputs at 2.083 kHz on pins 1 and 3. One of these is the beat frequency between the high frequency reference and the VCXO frequency that comes from the I-port of the phase-lock mixer, and the other is a TTL-level squarewave at 2.083 kHz that is generated in the Round-Trip Monitor module. The output of the MC4044 (pins 5 and 10) feeds an integrating amplifier, LH0022 (U7), the output of which goes to the frequency control of the VCXO via a buffer amplifier (U10). The output of the MC4044 varies over a range of approximately 0.8 to 2.1 volts as the relative phase on its inputs varies. Pin 12 of the LH0022 is held at 1.5 volts, and the action of the loop drives the MC4044 to equalize the input voltages of the LH0042.

The two inputs to the phase detector can be transposed by means of jumper wires on the circuit board to obtain high or low lock, i.e. the VCXO locked at 2.083 kHz higher or lower than the high frequency reference at the phase lock mixer, respectively. High lock is used in the LO Transmitter, but in an earlier version of the LO Receiver this phase lock unit was used in the low-lock mode.

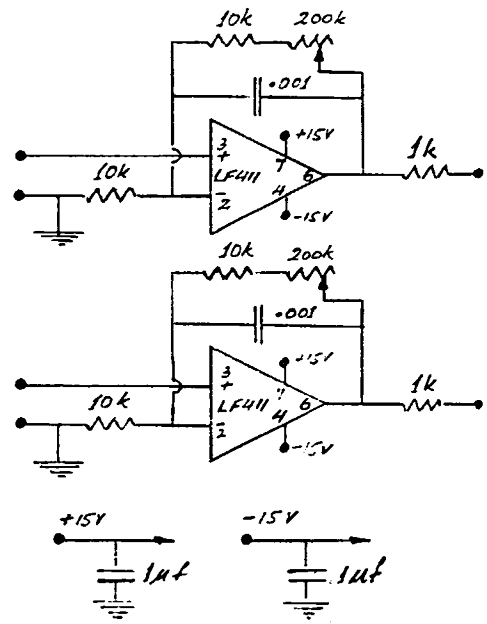


Fig. 3 Amplifier circuits for the outputs of the level-monitoring detectors. The 200k trimpots allow the outputs to be set to a standard value of -1 volt when the monitored signal has the desired level.

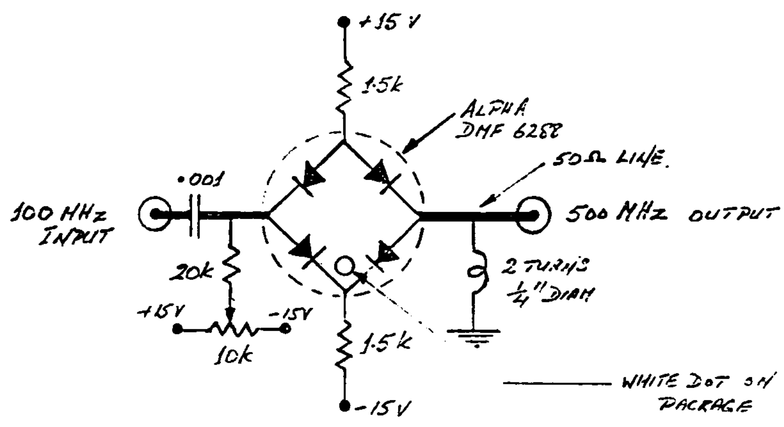


Fig. 4 X5 Multiplier circuit. The 10k trimpot is adjusted to minimize the amplitude of even-order harmonics in the output.

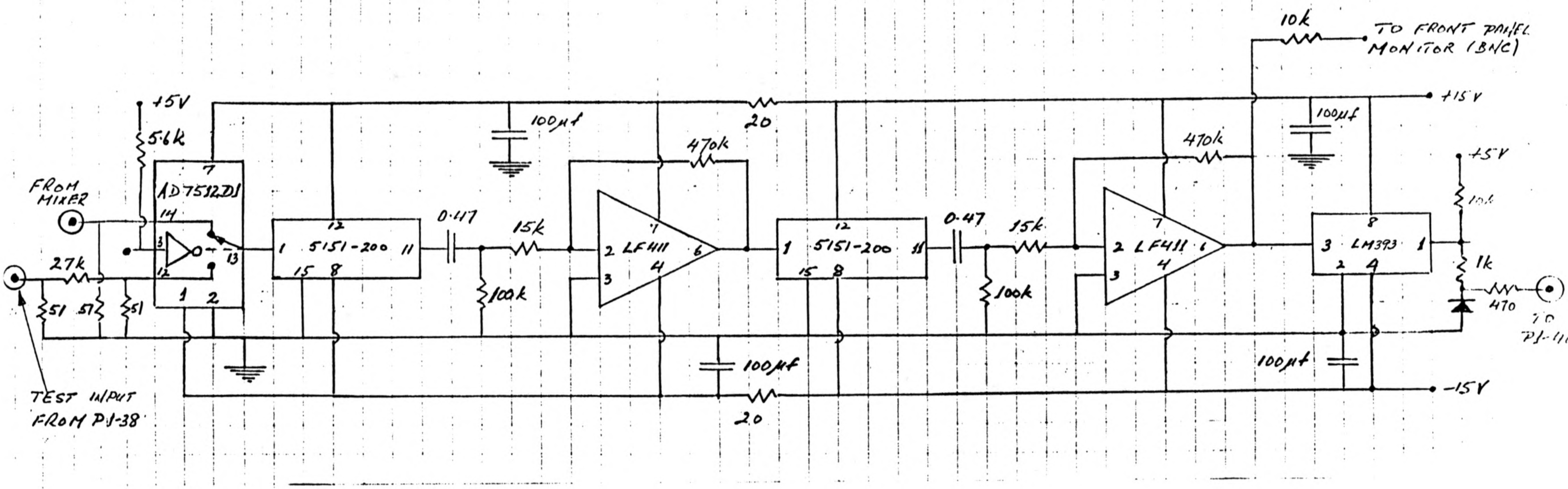


Fig. 5 Circuit of 130 Hz amplifier and comparator. The amplifier contains two active lowpass filter units with cutoff frequency 200 Hz.

A.L.T. 4/7/87
7/1/87 11/30/89

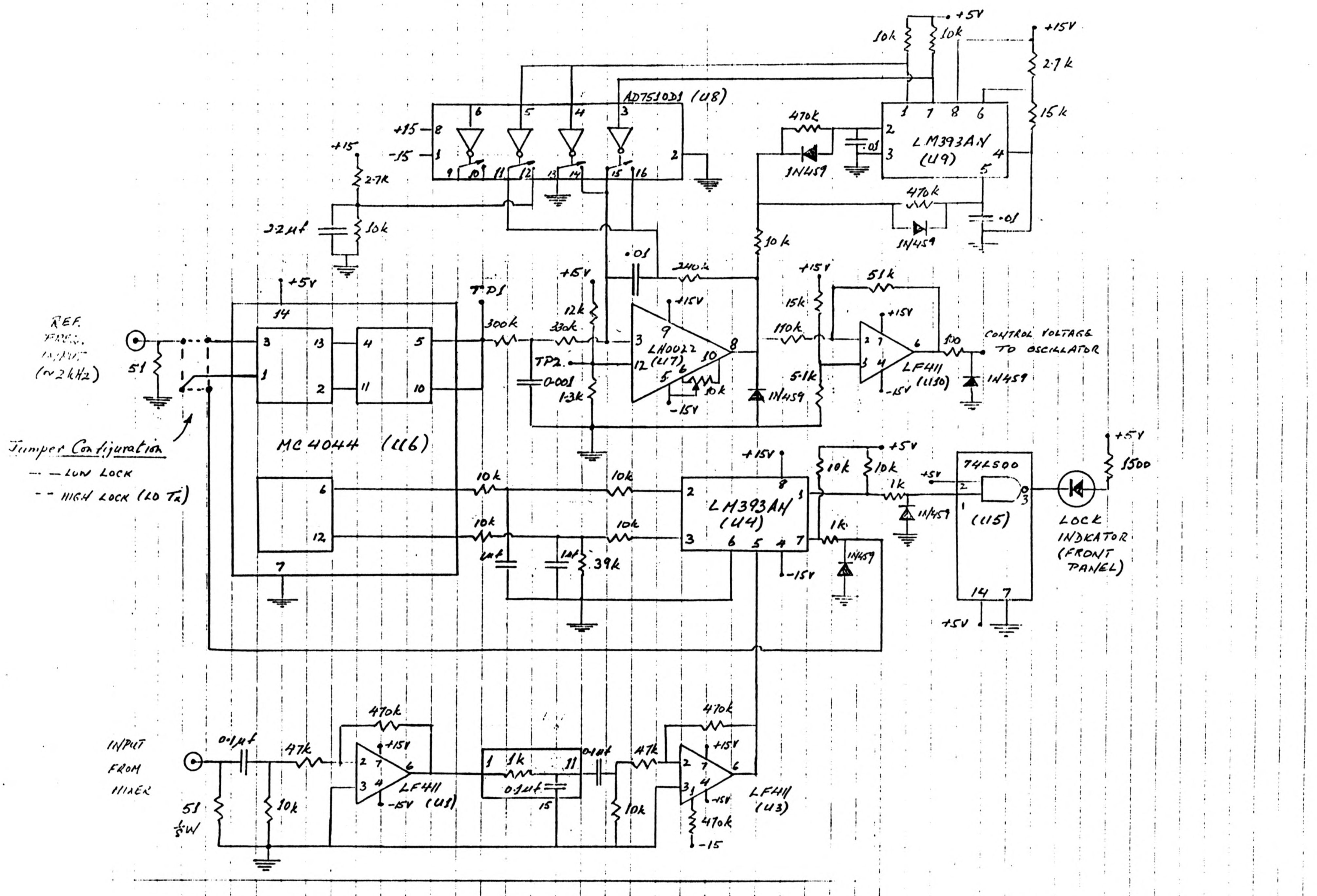


Fig. 6 Circuit diagram of phase lock unit used in the LO Transmitter module. This unit is designed for use with input signals near 2 kHz.

J.R.T. 5/1/86, 12/19/86, 4/23/87
6/4/87, 6/30/87,
7/5/89, 8/1/89, 11/6/89,
[redacted] 1/10/[redacted] 5/9[redacted]/91. [redacted]

The input from the phase-lock mixer is amplified in a lowpass amplifier consisting of two LF411 IC's (U1 and U3). As initially designed a 5151-2500 lowpass active filter (U2) with cutoff at 2.5 kHz was also included, but it was found to be better to replace this with a single RC time constant (1k and 0.1 μf) mounted on a dip header. In order to use the frequency discriminator action of the MC4044 to cause the loop to move into lock, the amplifier must pass the beat frequency from the mixer for any frequency within the tuning range of the VCXO. The single pole response allows this. The output signal from the LF411 stages goes to pin 5 of the LM393AN comparator (U4) which produces a TTL squarewave to drive the MC4044. The MC4044 also serves as a lock detector, and drives input pins 2 and 3 of comparator U4. When the loop is locked, pin 3 is positive with respect to pin 2, and when the loop is unlocked it is negative.

The MC4044 acts as a frequency comparator as well as a phase detector. Thus when the system is first switched on the LH0022 integrator should slew the VCXO into lock. In the case of the high-lock configuration, the system will go directly into lock so long as the VCXO frequency is higher than the 500 MHz reference at the phase-lock mixer. If the system happens to come up with the VCXO lower than the reference, the frequency comparator action will slew the VCXO away from lock until the LH0022 reaches the end of its range. (In the low-lock case the corresponding problem arises if the VCXO comes up at a higher frequency than the reference.) The solution is to detect when the integrator hits one end of its range and then make it jump to the other end, from which it will go straight into lock. This is accomplished using the comparator U9 and the FET switches AD7510D1 (U8). If the integrator output on pin 5 of U9 exceeds the 13 volts on pin 6, the switch at pins 15-16 of U8 closes and discharges the integrating capacitor (0.01 μf), causing the integrator output to fall to zero. If the output of the integrator on pin 2 of U9 goes below zero volts, the switches at pins 11-12 and 13-14 of the AD7510D1 both close charging the integrating capacitor up to 12 volts, and thus causing the integrator output to jump to the same value. Note that the connections from pin 8 of the LH0022 to pins 2 and 5 of U9 each contain 470k in parallel with a diode. This arrangement allows the comparator to follow the slewing of the LH0022 with a short time constant, but presents a longer time constant when the LH0022 jumps across its range, in order to give adequate time for the integrating capacitor to charge or discharge. If the lock is broken by removing one of the reference signals, the LH0022 will sweep across its range and jump back repetitively, producing a sawtooth waveform. The sweep period is usually about 100 msec, but both the direction and rate of the sweep depend upon the voltage from the MC4044, which in turn depends upon what the inputs to that IC happen to be. The loop will automatically go into lock as soon as the lock conditions are restored.

The components that determine the response of the loop are shown in Fig. 7. The MC4044 gain constant (phase sensitivity) is 0.12 volts/radian. The tuning sensitivity of the VCXO, Vectron CO-283VW-OR, is 8 kHz/volt at the oscillator terminal, but in the loop it is effectively 3.7 kHz/volt since it is fed through the buffer stage, U10, with voltage gain 0.46. The buffer is inserted to reduce the voltage range applied to the oscillator to approximately 0 - 6 volts. With these parameters and the R and C values in Fig. 7, the natural frequency of the loop is 104 Hz and the damping factor is 0.79.

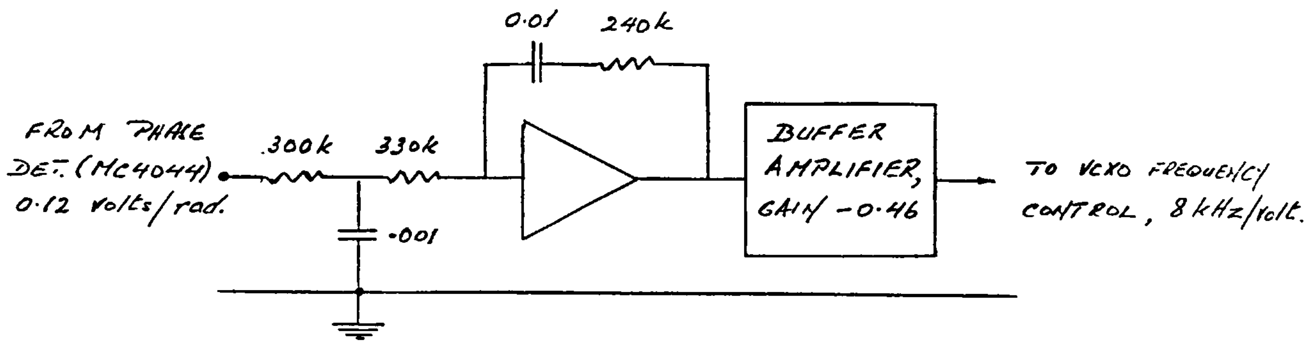


Fig. 7 Parameter values that determine the bandwidth and damping characteristics of the LO Transmitter phase-locked loop.

(4) Inputs and Outputs of the LO Transmitter.

OSP Connectors, Rear Panel

J7	100 MHz output
J9	100 MHz input
J10	500.000 MHz output

42-Pin AMP Connector, Rear Panel

1	Monitor detector level for 100 MHz
5	(coaxicon) 2.08 kHz input
10	+5 volts input
16	+15 volts input
17	-15 volts input
25	130 Hz amplifier input switch control, TTL high for input from mixer and TTL low for test signal
27	Lock indicator, TTL low for loop in lock
34	Ground
38	(coaxicon) 130 Hz test signal input
40	(coaxicon) 130 Hz output from amplifier and comparator unit
42	Ground

Front Panel

BNC	Output waveform of 130 Hz amplifier
LED	Lock indicator, on for loop in lock

SMA connectors, coupled arm of directional coupler to monitor signals in 500 MHz line

(5) Checkout of the LO Transmitter.

The following procedure refers to checkout of the module on the bench. Further checkout of the overall function, in particular the measurement of round trip phase, should be made with the module in the rack. Refer to the LO Transmitter block diagram in the upper half of Fig. 2. Apply a 100 MHz signal at 10 dBm level to the J9 OSP connector.

(1) Check the output of the monitoring detector and set the gain of the amplifier that it drives to provide -1 volt at pin 1 of the 42-pin connector for 10 dBm input at 100 MHz.

(2) Check the 100 MHz output at J7 OSP connector. It should be 11 ± 1 dBm. The second harmonic at this point should be about 23 dB below the 100 MHz level. If necessary adjust the attenuator at the input of the three-way power splitter, or the attenuator at output 3 of the splitter.

(3) Remove the 500/50 MHz filter at the output of the harmonic generator and monitor the output at this point with a spectrum analyzer. The amplitudes of the even harmonics of 100 MHz can be varied by adjusting the potentiometer on the board in the harmonic generator box. Adjust to

minimize the levels of the 400 and 600 MHz harmonics. The level at 500 MHz should be -12 to -13.5 dBm. If necessary, adjust the attenuator at the input of the three-way power splitter and repeat check (2).

(4) At the output of the two-way power splitter for the 500 MHz signal the 500 MHz level should be 11-12 dBm. The second harmonic at 1 GHz should be about 28 dB down, and the other harmonics of 100 MHz should be at least 50 dB down. The output level at OSP connector J10 should be 11 ± 1 dBm.

(5) Check the input waveform to the phase-lock unit from the I-port of the phase-lock mixer. It should be 0.05-0.15 volts p-p, and will not be a clean sine wave because the VCXO should be sweeping in frequency. The output of the module at OSP connector J10 should be terminated for this measurement.

(6) Adjust the phase-lock unit following the steps described below. Refer to the circuit diagram in Fig. 6.

(a) Remove IC's MC4044 and AD7510 from the board and connect test point TP1 (pins 5 and 10 of MC4044) to TP2 (pin 12 of LH0022). Monitor pin 6 of LF411 with an oscilloscope or test meter. The voltage at this point can be made to slew both positive and negative by adjustment of the offset pot for the LH0022. The pot should be set so that the voltage can be held steady (drift rate no more than, say, 0.1 volt in 30 sec.) near 2 volts, which is close to the output to the VCXO frequency control when the loop is in lock. Replace IC's.

(b) Check the waveform at the frequency control terminal of the VCXO. The voltage should sweep repetitively between -0.5 and 5.5 volts (± 0.5 volts) with a period of about 100 msec. Pin 8 of the LH0022 similarly sweeps between approximately 2 and 13 volts.

(c) Apply to pin 5 of the 42-pin Amp connector a TTL-level squarewave at 2 kHz frequency from a manually variable source. The loop should lock. The lock condition can be verified by varying the 2 kHz input frequency and noting the corresponding variation in the input waveform from the phase-lock mixer, or the variation of the VCXO control voltage. Note that it is useful to display the phase-lock mixer waveform and the 2 kHz TTL reference on two traces of an oscilloscope, with the sweep locked to the latter waveform. The mixer waveform should have a good sine wave shape with no obvious harmonic distortion or phase jitter. If there is jitter, it may be due to the RF reference input to the module at 100 MHz or 500 MHz, especially if a synthesized signal generator is being used. In tests in Charlottesville, a crystal oscillator was found to provide a more stable reference.

(d) In case of failure to lock, check the action of the phase detector as follows. Connect the frequency control terminal of the VCXO to a source of about 1.5 volts, and adjust this so that the output of the phase-lock mixer is a sine wave of frequency approximately 2 kHz. A squarewave version of this frequency appears at the MC4044, on pin 3 in an LO Tx or pin 1 in an LO Rx. The reference from the 2-kHz source will appear on the other pin of the pin-1/pin-3 pair. Monitor the output of the MC4044 at TP1 with an oscilloscope. The waveform is complicated, but the mean voltage should be approximately 2.1 when the frequency on pin 3 is greater than that on pin 1, and 0.8 when this condition is reversed. The voltage on TP2 should be intermediate between these two values.

(e) Check the operation of the lock detector. The lock detector senses the relative voltage of pins 6 and 12 of the MC4044. Monitor these voltages at pins 2 and 3 of the comparator U4. With the loop locked, pin 3 should be about 1 volt positive with respect to pin 2, and with the loop unlocked it should be negative. If one or both of the 100 MHz and 2 kHz inputs to the module have been removed to obtain the unlocked condition, this will affect the measured voltage.

(f) If the 100 MHz is being supplied by a synthesized signal generator, run the frequency up and down in 0.1 kHz steps. The loop should typically stay in lock over a range of -2 to +3.5 kHz of the 100 MHz, i.e. -10 to +17.5 kHz variation of the 500 MHz reference input to the phase-lock mixer. It is useful to display the VCXO control voltage on an oscilloscope during this check.

(g) On U3 (LF411) in Fig. 6 the purpose of the 470k resistor to -15 volts from pin 1 is to make the output of the amplifier slightly negative (about - 20 mv) when there is no input from the phase lock mixer. The output at pin 7 of comparator U4 is then TTL low, rather than indeterminate as it would be with zero output from U3. A TTL high on pin 7 of U4 with no signal from the phase lock mixer could cause the lock detector to give a false indication of lock. Check the U3 output level with no signal by removing the DIP header in the amplifier chain.

(7) Checkout of 130 Hz amplifier and comparator. Refer to Fig. 5 for the circuit diagram. The gain of the amplifier should be checked. At 130 Hz the voltage gain factor from the input terminal to pin 3 on the LM393 comparator should be in the range 800-1000. The lowpass response should have reduced the voltage gain by a factor of approximately 2 at 210 Hz and approximately 10 at 280 Hz. Pin 25 of the 42-pin connector should be high or open to connect the input of the amplifier to the signal input connector on the amplifier box.

(6) List of Drawings, Artwork, and Bills of Materials for LO Transmitter.

Schematic and Logic Diagrams	
Phase Lock Circuit for 2 kHz Reference	B53304S002 Rev F
130 Hz Amplifier and Comparator	B53304S004
X5 Multiplier	A53304S005
Monitor Detector Amplifiers	A53304S006 Rev A
2-Stage 500 MHz Amplifier	A53304S008
Bills of Materials	
L102 Module	A53304B003*
Phase Lock Unit for 2 kHz Reference	A53304B002
130 Hz Amplifier and Comparator	A53304B004
X5 Multiplier	A53304B005

Monitor Detector Amplifier Board	A53304B006
2-Stage 500 MHz Amplifier	A53304B008
Assembly Drawings	
L102 Module Assembly	D53304A003 Rev C*
Phase Lock Unit for 2 kHz Reference	C53304A013
Phase Lock Board for 2 kHz Reference	B53304A002 Rev F
130 Hz Amplifier and Comparator Board	B53004A004 Rev A
X5 Multiplier Board	A53304A005
Monitor Detector Amplifier Board	A53304A006
2-Stage 500 MHz Amplifier	A53304A008 Rev A
Printed Circuit Boards	
Phase Lock Board for 2 kHz Reference	B53304Q002 Rev F
X5 Multiplier Board	B53304Q004 Rev A
Monitor Detector Amplifier Board	B53304Q005 Rev B
Board for 130 Hz Amplifier and Comparator	B53304Q006 Rev A
Mechanical Drawings	
Center Mounting Plate	D53304M003 Rev D
Module Front Panel	B53304M001 Rev A
Box for Phase Lock Unit, 2 kHz Reference	B53304M006 Rev A
Component Mounting Spacers	B53304M008 Rev B
Box for 130 Hz Amplifier and Comparator	B53304M009 Rev A

* Requires updating as of 12/10/91.

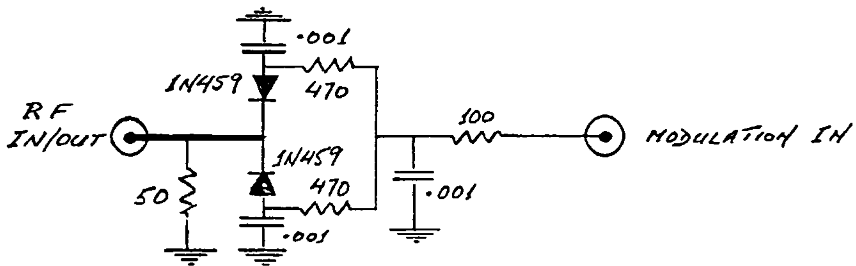
(7) Design of the LO Receiver Module.

A block diagram of the LO Receiver is shown in the lower half of Fig. 2. An input reference signal at 500.000 MHz from the LO Transmitter is applied at J10. This signal is split in a three-way power divider. The first output goes to a monitoring detector, the output of which is amplified to -1 volt in an amplifier for which the circuit is shown in Fig. 3.

The second output of the power divider is used to lock a VCXO at 500.000 MHz, using a phase-lock unit of the type described below in section 8. The VCXO output is filtered to remove harmonics of the frequency of the crystal (62.5 MHz) and harmonics of 500 MHz. The signal used to lock the VCXO comes from a 10 dB coupler and goes to the VCXO port of the phase lock unit.

The third output of the 500 MHz power splitter goes to the modulated reflector that produces sidebands at ± 1.953 kHz, which are returned for the round-trip phase measurement. The circuit of the modulated reflector is shown in Fig. 8.

The 100 MHz reference signal from the LO Transmitter enters at J8, and is split two ways. One component is amplified and provides the output at J1. The other goes to a monitoring detector, the output of which is amplified to -1 volt.



<u>Fig. 8</u> Circuit of the modulated reflector.

(8) The LO-Receiver Phase Lock Unit.

A circuit diagram of the phase lock unit is given in Fig. 9. It is designed to operate with both VCXO and reference frequencies of 500 MHz as inputs. Input levels for these two signals are both -4 ± 2 dBm. With 14.5 dB typical gain in the A18-1, and allowing 3.5 db attenuation in the DS-327 power divider and the JH-140 hybrid, the input levels to the PD-120 phase detectors are 7 ± 2 dBm. Of the two phase detectors in Fig. 9, the one on the right controls the phase lock loop and the one on the left the lock detector.

The output of the loop PD-120 drives the integrating amplifier LH0022 (U5), which drives a LF411 (U1) inverting amplifier with voltage gain of -0.46. The output of the LF411 stage controls the frequency of the VCXO. Note that at the VCXO a diode is connected from the frequency control terminal to ground to protect the VCXO from any negative voltage that might accidentally occur at that point. (In the LO Transmitter a similar protective diode is located in the phase lock unit.) If the loop is not locked, the lock indicator circuitry causes pin 4 of the AD7510D1 (U6) to be at TTL high, so the switch at pins 13-14 is closed. (The AD7510D1 switches are closed with TTL high on the control inputs.) Thus the summing junction of the LH0022 is connected through 2 M to -15 volts, which causes the output to sweep positive. When it goes higher than the 13.2 volts on pin 2 of the LM393 (U1), pin 1 goes high and the switch at pins 11-12 of AD7510D1 shorts the integrating capacitor C1. The output of the LH0022 then falls to zero and starts to sweep up again in voltage until lock is obtained. The sweep action is similar to that described for the LO transmitter phase lock unit. At the output of the LF411 that controls the VCXO frequency (U1), the sweep is negative going, from 6 to 0 (±0.5) volts. The printed circuitry associated with U1 has been designed so that if the existing components are removed it can be reconnected as a non inverting amplifier, which may be convenient if the unit is ever used with a different VCXO.

When the loop is in lock the output of the lock-detector PD-120 is approximately -0.3 volts, and this is amplified by a factor of -10 in U3 and applied to pin 6 of the LM393 (U2) comparator. The voltage on pin 5 of the LM393 is set to 2.8 volts, and thus the output on pin 7 is at TTL low for lock and high for no lock. When the loop is locked this voltage from pin 7 opens the contacts at pins 9-10 of the AD7510D1 (U6), and thereby lights a front panel LED. Note that if the loop is not locked but the VCXO is producing a low frequency beat waveform at the output of the lock detector PD-120, the LED may glow faintly, being lit on the negative half cycles of the beat waveform. This effect is reduced by the 0.002 μf capacitor in parallel with the 47k feedback resistor of U3, which reduces the frequency response. Note that this capacitor must not be too large or it will slow down the lock detector action. The lock detector must open the switch at pins 13-14 of the AD7510D1 quickly enough to stop the sweep action when lock is found or lock will not be retained.

If a frequency of 500 MHz is applied to one input terminal of a PD-120 phase detector, and a frequency a few kHz different is applied to the other, both at a level of 7 dBm, the output shows the beat frequency as a triangular waveform of amplitude 0.7 volts p-p. This becomes a sinusoid only if the

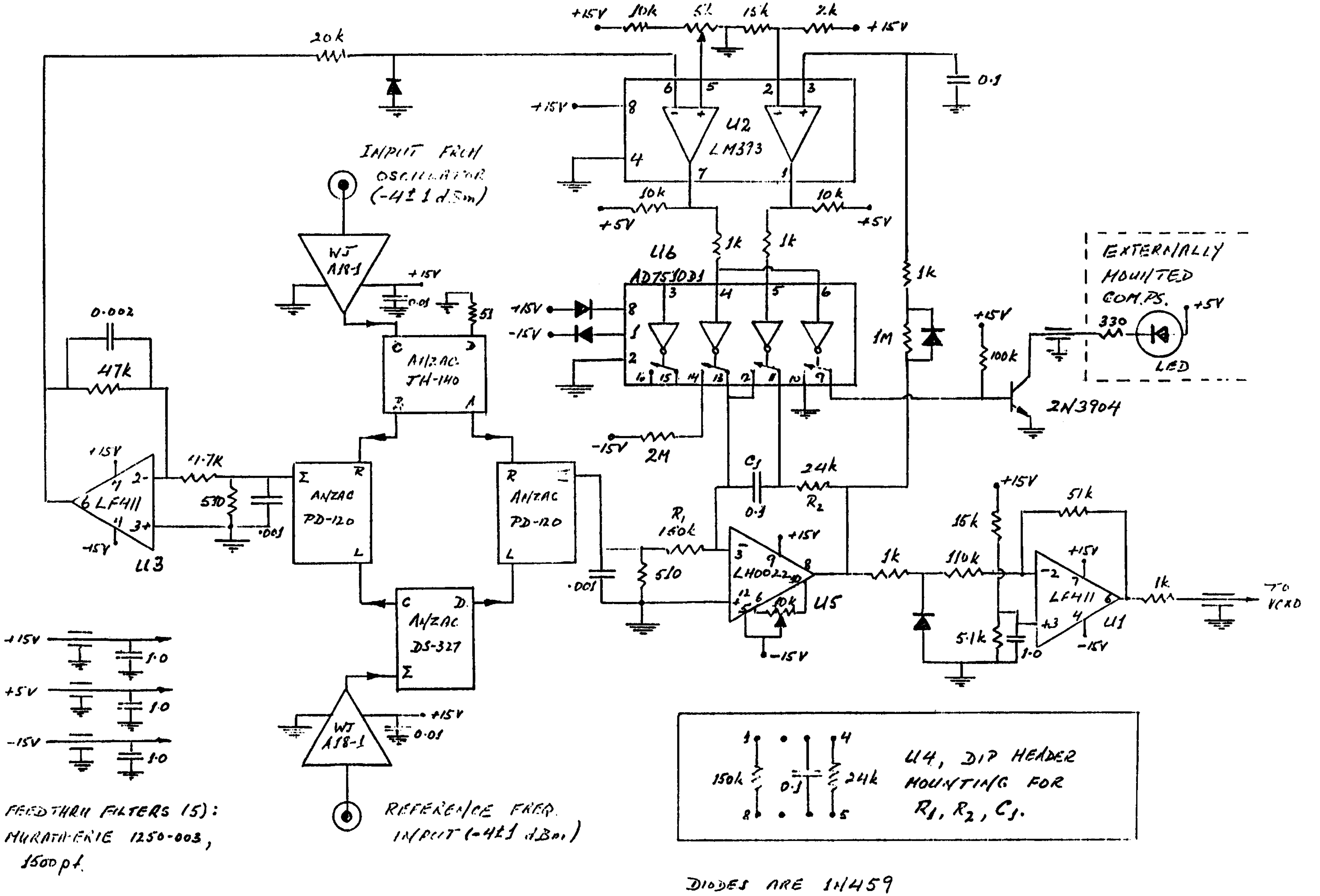


Fig. 9 Circuit diagram of the phase lock unit used in the LO Receiver module. This unit is designed for use with input signals at 500 MHz.

1/17/92.

inputs are reduced to 0 dBm. The recommended level on the PD-120 data sheet is 7 dBm, and the phase sensitivity is then 0.22 volts/radian. (Note this is a measured value which was consistent for several individual units. The value indicated by the curve in the PD-120 data sheet is 8.5 mv/deg. or 0.48 volts/radian, which appears to be wrong). Then for a tuning constant of 8 kHz/volt for the VCXO, values of R1=150k, R2=24k and C1=0.1 μf, and the LF411 stage gain of 0.46, the natural frequency of the loop is 93 Hz and the damping factor is 0.70. The components R1, R2, and C1 are mounted on an eight-pin DIP header (U4) on the board for convenience in adjustment.

(9) Inputs and Outputs of the LO Receiver.

OSP Connectors, Rear Panel

J1	100 MHz output
J2	500 MHz output
J8	100 MHz input
J9	1.953 kHz input
J10	500 MHz input

42-Pin AMP Connector, Rear Panel

1	Monitor detector level for 100 MHz
2	Monitor detector level for 500.002 MHz
10	+5 volts input
16	+15 volts input
17	-15 volts input
27	Lock indicator, TTL low for loop in lock
34	Ground
42	Ground

Front Panel

BNC	Loop voltage at oscillator frequency-control terminal
LED	Lock indicator, on for loop in lock

(10) Checkout of the LO Receiver.

Refer to the block diagram in the lower half of Fig. 2. The nominal input level for the 500 MHz signal is -1 dBm, which allows for 14 dB of cable loss, and the loss at a two way power splitter that provides a reference to the pulse calibration system.

(1) Apply -1 dBm at 500 MHz to OSP connector J10 and check the output level of the monitoring detector at output 1 of the three-way power splitter. Set the output of the detector amplifier to -1 volt.

(2) Check and adjust the phase-lock unit (Fig. 9) as follows.

(a) Remove IC's except for A18-1 amplifiers. Insert signals at approximately 500 MHz but differing in frequency by a few kHz into the two inputs. The signal levels should be -4 ± 2 dBm. One of the inputs will be from the VCXO, and for this test it is convenient to disconnect the frequency control signal to the VCXO and ground the terminal at the oscillator. The other input can be from a signal generator applied to OSP connector J10. At the outputs of the two PD-120 phase detectors the beat waveform should have an approximately triangular sawtooth profile. Amplitudes should be between 0.65 and 0.80 volts p-p. DC offsets should be no more than a few mv. The waveforms from the two phase detectors should be in phase quadrature.

(b) Insert the LH0022 (U5). Remove RF inputs to the unit and ground the output of the loop phase detector. This grounding can be done by connecting pins 7 and 8 on the DIP header (U4). Monitor pin 8 of the LH0022 and adjust the 10k trimpot for this IC so that a voltage of a few volts remains steady as described for the transmitter phase lock unit. Remove the phase detector grounding.

(c) Insert the other IC's. Set the 5k trimpot so that the potential on pin 5 of the LM393 (U2) is 2.8 volts. Set up a condition in which the loop cannot lock: e.g. remove reference input or remove the frequency control to the VCXO and ground the terminal on the VCXO. The control output from the loop to the VCXO should sweep with a period of about 200 ms from 6 ± 0.5 volts to zero or -0.5 volts. With all connections restored the loop should now lock.

(d) Vary the reference frequency and the VCXO should be able to lock over a range of about 20 kHz. The range may not be centered on 500 MHz, and the center frequency will depend on the individual VCXO. Monitor the frequency control voltage of the VCXO on an oscilloscope and see that it varies as the VCXO follows the reference frequency.

(3) The 500 MHz output power level at J2 should be 15 ± 1 dBm. Adjust the attenuator at the VCXO output if necessary. Also check the signal with a spectrum analyzer. All harmonics and subharmonics should be at least 60 dB below the wanted output.

(4) Insert a dual directional coupler into the 500 MHz input line at J10. Apply a 1.9 kHz, TTL-level signal to OSP connector J9. The level of the sidebands at ± 1.9 kHz on the signal going back from the LO Rx module should be -30 to -35 dB with respect to the forward going signal at 500 MHz to the module. It may be convenient to increase the frequency of the modulation from 1.9 kHz to, say, 10 kHz to help isolate the sidebands if the resolution of the spectrum analyzer is insufficient. The level of the sidebands does not vary significantly with frequency over such a range.

(5) Apply a signal at 100 MHz and 6 dBm to OSP connector J8. The output power at J1 should be 16 ± 1 dBm. If necessary, adjust the attenuator in this signal path at the output of the two way power splitter.

(6) With the same input level at 100 MHz, set the output of the amplifier for the level monitoring detector to read -1 volt.

(11) List of Drawings, Artwork, and Bills of Materials for LO Receiver.

Schematic and Logic Diagrams	
Phase Lock Circuit for 500 MHz Reference	B53304S001 Rev D
Monitor Detector Amplifiers	A53304S006 Rev A
Modulated Reflector	A53304S007
Bills of Materials	
L105 Module	A53304B009*
Monitor Detector Amplifier Board	A53304B006
Modulated Reflector	A53304B007
Assembly Drawings	
L105 Module Assembly	D53304A009 Rev A*
Phase Lock Board for 500 MHz Reference	C53304A001 Rev D
Monitor Detector Amplifier Board	A53304A006
Modulated Reflector Board	A53304A007
Printed Circuit Boards	
Phase Lock Board for 500 MHz Reference	D53304Q001 Rev C (2 parts)
Drill Dwg for above	C53304P001 Rev D
Modulated Reflector Board	B53304Q003 Rev A
Monitor Detector Amplifier Board	B53304Q005 Rev B
Mechanical Drawings	
Center Mounting Plate	D53304M004 Rev F
Module Front Panel	B53304M002
Box for Phase Lock Unit, 500 MHz Reference	C54120M011-4
Rework for above box	B53304M005 Rev C
Top Cover for above box	C54120M009-4
Bottom Cover for above box	B53304M015
Component Mounting Spacers	B53304M010 Rev A (2 parts)

* Requires updating as of 12/10/91.

(12) Specifications and Information Sheets.

VCXO	Vectron CO-283VW-OR
Diode Quad	Alpha DMF6288
Active Filters	Data Delay Devices 5151-200 and 5151-2500
Mixer	Mini-Circuits ZFM-150
Phase Detector	Anzac PD-120
Power Divider	Anzac DS-327
Quadrature Hybrid	Anzac JH-140
Integrated Circuits	(Note that only the first page of catalog information is given for the following items.)
	AD7510D1
	AD7512D1
	LF411
	LH0022
	LM393A
	MC4044
	UTO-572
	UTM-1055
	WJ-A18-1
	WJ-A19

VECTRON
The Crystal Oscillator Company

Vectron Laboratories, Inc.

166 Glover Avenue, Norwalk, Connecticut 06850
Telephone: 203/853-4433 TWX: 710/468-3796

May 20, 1987

National Radio Astronomy
2015 Ivy Rd.
Charlottesville, VA 22903

Attention: Karen Thach

Subject: Your Purchase Order No. B01980

Dear Ms. Thach:

On the subject purchase order you ordered our CO-283VW-R at 500 MHz crystal oscillator. Our part numbering system has recently been revised and the correct part number for this oscillator is CO-283VW-OR at 500 MHz. The enclosed data sheet shows this.

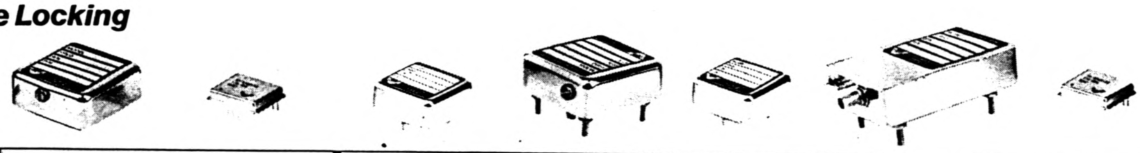
We'd appreciate your confirming order reflecting the "CO-283VW-OR" part and regret any inconvenience this causes you.

Cordially,

Bill Zarkower
Regional Manager

BZ/lls
Enclosure
cc: TVA

VCXOs for Phase Locking



	ECL		SINEWAVE				
Configuration	PC board mount	low profile hybrid DIP	PC board mount		Chassis mount with rf output connector		low profile hybrid DIP
Series	CO-233MEV	CO-434V	(a) CO-233V (b) CO-233VH	CO-233VF	CO-233VFW	CO-283VW-OK	CO-484V
Center Frequency	8-200 MHz	8-200 MHz	(a) 8-149.9 MHz (b) 150-200 MHz	8-400 MHz	8-400 MHz	400.1-600 MHz	8-200 MHz
Output Level	ECL compatible 10K output to 110 MHz MECLIII output above 110 MHz (Complementary output optional)		0.5 Vrms/50Ω (+7 dBm); Option "R": +13 dBm (not available in CO-484V). Harmonics are −20 dBc. Internal multiplier is generally used above 70 MHz, and resulting subharmonics are also −20 dBc. Harmonic and subharmonic levels can be reduced to −30 dBc or −40dBc in CO-233VF, CO-233VFW, CO-283VW and CO-484V.				
Supply	−5.2 Vdc at 30-60 mA		+15 Vdc (+12 Vdc to +24 Vdc optional); current ranges from 15 mA at 8 MHz to 100 mA at 600 MHz				

Deviation/Stability Alternatives

Code	Temperature Range	Temperature Stability	Deviation
0	0/+50°C	±10 ppm	±30 ppm
A	0/+50°C	±20 ppm	±50 ppm
B	0/+50°C	±35 ppm	±100 ppm
C*	0/+50°C	±35 ppm	±200 ppm
D	0/+70°C	±20 ppm	±40 ppm
E	0/+70°C	±40 ppm	±100 ppm
F*	0/+70°C	±40 ppm	±200 ppm
G	−20/+70°C	±30 ppm	±60 ppm
H	−20/+70°C	±40 ppm	±100 ppm
I*	−20/+70°C	±40 ppm	±200 ppm
J	−40/+85°C	±40 ppm	±60 ppm
K	−40/+85°C	±50 ppm	±100 ppm
L*	−40/+85°C	±50 ppm	±200 ppm
M	−55/+85°C	±50 ppm	±100 ppm
N*	−55/+85°C	±50 ppm	±200 ppm

J, K, L*: (−30°C lower limit for ECL models above 110 MHz due to MECLIII IC constraint).

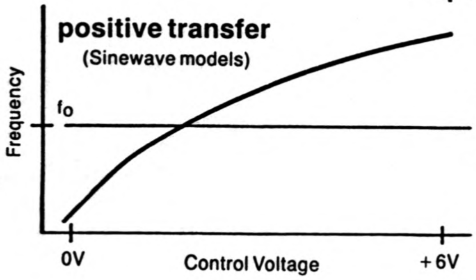
M, N*: (not available in ECL models above 110 MHz due to MECLIII IC constraint).

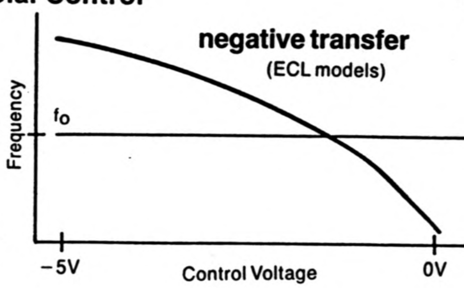
*The following notes apply to options C, F, I, L and N (±200 ppm deviation):
- They are only available at frequencies up to 25 MHz
- Linearity of ±10% is standard

	ECL		SINEWAVE				
Control Voltage	0 to −5V (lowest frequency at 0V) *±3V to ±10V optional for CO-233MEV		0 to +6V positive transfer function (lowest frequency at 0V) *±3V to ±10V optional except for CO-283VW				
	*(With bipolar control voltage option, transfer function is negative, linearity is ±10%, and an additional +12V to +24V supply is required for ECL models)						
Linearity	±20% smooth monotonic characteristic (±10% linearity available) ±10% is standard with bipolar control voltage and with deviation/stability options C, F, I, L and N at frequencies up to 25 MHz						
Modulation Rate	dc to 1 kHz; higher modulation rates available.						
Modulation Input Z	Greater than 50kΩ						
Aging Rate	Hybrid DIP Models: 3-5 ppm for first year, then 2 ppm/year thereafter—less than 20 ppm total over 10 years. Other Models: 5 ppm for first year, then 3 ppm/year thereafter. Option "Y": 2 ppm for first year, 1 ppm/year thereafter.						
Mechanical Tuning Option	"T"	N/A	"T"	"T"	"T"	"T"	N/A
	"T" indicates that a mechanical tuning option is available; add "T" to model number						
Size (See page 66)	2"x3"x½"	0.8"x0.98"x0.2" 16 pin double DIP	1½"x1½"x¾" CO-233V & VH differ in pin configuration	2"x2"x¾"	2"x2"x¾"	2"x3"x¾"	0.8"x0.98"x0.2" 16 pin double DIP

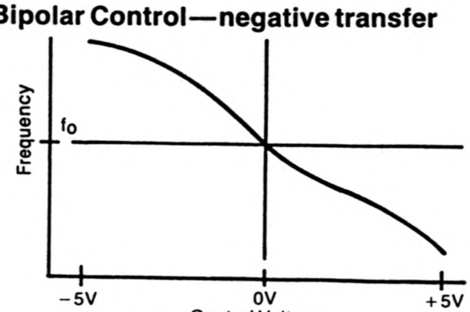
VCXO CHARACTERISTICS

Unipolar Control





Bipolar Control—negative transfer



HOW TO SPECIFY

Hybrid DIP Models

[ ] — [ ] [ ] at [ ]

- Basic model (e.g. CO-401V)
- Deviation/Stability Code
- "X" for standard; "B" for MIL-0-55310 Class B Screen Testing
- Frequency

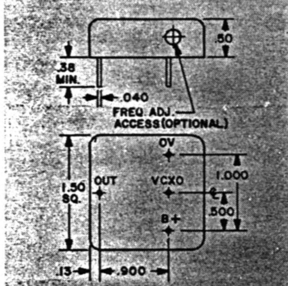
PCB and Chassis Mount Models

[ ] — [ ] [ ] at [ ]

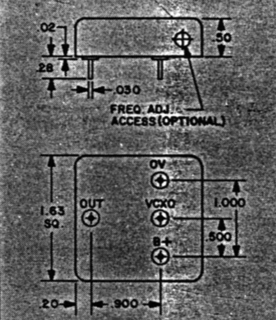
- Basic model (e.g. CO-233VF)
- Deviation/Stability Code
- Any desired lettered options in the following order:
  - T: Mechanical frequency adjust
  - R: +13 dBm sine output
  - Y: Improved aging
- Frequency

OUTLINE DRAWINGS

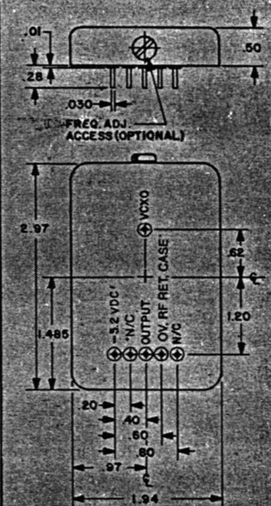
CO-231V CO-236V



CO-231VH

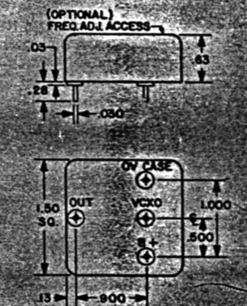


CO-233MEV

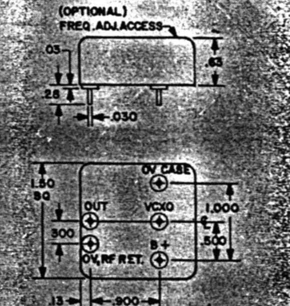


*Q̄ on this pin with complementary output option.

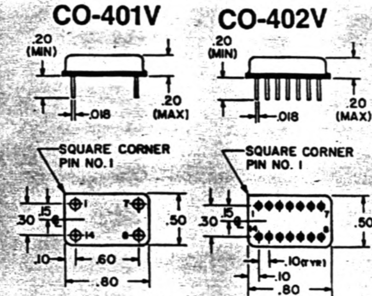
CO-233V



CO-233VH



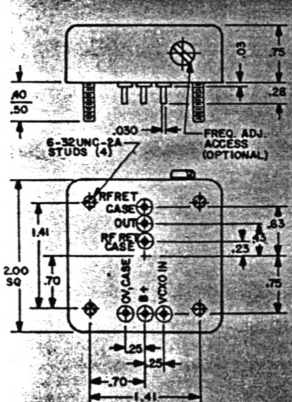
CO-401V CO-402V



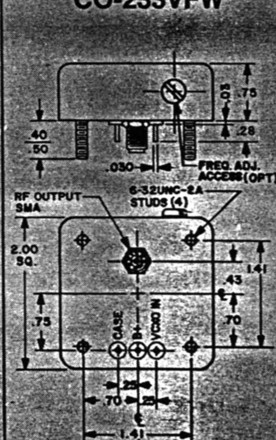
Available with insulated standoffs; increases height to 0.23" maximum

PIN	FUNCTION
1	VCXO
7	OV,Case
8	Output
14	+5V

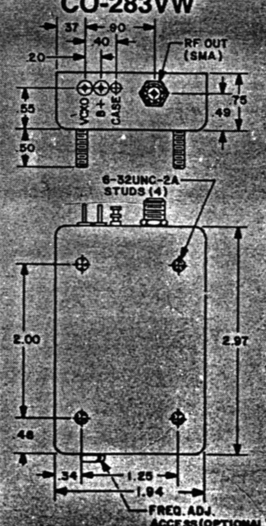
CO-233VF



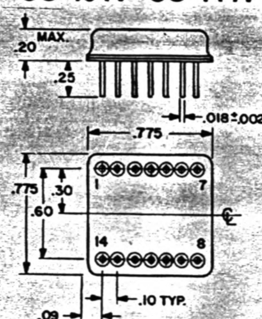
CO-233VFW



CO-283VW



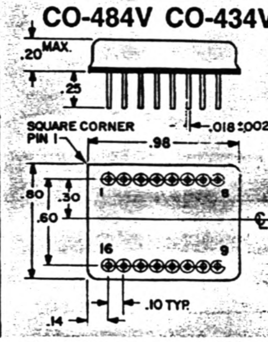
CO-404V CO-444V



PIN	FUNCTION CO-404V	FUNCTION CO-444V
*1	VCXO	VCXO
7	OV,Case	OV,Case
8	Output	Output
14	+5V	+5V

*Dot on top surface identifies pin 1.

CO-484V CO-434V

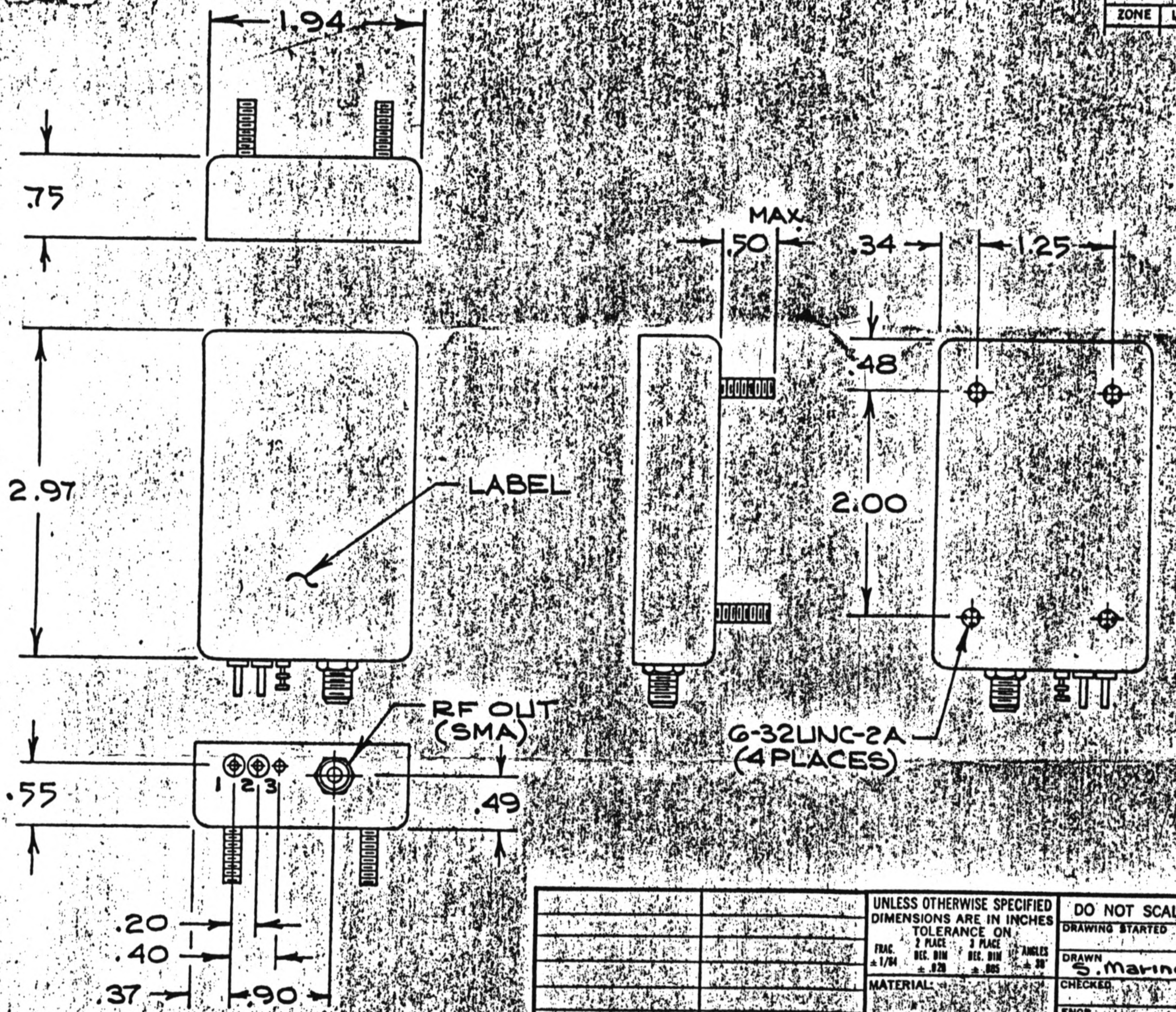


PIN	FUNCTION CO-484V	FUNCTION CO-434V
6	VCXO	VCXO
8	OV,Case	−5.2V*
9	Output	Output
16	Supply	OV, Case

*For complementary output option in CO-434V, Q̄ is on pin 10.

Markings do not appear on units—for reference only; case dimension tolerances are ± .02".

45158



PIN #	FUNCTION
1	VOLT CONTROL INPUT
2	B+
3	OV, CASE

PIN NO'S ARE FOR REF. ONLY
THEY DO NOT APPEAR ON UNIT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON:
FRAC. ±1/64 | 2 PLACE DEC. DIM ±.020 | 3 PLACE DEC. DIM ±.005 | ANGLES ±30'
MATERIAL:
FINISH:

DO NOT SCALE DRAWING
DRAWING STARTED | DATE
DRAWN S. Marino 5/12/83
CHECKED
ENGR

VECTRON
VECTRON LABORATORIES, INC.
NORWALK, CONN.

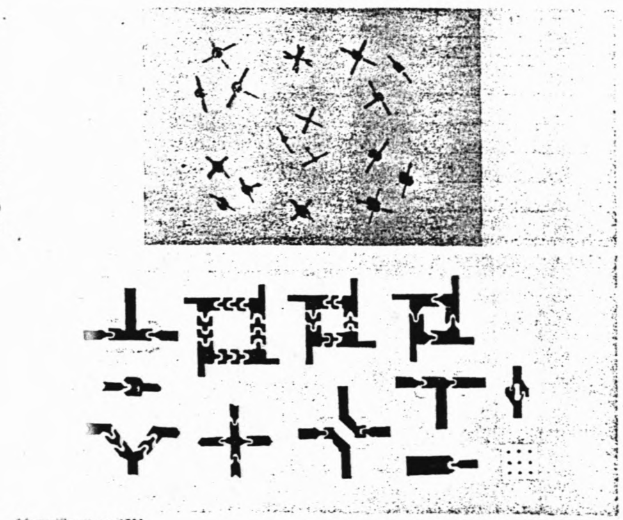
INSTALLATION
UHF OSCILLATOR
CO283 SERIES OSC.

SIZE	CODE IDENT NO.	
B	27802	283-05-006
SCALE FULL		SHEET

Silicon Beam-Lead and Chip Schottky Barrier Mixer Diodes

Features

- Ideal for MIC
- Low 1/f Noise
- Low Intermodulation Distortion
- Low Turn On
- Hermetically Sealed Packages



Magnification: 0.5X

Magnification: 10X

Description

Alpha beam-lead and chip Schottky barrier mixer diodes are designed for applications through 40 GHz in Ka-band. The beam-lead design eliminates the problem of bonding to the very small junction area that is characteristic of the low capacitance involved in microwave devices.

Beam-lead Schottky barrier mixer diodes are made by deposition of a suitable barrier metal on an epitaxial silicon substrate to form the junction. The process and choice of materials result in low series resistance along with a narrow spread of capacitance values for close impedance control.

A variety of forward knees is available, ranging from a low value for low, or starved, local oscillator drive levels to a higher value for high drive, low intermod mixer applications.

The beam-lead diodes are available in a wide range of packages as shown. They may also be mounted on the customer's circuit or on other substrate configurations. For those customers who prefer chip and wire for their MIC work, Alpha can supply a complete line of bondable chips. Capacitance ranges and series resistances are comparable with the packaged devices that are available through Ka-band. The unmounted diodes are especially well suited for use in microwave integrated circuits. The mounted devices can be easily inserted as hybrid elements in stripline, microstrip and other such circuitry.

Applications

Beam-lead and chip Schottky barrier diodes are categorized by noise figure for mixer applications in four frequency ranges: S, X, Ku and Ka-bands. However, they can also be used as modulators, high speed switches and low power limiters.

RF parameters, capacitance and breakdown voltage on chips and beam-lead diodes are tested on a sample basis, while production testing consists of series resistance and forward voltage measurements. A separate data sheet in this section describes beam-lead and chip diodes that are optimized for detector applications.

Several types of semiconductor-barrier metal systems are available, thus allowing proper selection for optimum mixer design. For most applications the N-type silicon, low drive types are preferable, especially for starved L.O. mixers. For doppler mixers, motion detectors or applications requiring low audio (1/f) noise, the P-type silicon, low drive types are preferred. For high level mixer applications requiring low intermodulation products, the N-type silicon, high drive types are most desirable.

Beam-lead diodes are ideally suited for balanced mixers, since they exhibit low parasitics and are extremely uniform. A typical V_f vs I_f curve is shown in Figure 1.

Typical noise figure vs L.O. drive is shown in Figure 2 for single N-type, low drive diode types.

Typical mixer circuits are shown in Figure 3 in order of complexity. The circuits shown in Figures 3a and 3b are recommended for narrower band applications.

The matching network can be an "L" network using discrete components at lower frequencies or a section of transmission line. The double balanced mixer in Figure 3c is recommended for broadband operation where noise figure is less important. The use of high drive diodes in this circuit allows the use of increased L.O. drive with a resultant decrease in intermodulation distortion.

See Sections 2 and 7 for Application Notes:

80800	Mixer and Detector Diodes
80850	Handling Precautions for Schottky Barrier and Point Contact Mixer and Detector Diodes
80000	Bonding Methods: Diode Chips, Beam-Lead Diodes and Capacitors

Silicon Beam-Lead and Chip Schottky Barrier Mixer Diodes

FREQUENCY TABLE

Band	Frequencies (GHz)
S	2 to 4
C	4 to 8
X	8.2 to 12.4
Ku	12.4 to 18.0
K	18.0 to 26.5
Ka	26.5 to 40.0

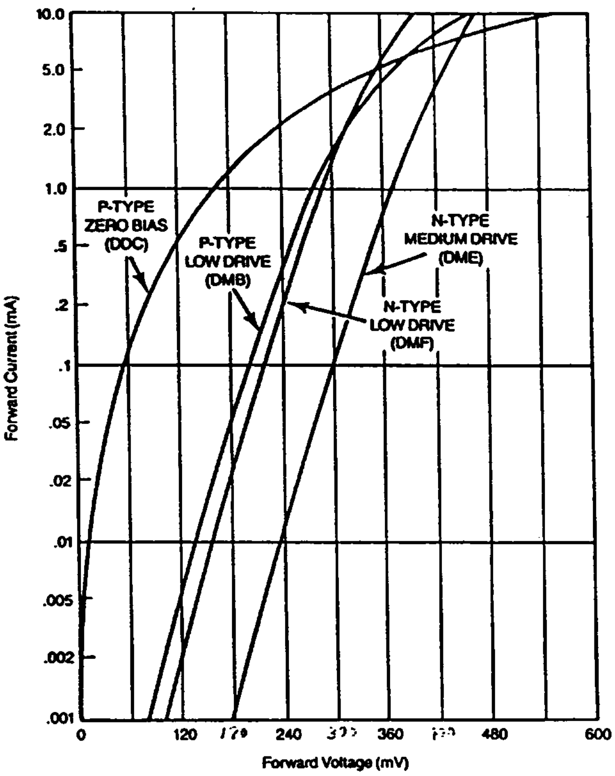


Figure 1a. Typical Forward DC Characteristic Curves — Voltage vs Current

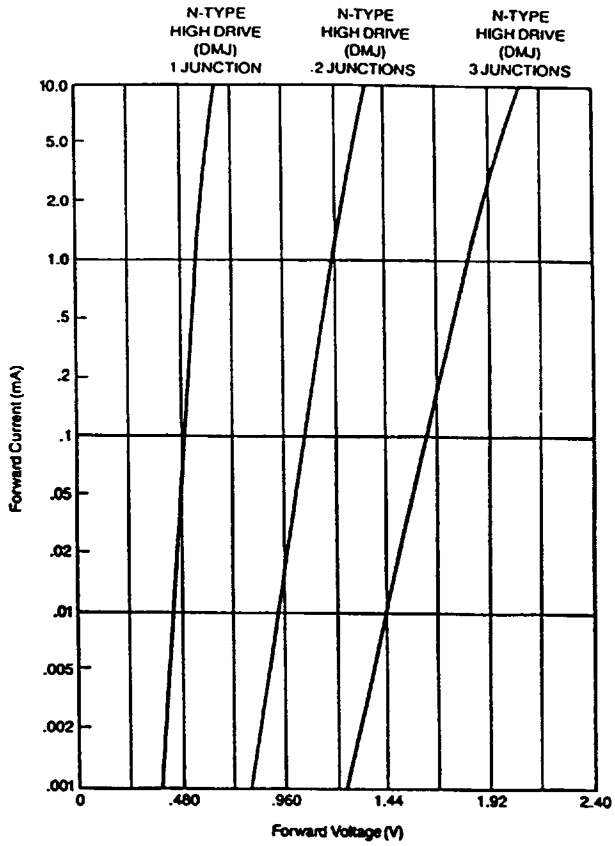


Figure 1b. Typical Forward DC Characteristic Curves — Voltage vs Current

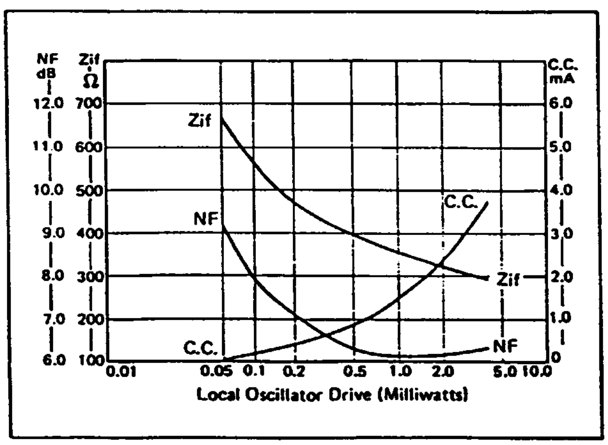


Figure 2. Typical X-Band Low Drive Mixer Diode — RF Parameters vs Local Oscillator Drive

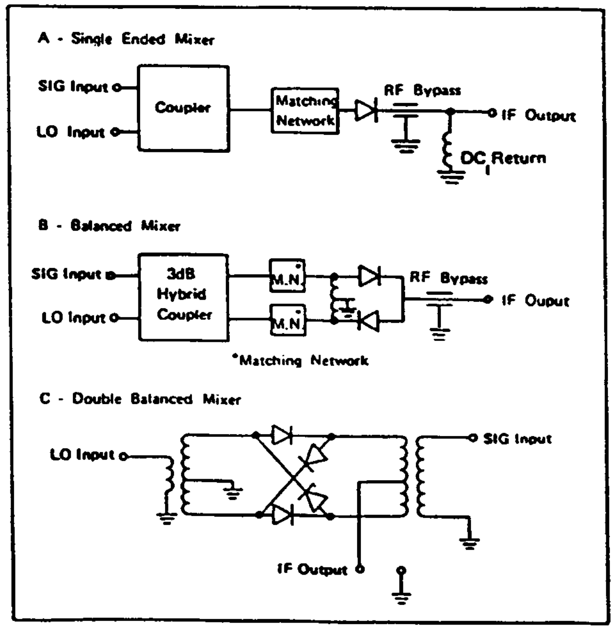


Figure 3. Typical Mixer Circuits

Silicon Beam-Lead and Chip Schottky Barrier Mixer Diodes

Beam-Lead Quad Rings, N-Type, High Drive, 12 Junction

Frequency Band	Type Number	Outline	NF[1] dB Max.	C_J 0V pF Min.	C_J 0V pF Max.	Rs[2] — Ω Max.	V_F 1mA mV Min.	V_F 1mA mV Max.	ΔV_F[4] 1mA mV Max.
Ku	DMJ4766	132-022	—	0.05	0.15	21	1650	2250	25
Ku	DMJ6564	398-022	—	0.05	0.15	21	1650	2250	25

Beam-Lead Quad Bridges, N-Type, Low Drive

Frequency Band	Type Number	Outline	NF[1] dB Max.	C_J 0V pF Min.	C_J 0V pF Max.	Rs[2] — Ω Max.	V_F 1mA mV Min.	V_F 1mA mV Max.	ΔV_F[4] 1mA mV Max.	V_B 10μA V Min.
L	DMF3059	132-004	—	—	1.20	9	225	350	15	1.0
L	DMF4540	337-004	—	—	1.20	9	225	350	15	1.0
S	DMF5848A	132-004	6.0	0.30	0.50	3	225	300	15	2.0
S	DMF5848	132-004	6.5	0.30	0.50	7	225	300	15	2.0
S	DMF3076A	294-004	6.0	0.30	0.50	3	225	300	15	2.0
S	DMF3076	294-004	6.5	0.30	0.50	7	225	300	15	2.0
S	DMF3067A	295-004	6.0	0.30	0.50	3	225	300	15	2.0
S	DMF3067	295-004	6.5	0.30	0.50	7	225	300	15	2.0
S	DMF3063A	325-004	6.0	0.30	0.50	3	225	300	15	2.0
S	DMF3063	325-004	6.5	0.30	0.50	7	225	300	15	2.0
X	DMF6288A	132-004	6.5	0.15	0.30	7	250	325	15	2.0
X	DMF6288	132-004	7.0	0.15	0.30	12	250	325	15	2.0
X	DMF3077A	294-004	6.5	0.15	0.30	7	250	325	15	2.0
X	DMF3077	294-004	7.0	0.15	0.30	12	250	325	15	2.0
X	DMF6558A	295-004	6.5	0.15	0.30	7	250	325	15	2.0
X	DMF6558	295-004	7.0	0.15	0.30	12	250	325	15	2.0
X	DMF4352A	325-004	6.5	0.15	0.30	7	250	325	15	2.0
X	DMF4352	325-004	7.0	0.15	0.30	12	250	325	15	2.0
X	DMF3079A	364-004	6.5	0.15	0.30	7	250	325	15	2.0
X	DMF3079	364-004	7.0	0.15	0.30	12	250	325	15	2.0
Ku	DMF6298A	132-004	7.5	0.05	0.15	16	275	350	15	2.0
Ku	DMF6298	132-004	8.0	0.05	0.15	25	275	350	15	2.0
Ku	DMF3078A	294-004	7.5	0.05	0.15	16	275	350	15	2.0
Ku	DMF3078	294-004	8.0	0.05	0.15	25	275	350	15	2.0
Ku	DMF6574A	295-004	7.5	0.05	0.15	16	275	350	15	2.0
Ku	DMF6574	295-004	8.0	0.05	0.15	25	275	350	15	2.0
Ku	DMF3080A	364-004	7.5	0.05	0.15	16	275	350	15	2.0
Ku	DMF3080	364-004	8.0	0.05	0.15	25	275	350	15	2.0

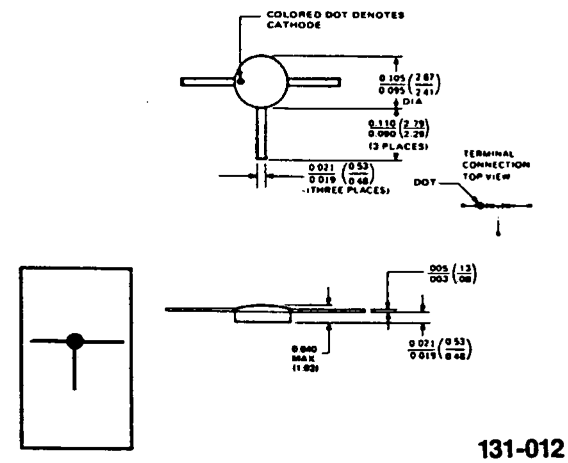
Notes:

1. N_{IF} = 1.5 dB, L.O. = 1.0 mW, R_L = 100Ω

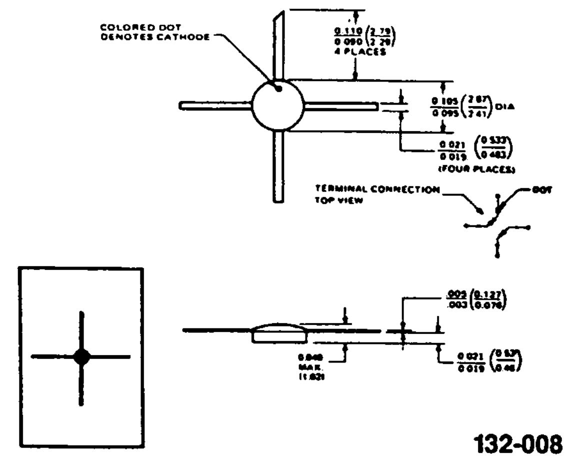
Band	Test Frequency (GHz)
S	3.1
X	9.4
Ku	16.0
Ka	34.9

2. $R_s = R_t - R_B$ where R_t is the total resistance measured across the diode terminals and R_B is the barrier resistance (2.8Ω for a Schottky barrier diode measured at 10mA. For multiple junction devices, the R_B would be 2.8Ω times the number of junctions between the diode terminals).
3. Electrical characteristics are specified for each junction except for those devices containing two or more junctions in series per arm. For these cases, the specification is for the arm.
4. Difference in forward voltage between leads within a pair or quad.

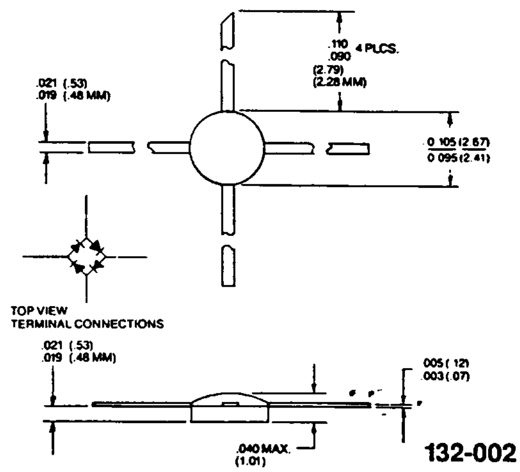
Outline Drawings



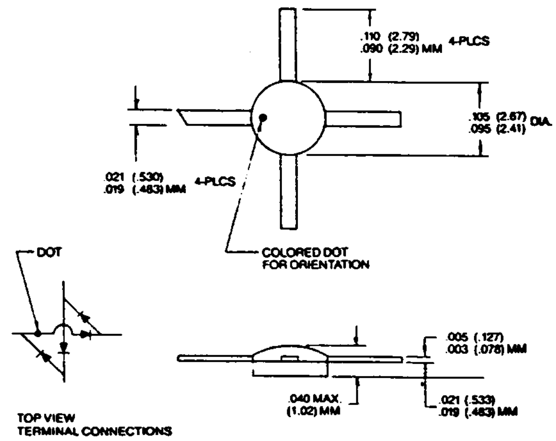
131-012



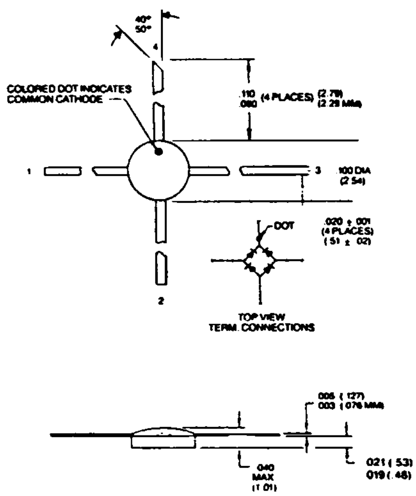
132-008



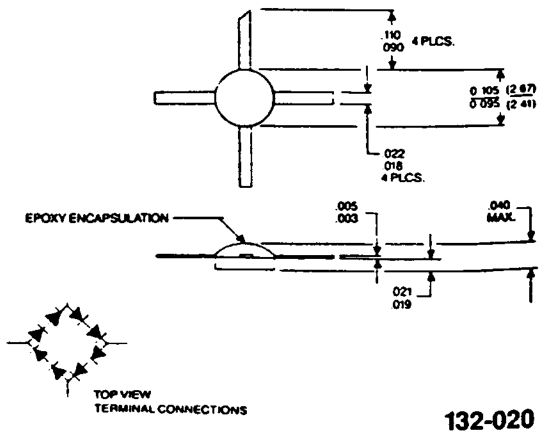
132-002



132-010



132-004



132-020

Note: Millimeters in parentheses.

data delay devices, inc.
385 Lakeview Ave., Clifton, N.J. 07011
Tel: (201) 772-1106

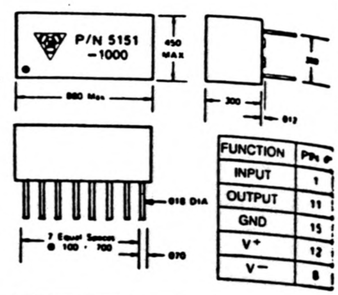
SHORT FORM CATALOG

DIP-ACTIVE FILTERS SERIES 5151-5353

SPECIFICATIONS

- **Transfer characteristics** — Butterworth
- **Gain in pass-band** — 0 db ± .2 db.
- **Cut-off frequency accuracy** — ± 2% @ -3 db.
- **Maximum input voltage** — 10 volts peak.
- **Skirt Attenuation** — 24 db / octave.
- **DC drift** — 20uV / °C typical.
- **Supply Voltage** — ±15V typical (±9V to ±18V operational).
- **Temperature range** — 0° to +70°C (standard); -55°C to +125°C (on request).
- **Temperature Coefficient** — .03% / °C. Better on request.
- **Power Consumption** — 200MW Maximum.

LOW-PASS FILTERS				HIGH-PASS FILTERS			
PART NO.	3 db FREQUENCY (HZ)	PART NO.	3 db FREQUENCY (HZ)	PART NO.	3 db FREQUENCY (HZ)	PART NO.	3 db FREQUENCY (HZ)
5151-1	1	5151-400	400	5353-10	10	5353-2,500	2,500
5151-10	10	5151-1,000	1,000	5353-100	100	5353-3,250	3,250
5151-20	20	5151-1,200	1,200	5353-160	160	5353-4,000	4,000
5151-40	40	5151-2,500	2,500	5353-400	400	5353-13,000	13,000
5151-50	50	5151-4,000	4,000	5353-500	500	5353-16,000	16,000
5151-100	100	5151-5,000	5,000	5353-1,000	1,000	5353-20,000	20,000
5151-200	200	5151-20,000	20,000	5353-1,800	1,800		

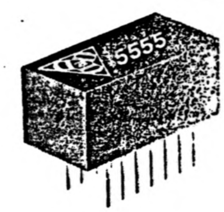


NOTE: The above table gives only a small number of designs available. Many other designs are availabe on request. Any frequency from 1HZ to 25KHZ can be selected. To make a part number, simply use the basic series number and the cut-off frequency.

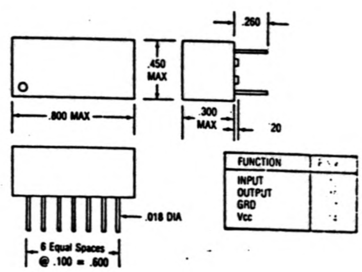
BAND-PASS FILTER SERIES 5555

PART NO.	fc(Hz)	PART NO.	fc(Hz)	PART NO.	fc(Hz)
5555-360	360	5555-1260	1260	5555-2280	2280
5555-420	420	5555-1320	1320	5555-2340	2340
5555-480	480	5555-1336	1336	5555-2400	2400
5555-540	540	5555-1380	1380	5555-2460	2460
5555-600	600	5555-1440	1440	5555-2520	2520
5555-560	660	5555-1477	1477	5555-2580	2580
5555-697	697	5555-1500	1500	5555-2640	2640
5555-720	720	5555-1560	1560	5555-2700	2700
5555-770	770	5555-1620	1620	5555-2760	2760
5555-780	780	5555-1633	1633	5555-2820	2820
5555-840	840	5555-1680	1680	5555-2280	2880
5555-852	852	5555-1740	1740	5555-2940	2940
5555-900	900	5555-1800	1800	5555-3000	3000
5555-941	941	5555-1860	1860	5555-3060	3060
5555-960	960	5555-1920	1920	5555-3120	3120
5555-1020	1020	5555-1980	1980	5555-3180	3180
5555-1080	1080	5555-2040	2040	5555-3240	3240
5555-1140	1140	5555-2100	2100	5555-3300	3300
5555-1200	1200	5555-2160	2160	5555-3360	3360
5555-1209	1209	5555-2220	2220		

SPECIFICATIONS

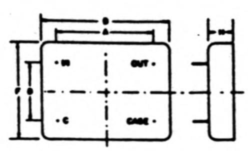


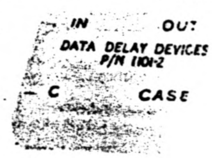
- **Response:** See graph.
- **Gain @ fc:** 10 db typical.
- **Center Frequency Accuracy:** ±1%.
- **Input Voltage:** 1v rms Max.
- **Supply Voltage:** 15Vdc.
- **Temperature Range:** 0° to 70°C.
- **Temperature Coefficient:** .03%/°C.
- **Power Consumption:** 625 MW @ 25°C.
- **Output Load:** 600 Min.



LOW PROFILE FILTERS SERIES 1100

CASE Metal flat case to reduce hum pick-up.
PINS Straight pins for PC mounting





LOW-PASS

PART NO.	Imp. IN/OUT	PASS-BAND (1db)	(3db)	STOP-BAND	CASE NO.
1101-1	10K	DC to 460Hz	600Hz	40db above 750Hz	1
1101-2	600	DC to 3KHz	3.4KHz	40db above 4.2KHz	1
1101-3	10K	DC to 4.4KHz	5KHz	43db above 6.3 KHz	1
1101-4	1K	DC to 9KHz	10KHz	43db above 12.8KHz	1
1101-5	600	DC to 15KHz	18KHz	43 db above 23KHz	1
1101-6	600	DC to 43KHz	50KHz	43db above 64KHz	2

BROAD BAND-PASS

PART NO.	Imp. IN/OUT	PASS-BAND	STOP-BAND (36db) BELOW	ABOVE	CASE NO.
1103-1	10K	1KHz to 2KHz	0.5KHz	4KHz	3
1103-2	10K	2KHz to 4KHz	1KHz	8KHz	3
1103-3	10K	4KHz to 8KHz	2KHz	16KHz	3
1103-4	10K	10KHz to 20KHz	5KHz	40KHz	4

HIGH-PASS

PART NO.	Imp. IN/OUT	PASS-BAND (1db)	(3db)	STOP-BAND	CASE NO.
1102-1	10K	300Hz & above	200Hz	40db below 140Hz	1
1102-2	10K	600Hz & above	400Hz	40db below 280Hz	1
1102-3	10K	1.2KHz & above	800Hz	40db below 560Hz	1
1102-4	10K	3KHz & above	2KHz	40db below 1.4KHz	2
1102-5	10K	6KHz & above	4KHz	40db below 2.8KHz	2

CASE DIMENSIONS

CASE NO.	A IN.	A M.M.	B IN.	B M.M.	D IN.	D M.M.	F IN.	F M.M.	H IN	H M.M.
1	1.4	35.56	1.875	47.63	1.4	35.56	2.0	50.8	0.5	[illegible]
2	1.4	35.56	2.0	50.8	0.8	20.32	1.5	38.1	0.375	[illegible]
3	1.4	35.56	2.0	50.8	0.8	20.32	1.5	38.1	0.5	[illegible]
4	0.8	20.32	1.25	31.75	1.0	25.4	1.75	44.45	0.375	[illegible]

DATA DELAY DEVICES INC. • 385 Lakeview Avenue, Clifton, N.J. 07011 • (201) 772-1106

broadband, high dynamic range

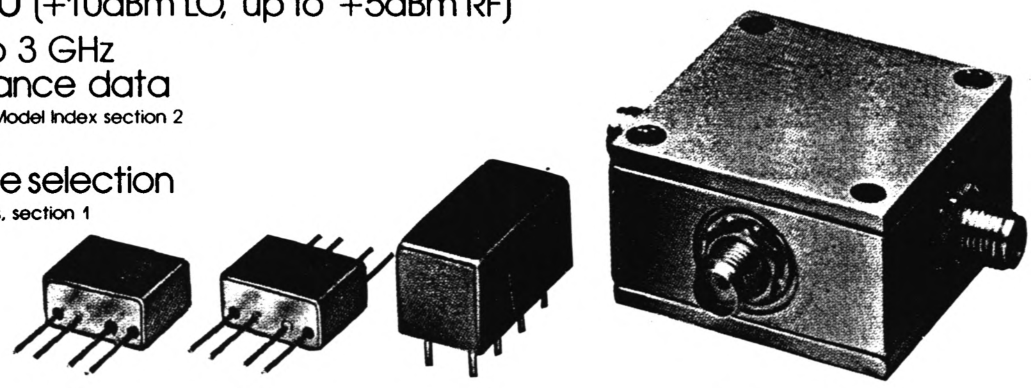
Frequency Mixers

LEVEL 10 (+10dBm LO, up to +5dBm RF)

50 KHz to 3 GHz
performance data
curves, tables, Model Index section 2

case style selection

outline drawings, section 1



TFM LMX SRA ZFM

	MODEL NO.	FREQUENCY MHz LO/RF f_L-f_U	IF	CONVERSION LOSS dB Mid-Band m		Total Range		LO-RF ISOLATION, dB L		M		U		LO-IF ISOLATION, dB L		M		U		PRICE, $	
				Typ.	Max.	Typ.	Max.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Ea.	Qty.
TFM case B13	TFM-15	10-3000	10-800	6.3	8.0	6.5	8.5	35	25	35	25	35	25	30	20	30	20	30	20	49.95	(1-9)
	TFM-150*	10-2000	DC-1000	6.0	8.0	6.5	8.0	32	25	35	25	35	25	33	20	30	20	30	20	39.95	(1-9)
LMX case BB48	LMX-123	10-3000	10-3000	7.5	8.0	7.5	8.5	35	25	35	20	30	15	35	25	30	25	30	20	59.95	(6-24)
	LMX-148	10-1500	DC-1500	6.0	7.0	6.0	10	45	40	35	30	25	20	40	35	35	25	20	12	24.95	(6-24)
SRA case A01	SRA-215	.05-1500	.05-500	6.0	7.5	7.0	9.0	25	20	35	25	30	20	25	20	35	25	25	15	23.95	(5-24)
	SRA-220	.05-2000	.05-500	6.0	7.5	7.0	9.0	25	20	40	30	30	20	25	20	40	30	25	15	26.95	(5-24)
ZFM case K18	ZFM-15	10-3000	10-800	6.3	7.5	6.5	8.5	35	25	35	25	35	25	30	20	30	20	30	20	79.95	(1-9)
	ZFM-150	10-2000	DC-1000	6.0	7.0	6.5	8.0	32	25	35	25	35	20	33	28	30	20	25	20	59.95	(1-9)

L = low range (f_L to 10 f_L) M = mid range (10f_L to $f_U/2$) U = upper range ($f_U/2$ to f_U)
m = mid band (2f_L to $f_U/2$)

harmonic attenuation

MODEL TFM-15

Harmonics RF Order	RF CAL	1	2	3	4	5	6	7	8	9	10
1	0	0	31	17	42	32	48	47	52	65	59
2	83	38	45	39	48	46	76	69	70	64	71
3	87	39	49	37	52	42	57	63	65	65	65
4	89	64	60	58	56	59	60	62	69	74	70
5	90	74	69	59	72	55	74	58	71	67	72
6	83	83	76	74	67	69	67	72	70	74	78
7	83	76	83	81	79	69	71	66	70	69	77
8	84	75	76	81	82	77	77	80	78	78	77
9	84	77	76	75	82	80	81	82	80	79	80
10	81	76	76	74	75	80	81	81	81	80	81

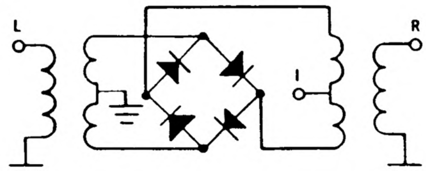
Harmonic LO Order

Model: TFM
LO = +10 dBm, 969.01 MHz
RF = 0 dBm, 999.1 MHz

NOTES:
- ■ NON-HERMETIC
- * Below 10 MHz IF, conversion loss increases up to 6dB higher as frequency decreases to DC.

1. For quality control procedures, environmental specifications, and Hi-Rel, MIL and TX description see section 1.
2. Absolute Maximum Ratings, RF power 50 mW level 10, 200 mW level 13, peak IF current 40 mA, see section 1.
3. For connector types and case mounting options, see case style outline drawings, section 1.
4. Prices and specifications subject to change without notice.

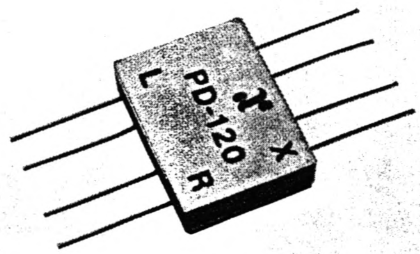
schematic



Mini-Circuits P.O. BOX 166, Brooklyn, New York 11235 (718) 934-4500

MODEL PD-120 | PHASE DETECTOR 5-1000 MHz

Wide Bandwidth
Low DC Offset



Guaranteed Specifications*

(From −55°C to +85°C)

Frequency Range		5-1000 MHz
Maximum DC Output	5-500 MHz	300 mV Min
	5-1000 MHz	250 mV Min
Isolation (L-R)	5-200 MHz	50 dB Min
	200-500 MHz	40 dB Min
	500-1000 MHz	30 dB Min
DC Offset (100 MHz RF)		1.0 mV Max

Operating Characteristics

Impedance	
(L,R Ports)	50 Ohms Nominal
Load (X Port)	500 Ohms
Input Power (L & R Ports)	+7 dBm Nominal
Maximum Input (Non-Destruct)	
Total Power	300 mW Max @ 25°C
	Derated to 85°C @ 3.2 mW/°C
DC Output Polarity	Negative
Package Type	Flatpack (FP-2)
	(See page 474 for physical dimensions.)

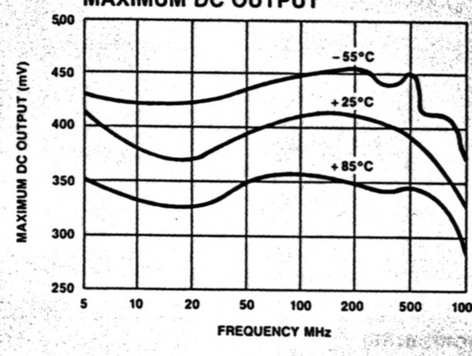
Environmental
These units are designed to meet the environmental and screening requirements of Table 1A, page 496 of the Adams-Russell catalog.

Pin Configuration	RF; P8, LO; P5, IF; P4.
	All other pins and case are ground.

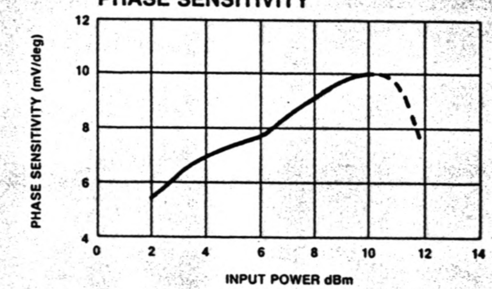
*All specifications apply when operated at +7 dBm available LO and RF power and 50 ohms impedance at the L & R ports and with 500 ohm load at the X port.

Typical Performance

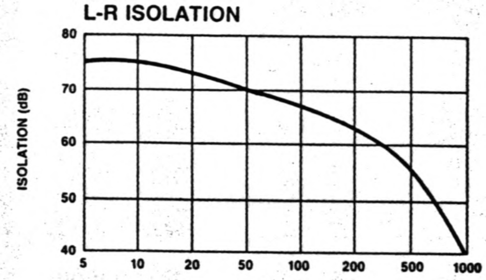
MAXIMUM DC OUTPUT



PHASE SENSITIVITY



L-R ISOLATION



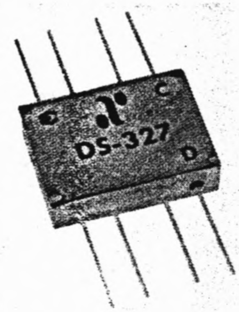
Ordering Information

Model No.	Part No.	Connectors	Unit Price (5-9 Units)
PD-120	8519	Pin	$62

Delivery is from stock.

MODEL DS-327 | FLATPACK TWO-WAY POWER DIVIDER 5-1000 MHz

Broadband, IN Phase Divider
Low Loss — 0.3 dB Typical
Amplitude Balance — 0.05 dB Typical



Guaranteed Specifications*

(From −55°C to +85°C)

Frequency Range		5-1000 MHz
Insertion Loss (Less coupling)	5-500 MHz 500-1000 MHz	0.5 dB Max 1.0 dB Max
Isolation	5-500 MHz 500-1000 MHz	25 dB Min 20 dB Min
Amplitude Balance	5-1000 MHz	0.2 dB Max
Phase Balance	5-500 MHz 500-1000 MHz	2° Max 3° Max
VSWR (All Ports)	10-500 MHz 5-1000 MHz	1.3:1 Max 1.5:1 Max

Operating Characteristics

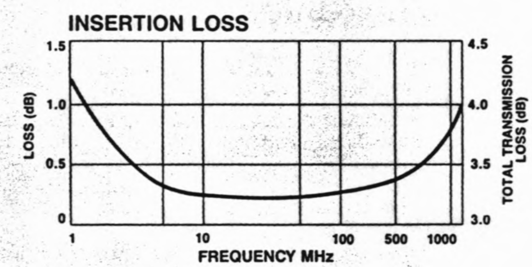
Impedance	50 Ohms Nominal
Maximum Power Rating or Input Power	1 Watt Max
Internal Load Dissipation	0.05 Watt Max
Package Type	Flatpack (FP-2) (See page 474 for physical dimensions.)

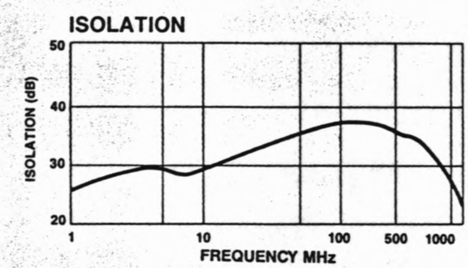
Environmental
These units are designed to meet the environmental and screening requirements of Table 1A, page 496 of the Adams-Russell catalog.

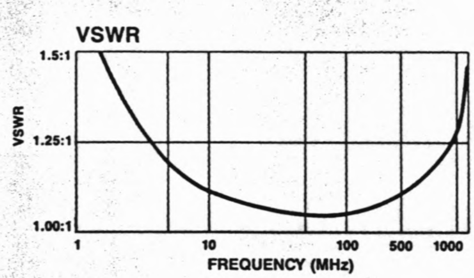
Pin Configuration	Σ; P1, Output 'C'; P4, Output 'D'; P8 Case and all other pins ground.

*All specifications apply with 50 ohm source and load impedance.

Typical Performance







Ordering Information

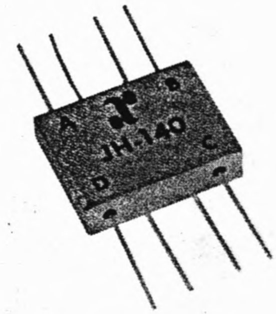
Model No.	Part No.	Connectors	Unit Price (5-9 Units)
DS-327	6699	Pin	$58

Delivery is from stock.

MODEL JH-140

HIGH FREQUENCY QUADRATURE HYBRID 500-1000 MHz

Octave Bandwidth
Low VSWR — 1.2:1 Typical
Miniature Size — ½″ x ⅜″ Flatpack



Guaranteed Specifications*

(From −55°C to +85°C)

Frequency Range	500-1000 MHz
Insertion Loss (Less coupling)	0.3 dB Max Avg**
Isolation	20 dB Min
Amplitude Balance	1.0 dB Max
VSWR	1.2:1 Max
Deviation from Quadrature	2° Max

Operating Characteristics

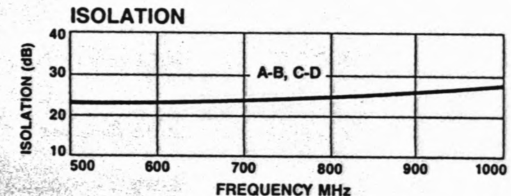
Impedance	50 Ohms Nominal
Input Power	25 Watts Max @ 25°C; Derated to 1 Watt @ 85°C
Package Type	Flatpack (FP-2) (See page 474 for physical dimensions.)

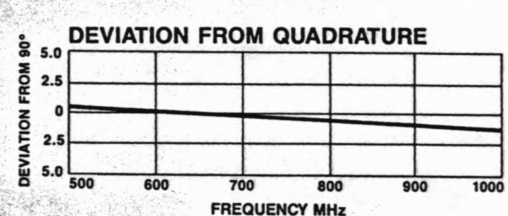
Environmental
These units are designed to meet the environmental and screening requirements of Table 1A, page 496 of the Adams-Russell catalog.

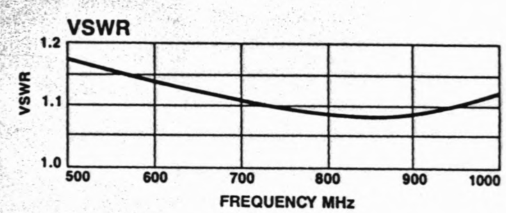
Pin Configuration	A; P1, B; P4, C; P8, D; P5. All other pins are ground.

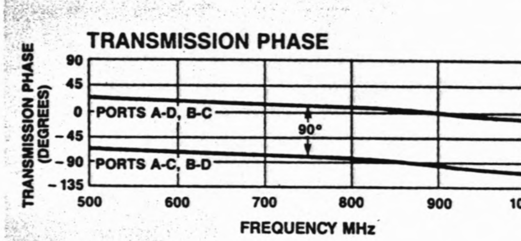
*All specifications apply with 50 ohm source and load impedance.
**Average of coupled outputs less 3 dB.

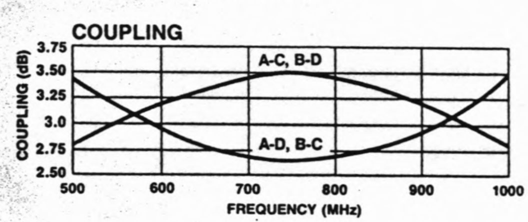
Typical Performance











Phasing Diagram

IN \ OUT	A	B	C	D
A		ISO.	−90°	0°
B	ISO.		0°	−90°
C	−90°	0°		ISO.
D	0°	−90°	ISO.	

Ordering Information

Model No.	Part No.	Connectors	Unit Price (5-9 Units)
JH-140	6619	Pin	$76

Delivery is from stock.

ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI/AD7511DI/AD7512DI

FEATURES

Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically Isolated CMOS
Standard 14-/16-Pin DIPs and 20-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

ORDERING INFORMATION[1]

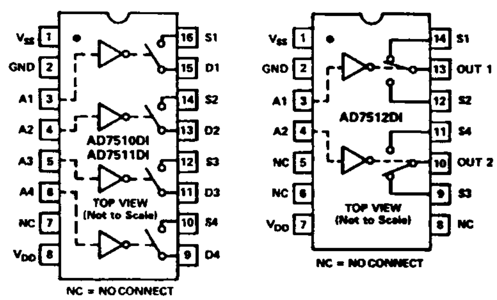
Temperature Range and Package[2]

0 to +70°C	−25°C to +85°C	−55°C to +125°C
Plastic DIP[3]	Hermetic[4]	Hermetic[4]
AD7510DIJN	AD7510DIJQ	AD7510DISQ
AD7510DIKN	AD7510DIKQ	AD7510DITQ
AD7511DIJN	AD7511DIJQ	AD7511DITQ
AD7511DIKN	AD7511DIKQ	AD7512DISQ
AD7512DIJN	AD7512DIJQ	AD7512DITQ
AD7512DIKN	AD7512DIKQ	
PLCC[5] (P-20A)		LCCC[6] (E-20A)
AD7510DIJP		AD7510DISE
AD7510DIKP		AD7511DISE
AD7511DIJP		AD7511DITE
AD7511DIKP		AD7512DISE
AD7512DIJP		AD7512DITE
AD7512DIKP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]For AD7510DIJN/KN and AD7511DIJN/KN package outline N-16; for AD7512DIJN/KN package outline N-14.
[4]For AD7510DIJQ/KQ/SQ and AD7511DIJQ/KQ/SQ/TQ package outline Q-16; for AD7512DIJQ/KQ/SQ/TQ package outline Q-14.
[5]PLCC: Plastic Leaded Chip Carrier.
[6]LCCC: Leadless Ceramic Chip Carrier.

AD7510DI/AD7511DI/AD7512DI
FUNCTIONAL BLOCK DIAGRAMS
AND PIN CONFIGURATIONS

DIP

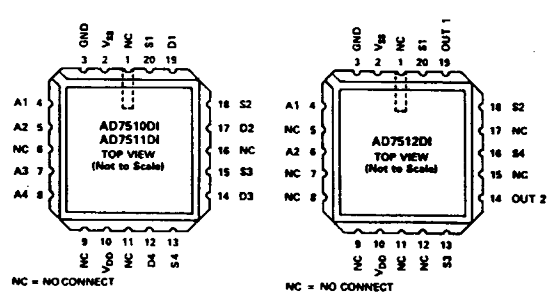


CONTROL LOGIC

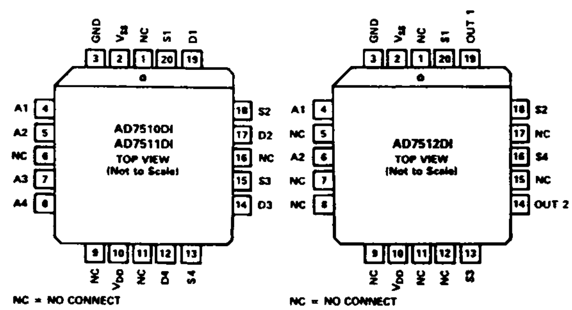
AD7510DI: Switch "ON" for Address "HIGH"
AD7511DI: Switch "ON" for Address "LOW"
AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

PIN CONFIGURATIONS

LCCC



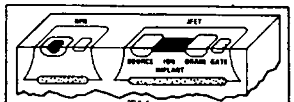
PLCC



7

National Semiconductor

Operational Amplifiers/Buffers



BI-FET II™ Technology

LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

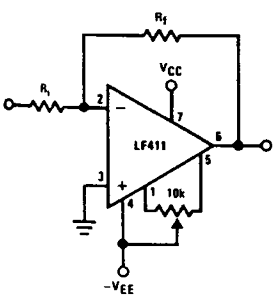
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage — 0.5 mV (max)
- Input offset voltage drift — 10 μV/°C (max)
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 3 MHz (min)
- High slew rate — 10V/μs (min)
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection



Ordering Information

LF411XYZ

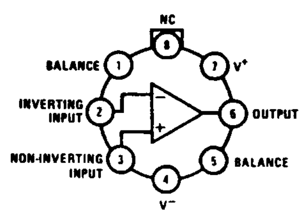
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

LF411AMH/LF411MH, LF411ACH/LF411CH
Metal Can Package

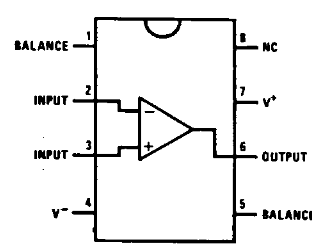


TOP VIEW

Note. Pin 4 connected to case.

Order Number LF411AMH, LF411MH, LF411ACH or LF411CH
See NS Package H08B

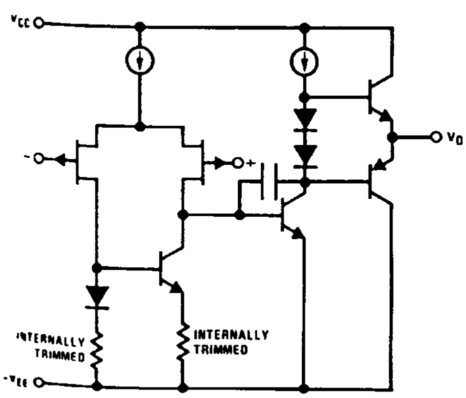
LF411ACN, LF411CN
Dual-In-Line Package



TOP VIEW

Order Number LF411ACN or LF411CN
See NS Package N08A

Simplified Schematic



BI-FET II™ is a trademark of National Semiconductor Corp.

National Semiconductor

Operational Amplifiers/Buffers

LH0022/LH0022C High Performance FET Op Amp
LH0042/LH0042C Low Cost FET Op Amp
LH0052/LH0052C Precision FET Op Amp

General Description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 microvolts maximum offset and 5 μV/°C offset drift. Input offset current is less than 500 femtoamps at room temperature and 500 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the -55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the -25°C to +85°C temperature range.

Features

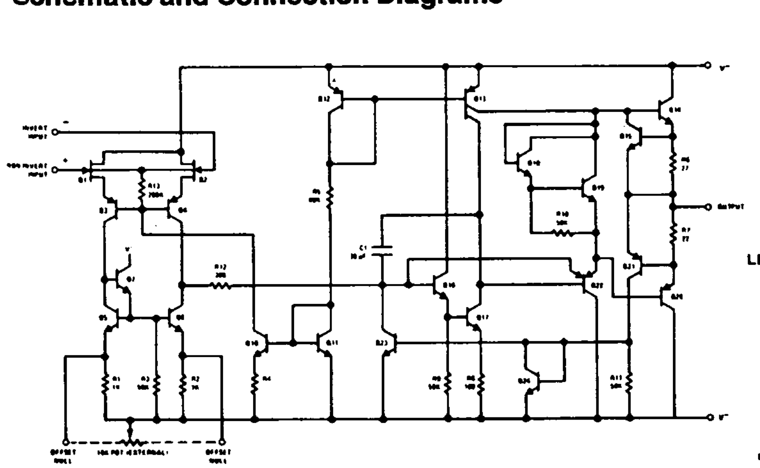
- Low input offset current – 500 femtoamps max. (LH0052)
- Low input offset drift – 5 μV/°C max (LH0052)
- Low input offset voltage – 100 microvolts-typ.
- High open loop gain – 100 dB typ.
- Excellent slew rate – 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

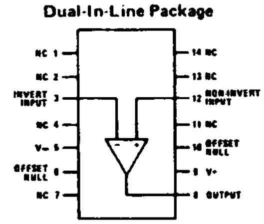
Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

Schematic and Connection Diagrams



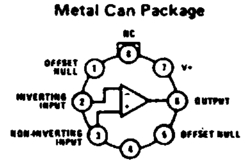
Dual-In-Line Package



TOP VIEW

Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD
See Package D14E

Metal Can Package



TOP VIEW

Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH
See Package H08A

*Previously Called NH0022/NH0022C

National Semiconductor

Voltage Comparators

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

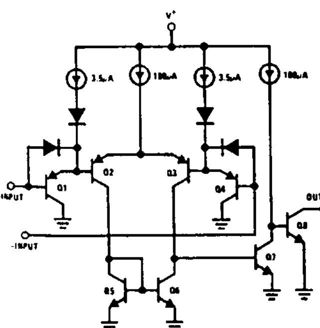
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

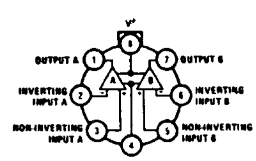
Features

- Wide single supply
  - Voltage range 2.0 V_{DC} to 36 V_{DC}
  - or dual supplies ±1.0 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.8 mA)—independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



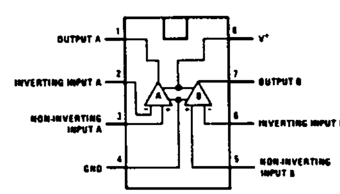
Metal Can Package



TOP VIEW

Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

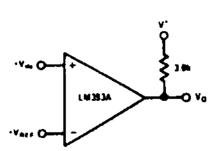
Dual-In-Line Package



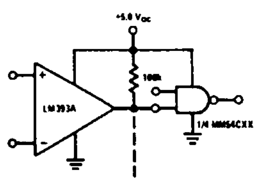
TOP VIEW

Order Number LM393N, LM393AN, or LM2903N
See NS Package N08B

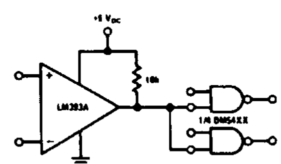
Typical Applications ($V^+ = 5.0\ V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

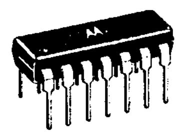
MC4344 • MC4044

ISSUE A

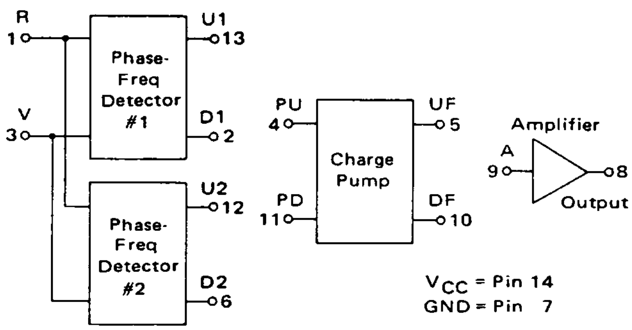
The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts MTTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

F SUFFIX
CERAMIC PACKAGE
CASE 607
(TO-86)

L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

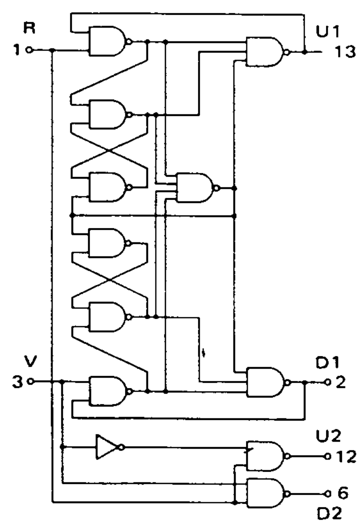


P SUFFIX
PLASTIC PACKAGE
CASE 646
(TO-116)
MC4044 only

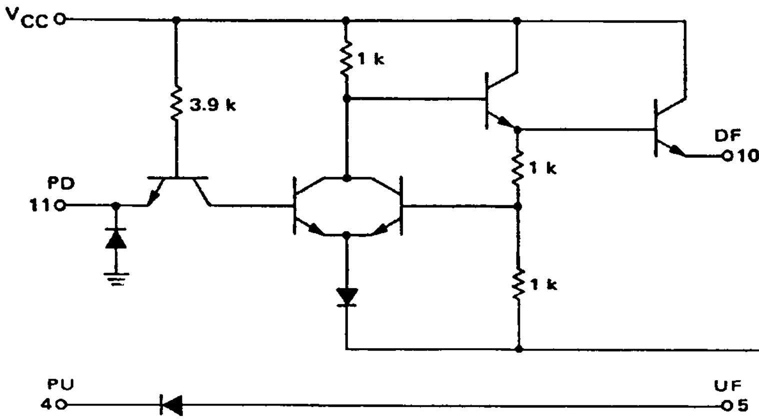


Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

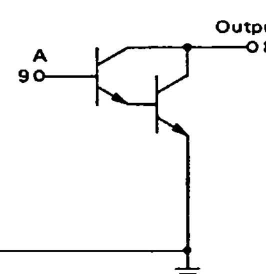
PHASE DETECTOR



CHARGE PUMP



AMPLIFIER



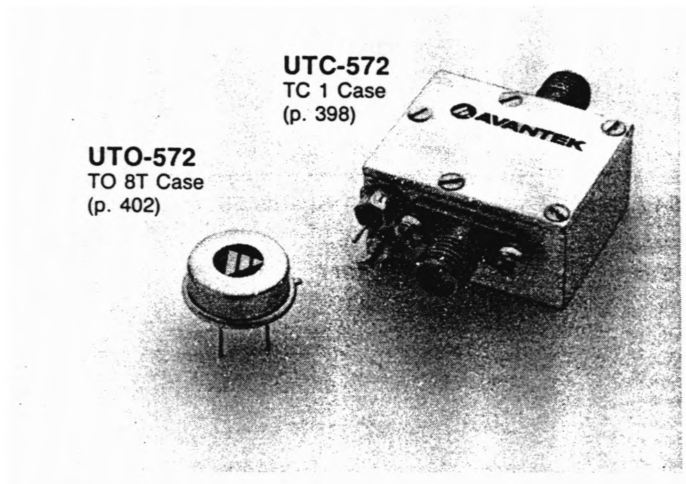
UTO-572

Reverse Isolation Amplifiers 50-500 MHz

AVANTEK

FEATURES

- High Reverse Isolation
- Wideband
- Low VSWR



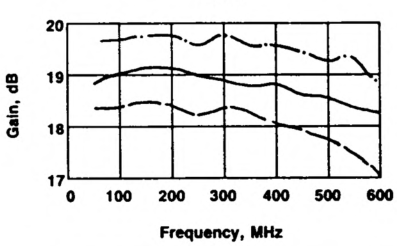
ELECTRICAL SPECIFICATIONS (Measured in a 50-ohm system @ +15 VDC nominal unless otherwise noted)

Symbol	Characteristic	Typical $T_C = 25°C$	Guaranteed Specifications $T_C = 0°-50°C$	Guaranteed Specifications $T_C = -55°- +85°C$	Unit
BW	Frequency Range	50-500	50-500	50-500	MHz
GP	Small Signal Gain	18.5	18.0 Min.	17.0 Min.	dB
—	Gain Flatness	±0.3	±0.5 Max.	±1.0 Max.	dB
NF	Noise Figure	3.0	3.5 Max.	3.7 Max.	dB
—	Reverse Isolation	50	45	45	dB
$P_{1\,dB}$	Power Output @ + 1 dB Compression	+12.0	+11.0 Min.	+10.0 Min.	dBm
—	Input VSWR	1.5:1	2.0:1 Max.	2.0:1 Max.	—
—	Output VSWR	1.5:1	2.0:1 Max.	2.0:1 Max.	—
IP_3	Two Tone 3rd Order Intercept Point	+24.0	—	—	dBm
IP_2	Two Tone 2nd Order Intercept Point	+34.0	—	—	dBm
HP_2	One Tone 2nd Harmonic Intercept Point	+42.0	—	—	dBm
I_D	DC Current	32	—	—	mA

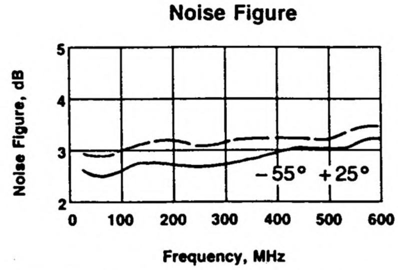
TYPICAL PERFORMANCE OVER TEMPERATURE (@ +15 VDC unless otherwise noted)

KEY: +25°C ————
+85°C — — — —
−55°C —·—·—

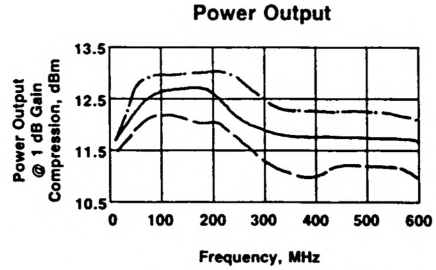
Gain



Noise Figure



Power Output



MAXIMUM RATINGS

DC Voltage .... +17 Volts
Continuous RF Input Power .... +13 dBm
Operating Case Temperature .... −55°C to +115°C
Storage Temperature .... −62°C to +150°C
"R" Series Burn-In Temperature .... +115°C

THERMAL CHARACTERISTICS*

θ_{JC} .... 190°C/W
Active Transistor Power Dissipation .... 150/180 mW
Junction Temperature Above Case Temperature .... 29/35°C

*For further information, see High Reliability section.

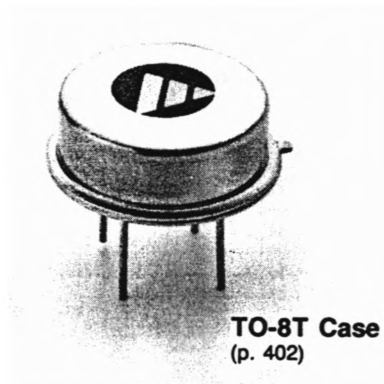
WEIGHT: (typical) UTO—2.1 grams; UTC—21.5 grams

UTM-1055

High Gain Modular Amplifier 10-1000 MHz

FEATURES

- **MODAMP™ Silicon Monolithic Gain Stages**
- **Gain: 16.2 dB (Typ.)**
- **Output Power: +16.5 dBm (Typ.)**
- **Increased Reliability**



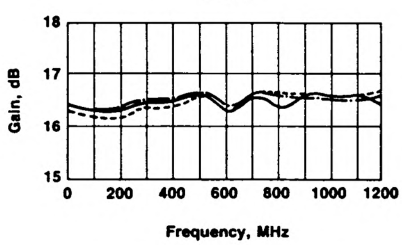
TO-8T Case
(p. 402)

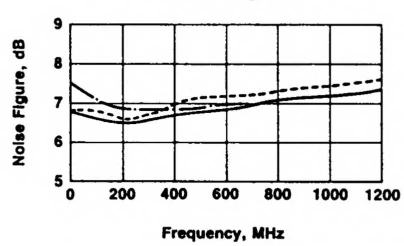
ELECTRICAL SPECIFICATIONS (Measured in a 50-ohm system @ +15 VDC nominal)

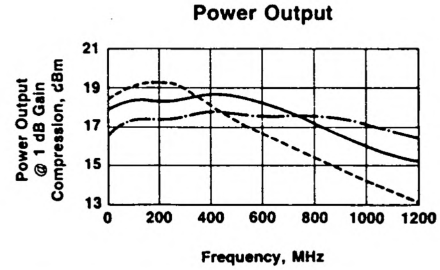
Symbol	Characteristic	Typical T_C = 25°C	Guaranteed Specifications		Unit
			T_C = 0°-50°C	T_C = −55°- +85°C	
BW	Frequency Range	10-1000	10-1000	10-1000	MHz
GP	Small Signal Gain	16.2	15.5 Min.	15.0 Min.	dB
—	Gain Flatness	±0.2	±0.7 Max.	±0.7 Max.	dB
NF	Noise Figure	7.0	8.0 Max.	8.5 Max.	dB
$P_{1 dB}$	Power Output @ + 1 dB Compression	+16.5	+15.0 Min.	+12.0 Min.	dBm
—	Input VSWR	1.4:1	1.7:1 Max.	1.7:1 Max.	—
—	Output VSWR	1.2:1	1.7:1 Max.	1.7:1 Max.	—
IP_3	Two Tone 3rd Order Intercept Point	+29.0	—	—	dBm
IP_2	Two Tone 2nd Order Intercept Point	+45.0	—	—	dBm
HP_2	One Tone 2nd Harmonic Intercept Point	+50.0	—	—	dBm
I_D	DC Current	135		—	mA

TYPICAL PERFORMANCE OVER TEMPERATURE (@ +15 VDC unless otherwise noted)

KEY: +25°C ———— / +85°C — — — — / −55°C —·—·—







MAXIMUM RATINGS

DC Voltage	+17 Volts
Continuous RF Input Power	+20 dBm
Operating Case Temperature	−55°C to +100°C
Storage Temperature	−62°C to +150°C
"R" Series Burn-In Temperature	+85°C

THERMAL CHARACTERISTICS

θ_{JC} [1]	110/110°C/W
Active Transistor Power Dissipation[1]	300/480 mW
Junction Temperature Above Case Temperature[1]	33/53°C

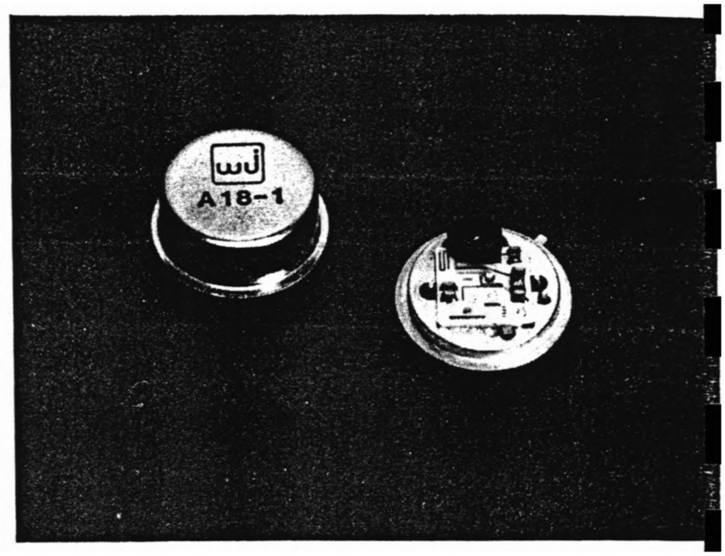
Note 1: Values refer to 1st and 2nd stage transistors respectively.

WEIGHT: (typical) — 2.1 grams

WJ-A18-1

10 TO 1000 MHz
TO-8 CASCADABLE AMPLIFIER

- HIGH OUTPUT LEVEL:
  +16 dBm (TYP.)
- HIGH THIRD ORDER I. P.
  +30 dBm (TYP.)
- LOW VSWR: 1.5:1 (TYP.)



Specifications*

Characteristics	Typical	Guaranteed 0° - 50°C	Guaranteed -54°C - +85°C
Frequency (Min.)	5-1100 MHz	10-1000 MHz	10-1000 MHz
Small Signal Gain (Min.)	14.7 dB	14.0 dB	13.5 dB
Gain Flatness (Max.)	<±0.3 dB	±0.5 dB	±1.0 dB
Noise Figure (Max.)	3.8 dB	5.0 dB	5.5 dB
Power Output at 1 dB Compression (Min.)	+16.0 dBm	+15.0 dBm	+14.5 dBm
VSWR (Max.) Input/Output	1.5:1	1.8:1	2.0:1
DC Current (Max.) at 15 Volts	44 mA	46 mA	48 mA

*Measured in a 50-ohm system at +15 Vdc Nominal.

Typical Intermodulation Performance at 25°C

Second Order Harmonic Intercept Point . . . . +45 dBm (Typ.)
Second Order Two-Tone Intercept Point . . . . +42 dBm (Typ.)
Third Order Two-Tone Intercept Point . . . . +30 dBm (Typ.)

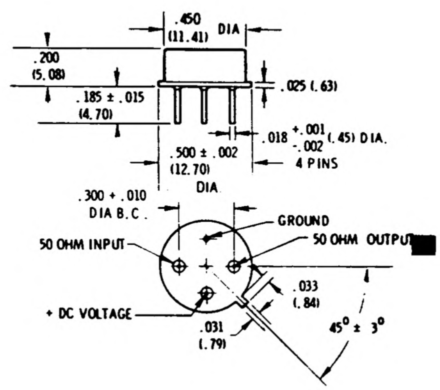
Absolute Maximum Ratings

Storage Temperature . . . . -62°C to +125°C
Maximum Case Temperature . . . . 125°C
Maximum DC Voltage . . . . +17 Volts
Maximum Continuous RF Input Power . . . . +13 dBm
Maximum Short Term RF Input Power . . . . 50 Milliwatts
(1 Minute Max.)
Maximum Peak Power . . . . 0.5 Watt
(3 μsec Max.)
"S" Series Burn-In Temperature (Case) . . . . 125°C

Weight approximately 2.0 grams (0.07 oz.)

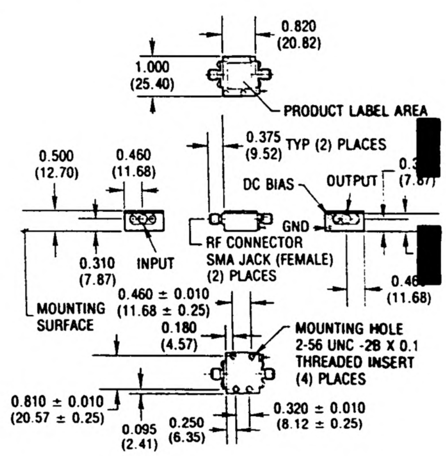
Outline Drawings

A18-1



DIMENSIONS ARE IN INCHES (MILLIMETERS)
± .005 (.13) UNLESS OTHERWISE SPECIFIED

CA18-1



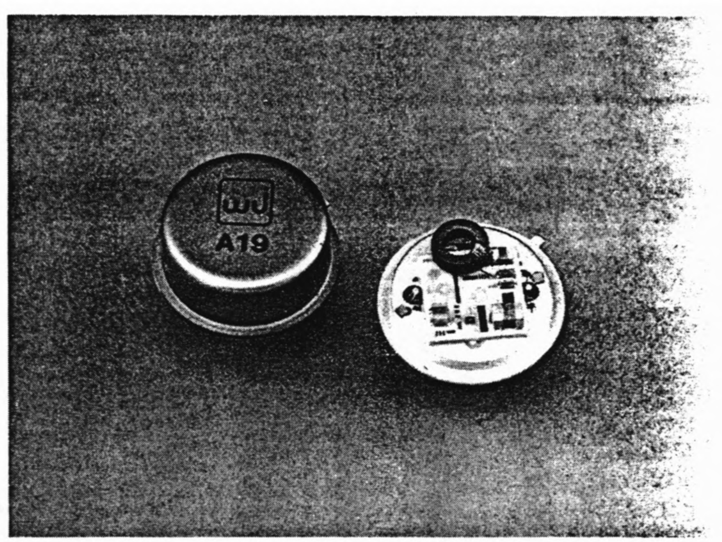
DIMENSIONS ARE IN INCHES (MILLIMETERS)
± .015 (.38) UNLESS OTHERWISE SPECIFIED

*WJ-CA18-1 is standard WJ-A18-1 installed in miniature SMA connector housing guaranteed over 0°C to 50°C temperature range. See Cascaded Thin Film Amplifi

WJ-A19

10 TO 1000 MHz
TO-8 CASCADABLE AMPLIFIER

- HIGH OUTPUT POWER: +21 dBm (TYP.)
- HIGH THIRD ORDER I.P.: +34 dBm (TYP.)



Specifications*

Characteristics	Typical	Guaranteed 0°-50°C	Guaranteed -54°C - +85°C
Frequency (Min.)	5-1050 MHz	10-1000 MHz	10-1000 MHz
Small Signal Gain (Min.)	7.5 dB	6 dB	5.5 dB
Gain Flatness (Max.)	< ±0.3 dB	±1.0 dB	±1.3 dB
Noise Figure (Max.)	9 dB	10.5 dB	11.0 dB
Power Output at 1 dB Compression (Min.)	+21 dBm	+20 dBm	+19 dBm
VSWR (Max.) Input/Output	< 1.8:1	2.2:1	2.2:1
DC Current (Max.) at 15 Volts	100 mA	109 mA	114 mA

*Measured in a 50-ohm system at +15 Vdc Nominal.

Typical Intermodulation Performance at 25°C

Second Order Harmonic Intercept Point .... +45 dBm (Typ.)
Second Order Two-Tone Intercept Point .... +40 dBm (Typ.)
Third Order Two-Tone Intercept Point .... +34 dBm (Typ.)

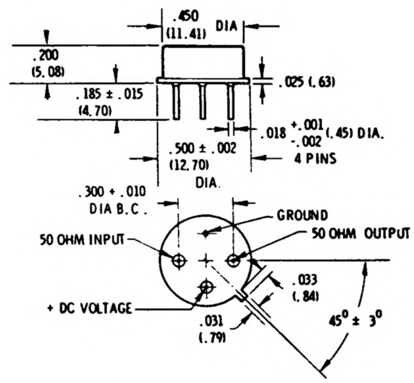
Absolute Maximum Ratings

Storage Temperature .... -62°C to +125°C
Maximum Case Temperature .... 85°C
Maximum DC Voltage .... +17 Volts
Maximum Continuous RF Input Power .... +17 dBm
Maximum Short Term RF Input Power .... +20 dBm (1 Minute Max.)
Maximum Peak Power .... 0.5 Watt (3 μsec Max.)
"S" Series Burn-In Temperature (Case) .... 85°C

Weight approximately 2.0 grams (0.07 oz.)

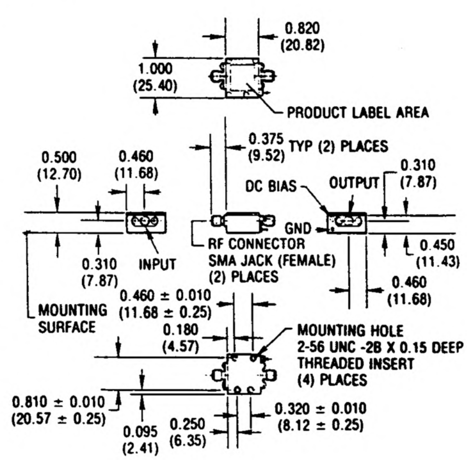
Outline Drawings

A19



DIMENSIONS ARE IN INCHES (MILLIMETERS) ± .005 (.13) UNLESS OTHERWISE SPECIFIED

CA19



DIMENSIONS ARE IN INCHES (MILLIMETERS) ± .015 (.38) UNLESS OTHERWISE SPECIFIED

*WJ CA19 is standard WJ A19 installed in miniature SMA connector housing and guaranteed over 0° C to 50° C temperature range