VLBA TECHNICAL
REPORT NO. 18

F117

FRONT END CONTROL MODULE

E. SCHLECHT
July 1990

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Specifications

Maximum Voltage to Analog Inputs	± 20 VOLT
Analog Voltage Measurement Range	± 10 VOLT
Number of analog inputs	12
Number of internal analog measurements	2
Number of digital inputs	2
Number of digital readbacks	2
Number of digital command outputs	2
Module Ser. No. relative address	24 hexadecimal
Address ID code range	00-0F hexadecimal
Analog monitor relative address range	08-1F hexadecimal
Digital monitor relative address range	20-24 hexadecimal
Command relative address range	20, 22 hexadecimal
Power supply voltages required	+5, ±15, +28 VOLT

Address ID Code For Each Frequency

Frequency	FE No.	Code	Frequency	FE No.	Code
75 MHz	F101	00	10.7 GHz	F107	06
330/610 MHz	F102	01	15 GHz	F108	07
1.5 GHz	F103	02	23 GHz	F109	08
2.3 GHz	F104	03	43 GHz	F110	09
4.8 GHz	F105	04	86 GHz	F111	0A
8.4 GHz	F106	05			

FRONT PANEL CONNECTIONS AND ADJUSTMENTS

25-pin D-connectors: Are connected through two 25-conductor cables to the associated Front end, except for the 330/610 MHz front end controller, which is connected to the F118 adaptor.

Module Replacement Procedure

I. Removal. Unscrew the knurled plastic screws on the two connectors attached to the front panel. Unplug the connectors from the front panel. Loosen the captivated screws and use the module puller to remove the module from the bin.

II. Replacement. To install a new module, simply insert the module into the bin and tighten the captivated screws. Push the connectors from the cables leading to the front end onto the appropriate connectors on the front panel, and tighten the knurled screws.

COMMANDS

Function: Cryogenics State Control
Relative Address: 20h (hexadecimal)

Command	bits: X 2	C 1	$\overline{H}$ 0	Action
7	1	1	1	Cool
4	1	0	0	Stress
5	1	0	1	Off
2	0	1	0	Heat
6	1	1	0	Pump
(0)	(0	0	0)	(Stress)*

* Not normally used.

Function: Calibrator Control
Relative Address: 22h (hexadecimal)

Command	Action
0000	Cal Off
0002	Lo Cal Continuous
0001	Lo Cal Modulated
0008	Hi Cal Continuous
0004	Hi Cal Modulated

MONITORS

Relative Address (hex)	Type	Description	Multiplier*	Units	Normal Value
04	Analog	Lo-Cal Diode Current	120	mA	10 mA (on)
05	Analog	Hi-Cal Diode Current	120	mA	10 mA (on)
06	Analog	Lo-Cal Diode Voltage	4	Volts	28 V (on)
07	Analog	Hi-Cal Diode Voltage	4	Volts	28 V (on)
08	Analog	Pump Vacuum Sensor	1	Volts	--
09	Analog	AC Current	0.1	Amps	0.5 A
0A	Analog	LED Voltage	1	Volts	
0B	Analog	Sensor Voltage	1	Volts	
0C	Analog	7.5 V Reference	1	Volts	7.5 V
0D	Analog	Hi Q GND	1	Volts	0 V
10	Analog	Left FET #1 Volt.	1	Volts	
11	Analog	Right FET #1 Volt.	1	Volts	
12	Analog	Left FET #2 Volt.	1	Volts	
13	Analog	Right FET #2 Volt.	1	Volts	
14	Analog	15 K Temp Sens.	100	Kelvin	15 K
15	Analog	50 K Temp Sens.	100	Kelvin	50 K
16	Analog	300 K Temp Sens.	100	Kelvin	300 K
17	Analog	Dewar Vacuum Sensor	1	Volts	
18 - 1F	Analog	External Multiplexer			
20	Digital	State Command Readback		See next page.	
21	Digital	Digital Mon. Word		See next page.	
22	Digital	Cal Command Readback		See next page.	
23	Digital	Digital ID Word		See next page.	
24	Digital	FE Control Module Serial No.		See next page.	

* The analog data values can be converted directly to Volts by dividing them by 3276.8. The resulting voltages can then be expressed in the Units shown by multiplying them by the corresponding Multipliers.

INTERPRETATION OF DIGITAL MONITOR VALUES

State Command Readback: Address = 20h (bits 0-7)

Results	bit: X 2	C 1	$\overline{H}$ 0	State
7	1	1	1	Cool
4	1	0	0	Stress
5	1	0	1	Off
2	0	1	0	Heat
6	1	1	0	Pump
(0)	0	0	0	Start-Up Reset State (Stress)

Digital Monitor Word: Address = 21h bits 0-5

FE Cryo state: bits 0-2
Results: Same as State Command Readback above.

Manual/Computer Switch position: bit 3
Results: 0 = MANUAL 1 = COMPUTER

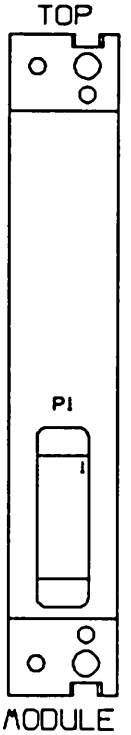
Pump Request Condition: bit 4
Results: 0 = not req 1 = ON (requested)

Pump Valve Position: bit 5
Results: 0 = CLOSED 1 = OPEN

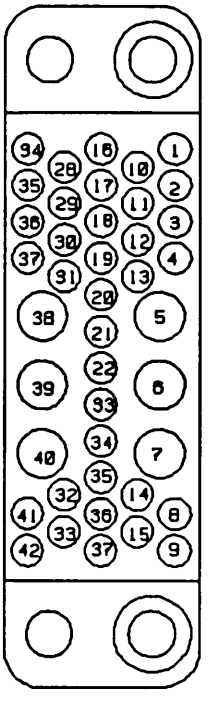
Cal Command Readback: Address = 22h bits 0-7
Results: Same as Command (previous page).

Digital ID Word: Address = 23h bits 0-11
Shows frequency band, serial number and modification level of each Front End:
Bits 0 - 3 : Frequency [F0 - F3]
Bits 4 - 5 : Modification [M0 - M1]
Bits 6 - 11: Serial Number [S0 - S5]

FE Control Module Serial No.: Address = 24h bits 0-7
Serial number of the F117 module.

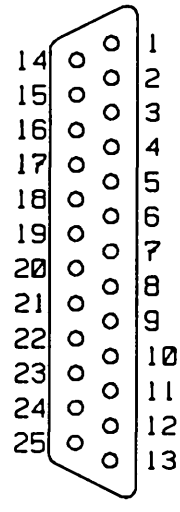


MODULE
(REAR VIEW)



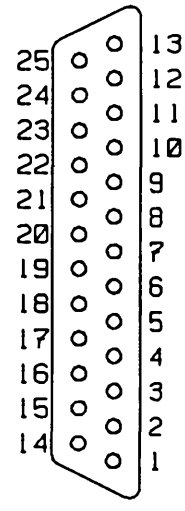
P1 (REAR VIEW)

P1					
PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1			22		
2			23		
3			24		
4			25		
5			26		
6			27		
7			28		
8	XMIT +		29	+ 28 V SUPPLY	100 mA max
9	XMIT -		30		
10	+ 5 V SUPPLY	930 mA	31		
11			32		
12	MODULATOR INPUT		33		
13			34	GROUND	
14	RCV +		35	RST +	
15	RCV -		36	RST -	
16	+ 15 V SUPPLY	45 mA	37		
17	- 15 V SUPPLY	40 mA	38		
18			39		
19			40		
20			41		
21			42		



J1 (FRONT VIEW)

PLUG



J2 (FRONT VIEW)

SOCKET

J1					
PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1	PUMP VACUUM		14	VACUUM SENSOR	
2	DEWAR VACUUM		15	ANLG 3+ (EXT)	
3	15 K TEMP SENS		16	ANLG 3- (EXT)	
4	50 K TEMP SENS		17	ADDR 0 (EXT)	
5	300 K TEMP SENS		18	ADDR 1 (EXT)	
6	AC CURRENT SENS		19	ADDR 2 (EXT)	
7	RIGHT FET #1 BIAS		20	SOLENOID MONITOR	
8	RIGHT FET #2 BIAS		21	PUMP MONITOR	
9	LEFT FET #1 BIAS		22	M	
10	LEFT FET #2 BIAS		23	X MONITOR	
11	LED VOLTAGE		24	C MONITOR	
12			25	H MONITOR	
13	Q GROUND				
J2					
1	GROUND		14	F0	
2	+ 15 V SUPPLY		15	F1	
3	- 15 V SUPPLY		16	F2	
4			17	F3	
5			18	S0	
6	X OUTPUT		19	S1	
7	C OUTPUT		20	S2	
8	H OUTPUT		21	S3	
9	PARITY*		22	S4	
10			23	S5	
11	CAL OUTPUT		24	M0	
12	HI-CAL OUTPUT		25	M1	
13	GROUND				

Description of I/O Lines

42-PIN REAR PANEL CONNECTOR:

XMIT+, XMIT-: Monitor/Control transmit bus input from station computer.
+5 VOLT SUPPLY: +5 V input from power supply.
MODULATOR: TTL input for 80 Hz calibrator noise diode modulating signal; it switches the diode on and off.
RCV+, RCV-: Monitor/Control receive bus output to station computer.
+15 VOLT SUPPLY: +15 V input from power supply.
-15 VOLT SUPPLY: -15 V input from power supply.
+28 VOLT SUPPLY: +28 V input from power supply.
GROUND: Module ground for signals and return for power supplies.

DB-25 MALE FRONT PANEL CONNECTOR (J1, MONITOR):

PUMP VACUUM: Input voltage from the vacuum sensor in the front end pump line.
DEWAR VACUUM: Input voltage from the vacuum sensor in the front end dewar.
15 K TEMP SENSOR: Input voltage from the temperature sensor at the 15 K refrigerator stage in the front end.
50 K TEMP SENSOR: Input voltage from the temperature sensor at the 50 K refrigerator stage in the front end.
300 K TEMP SENSOR: Input voltage from the temperature sensor in the front end card cage at room temperature.
AC CURRENT: Input voltage from the refrigerator AC current sensor.
RIGHT FET #1 BIAS: Bias voltage input from the first FET of the low noise amplifier for the RCP channel.
RIGHT FET #2 BIAS: Bias voltage input from the later FET's of the low noise amplifier for the RCP channel.
LEFT FET #1 BIAS: Bias voltage input from the first FET of the low noise amplifier for the LCP channel.
LEFT FET #2 BIAS: Bias voltage input from the later FET's of the low noise amplifier for the LCP channel.
LED VOLTAGE: Voltage measured across a resistor feeding the LED's used in HEMT amplifiers in the front end. Allows LED current to be measured.
QUALITY GROUND: Common ground return for all analog sensors in the front end.
VACUUM SENSOR: Direct, non-linearized input from the Dewar vacuum sensor. Allows more accurate pressure calculation.
ANLG 3+, ANLG 3-: Extra analog input used with an external multiplexer controlled by ADDR 0-2 (below).
ADDR 0-2: Address output lines for control of external multiplexer for additional analog inputs. Used with ANLG 3 (above).

Description of I/O Lines (cont.)

DB-25 MALE FRONT PANEL CONNECTOR (J1, MONITOR) (cont.):

SOLENOID MONITOR: TTL input indicating position of the pump line solenoid. LO = closed, HI = open.
PUMP MONITOR: TTL input indicating if vacuum pumping is requested by the front end. LO = pump off, HI = pump on.
M (MAN/CPU): TTL input indicating whether the front end is controlled manually or by the station computer. LO = manual, HI = computer.
X/C/H MONITOR: Monitor inputs for the cryogenic state of the front end. See software control listing above for interpretation.

DB-25 FEMALE FRONT PANEL CONNECTOR (J2, CONTROL):

GROUND: Power supply return ground for front end. Connected to Pin 13.
+ 15V SUPPLY: Supply output for the front end.
- 15V SUPPLY: Supply output for the front end.
X/C/H OUTPUT: Cryogenic state control bits output.
PARITY: Parity bit for error checking of frequency bits used in ID word for the M/C Standard Interface. See description below.
CAL OUTPUT: +28 Volt output to power the front end's low-level calibrator diode.
HI CAL OUTPUT: +28 Volt output to power the front end's high-level calibrator diode.
GROUND: Power supply return ground for front end. Connected to Pin 1.
F0-F3: Frequency bits of ID number input from front end.
S0-F5: Serial number bits of ID number input fromfront end.
M0-M1: Modification bits of ID number input from front end.

Related Documents

1. Specification of Monitor and Control Standard Interface, A55001N002-A, L. R. D'Addario, November, 1985.

2. Specification of Monitor and Control Bus at VLBA Stations, A55001N001, B. G. Clark, December 1984.

3. Discussion of the Front-End Monitor and Control System, VLBA Electronics Memo 41, Dick Thompson, April, 1985.

4. Vertex Room Interfacing, VLBA Electronics Memo 42, R. Norrod, April, 1985.

5. Front-End Monitor and Control, VLBA Electronics Memo 43, S. Weinreb, April, 1985.

6. Meeting on Front-End Interface, VLBA Electronics Memo 44, Dick Thompson, May, 1985.

7. Front-End Changes, VLBA Electronics Memo 60, S. Weinreb, February, 1986.

I. General Description.

The purpose of the Front End Interface (F117) modules is to provide a link between the Monitor/Control system and the front ends, which, with one exception, are cryogenic. Each F117 has the capability to monitor the analog and digital signals associated with the various subsystems in each front ends. The F117 also allows control of the front end by computer command. Generally, the subsystems monitored and controlled by the F117 include the cryogenics, the vacuum pump, the calibrator noise sources, temperature sensors, and FET bias voltages and currents.

II. Circuit Description.

Referring to the F117 schematic, C53510S003, the circuitry on the left communicates with the Monitor/Control Standard Interface board, which is described in its Specification (see "Related Documents" above). IC's 1AB, 1AA, 1B, 1CB and 1D are used for handshaking and address decoding. IC 5D allows the Standard Interface (MCSI) to read the serial number of the module. This serial number is set by wires on the 100-pin connector into which the wirewrap board is plugged. The set of IC's 2A - 2E, 3A, and 3B are latches and buffers that allow the digital commands to be output, and the digital monitors to be read onto the M/C bus. IC 2A is the cryogenic ('cryo') state latch and 3A allows the cryo state to be read back at the same address. The readback makes the address look like a memory location to the computer; that is, the number written can be read back. 2B is the calibrator state latch, and 3B is its readback. IC's 2C and 2D read the Frequency number, Serial number and Revision number of the front end. This is a 12-bit number which is brought down on 12 lines from the front end, and is unique to each front end. IC 2E is a digital state monitor latch which allows the monitoring of various front end parameters, including the cryo state. This

allows verification that the cryo state command was properly received and interpreted by the front end.

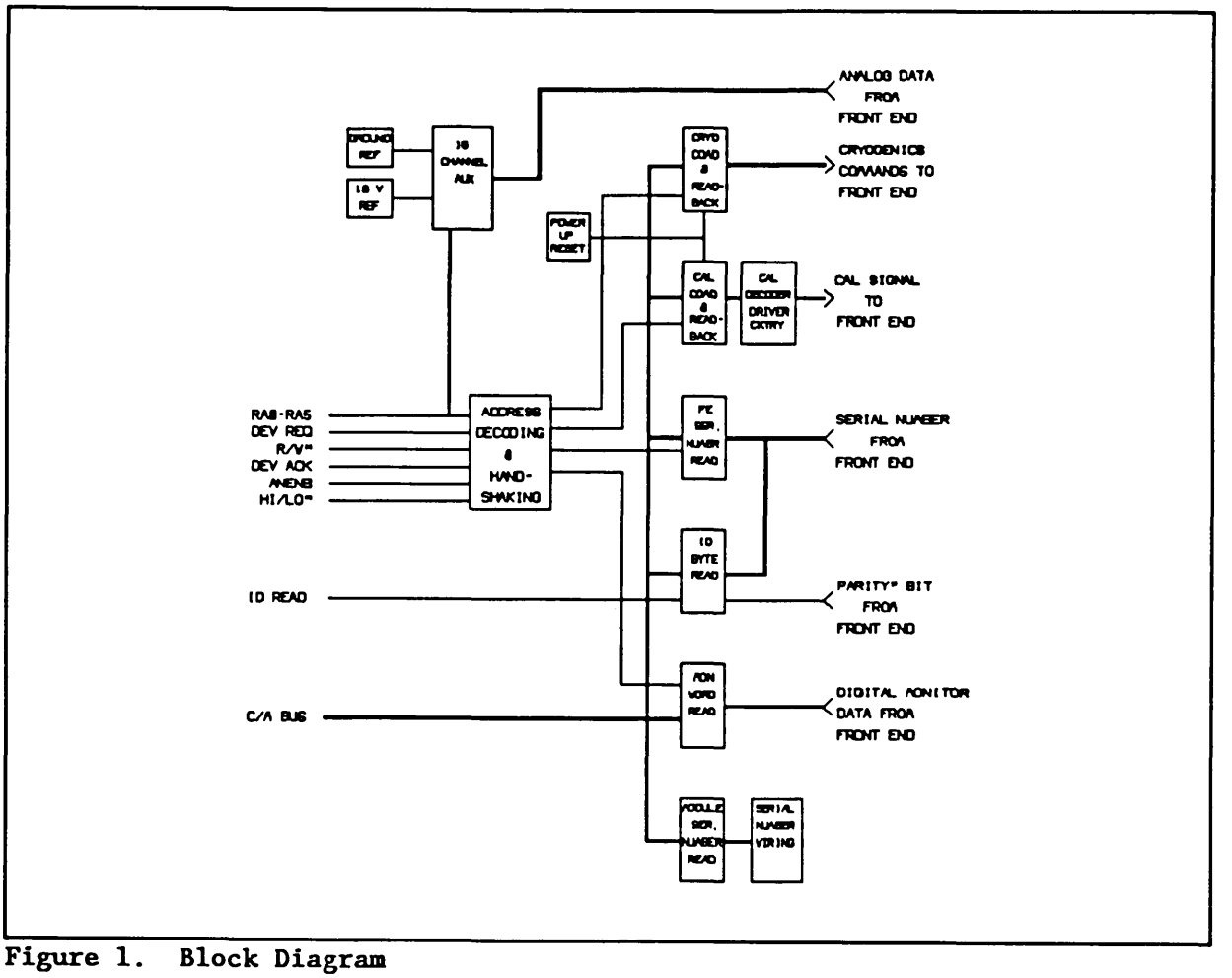


Figure 1. Block Diagram

IC 5E is the ID read latch. It allows the MCSI to read the ID and parity bits which include the Frequency bits F0 - F3 from the front end, along with some hard wired bits identifying the device as a front end. This allows the M/C Standard Interface board to know that it is connected to a front end as well as its frequency band. This ID process is described in more detail in the MCSI specification.

To the right of the latches, gates 1AC, 1AD, 1CC, and 1CD decode the Calibrator (Cal) commands for the Cal source driver circuitry. The Cal modulator

signal (MOD) is received by 5A, and goes to AND gates 1AC and 1AD. IC 4C is a quad transistor array used as a twin two-transistor driver for the low and high (solar) Cal signals. These drivers have been optimized to give a minimum voltage drop, less than 0.1 volt @ 50 mA drive current. The output currents are sampled by IC 3D to give an output voltage proportional to the current. IC 3E is a dual comparator which cuts off the output drive if the current rises above a level which is set by R53 and R54. These resistors also serve to set the reference level for the MOD signal receiver. Potentiometers R55 and R56 set the current to voltage ratio and are adjusted in the calibration procedure. ANLG 6+ and ANLG 7+ are voltage measurement points to allow the cal voltages to be monitored.

On the far left side, IC 4A is a 16-channel single-ended CMOS analog multiplexer. The analog monitor voltages from the front end are all referenced to a single "quality" ground. This IC multiplexes these onto a single double ended output which goes to the MCSI board. If additional inputs external to the module are required (specifically, in the F118 module), the F117 provides one differential input ANLG 3± and 3 address lines, ADDR0 - ADDR2 to provide for 8 additional analog inputs. These lines are connected through J1 on the front panel.

IC 3C is a 7.5 volt reference which, along with ground, allow the analog voltage measurement circuitry to be checked and adjusted. IC 1F is a power-up reset. If a power failure occurs 1F sets all command latches to logical zero upon reapplication of power. This puts the front end into the COOL mode, and turns off the cal signals.

Further information about specific details of the operation of the F117 module can be found elsewhere in this manual, or in the documents listed under "Related Documents".

III. Test Procedure.

The test procedure for the F117 module is automated, for the most part, using a computer to 'exercise' the module.

REQUIREMENTS:

1. IBM PC or compatible. Must have serial port on COM1.
2. RS-232 to RS-422/485 converter.
3. MODTEST program.
4. Oscilloscope.
5. Voltmeter, preferably digital.
6. Power supply to supply +5 V, ±15 V and + 28 V power.
7. Cable to connect the module to the power supply and to the RS-422 converter (described below).
8. Two 25-conductor cables each with a male D-25 connector on one end, and a female D-25 on the other.
9. F117 test box.

Connect the power supply, the RS-422 converter and the module together with the cable as shown in Figure 2. Boot the computer up normally, and put the disk with the MODTEST program into whichever disk drive is normally used for running external programs. The DOS disk need not be in the drive, and the MODTEST program can be copied onto a hard disk, if desired. Type 'MODTEST' to execute the program. The program will indicate what to do to check out the module.

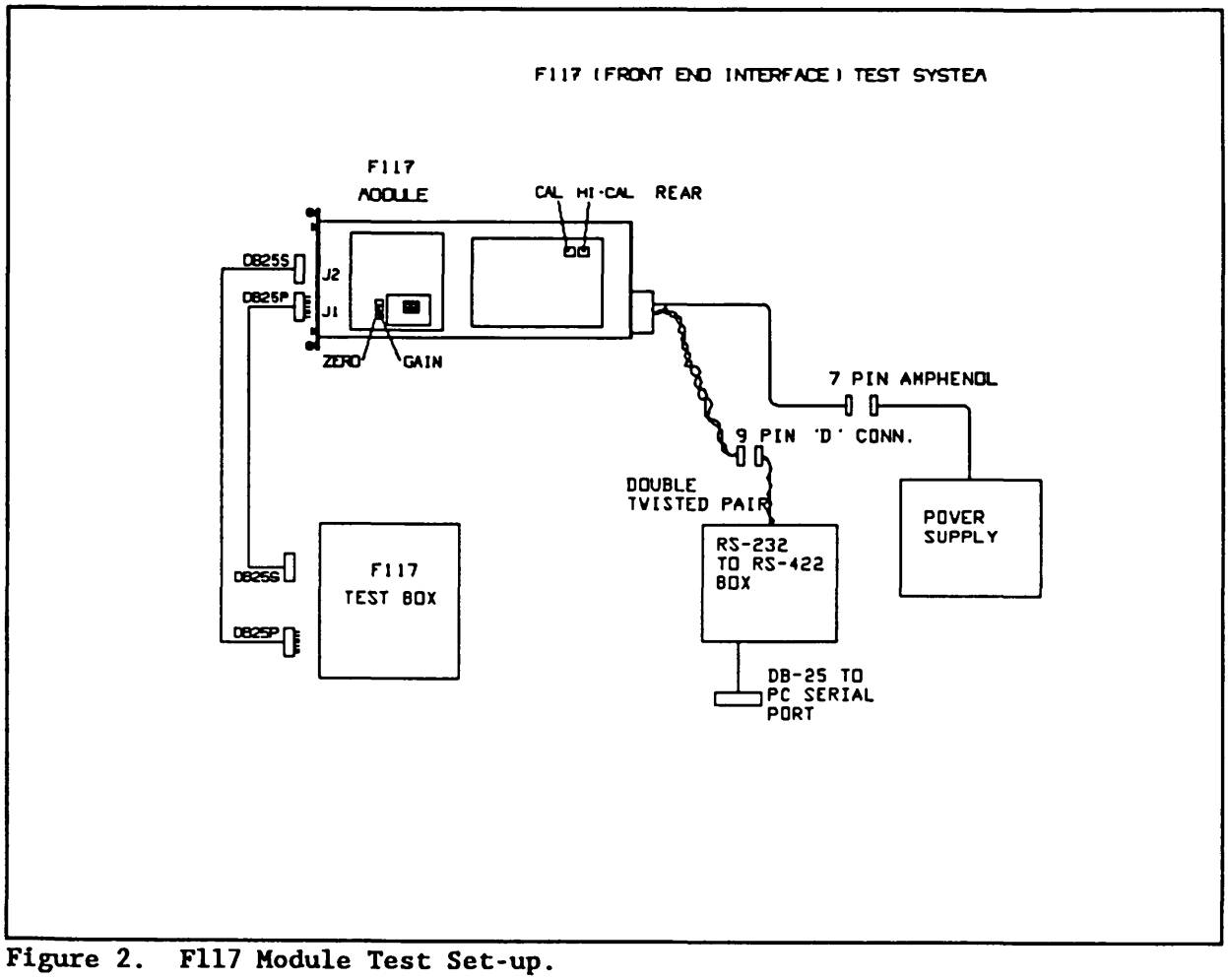


Figure 2. F117 Module Test Set-up.

F117 TEST CABLE

P1 = 42-pin rack type AMP connector.
P2 = 7-pin blue Amphenol plug.
P3 = 9-pin DB-9P plug.
P4 = BNC male plug.

P1

FROM	TO	COLOR	USE
P1-8	P3-1	red	XMIT+
P1-9	P3-2	black	XMIT-
P1-10	P2-E	orange	+5 V
P1-12	P4-cntr	RG-188	MOD
P1-14	P3-8	white	RCV+
P1-15	P3-9	black	RCV-
P1-16	P2-D	red	+15 V
P1-17	P2-F	yellow	-15 V
P1-29	P2-C	gray	+28 V
P1-34	P2-A	black	GND

P2

FROM	TO	COLOR	USE
P2-A	P1-34	black	GND
P2-C	P1-29	gray	+28 V
P2-D	P1-16	red	+15 V
P2-E	P1-10	orange	+5 V
P2-F	P1-17	yellow	-15 V

P3

FROM	TO	COLOR	USE
P3-1	P1-8	red	XMIT+
P3-2	P1-9	black	XMIT-
P3-8	P1-14	white	RCV+
P3-9	P1-15	black	RCV-

P4

FROM	TO	COLOR	USE
P4-cntr	P1-12	RG-188	MOD
P4-shld	NOT CONNECTED		

VLBA FRONT END MODULE F117 INTERNAL WIRING HARNESS JULY,7,1987
DRAWING:A53510W006 WILLIAM WIREMAN
REVISIONS: DATE:
NOTE: (L) INDICATES THE SIGNAL IS LOW TRUE, EX. HI-LO(L) LO=LOW SIGNAL
PART I-WIREWRAP CONNECTOR WIRING

PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1.	GND	REF GND	BLK	22	2.	5V	TB1-4	ORG	22
3.	GND				4.	5V			
5.	ANLG 4+	P1-5	WHT/GRY	26	6.	ANLG 5+	P1-6	WHT/VIO	26
7.					8.	Q GND	J1-13	BLK	22
9.	*Q GND	P1-19	BLK	26	10.	ANLG 1 & 2+	P1-2	WHT/GRN	26
11.	R/W(L)	P1-49	WHT/BLU	26	12.	DEV REQ	P1-35	WHT/BRN	26
13.	ANLG 6+	P1-7	WHT/YEL	26	14.	ANLG 7+	P1-8	WHT/BLK	26
15.	DEV ACK	P1-36	WHT/GRY	26	16.	ID READ	P2-9	WHT/ORG	26
17.	HI-LO(L)SEL	P1-17	WHT/GRN	26	18.	ANENB	P1-37	WHT/VIO	26
19.	S/N 0	GND/5V	BUSS	26	20.	S/N 1	GND/5V	BUSS	26
21.	S/N 2	GND/5V	BUSS	26	22.	S/N 3	GND/5V	BUSS	26
23.	S/N 4	GND/5V	BUSS	26	24.	S/N 5	GND/5V	BUSS	26
25.	S/N 6	GND/5V	BUSS	26	26.	S/N 7	GND/5V	BUSS	26
27.	GND	WW BD	BUSS	26	28.	5V	WW BD	BUSS	26
NOTE: STRAP SERIAL/NUMBER TO PINS 27 FOR ZERO AND 28 FOR A ONE, EX. S/N=18									
STRAP S/N 0,2,3,5,6,7 TO GND PIN 27 AND S/N 1,4 TO 5V PIN 28									
29.	ADDR 0	P1-48,J1-17	WHT/VIO	26	30.	ADDR 1	P1-47,J1-18	WHT/YEL	26
31.	ADDR 2	P1-46,J1-19	WHT/BLK	26	32.	ADDR 3	P1-45	WHT/RED	26
33.	ADDR 4	P1-44	WHT/BLK	26	34.	ADDR 5	P1-43	WHT/YEL	26
35.	C/M 0	P1-33	WHT/ORG	26	36.	C/M 1	P1-16	WHT/ORG	26
37.	C/M 2	P1-32	WHT/BLU	26	38.	C/M 3	P1-15	WHT/BLU	26
39.	C/M 4	P1-31	WHT/RED	26	40.	C/M 5	P1-14	WHT/RED	26
41.	C/M 6	P1-30	WHT/BLK	26	42.	C/M 7	P1-13	WHT/BLK	26
43.	C/M 8	P1-29	WHT/YEL	26	44.	C/M 9	P1-12	WHT/YEL	26
45.	C/M 10	P1-28	WHT/VIO	26	46.	C/M 11	P1-11	WHT/VIO	26
47.	C/M 12	P1-27	WHT/GRY	26	48.	C/M 13	P1-10	WHT/GRY	26
49.	GND				50.				
51.	C/M 14	P1-26	WHT/BRN	26	52.	C/M 15	P1-9	WHT/BRN	26
53.					54.				
55.	CAL	J2-11	BLU	22	56.	HI-CAL	J2-12	VIO	22
57.	LF1	J1-9	WHT/RED	26	58.	RF1	J1-7	WHT/YEL	26
59.	LF2	J1-10	WHT/BLU	26	60.	RF2	J1-8	WHT/BLK	26
61.	15 K	J1-3	WHT/GRN	26	62.	50 K	J1-4	WHT/BRN	26
63.	300 K	J1-5	WHT/GRY	26	64.	VD	J1-2	WHT/ORG	26
65.	VP	J1-1	WHT/BLU	26	66.	ACI	J1-6	WHT/VIO	26
67.	LED(L)	J1-11	WHT/ORG	26	68.	SENS	J1-14	WHT/GRN	26
69.	PA	J2-9	WHT/RED	26	70.	H(L)	J2-8	WHT/BLK	26
71.	C	J2-7	WHT/YEL	26	72.	X	J2-6	WHT/VIO	26
73.	GND				74.				
75.	H-MON(L)	J1-25	WHT/GRY	26	76.	C-MON	J1-24	WHT/BRN	26
77.	X-MON	J1-23	WHT/GRN	26	78.	M(L)	J1-22	WHT/ORG	26
79.	P	J1-21	WHT/BLU	26	80.	S	J1-20	WHT/RED	26
81.	F 0	J2-14	WHT/BLK	26	82.	F 1	J2-15	WHT/RED	26
83.	F 2	J2-16	WHT/BLU	26	84.	F 3	J2-17	WHT/ORG	26
85.	M 0	J2-24	WHT/RED	26	86.	M 1	J2-25	WHT/BLU	26
87.	S 0	J2-18	WHT/GRN	26	88.	S 1	J2-19	WHT/BRN	26

INTERNAL WIRING HARNESS (cont.)

89. S 2	J2-20	WHT/GRY	26	90. S 3	J2-21	WHT/VIO	26
91. S 4	J2-22	WHT/YEL	26	92. S 5	J2-23	WHT/BLK	26
93. MOD	FT-6	WHT/RED	26	94. -15V	TB1-5	YEL	22
95. 15V	TB1-6	RED	22	96. 28V	TB1-7	GRY	22
97. GND				98. 5V			
99. GND	REF GND	BLK	22	100. 5V	TB1-4	ORG	22

PART II-STANDARD INTERFACE BOARD WIRING

JACK P1				JACK P2			
PIN FUNCTION	SOURCE	COLOR	GA	PIN FUNCTION	SOURCE	COLOR	GA
1.				1. 5V			
2. ANLG 1+	W-10	WHT/GRN	26	2.			
3. ANLG 2+	P1-2	BUSS	26	3.			
4. ANLG 3+	J1-15	WHT/BRN	26	4.			
5. ANLG 4+	W-5	WHT/GRY	26	5.			
6. ANLG 5+	W-6	WHT/VIO	26	6.			
7. ANLG 6+	W-13	WHT/YEL	26	7.			
8. ANLG 7+	W-14	WHT/BLK	26	8.			
9. C/M 15	W-52	WHT/BRN	26	9. ID READ	W-16	WHT/ORG	26
10. C/M 13	W-48	WHT/GRY	26	10.			
11. C/M 11	W-46	WHT/VIO	26	11.			
12. C/M 9	W-44	WHT/YEL	26	12.			
13. C/M 7	W-42	WHT/BLK	26	13. GND	REF GND	BLK	22
14. C/M 5	W-40	WHT/RED	26	14. 5V	TB1-4	ORG	22
15. C/M 3	W-38	WHT/BLU	26	15. 15V	TB1-6	RED	22
16. C/M 1	W-36	WHT/ORG	26	16. -15V	TB1-5	YEL	22
17. HI-LO(L)SEL	W-17	WHT/GRN	26	17.			
18.				18.			
19. *Q GND	W-9	BLK	26	19. RCV+	FT-7	WHT-PR	26
20. *Q GND	P1-19	BUSS	26	20. RCV-	FT-9	BLK-PR	26
21. ANLG 3-	J1-16	WHT/GRY	26	21. XMIT+	FT-8	RED-PR	26
22. ANLG 4-	P1-38	BUSS	26	22. XMIT-	FT-10	BLK-PR	26
23. ANLG 5-	P1-38	BUSS	26	23.			
24. ANLG 6-	P1-38	BUSS	26	24.			
25. ANLG 7-	P1-38	BUSS	26	25. GND			
26. C/M 14	W-51	WHT/BRN	26				
27. C/M 12	W-47	WHT/GRY	26				
28. C/M 10	W-45	WHT/VIO	26				
29. C/M 8	W-43	WHT/YEL	26				
30. C/M 6	W-41	WHT/BLK	26				
31. C/M 4	W-39	WHT/RED	26				
32. C/M 2	W-37	WHT/BLU	26				
33. C/M 0	W-35	WHT/ORG	26				
34. GND	REF GND	BLK	22				
35. DEV REQ	W-12	WHT/BRN	26				
36. DEV ACK	W-15	WHT/GRY	26				
37. ANENB	W-18	WHT/VIO	26				
38. GND P1-22,23,24,25		BUSS	26				
39. -15V	TB1-5	YEL	22				
40. 15V	TB1-6	RED	22				
41.							

INTERNAL WIRING HARNESS (cont.)

42.				
43.	ADDR 5	W-34	WHT/YEL	26
44.	ADDR 4	W-33	WHT/BLK	26
45.	ADDR 3	W-32	WHT/RED	26
46.	ADDR 2	W-31	WHT/BLK	26
47.	ADDR 1	W-30	WHT/YEL	26
48.	ADDR 0	W-29	WHT/VIO	26
49.	R/W(L)	W-11	WHT/BLU	26
50.	5V	TB1-4	ORG	22

PART III-REAR PANEL CONNECTOR WIRING

JACK 11 (AMP 42 PIN)

PIN	FUNCTION	SOURCE	COLOR	GA	PIN	FUNCTION	SOURCE	COLOR	GA
1.					2.				
3.					4.				
5.					6.				
7.					8.	XMIT+	FT-8	RED-PR	26
9.	XMIT-	FT-10	BLK-PR	26	10.	5V	FT-2	ORG	20
11.					12.	MOD	FT-6	WHT/RED	26
13.					14.	RCV+	FT-7	WHT-PR	26
15.	RCV-	FT-9	BLK-PR	26	16.	15V	FT-5	RED	20
17.	-15V	FT-3	YEL	20	18.				
19.					20.				
21.					22.				
23.					24.				
25.					26.				
27.					28.				
29.	28V	FT-4	GRY	20	30.				
31.					32.				
33.					34.	GND	FT-1	BLK	20
35.					36.				
37.					38.				
39.					40.				
41.					42.				

PART IV-REAR SHIELD PANEL, FILTER FEEDTHRU

INTERNAL CONNECTIONS					REAR PANEL CONNECTIONS				
PIN	SOURCE	SOURCE	COLOR	GA	PIN	SOURCE	SOURCE	COLOR	GA
1.	GND	TB1-1	BLK	20	1.	GND	J11-34	BLK	20
2.	5V	TB1-4	ORG	20	2.	5V	J11-10	ORG	20
3.	-15V	TB1-5	YEL	20	3.	-15V	J11-17	YEL	20
4.	28V	TB1-7	GRY	20	4.	28V	J11-29	GRY	20
5.	15V	TB1-6	RED	20	5.	15V	J11-16	RED	20
6.	MOD	W-93	WHT/RED	26	6.	MOD	J11-12	WHT/RED	26
7.	REC +	P2-19	WHT-PR	26	7.	REC +	J11-14	WHT-PR	26
8.	XMIT +	P2-21	RED-PR	26	8.	XMIT +	J11-8	RED-PR	26
9.	REC -	P2-20	BLK-PR	26	9.	REC -	J11-15	BLK-PR	26
10.	XMIT -	P2-22	BLK-PR	26	10.	XMIT -	J11-9	BLK-PR	26

NOTE:WIRES ON FEEDTHRU'S 7 & 9, 8 & 10 ARE TWISTED PAIRS

INTERNAL WIRING HARNESS (cont.)

PART V-POWER DISTRIBUTION TERMINAL BLOCK

POWER SUPPLY INPUT					POWER DISTRIBUTION		
PIN	FUNCTION	SOURCE	COLOR	GA	SOURCE	COLOR	GA
TB1-1	GND	FT-1	BLK	20	GND REF	BLK	22
TB1-2							
TB1-3							
TB1-4	5V	FT-2	ORG	20	P1-50, P2-14, W-2, W-100	ORG	22
TB1-5	-15V	FT-3	YEL	20	P1-39, P2-16, W-94, J2-3	YEL	22
TB1-6	15V	FT-5	RED	20	P1-40, P2-15, W-95, J2-2	RED	22
TB1-7	28V	FT-4	GRY	20	W-96	GRY	22

PART VI-FRONT PANEL CONNECTOR WIRING

J1-MONITOR

PIN	FUNCTION	SOURCE	COLOR	GA
1.	VP	W-65	WHT/BLU	26
2.	VD	W-64	WHT/ORG	26
3.	15 K	W-61	WHT/GRN	26
4.	50 K	W-62	WHT/BRN	26
5.	300 K	W-63	WHT/GRY	26
6.	ACI	W-66	WHT/VIO	26
7.	RF1	W-58	WHT/YEL	26
8.	RF2	W-60	WHT/BLK	26
9.	LF1	W-57	WHT/RED	26
10.	LF2	W-59	WHT/BLU	26
11.	LED	W-67	WHT/ORG	26
12.				
13.	Q GND	W-8	BLK	22
14.	SENS	W-68	WHT/GRN	26
15.	ANLG 3+	P1-3	WHT/BRN	26
16.	ANLG 3-	P1-20	WHT/GRY	26
17.	ADDR 0	W-29	WHT/VIO	26
18.	ADDR 1	W-30	WHT/YEL	26
19.	ADDR 2	W-31	WHT/BLK	26
20.	S	W-80	WHT/RED	26
21.	P	W-79	WHT/BLU	26
22.	M(L)	W-78	WHT/ORG	26
23.	X MON	W-77	WHT/GRN	26
24.	C MON	W-76	WHT/BRN	26
25.	H MON(L)	W-75	WHT/GRY	26

J2-CONTROL

PIN	FUNCTION	SOURCE	COLOR	GA
1.	GND	REF GND	BLK	22
2.	15V	TB1-6	RED	22
3.	-15V	TB1-5	YEL	22
4.				
5.				
6.	X	W-72	WHT/VIO	26
7.	C	W-71	WHT/YEL	26
8.	H(L)	W-70	WHT/BLK	26
9.	PA(L)	W-69	WHT/RED	26
10.				
11.	CAL	W-55	BLU	22
12.	HI-CAL	W-56	VIO	22
13.	GND	REF GND	BLK	22
14.	F 0	W-81	WHT/BLK	26
15.	F 1	W-82	WHT/RED	26
16.	F 2	W-83	WHT/BLU	26
17.	F 3	W-84	WHT/ORG	26
18.	S 0	W-87	WHT/GRN	26
19.	S 1	W-88	WHT/BRN	26
20.	S 2	W-89	WHT/GRY	26
21.	S 3	W-90	WHT/VIO	26
22.	S 4	W-91	WHT/YEL	26
23.	S 5	W-92	WHT/BLK	26
24.	M 0	W-85	WHT/RED	26
25.	M 1	W-86	WHT/BLU	26

Data Sheets - Selected Portions

1. TL082 Texas Instruments
2. HI506A Harris Semiconductor
3. LM393A National Semiconductor
4. SN75141N Texas Instruments
5. AD584 Analog Devices
6. TPQ6502 Sprague

STOCK 021, 2, 4 CDEN

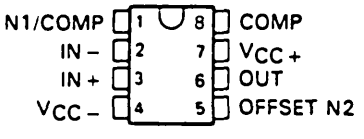
TYPES TL080 THRU TL085, TL080A THRU TL084A TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

D2297, FEBRUARY 1977—REVISED SEPTEMBER 1983

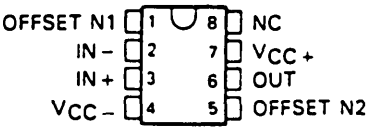
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- Low-Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% TYP
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

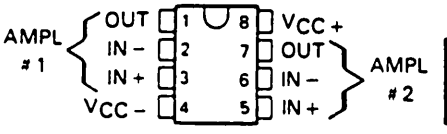
TL080, TL080A
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



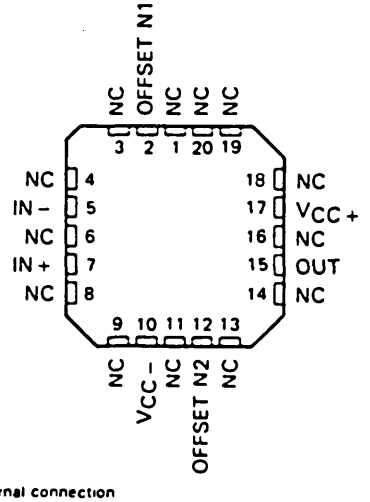
TL081, TL081A, TL081B
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



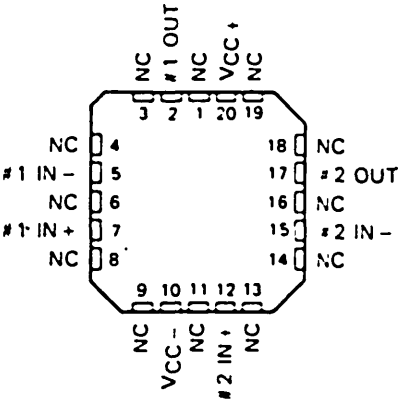
TL082, TL082A, TL082B
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL081M . . . FH OR FK
CHIP CARRIER PACKAGE
(TOP VIEW)



TL082M . . . FH OR FK
CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL080	TL081	TL082	TL083	TL084	TL085
TL08_M	JG	FH, FK, JG	FH, FK, JG	FH, FK, J	FH, FK, J, W	*
TL08_I	JG, P	JG, P	JG, P	J, N	J, N	*
TL08_C	JG, P	JG, P	JG, P	J, N	J, N	N
TL08_AC	JG, P	JG, P	JG, P	J, N	J, N	*
TL08_BC	*	JG, P	JG, P	*	J, N	*

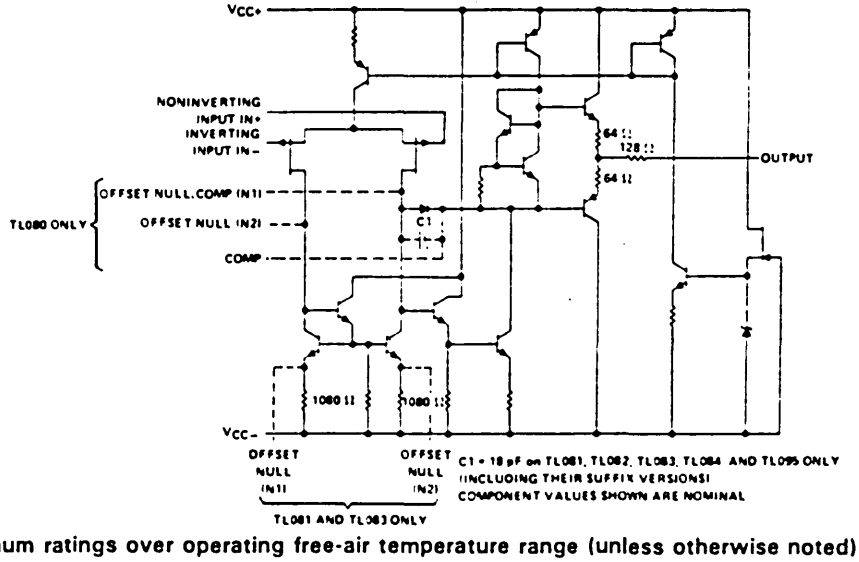
*These combinations are not defined by this data sheet.

description

The TL08_ JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08_ family.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FH, FK, J, JG, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the J and JG packages, TL08_M chips are alloy-mounted; TL08_I, TL08_C, TL08_AC, and TL08_BC chips are glass-mounted.

HARRIS

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

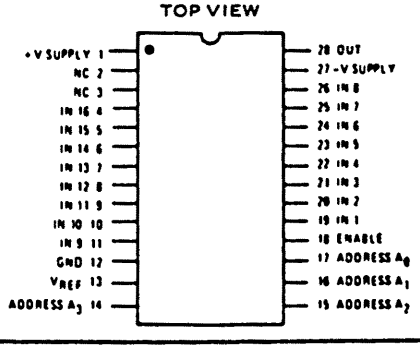
DESCRIPTION

The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

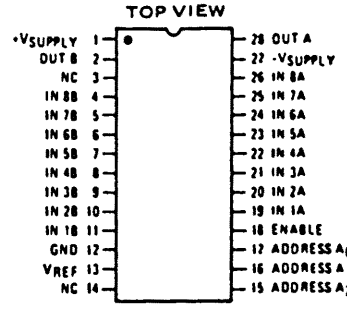
The HI-506A/507A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUT

HI-506A

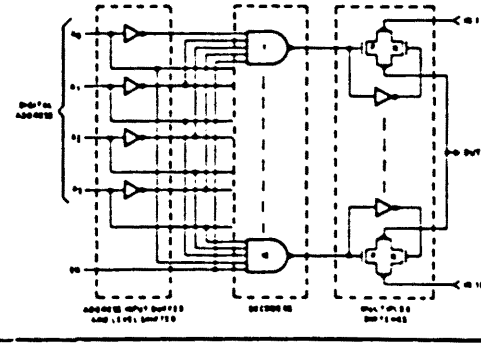


HI-507A

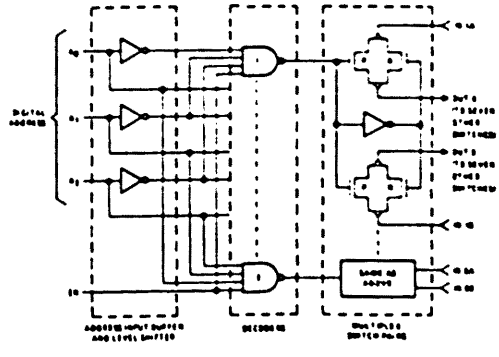


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 — 44V
V_{REF} to Ground V+ to Ground — 22V
V_{EN}, V_A, Digital Input Overvoltage:
V_A | V_{Supply} (+) — +4V
V_A | V_{Supply} (–) — –4V
Analog Overvoltage:
V_S | V_{Supply} (+) — +20V
V_S | V_{Supply} (–) — -20V

Total Power Dissipation* — 1200mW
Operating Temperature
HI-506A/507A-2 — -55°C to +125°C
HI-506A/507A-5 — 0°C to +75°C
Storage Temperature — -65°C to +150°C

*Derate 19.7mW/°C above T_A = 110°C.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER		TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS									
*V_S, Analog Signal Range		Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)		+25°C		1 2	1 5		1.5	1 8	KΩ
		Full		1 5	2 0		1.8	2 0	KΩ
*I_S (OFF), Off Input Leakage Current		+25°C		0 03			0 03		nA
		Full			±50			±50	nA
*I_O (OFF), Off Output Leakage Current		+25°C		1 0			1 0		nA
	HI-506A	Full			±300			±300	nA
	HI-507A	Full			±200			±200	nA
*I_O (OFF) with Input Overvoltage Applied (Note 2)		+25°C		4 0			4 0		nA
		Full			2 0				µA
*I_O (ON), On Channel Leakage Current		+25°C		0 1			0.1		nA
	HI-506A	Full			±300			±300	nA
	HI-507A	Full			±200			±200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)		Full			±50			±50	nA
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold | TTL Drive		Full			0 8			0 8	V
V_{AH}, Input High Threshold | (Note 7)		Full	4 0			4 0			V
V_{AL} | MOS Drive (Note 3)		+25°C			0 8			0 8	V
V_{AH} |		+25°C	6 0			6 0			V
*I_A, Input Leakage Current (High or Low)		Full			1 0			1 0	µA
SWITCHING CHARACTERISTICS									
t_A, Access Time		+25°C		0 5			0 5		µs
		Full			1.0			1.0	µs
t_{OPEN}, Break-Before-Make Delay		+25°C	25	80		25	80		ns
$t_{ON (EN)}$, Enable Delay (ON)		+25°C		300	500		300		ns
		Full			1000			1000	ns
$t_{OFF (EN)}$, Enable Delay (OFF)		+25°C		300	500		300		ns
		Full			1000			1000	ns
Settling Time (0.1%)		+25°C		1 3			1 3		µs
(0.025%)		+25°C		4 4			4 4		µs
"Off Isolation" (Note 4)		+25°C	50	68		50	68		dB
$C_{S (OFF)}$, Channel Input Capacitance		+25°C		5			5		pF
$C_{O (OFF)}$, Channel Output Capacitance	HI-506A	+25°C		50			50		pF
	HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance		+25°C		5			5		pF
$C_{DS (OFF)}$, Input to Output Capacitance		+25°C		0.1			0 1		pF
POWER REQUIREMENTS									
P_D, Power Dissipation		Full		7.5			7 5		mW
*I_+, Current Pin 1 (Note 5)		Full		0 5	2 0		0 5	2 0	mA
*I_-, Current Pin 27 (Note 5)		Full		0 02	1 0		0 02	1 0	mA
*I_+, Standby (Note 6)		Full		0 5	2 0		0 5	2 0	mA
*I_-, Standby (Note 6)		Full		0 02	1 0		0 02	1 0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = - 100 µA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L =15pF, V_S = 7VRMS, f = 500KHz.
5. V_{EN} = +4.0V
6. V_{EN} = 0.8V
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommanded.

*100% tested for Dash 8 at +25°C and +125°C only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

National Semiconductor

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

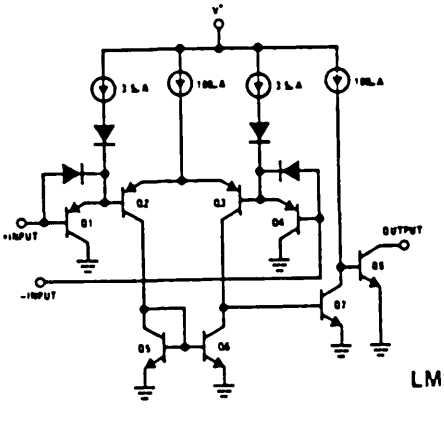
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

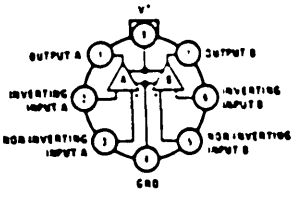
Features

- Wide single supply
  Voltage range 2.0 V_{DC} to 36 V_{DC}
  or dual supplies ±1.0 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.8 mA)—independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



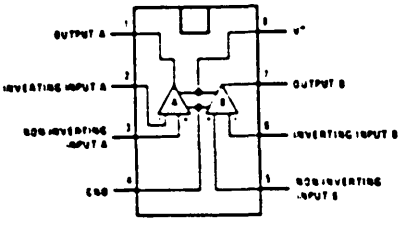
Metal Can Package



TOP VIEW

Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

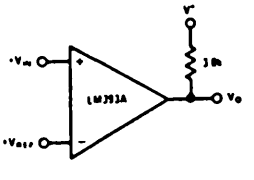
Dual-In-Line Package



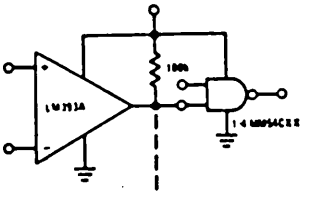
TOP VIEW

Order Number LM393N, LM393AN, or LM2903N
See NS Package N08B

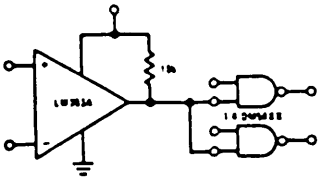
Typical Applications (V^+ = 5.0 V_{DC})



Basic Comparator



Driving CMOS



Driving TTL

TYPES SN55140, SN55141, SN55142, SN55143, SN75140, SN75141, SN75142, SN75143 DUAL LINE RECEIVERS

BULLETIN NO. DL-S 7712456, JANUARY 1977

features common to all eight types

- Single 5-V Supply
- ±100 mV Sensitivity
- For Applications As:
  Single-Ended Line Receiver
  Gated Oscillator
  Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications

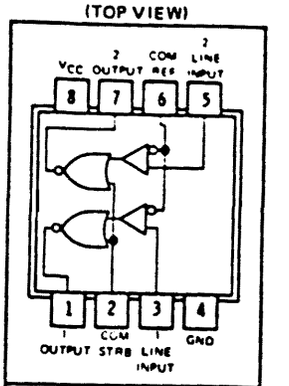
features of '140 and '141

- Common Reference Pin
- Common Strobe
- '141 Has Diode-Protected Input Stage for Power-Off Condition

features of '142 and '143

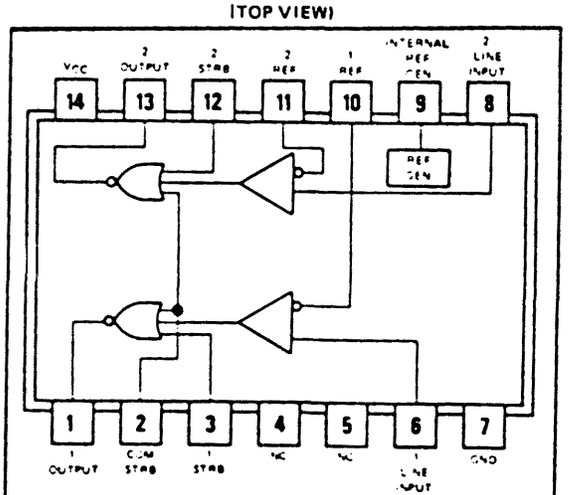
- Individual Reference Pins
- Common and Individual Strobes
- Internal 2.5-Volt Reference Available
- '143 Has Diode-Protected Input Stage for Power-Off Condition

SN55140, SN55141 . . .
JG DUAL-IN-LINE PACKAGE
SN75140, SN75141 . . .
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
see function table

SN55142, SN55143 . . . J DUAL-IN-LINE PACKAGE
SN75142, SN75143 . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 volts to 3.5 volts, making it possible to optimize noise immunity for a given system design. A 2.5-volt internal reference is available for use on the '142 and '143. Due to its low input current (less than 100 microamperes), it is ideally suited for party-line (bus-organized) systems.

The '140 has a common reference voltage pin and a common strobe. The '141 is the same as the '140 except that the input stage is diode protected. Each receiver of the '142 has an individual reference voltage pin and an individual strobe, and the dual receiver has a common strobe as well. The '143 is the same as the '142 except that the input stage is diode protected. The internal reference voltage of the '142 and '143 can be externally adjusted with a single resistor from 1.5 volts to 3.5 volts.

'140, '141 FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
$\leq V_{ref} - 100$ mV	L	H
$> V_{ref} + 100$ mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

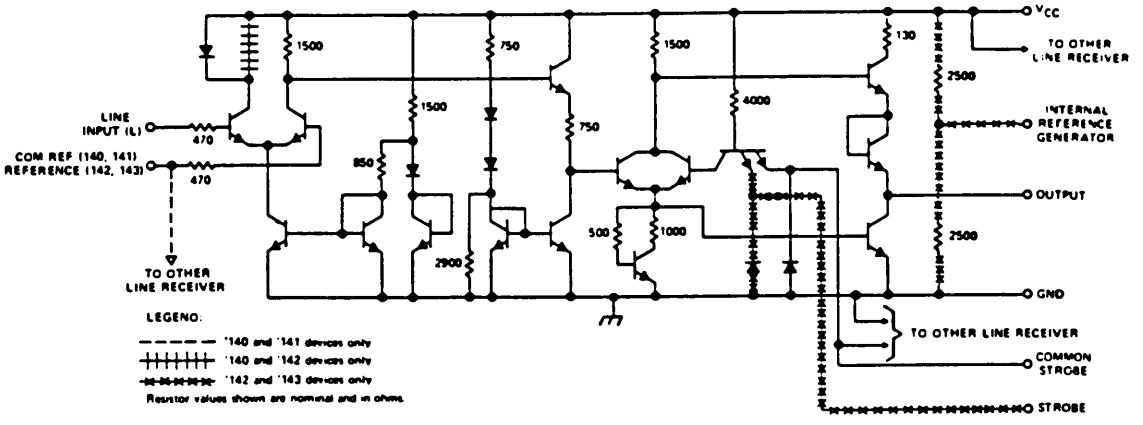
'142, '143 FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	INDIVIDUAL STROBE	COMMON STROBE	OUTPUT
$\leq V_{ref} - 100$ mV	L	L	H
$> V_{ref} + 100$ mV	X	X	L
X	H	X	L
X	X	H	L

H = high level, L = low level, X = irrelevant

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Reference input voltage, V_{ref}	5.5 V
Line input voltage with respect to ground	−2 V to 5.5 V
Line input voltage with respect to V_{ref}	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	600 mW
Operating free-air temperature range: SN55' Circuits	−55°C to 125°C
SN75' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J or JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. Unless otherwise specified, voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 18. In the J and JG packages, these chips are glass-mounted.

recommended operating conditions

	SN55' CIRCUITS			SN75' CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Reference input voltage, V_{ref}	1.5		3.5	1.5		3.5	V
Input voltage, line or strobe, V_I	0		5.5	0		5.5	V
Operating free-air temperature, T_A	−55		125	0		70	°C

ANALOG DEVICES

Pin Programmable Precision Voltage Reference

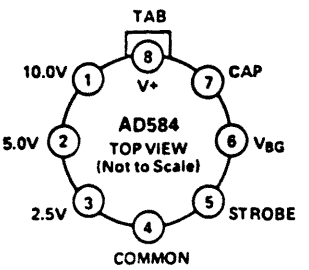
AD584*

FEATURES

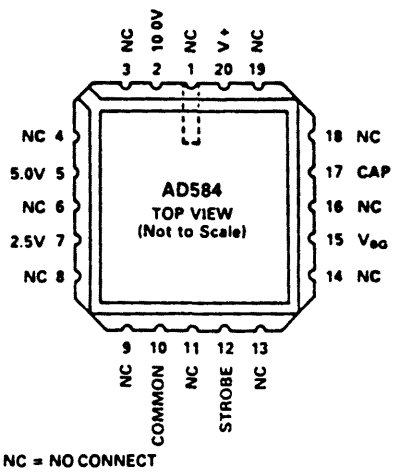
- Four Programmable Output Voltages: 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient: 5ppm/°C max, 0 to +70°C (AD584L) 15ppm/°C max, −55°C to +125°C (AD584T)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability

AD584 PIN CONFIGURATIONS

8-Pin TO-99



20-Pin LCC



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C; the AD584S and T are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed eight-terminal TO-99 metal can.

*Covered by U.S. Patent No. 3,887,863; RE 30,586

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).

8

Applying the AD584

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

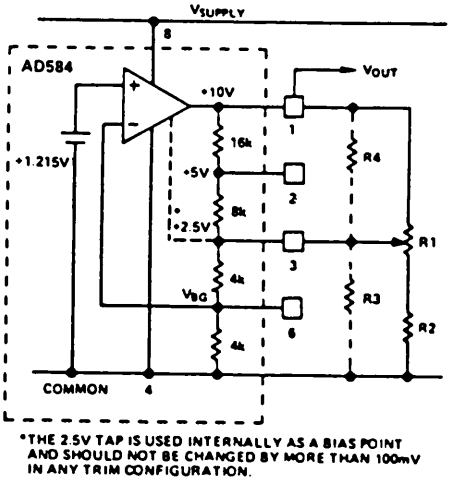


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

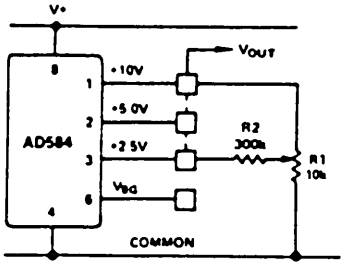


Figure 2. Output Trimming

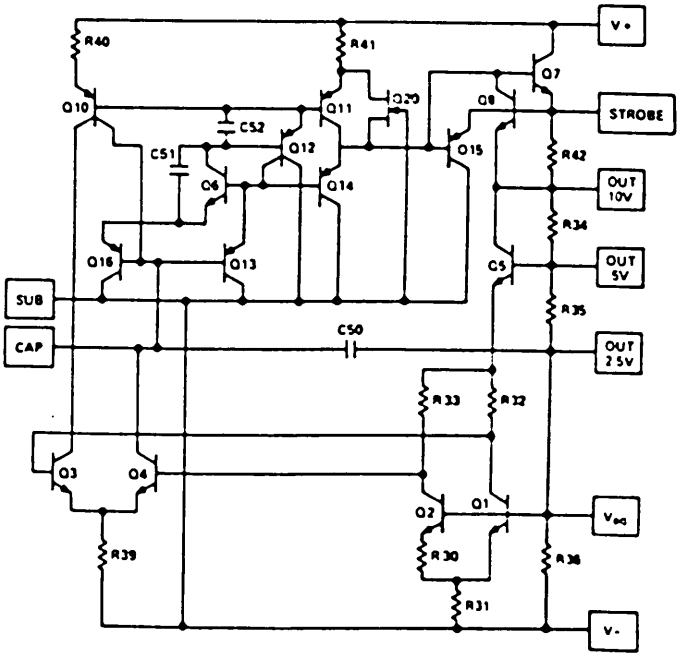
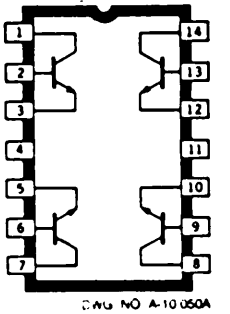


Figure 3. Schematic Diagram

SERIES TPQ
QUAD TRANSISTOR ARRAYS

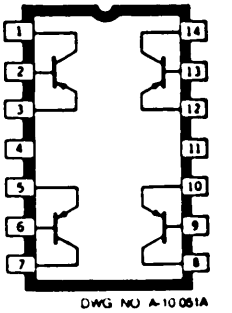
SPRAGUE SERIES TPQ quad transistor arrays are general-purpose silicon transistor arrays consisting of four independent devices. Shown are 12 NPN types, 12 PNP types, and nine NPN/PNP complementary pairs.

All of these devices are furnished in a 14-pin dual in-line plastic package. The molded package is identical to that used in most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.



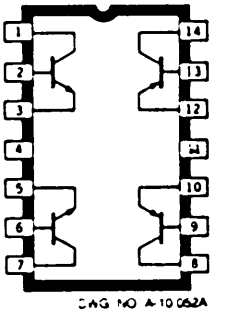
DWG NO A-10,050A

TPQ2221
TPQ2222
TPQ2483
TPQ2484
TPQ3724
TPQ3725
TPQ3725A
TPQ3904
TPQ5550
TPQ5551
TPQA05
TPQA06



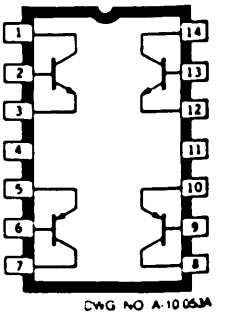
DWG NO A-10,061A

TPQ2906
TPQ2907
TPQ2907A
TPQ3798
TPQ3799
TPQ3906
TPQ4258
TPQ4354
TPQ5400
TPQ5401
TPQA55
TPQA56



DWG NO A-10,052A

TPQ6001
TPQ6002
TPQ6100
TPQ6100A



DWG NO A-10,053A

TPQ6501
TPQ6502
TPQ6600
TPQ6600A
TPQ6700

ABSOLUTE MAXIUMUM RATINGS

Power Dissipation, P_D (Each Transistor) . . . . . 500 mW
(Total Package) . . . . . 2.0 W*
Operating Temperature Range, T_A . . . . . −55°C to +150°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

*Derate at the rate of 16 mW/°C above T_A = +25°C

Additional information on
TPP and TPQ Transistor arrays is available from:

Sprague Electric Company
Discrete Semiconductor Operation
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

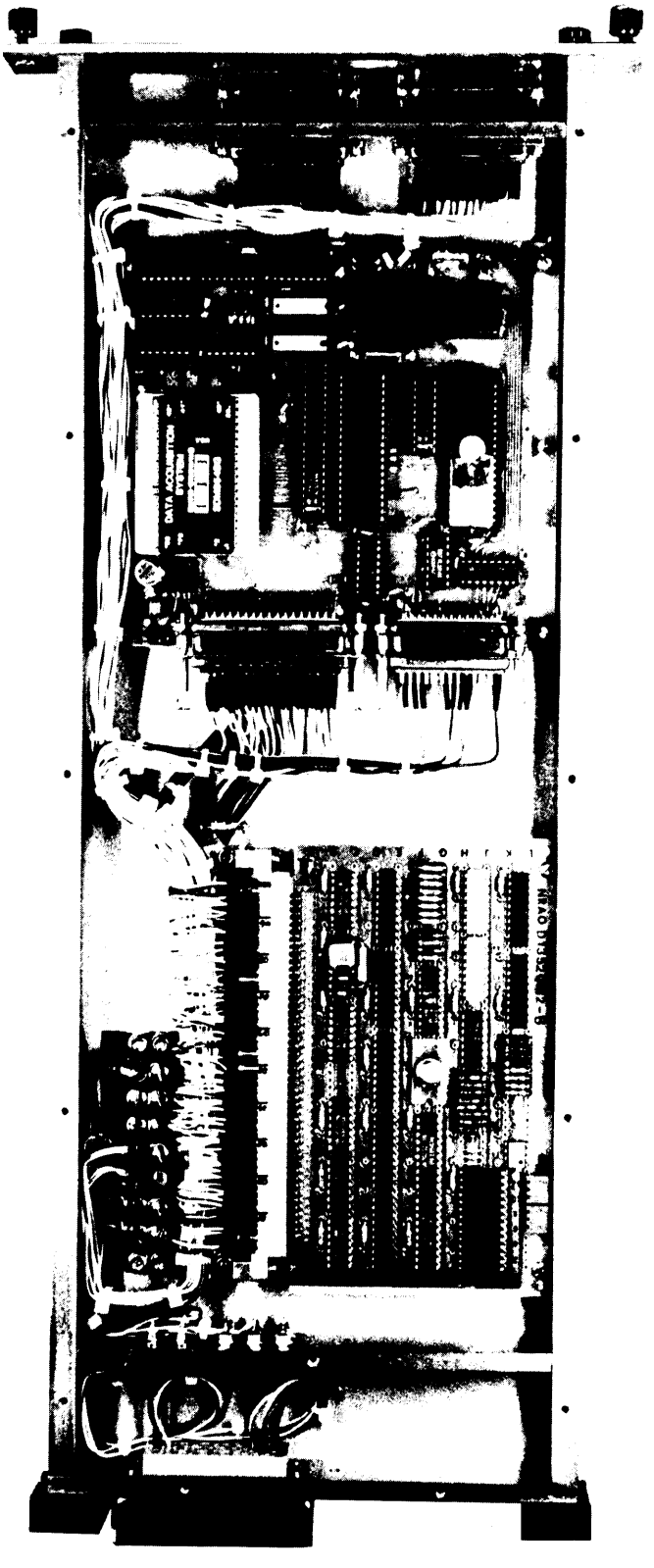
I_C (A)	Max. C_{ob} (pF)	Similar Discrete Devices
0	8.0	2N2906
0	8.0	2N2907
0	8.0	2N2907A
0	4.0	2N3798
0	4.0	2N3799
0	4.5	2N3906
0	3.0	2N4258
0	30 (Note 1)	2N4354
0	6.0	2N5400
0	6.0	2N5401
–	15	MPSA55
–	15	MPSA56

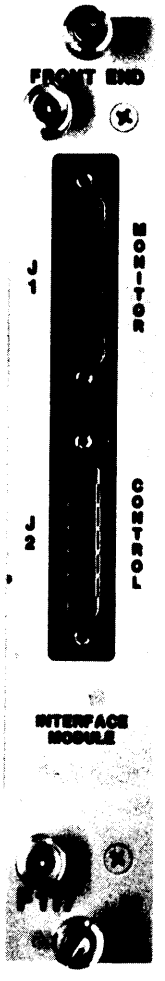
ELECTRICAL CHARACTERISTICS at T_A = +25°C

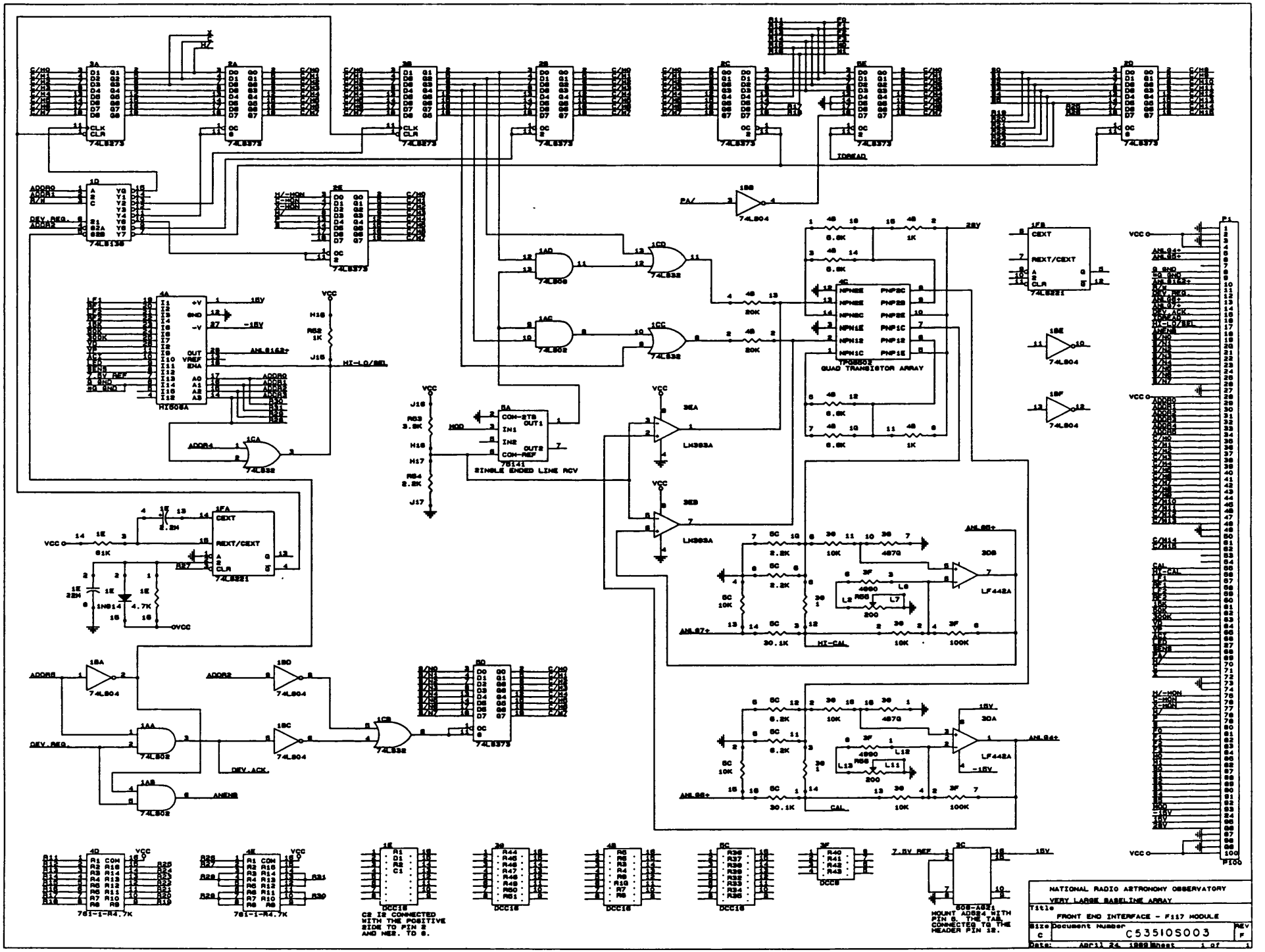
Part Number (See Note)	Min. BV_{CBO} (V)	Min. BV_{CEO} (V)	Min. BV_{EBO} (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	D-C Current Gain Min. h_{FE}	D-C Current Gain Conditions I_C (mA)	D-C Current Gain Conditions V_{CE} (V)	Saturation Voltage Max. V_{CE} (V)	Saturation Voltage Max. V_{BE} (V)	Saturation Voltage @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	Max. C_{ob} (pF)	Similar Discrete Devices
Two NPN/Two PNP Devices															
TPQ6001	60	30	5.0	30	50	25 35 40 20	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2221 and 2N2906
TPQ6002 (Note 1)	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907
TPQ6100	60	40	5.0	10	50	50 75 75 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2483 and 2N3798
TPQ6100A	60	45	5.0	10	50	100 150 150 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2484 and 2N3799
TPQ6501	60	30	5.0	30	50	25 35 40 20	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2221 and 2N2906
TPQ6502	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907
TPQ6600	60	40	5.0	10	50	50 75 75 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2483 and 2N3798
TPQ6600A	60	45	5.0	10	50	100 150 150 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2484 and 2N3799
TPQ6700	40	40	5.0	50	30	30 50 70	0.1 1.0 10	1.0 1.0 1.0	0.25	0.90	10	200	10	4.5	2N3904 and 2N3906

NOTE:
NPN/PNP complementary pairs. Polarity shown is for NPN devices.

TO




FRONT END
J1
MONITOR
J2
CONTROL
INTERFACE
MODULE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HI508A
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LF442A
TPS8802
GUAD TRANSISTOR ARRAY
75141
DIFFERENTIAL LINE RCV
IDREAD
DEV.REQ.
DEV.ACK.
ANENB
HI-LO/SEL
HI-CAL
CAL
-OVCC
P100
NATIONAL RADIO ASTRONOMY OBSERVATORY
VERY LARGE BASELINE ARRAY
Title
FRONT END INTERFACE - F117 MODULE
Size C
Document Number C535105003
REV F
Date: April 24, 1989 Sheet 1 of 1