Very Long Baseline Array Project

NO. 21

Technical Manual

L108

STATION TIMING MODULE

NATIONAL RADIO ASTRONOMY OBSERVATORY
P. O. Box O • Socorro, New Mexico 87801

OPERATED BY ASSOCIATED UNIVERSITIES INC.,
UNDER COOPERATIVE AGREEMENT WITH THE NATIONAL SCIENCE FOUNDATION

NO. 21

Technical Manual

L108

STATION TIMING MODULE

E. SCHLECHT
November 1990

Table of Contents

I. General Description.

The VLBA station timing module has several functions:

1. To provide 1 microsecond long timing pulses every second for the formatter circuitry. This is done by counting five million clock cycles of the 5 MHz reference from the MASER clock source.

2. To provide a 10 millisecond long pulse every second for the station computer, in order to synchronize it with the formatter circuitry.

3. To provide an 80 Hz square wave signal for the switched noise source calibration system.

4. To synchronize the above signals to an externally supplied one second timing source on manual command. The external signal is to be derived from a Global Positioning System satellite timing signal.

The outputs thus consist of eight 1 pulse per second (1PPS) signals 1μs long, one 1PPS signal 10 ms long and three 80 Hz signals, all on the rear panel. One 1PPS signal 1μs long and an 80 Hz output appear on the front panel. The inputs consist of the 5 MHz MASER rear panel input, and inputs for the external 1 PPS signal, one for positive and one for negative pulses, both on the front panel. The front panel also has a pushbutton switch to command the module to synchronize the MASER-derived 1 PPS signal with the external one.

II. Circuit Description.

The timing module circuitry includes two divider chains, one to produce the 1 PPS signal, the other to produce the 80 Hz. The 80 Hz divider chain operates independently from the 5 MHz input, except that it is reset and started by the 1 PPS signal. The reason for this particular design configuration (instead of counting down to 80 Hz then dividing by 80) is that it is desirable to mimic the 80 Hz signal produced in the formatter system. That signal is produced the same way, that is, by independently counting down to 80 Hz and synchronizing the resulting signal to the system 1 PPS timing signal from the L108.

The 1 PPS signal is produced as follows: the incoming 5 MHz is squared in a voltage comparator, whose output switches every time the input sine wave crosses zero (plus the delay time). In the circuit diagram, the comparator is IC 2F. The output is fed to the synchronous divider chain consisting of IC's 5A through 5F and 4A. Note that it is fed through the invertor 2CF. This is because pins 6 and 7 of the comparator are complementary outputs. Pin 7 is of the same polarity as the input signal. Since it is used to directly drive the Schottky TTL resynchronizer flip/flop, pin 6 and the invertor are used so as not to load the output too much. The synchronizer is described below.

IC's 5A through 5F are connected as divide by ten counters, and are cleared by a signal on pin 1. Pin 15 of each stage is connected to pin 10 of the following stage to synchronize the counters. This results in an output signal which is delayed from the input by only one counter delay rather than seven.

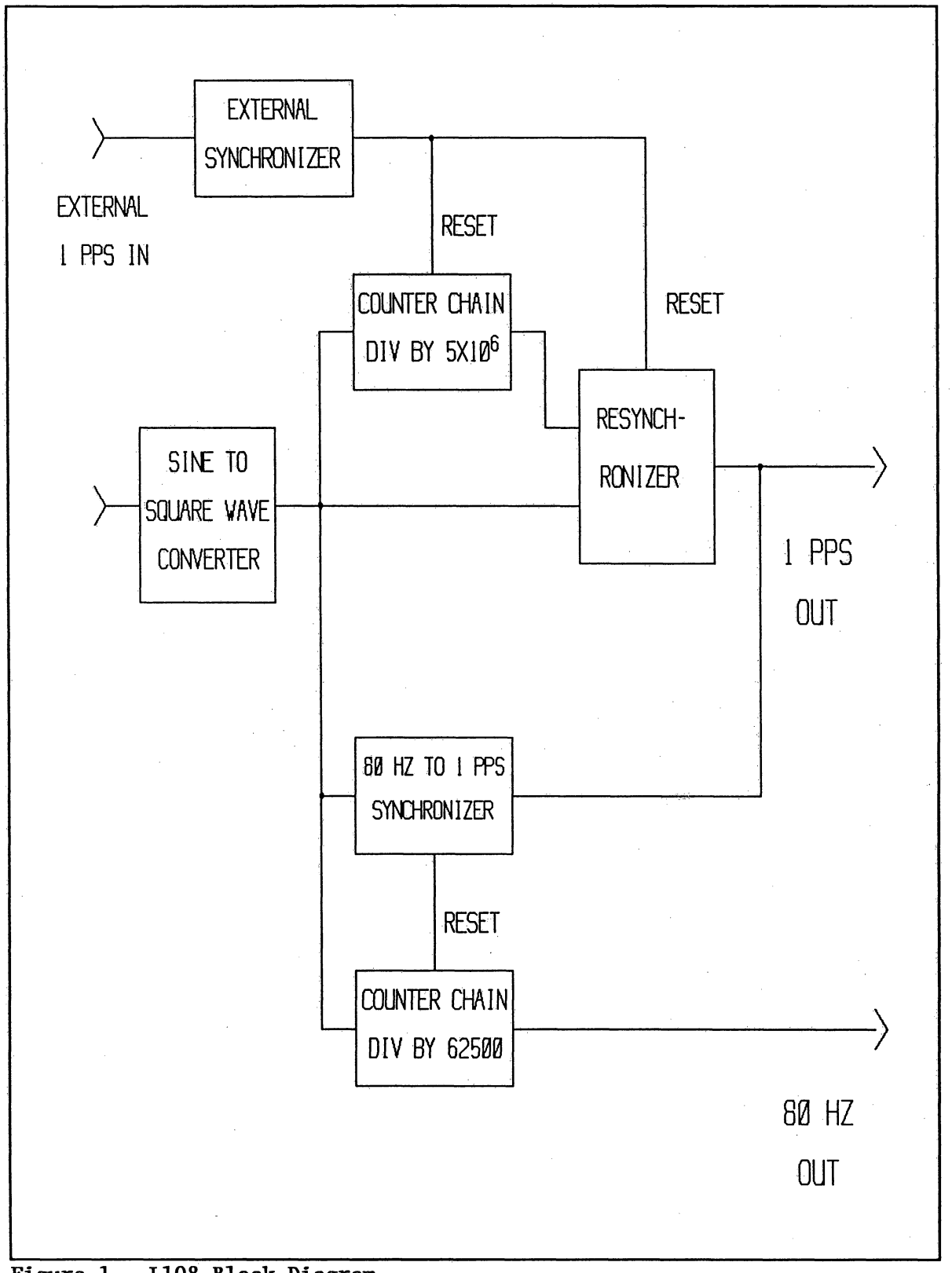


Figure 1. L108 Block Diagram.

IC 4A is a different type of counter, to enable counting to five instead of to 10. This is done by preloading a '5' into the load inputs of IC 4A every time it counts to maximum, rather than letting it return to zero. Normally the way to do this would be to take the ripple carry output (RCO) of the counter and use it to load the '5' into the inputs. Unfortunately, this would clear the RCO/LOAD pulse prematurely, resulting in a spike which would cause erratic operation. Thus the circuitry of 4EB and 2EA is used to generate a LOAD pulse that is exactly one half clock cycle long to load the '5' into counter 4A. It requires an RCO output more than 1/2 cycle before the final count, however. Since the RCO of the 74LS190 does not go active until 1/2 cycle before, it cannot set flip flop 4EB early enough. Hence, the RCO of IC 5A is used instead. It must be gated by the MAX/MIN of 4A since 5A's RCO occurs every fifth of a second. MAX/MIN itself cannot be used because it goes active 1/5 of a second early, when a '9' appears on the outputs of 4A. Thus the RCO from 5A is 'AND'ed with MAX/MIN from 4A in IC 2EA.

The output of 2EA goes to 2DB. When output pin 2D6 is high, flip-flop 4EB's CLEAR is deactivated at the start of the last cycle of the 1 second period, allowing its output to change state on the next clock transition. Output 4E7 is high at this point. At the next clock transition which comes half-way through the last cycle, the F/F switches state, causing pin 4E7 to go low (output Q^*) which LOADs 4A through 2E6 which acts as a negative logic OR. (The other input, 2E4, is for the general CLEAR signal). At that point MAX/MIN from 4A goes low again, thus putting a low on pin 5 of OR gate 2DB. However, the F/F 4EB is not cleared, since the clock fed into 2DB is high and does not go low to clear 4EB until the end of the clock cycle.

The 74LS190 could not be used in place of the 74LS160's because of the

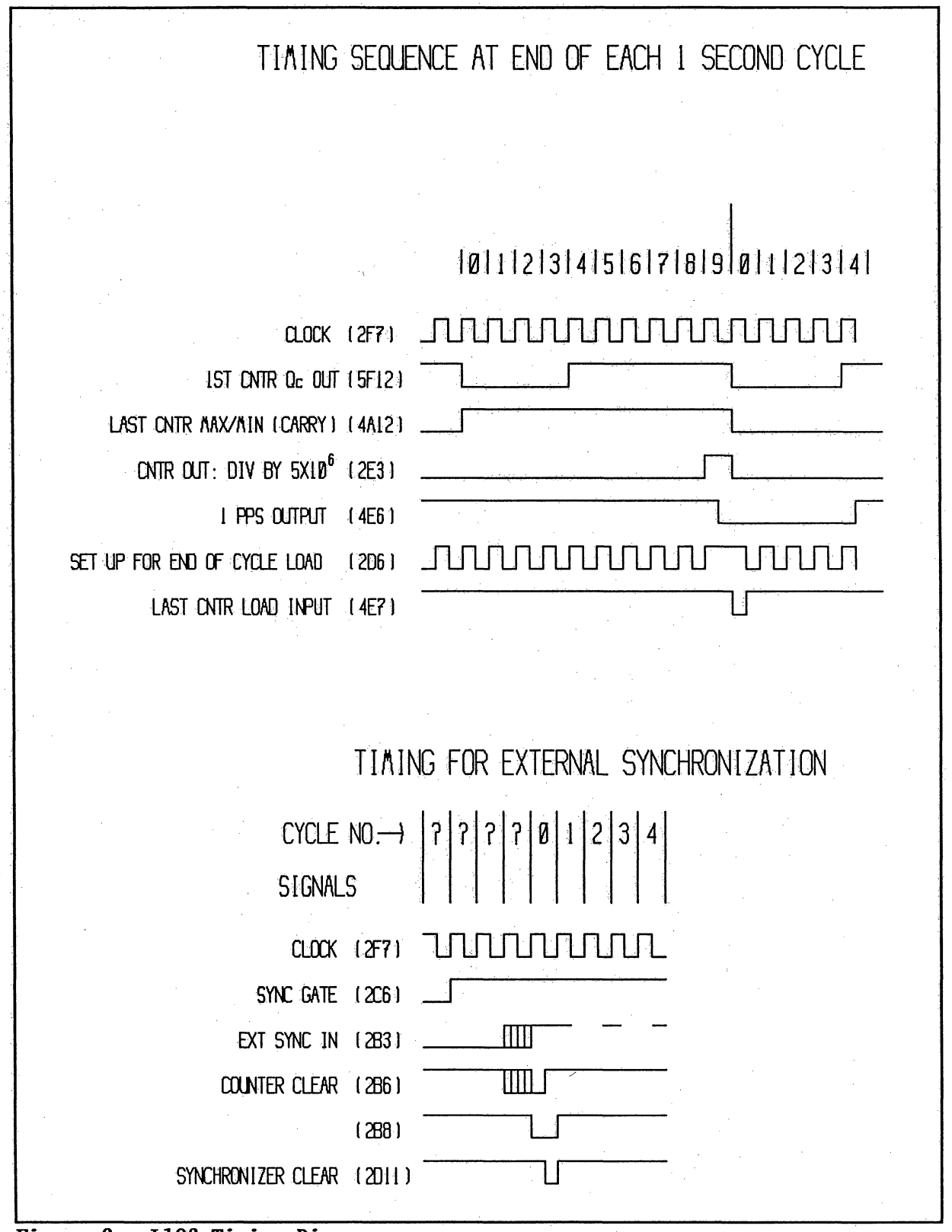


Figure 2. L108 Timing Diagram.

necessity for a longer RCO to properly trigger flip-flop 4EB. On the other hand, the 74LS160 can not be used in place of the 74LS190 at 4A because the LOAD action of the 74LS160 is synchronous with the clock. It is required to be able to load the final stage of the counter with '5' at the same time that the other stages are cleared (CLEAR is asynchronous on the 74LS160.) The clear signal for the first six stages and load for the seventh (through 2EB which acts as an OR for the active low LOAD signal) is derived from the synchronizing circuitry of IC's 2B and 2DD.

The output of IC 2EA not only LOADs the counter 4A, but also goes to the output synchronizing flop-flop, 4EA. This is a fast Schottky type F/F used to synchronize the output of the counter chain to the clock, ensuring that the counter delay is not included in the delay between the output and the clock. Referring to the timing diagram, the once per second, one cycle long divider output from IC 2EA is applied to the J input of the J-K flip-flop. The K input comes from the C output of the first counter in the chain, and is low at the time that the J signal goes high. The counters count on the low to high transition of the 5 MHz clock, so the J input from 2EA goes high at the beginning of the 4,999,999th clock cycle. Since the 74S112 clocks on the high to low transition of the clock (applied at pin 4E1) the flip-flop clocks 1 half cycle later, and the outputs go active: this is the beginning of the 1 PPS output pulse. The next clock occurs after the J input from the divider chain goes low again, but the outputs of the F/F remain the same since the K input is still low (see the data sheet on the '112). The C output of 5F goes high 1 μsec later as it counts up. This causes the outputs of 4EA to go inactive 1/2 cycle later, resulting in a pulse 1 μsec long. Hence it can be seen that the 1 PPS signal is synchronized with the 5 MHz clock with only the

delay of the comparator 2F and the flip-flop 4E5 (about 15 nsec) between them, without the counter delay.

Further, due to the approximately 1/2 cycle delay, it is possible to synchronize the 1 PPS to the external 1 PPS with an error of ± 250 nsec rather than +500/-0. As seen on the timing diagram, this would be necessary due to the extra 1/2 cycle added to the CLEAR pulse which is required to keep the pulse from being too short. The CLEAR is reset in the middle of what becomes the 0th count of the chain, that is the counter counts to '1' 1/2 cycle later. Since the 1 PPS output goes active in the middle of the 4,999,999th count, the average 1 cycle delay in the CLEAR is accommodated. These outputs (Q and Q^*) go to the driver circuitry to produce the final 1 PPS outputs.

The 1 PPS signal derived by the circuitry described above is synchronized to an outside 1 PPS signal by IC's 2B and 2DD. The external 1 PPS is brought in by IC 4FA which acts as a differential receiver. The high impedance '+' and '-' inputs are tied low and high respectively. Thus if the '+' input gets a positive transition or the '-' gets a negative transition that causes the '+' to be at a higher voltage than the '-', pin 4F3 goes high. This allows an external signal of either polarity to be used.

The outside 1 PPS signal triggers the monostable, IC 1EA. This non-retriggerable monostable allows only one transition to pass through, thus serving to filter low-quality 'ringing' signals observed from some GPS receivers.

The output from the monostable clocks the D flip-flop 2BA. Normally the D input 2B2 is low so the clock signal just transfers a low to the output. The D input comes from a front panel switch which is normally open. When it is depressed, it grounds the input of 2CC, whose output goes high so the D input

2B2 goes high. As seen on the timing diagram, the next transition of the external 1 PPS clock transfers the high to pin 2B5. Pin 2B6 is an inverted version which goes low, clearing the counters connected to it. The second D flip-flop, 2BB is used to reset the CLEAR produced by 2BA. The high output of 2BA goes to the D input of 2BB which is clocked in by the next low to high transition of the 5 MHz MASER clock signal. This results in the Q^* output 2B8 going low. However, the output of the OR gate 2DD does not go low until the 5 MHz clock goes low again. Then 2BA and 2BB are cleared, and the counter CLEAR signal is reset back high (inactive) again. This results in a CLEAR signal that lasts from the time the external 1 PPS transitions until the next high to low transition of the 5 MHz MASER clock that is at least 1/2 cycle later.

Flip-flop 3AA works similarly to the resynchronizer, 4EA. The high to low 1 PPS transition of pin 4E6 sets F/F 3AA. This preset signal goes inactive after 1 μsec. The next high to low transition of the clock at 3A3 clocks the D input of 3AA to the outputs. Since the D input is tied low, this just clears 3AA. The clock is derived from the ANDed outputs of counter 5B, and goes high 10 msec after the 1 PPS signal. The result is a 10 millisecond pulse whose start is delayed from the start of the 1 μsec pulse by the gate delay of 3AA. Since this is just used to synchronize the VLBA station computer to the MASER, this delay is not critical.

The 80 Hz noise calibrator switching signal is produced by the counter chain 4B, 4C, 4D. This signal is synchronized to the 1 PPS by the flip-flops in IC 2A, similar to the use of IC 2B. The input to the chain is through one of the output drivers IC 1C5 and the receiver 4F5. This is to keep the circuit delays close to the delays in the same circuit which is part of the baseband converter. For the same reason the counter chain is not resynchronized,

despite the delay created by the ripple counters in the 74LS390.

The IC's 1A, 1B, 1C and 1D are 50 ohm TTL level single ended transmission line drivers to drive the output signals. Note that the outputs consist of 5 positive 1 PPS signals 1 μsec long, 3 negative 1 PPS signals 1 μsec long, 1 negative 1 PPS signal 10 msec long and four 80 Hz signals.

Related Documents

1. Timekeeping at the VLBA Stations, VLBA Memo 504, Larry R. D'Addario, September, 1985.

2. VLBA Station Timekeeping, an Alternative, VLBA Memo 510, B. G. Clark, November 1985.

3. Station Timing System, VLBA Electronics Memo 70, A. R. Thompson, May, 1986.

III. Test Procedure.

REQUIREMENTS:

1. Storage oscilloscope. Storage capability is required to measure the length of the 1 microsecond pulse which is has a repetition rate of once per second. Either a digital or storage tube type can be used.

2. Function generator, capable of producing TTL-level square or pulse waveforms.

The module is checked most easily in the C-rack. However, it can be checked on the bench by connecting the appropriate power supplies, and injecting a 5 MHz signal.

I. Check that a positive TTL-level pulse appears at the front panel output (1 PPS). The pulse should be 1 microsecond long, an should appear at a rate of once per second.

II. Check that an 80 Hz signal appears at the 80 Hz jack on the front panel.

III. Check the synchronization circuit. Set scope to:
50 ms/div
5 volt/div, channels 1 and 2
"NORM" trigger (not "AUTO")
Trigger voltage about +2 Volt
Trigger on channel 1
Display channel 2 only

Set the function generator to positive pulse (or square) waveform just slightly less than 1 pulse per second (1 Hz). The level should be TTL (0.2 Volt low, 4.0 Volt high). Connect the 1 PPS front panel output to channel 1 on the scope. Using a BNC T-connector, connect the function generator output to both the **EXT. SYNC + front panel connector** and **channel 2** of the scope.

The channel 2 trace showing the function generator pulses should appear, and be updated once per second, triggered by the 1 μsec pulses from the module. The pulses should drift slowly across the screen. Adjust the frequency on the function generator so that the pulses drift to the right at about 1 division per second.

Press the reset button with a pen or something. The **POSITIVE** transition of the pulse should be frozen at about 1 division from the left edge of the screen. It should stay until the reset is released, whereupon it should resume its rightward movement.

Set the function generator to negative pulses, and switch the BNC plug from the EXT. SYNC + to the EXT. SYNC - connector on the front panel. Then repeat as above, except that the **NEGATIVE** transition should be frozen 1 division to the right of the left edge of the screen. Otherwise, the behavior should be the same.

IV. Finally, check the lower panel BNC connector outputs in the C-rack. Use the scope to verify these outputs:

1 PPS outputs 1 - 4: 1 μsec POSITIVE pulse.
1 PPS outputs 5 - 7: 1 μsec NEGATIVE pulse.
1 PPS output 8: 10 msec NEGATIVE pulse.

80 Hz outputs 1 - 3: 80 Hz square wave, 50 % duty cycle.

5 MHz outputs 1 - 8: 5 MHz sine wave.

FRONT PANEL CONNECTIONS AND ADJUSTMENTS

1. RESET (Button). This button is covered by a screw-on cap. To push it, unscrew and remove the cap, and push the button with any pointed object, such as a pencil. This should only be done when major system timing resynchronization is requested.

2. EXT. SYNC + (BNC Connector INPUT). This is the input for the external positive-edge 1 Pulse Per Second input. Pressing the RESET button synchronizes the system 1 PPS clock to this input.

3. EXT. SYNC - (BNC Connector INPUT). Same as number 2 above, except it responds to negative-edge pulses.

4. 1 PPS (BNC Connector OUTPUT). Sample of the 1 Pulse Per Second signal generated by the L108 module. The pulses are

Specifications

Primary clock input from MASER:	
Frequency	5 MHz
wave form	sine wave
level	0.1 to 2.0 V RMS (-7 to +20 dBm)
input impedance	50 Ω
External sync clock input:	
frequency	1 Hz
signal type	TTL, any duty cycle
polarity	positive or negative depending on which front panel input is used

REAR PANEL OUTPUTS:

Station timing outputs:	
frequency	1 Hz
SIGNAL 1 type (No. outputs):	1 μs positive pulse (4)
SIGNAL 2 type (No. outputs):	1 μs negative pulse (3)
SIGNAL 3 type (No. outputs):	10 ms negative pulse (1)
signal levels:	TTL level driver for 50 Ω cable
Calibrator diode outputs:	
frequency	80 Hz
signal wave-form	square wave, 50 % duty cycle
signal type/level	TTL level driver for 50 Ω cable
number of outputs	4

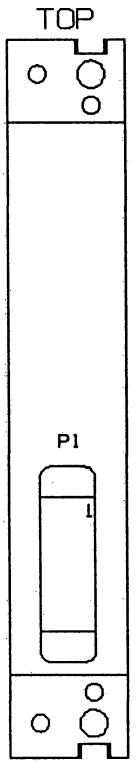
FRONT PANEL OUTPUTS:

Station timing output:	1 μs negative pulse (Signal 1)
Calibrator diode output:	Same as above

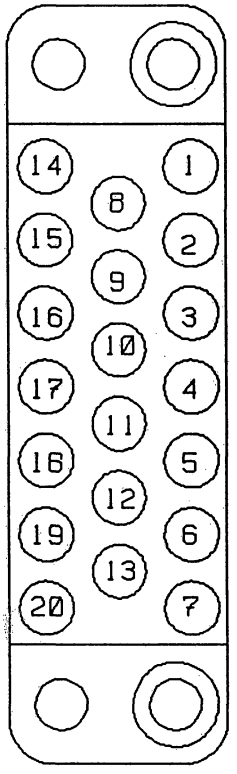
Power supply requirements +5, ±15 volts

Drawing List

Description	Number
Assembly Drawing	D53311A001
Wire-wrap Board Layout Drawing	A53311A002
Bill of Materials	A53311B001
Front Panel Silkscreen Artwork	B53311I001
Schematic Diagram	D53311S001
Wiring Harness List	A53311W001
Wire List	A53311W002



MODULE
(REAR VIEW)



P1 (REAR VIEW)

P1					
PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1	GROUND		11	1 PPS OUT 6	TTL (50 ohm)
2	+ 5V SUPPLY	400 mA	12	1 PPS OUT 7	" "
3	5 MHz IN	0.05 to 5 V PK	13	1 PPS OUT 8	" "
4			14	-15 V SUPPLY	40 mA
5	1 PPS OUT 1	TTL (50 ohm)	15	+15 V SUPPLY	10 mA
6	1 PPS OUT 2	" "	16	1 PPS OUT 10	TTL (50 ohm)
7	1 PPS OUT 3	" "	17	80 HZ OUT 1	" "
8			18	80 HZ OUT 2	" "
9	1 PPS OUT 4	" "	19	80 HZ OUT 3	" "
10	1 PPS OUT 5	" "	20		

Description of Rear Panel I/O Lines

20-PIN REAR PANEL CONNECTOR:

GROUND:	Module ground for signals and return for power supplies.
+5 VOLT SUPPLY:	+5 V input from power supply.
5 MHz IN:	Input from MASER.
EXT SYNC +:	Rear panel sync input, for + edge sync.
1 PPS OUT 1:	10 millisecond, negative pulse, 1 Hz.
1 PPS OUT 2-4:	1 microsecond, negative pulse, 1 Hz.
1 PPS OUT 5-8:	1 microsecond, positive pulse, 1 Hz.
+15 VOLT SUPPLY:	+15 V input from power supply.
-15 VOLT SUPPLY:	-15 V input from power supply.
1 PPS OUT 10:	1 microsecond, negative pulse, 1 Hz.
80 HZ OUT 1-3:	Noise calibrator diode modulation signal.

STATION TIME L108 MODULE INTERNAL WIRING HARNESS 12-14-87

DRAWING:A5311W002 WILLIAM WIREMAN FILE:B:L108HARN

NOTE: (L) INDICATES THE SIGNAL IS LOW TRUE, EX. HI-LO(L) LO=LOW SIGNAL

PART I-WIREWRAP CONNECTOR WIRING

PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1.	GND	REF GND	BLK	22	2.	5V	J1-2	ORG	22
3.	GND				4.	5V			
5.	1PPS OUT1	J1-5	CO-AX	RG-188	6.	1PPS RET1	J1-5	SHIELD	
7.	1PPS OUT2	J1-6	CO-AX	RG-188	8.	1PPS RET2	J1-6	SHIELD	
9.	1PPS OUT3	J1-7	CO-AX	RG-188	10.	1PPS RET3	J1-7	SHIELD	
11.	1PPS OUT4	J1-9	CO-AX	RG-188	12.	1PPS RET4	J1-9	SHIELD	
13.	1PPS OUT5	J1-10	CO-AX	RG-188	14.	1PPS RET5	J1-10	SHIELD	
15.	1PPS OUT6	J1-11	CO-AX	RG-188	16.	1PPS RET6	J1-11	SHIELD	
17.	1PPS OUT7	J1-12	CO-AX	RG-188	18.	1PPS RET7	J1-12	SHIELD	
19.	1PPS OUT8	J1-13	CO-AX	RG-188	20.	1PPS RET8	J1-13	SHIELD	
21.	1PPS OUT9	FP-BNC3	CO-AX	RG-188	22.	1PPS RET9	FP-BNC3	SHIELD	
23.					24.				
25.					26.				
27.	GND	REF GND	BLK	22	28.				
29.					30.				
31.					32.				
33.					34.				
35.					36.				
37.					38.				
39.					40.				
41.					42.				
43.					44.				
45.					46.				
47.					48.				
49.	GND	FP-SWT-NO	BLK	26	50.				
51.	SYNCSWT(L)	FP-SWT-C	WHT/BLK	26	52.				
53.					54.				
55.					56.				
57.					58.				
59.					60.				
61.					62.				
63.					64.				
65.					66.				
67.					68.				
69.					70.				
71.	5MHZ	J1-3	CO-AX	RG-188	72.	5MHZ RET	J1-3	SHIELD	
73.	GND	REF GND	BLK	22	74.				
75.	80HZ OUT1	J1-17	CO-AX	RG-188	76.	80HZ RET1	J1-17	SHIELD	

INTERNAL WIRING HARNESS (cont.)

77.	80HZ OUT2	J1-18	CO-AX	RG-188	78.	80HZ RET2	J1-18	SHIELD	
79.	80HZ OUT3	J1-19	CO-AX	RG-188	80.	80HZ RET3	J1-19	SHIELD	
81.	80HZ OUT4	FP-BNC4	CO-AX	RG-188	82.	80HZ RET4	FP-BNC4	SHIELD	
83.					84.				
85.					86.				
87.	1PPS OUT10	J1-16	CO-AX	RG-188	88.	1PPS RET10	J1-16	SHIELD	
89.	EXT.SYNC+	FP-BNC1	CO-AX	RG-188	90.	EXT.SYNC-	FP-BNC1	CO-AX	RG-188
	EXT.SYNC+ RET TIE SHIELD TO REF GND					EXT.SYNC- RET TIE SHIELD TO REF GND			
91.					92.				
93.					94.				
95.	15V	J1-15	RED	22	96.	-15V	J1-14	YEL	22
97.	GND				98.	5V			
99.	GND	REF GND	BLK	22	100.	5V	J1-2	ORG	22

NOTE: BYPASS 15V AND -15V TO REF GND WITH 6.8 ufd. @75V TANTALUM CAPACITORS
REF GND- FORMED USING A 18 ga. WIRE SOLDERED TO GROUND LUG MOUNTED AT EACH END OF WIREWRAP CONNECTOR MOUNTING BLOCKS

PART II-REAR PANEL CONNECTOR WIRING - JACK 1 (AMP 20 PIN)

PIN	FUNCTION	SOURCE	COLOR	GA	PIN	FUNCTION	SOURCE	COLOR	GA
1.	GND	REF GND	BLK(X2)	22	2.	5V	WW-2,100	ORG(X2)	22
3.	5MHZ	W-71	CO-AX	RG-188	4.				
	5MHZ RET	W-72	SHIELD						
5.	1PPS OUT1	W-5	CO-AX	RG-188	6.	1PPS OUT2	W-7	CO-AX	RG-188
	1PPS RET1	W-6	SHIELD			1PPS RET2	W-8	SHIELD	
7.	1PPS OUT3	W-9	CO-AX	RG-188	8.				
	1PPS RET3	W-10	SHIELD						
9.	1PPS OUT4	W-11	CO-AX	RG-188	10.	1PPS OUT5	W-13	CO-AX	RG-188
	1PPS RET4	W-12	SHIELD			1PPS RET5	W-14	SHIELD	
11.	1PPS OUT6	W-15	CO-AX	RG-188	12.	1PPS OUT7	W-17	CO-AX	RG-188
	1PPS RET6	W-16	SHIELD			1PPS RET7	W-18	SHIELD	
13.	1PPS OUT8	W-19	CO-AX	RG-188	14.	-15V	W-96	YEL	22
	1PPS RET8	W-20	SHIELD						
15.	15V	W-95	RED	22	16.	1PPS OUT10	W-87	CO-AX	RG-188
						1PPS RET10	W-88	SHIELD	
17.	80HZ OUT1	W-75	CO-AX	RG-188	18.	80HZ OUT2	W-77	CO-AX	RG-188
	80HZ RET1	W-76	SHIELD			80HZ RET2	W-78	SHIELD	
19.	80HZ OUT3	W-79	CO-AX	RG-188	20.				
	80HZ RET3	W-80	SHIELD						

PART III-FRONT PANEL BNC TEST POINTS & SYNC. SWT.

CONNECTOR	FUNCTION	SOURCE	COLOR	GA	RET SOURCE	COLOR	
BNC-1	EXT.SYNC+	W-89	CO-AX	RG-188	REF GND	SHIELD	TOP
BNC-2	EXT.SYNC-	W-90	CO-AX	RG-188	REF GND	SHIELD	
BNC-3	1PPS OUT9	W-21	CO-AX	RG-188	W-22	SHIELD	
BNC-4	80HZ OUT4	W-81	CO-AX	RG-188	W-82	SHIELD	BOTTOM
RESET SWITCH							
FP-SWT-C	SYNC SWT	W-51	WHT/BLK	26			
FP-SWT-NO	GND	W-49	BLK	26			
FP-SWT-NC		N.C.					

NATIONAL RADIO ASTRONOMY OBSERVATORY

Title: STATION TIMER SCHEMATIC - L108 MODULE

Size: D | Document Number: 0533118001 | REV: D

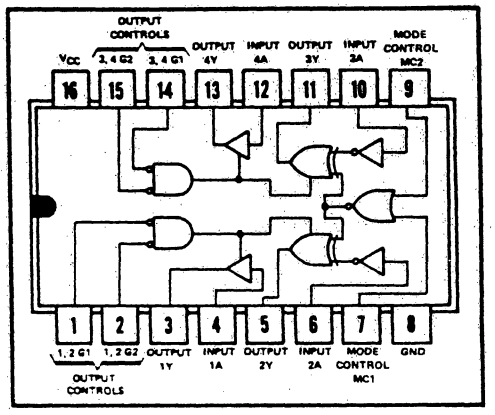
Date: March 8, 19[illegible] | Sheet 1 of 1

TYPES DS7831, DS7832, DS8831, DS8832 LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7712496, JANUARY 1977

- TTL Compatible
- Propagation Delay Time . . . 15 ns Typ
- Very Low Output Impedance with High Drive Capability
- 40-mA Sink and Source Capability
- Gating Control to Allow Either Single-Ended or Differential Operation
- Three-State Outputs for Party-Line (Data-Bus) Operation

DS7831, DS7832.....J PACKAGE
DS8831, DS8832.....J OR N PACKAGE
(TOP VIEW)



description

The DS7831, DS7832, DS8831, and DS8832 can be used as either quadruple single-ended line drivers or as dual differential line drivers. This multi-mode operation and simple logic control make these devices especially useful for party-line or bus-organized systems. The DS7831 and DS8831 have output clamp diodes to V_{CC}; the DS7832 and DS8832 do not.

For one of these circuits to operate as four independent single-ended line drivers, both mode-control pins must be low. In this mode, no signal inversion takes place between inputs and outputs. To operate as a dual differential line driver, at least one of the mode control inputs must be high. Inputs 1A and 2A should be connected together as should 3A and 4A. Then signals applied to the inputs will appear noninverted at 1Y and 4Y and inverted at 2Y and 3Y, provided the output control pins are low.

While enabled, these outputs provide good drive capability for capacitive loads, and fast transitions from both low-to-high levels and high-to-low levels.

Taking either of the associated output controls high disables the outputs. When disabled, these three-state outputs neither load nor drive a line and hundreds of these devices may be connected to a common bus line. Only one output should be enabled at a time.

The DS7831 and DS7832 are characterized for operation over the full military temperature range of −55°C to 125°C. The DS8831 and DS8832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OUTPUT CONTROLS		MODE CONTROLS		DATA INPUT	OUTPUT	DATA INPUT	OUTPUT
G1	G2	MC1	MC2	1A/4A	1Y/4Y	2A/3A	2Y/3Y
L	L	L	L	H	H	H	H
L	L	L	L	L	L	L	L
L	L	X	H	H	H	H	L
L	L	H	X	L	L	L	H
H	X	X	X	X	Z	X	Z
X	H	X	X	X	Z	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

TYPES DS7831, DS7832, DS8831, DS8832
LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range: DS78' . . . . . −55°C to 125°C
DS88' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, DS7831 and DS7832 chips are alloy-mounted; DS8831 and DS8832 chips are glass-mounted.

recommended operating conditions

	DS78'			DS88'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_O			5.5			5.5	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature range, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −2 mA	DS7831,DS7832	2.4	3.1		V
			I_{OH} = −5.2 mA	DS8831,DS8832	2.4	3.0		
			I_{OH} = −40 mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		I_{OL} = 32 mA		0.26	0.4	V
				I_{OL} = 40 mA		0.3	0.5	
V_{OK}	Output clamp voltage	V_{CC} = 5 V, T_A = 25°C	I_O = −12 mA				−1.5	V
			I_O = 12 mA	DS7831,DS8831			V_{CC} + 1.5	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, T_A = 25°C		V_O = 2.4 V			40	μA
				V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,		T_A = MAX	−40	−70	−120	mA
I_{CC}	Supply current	V_{CC} = MAX				50	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V.
§ Only one output should be shorted at a time.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

National Semiconductor

Voltage Comparators

LM160/LM260/LM360 High Speed Differential Comparator

General Description

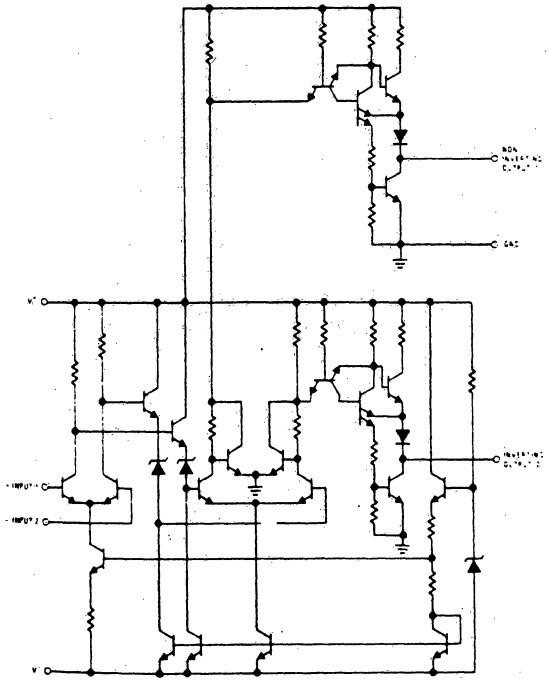
The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 500 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disc file systems.

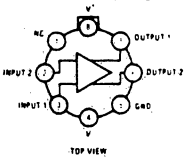
Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Schematic and Connection Diagrams

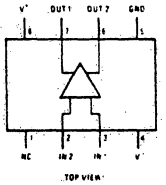


Metal Can Package



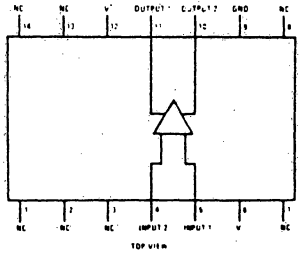
Order Number LM160H, LM260H or LM360H
See NS Package H08C

Dual-In-Line Package



Order Number LM360N
See NS Package N08B

Dual-In-Line Package



Order Number LM360N-14
See NS Package N14A

Order Number LM160J-14, LM260J-14
See NS Package J14A

Absolute Maximum Ratings

Positive Supply Voltage	+8V	Operating Temperature Range	
Negative Supply Voltage	−8V	LM160	−55°C to +125°C
Peak Output Current	20 mA	LM260	−25°C to +85°C
Differential Input Voltage	±5V	LM360	0°C to +70°C
Input Voltage	$V^+ \geq V_{IN} \geq V^-$	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm5V$ (Note 1)		13	25	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 2)		12	20	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 3)		14		ns
Response Time Difference Between Outputs					
$(t_{pd}$ of $+V_{IN1}) - (t_{pd}$ of $-V_{IN2})$	$T_A = 25°C$, (Note 1)		2		ns
$(t_{pd}$ of $+V_{IN2}) - (t_{pd}$ of $-V_{IN1})$	$T_A = 25°C$, (Note 1)		2		ns
$(t_{pd}$ of $+V_{IN1}) - (t_{pd}$ of $+V_{IN2})$	$T_A = 25°C$, (Note 1)		2		ns
$(t_{pd}$ of $-V_{IN1}) - (t_{pd}$ of $-V_{IN2})$	$T_A = 25°C$, (Note 1)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\mu A$, $V_S = \pm4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		.25	.4	V
Positive Supply Current	$V_S = \pm6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm6.5V$		−9	−16	mA

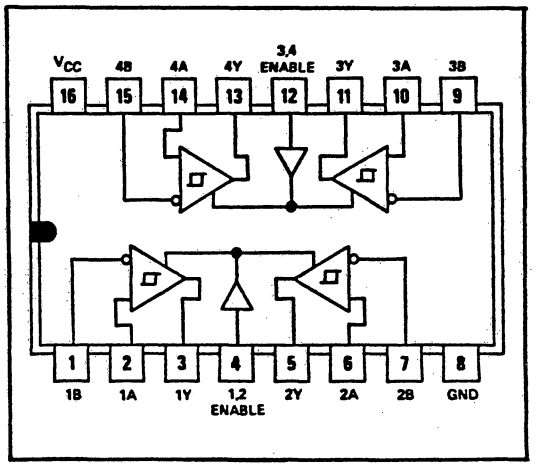
Note 1: Response time measured from the 50% point of a 30 mV_{p-p} 10 MHz sinusoidal input to the 50% point of the output.
Note 2: Response time measured from the 50% point of a 2 V_{p-p} 10 MHz sinusoidal input to the 50% point of the output.
Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPE SN75175
QUADRUPLE DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12772, OCTOBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for MC3486

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

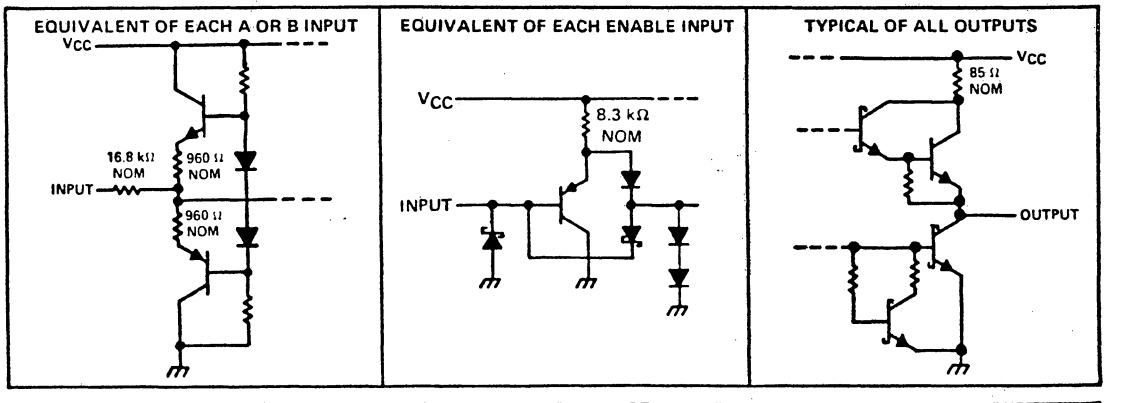
The SN75175 is a monolithic quadrupled differential line receiver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422A and RS-423A and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each receiver features two active-high enables, each common to two receivers. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, A or B inputs	±25 V
Differential input voltage (see Note 2)	±25 V
Enable input voltage	7 V
Low-level output current	50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package	1025 mW
N Package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package	260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at a rate of 8.2 mW/°C and the N package to 736 mW at 70°C at a rate of 9.2 mW/°C. In the J package, SN75175 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 16 mA		−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 4: Refer to EIA standards RS-422A and RS-423A for exact conditions

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level				25	35	ns

PARAMETER MEASUREMENT INFORMATION

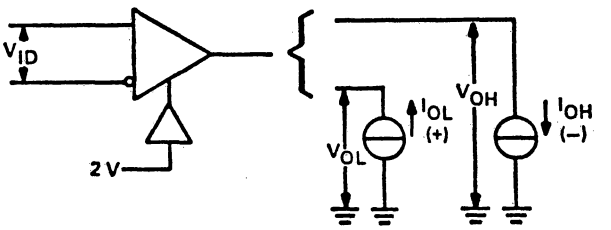


FIGURE 1–V_{OH}, V_{OL}

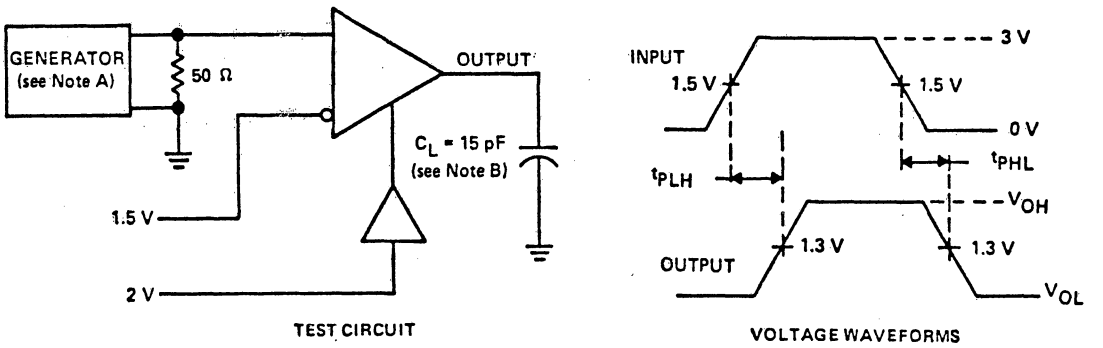


FIGURE 2–PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, t_r = t_f = 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and stray capacitance.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265