VLBA Technical Report No. 22

FRONT-END CONTROL MODULE
Module Type F117

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1.0 INTRODUCTION

This manual describes the VLBA F117, Front-End Control Interface module that is used to control and monitor Single-Band, Front-Ends on the VLBA antennas. The emphasis of this manual is on the F117 theory of operation (Section 2) and maintenance (Section 3). Construction details are not included but all drawings used in F117 fabrication are listed in the BOM (Bill of Materials) drawing. Section 4 contains the drawings and Section 5 contains data sheets for the special-purpose components used in F117. Section 6 (the Appendix) lists NRAO reports that describe Single-Band, Front-Ends, the Standard Interface Board and related equipment. The appendix also has a listing of the AOC F117 test program used to bench-test and align the F117.

This manual is an upgrade of an earlier F117 manual and describes the module in more detail. All the tables, drawings, figures, wire list, etc. contained in the first manual have been retained. Additional manual features are a brief description of the VLBA Monitor and Control Bus (MCB), a brief description of the Standard Interface Board (SIB) and the interactions of the Standard Interface Board with the Front-End interface circuitry contained on the Wire-Wrap board. The operation of the Wire-Wrap board circuitry is more fully described.

The manual contains several additional drawings. These include the schematic diagram of the Standard Interface Board, the F117 Assembly Drawing, a module wiring schematic diagram, and a more detailed drawing of the Wire-Wrap board circuitry.

A detailed description of the AOC bench tests and test fixture used to align and trouble-shoot the F117 have been included. The AOC bench tests are performed by a test program in an IBM-compatible PC and have been implemented in Microsoft Basic. The F117 test operations performed by the program are described but the details of the program operation are not described. The program is included in the Appendix for readers interested in the program operation.

A brief description of the Single-Band Front-End is included to provide a functional perspective to the the F117 circuitry. The description includes Front-End control logic, command and digital monitor data formats, analog signals and their normal range, and a description of the Front-End supportive environment.

F117 Physical Description

At this point, the reader should refer to drawing D53510A001 (in Section 4) which depicts the F117 Assembly. Figure 1 (next page) is a photograph of the F117 with one side plate removed. The F117 is a 1-wide, RFI-type VLBA module with one 42-pin AMP rear panel connector (P1) that mates with the 42-socket AMP bin connector. Module and Front-End DC power, the Monitor and Control Bus, and the 80 Hz calibration switching signal (MOD) are routed through this connector. Figure 2 (following Figure 1) shows the F117 rear panel and pin-signal assignments. The P1 signals are described below.

Two front-panel DB25 connectors (J1 - control and J2 - monitor) interface the F117 to the associated Front-End's corresponding DB25 connectors via two shielded, 25-conductor cables. These connectors carry Front-End DC power, control and monitor signals and three digital status code values from the Front-End that indicate the Front-End's **Band Code, Modification Code** and **Serial Number.** The usage of these status codes is described below. J1 (control) is a pin connector and J2 (monitor) is a socket connector. Figure 3 (following Figure 2) shows the front panel and the connector's pin-signal assignments.

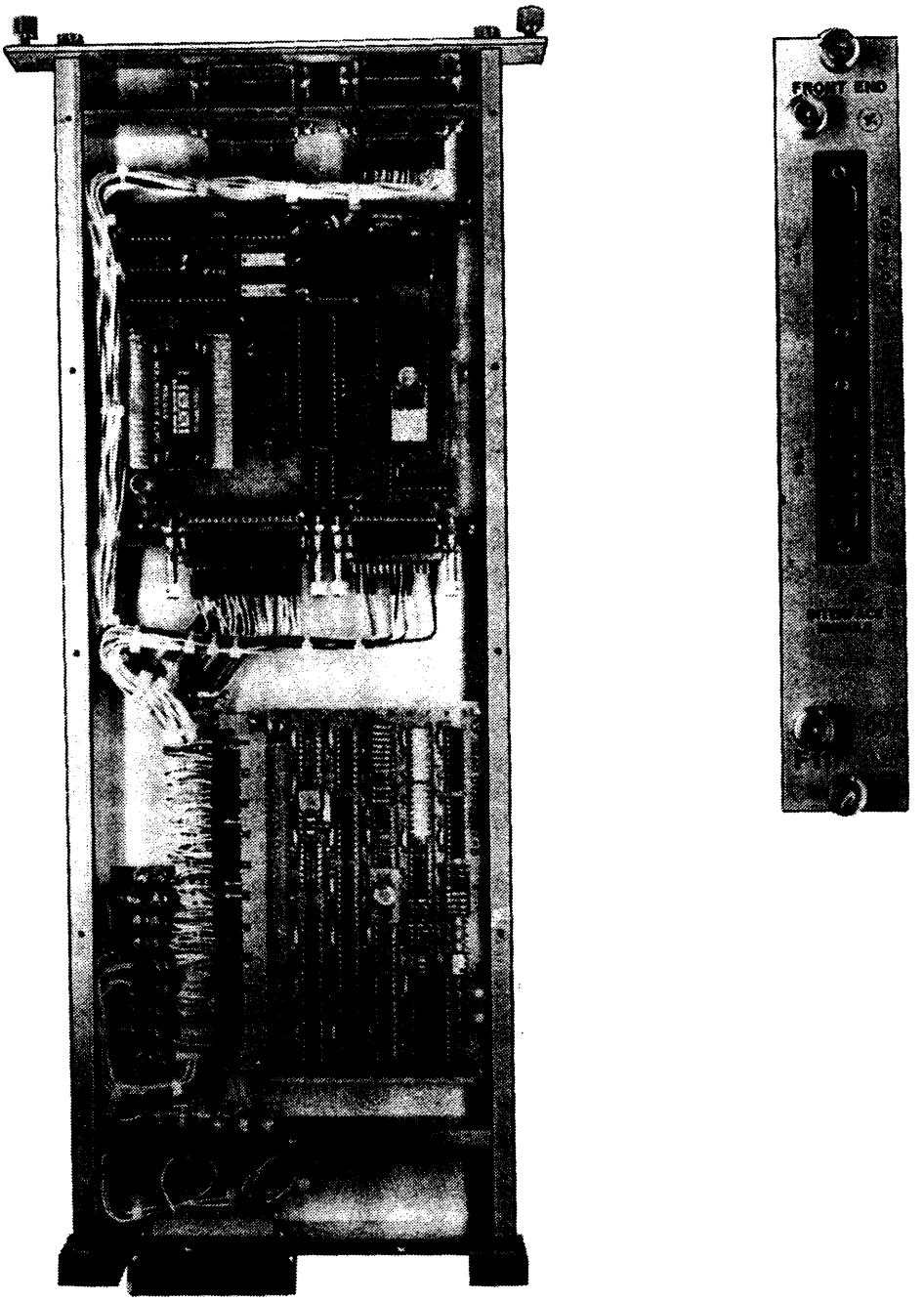
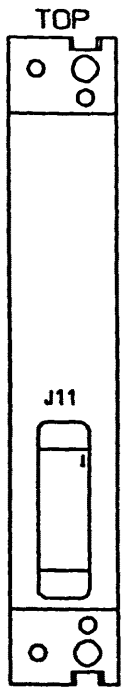
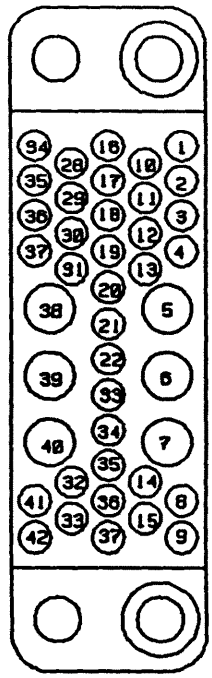


FIGURE 1, F117 WITH
SIDE PLATE REMOVED

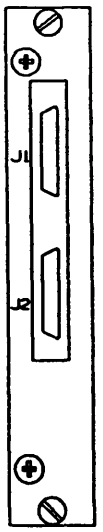


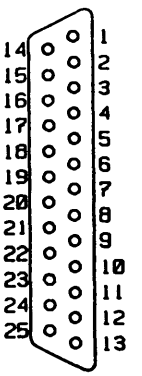


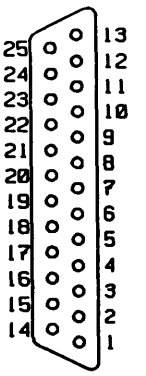
J11, MODULE I/O

PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1			22		
2			23		
3			24		
4			25		
5			26		
6			27		
7			28		
8	XMT+ TRANSMIT BUS		29	+28 V SUPPLY,	100 mA MAX
9	XMT- TRANSMIT BUS		30		
10	+5 VOLT SUPPLY		31		
11			32		
12	MOD, MODULATION INPUT		33		
13			34	DC COMMON	
14	RCV+ RECEIVE BUS		35	RST+ RESET BUS	
15	RCV- RECEIVE BUS		36	RST- RESET BUS	
16	+15 V SUPPLY,	45 mA	37		
17	-15 V SUPPLY,	40 mA	38		
18			39		
19			40		
20			41		
21			42		

FIGURE 2, F117 REAR PANEL AND J11 PINOUT







J1 (FRONT VIEW) J2 (FRONT VIEW)

PLUG SOCKET

J1, FRONT END MONITOR

PIN	FUNCTION	PIN	FUNCTION
1	VP - PUMP VACUUM	14	SENS - SENSITIVE VACUUM MONITOR
2	VD - DEWAR VACUUM	15	ANLG3 - (EXTERNAL ANALOG +)
3	15K - 15 K STAGE TEMP SENSOR	16	ANLG3 - (EXTERNAL ANALOG -)
4	50K - 50 K STAGE TEMP SENSOR	17	ADDR0 - (FOR ANLG3)
5	300K - 300 K STAGE TEMP SENSOR	18	ADDR1 - (FOR ANLG3)
6	ACI - AC CURRENT MONITOR	19	ADDR3 - (FOR ANLG3)
7	RF#1 - RIGHT FET #1 BIAS	20	S - SOLENOID VALVE MONITOR
8	RF#2 - RIGHT FET # 2 BIAS	21	P - VACUUM PUMP MONITOR
9	LF#1 - LEFT FET #1 BIAS	22	M(L) - FE CONTROL SW POS MONITOR
10	LF#2 - LEFT FET #2 BIAS	23	X MONITOR
11	LED - LED VOLTAGE	24	C MONITOR
12		25	H(L) MONITOR
13	Q GROUND		

J2, FRONT END CONTROL

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	14	F0 - BAND ID CODE, BIT 0
2	+ 15 VOLT POWER	15	F1 - " " " , BIT 1
3	- 15 VOLT POWER	16	F2 - " " " , BIT 2
4		17	F3 - " " " , BIT 3
5		18	S0 - FE S/N, BIT 0
6	X COMMAND	19	S1 - " " , BIT 1
7	C COMMAND	20	S2 - " " , BIT 2
8	H(L) COMMAND	21	S3 - " " , BIT 3
9	PA(L)	22	S4 - " " , BIT 5
10		23	S5 - " " , BIT 6
11	LO-CAL DRIVE	24	M0 - MOD LEVEL, BIT 0
12	HI-CAL DRIVE	25	M1 - " " , BIT 1
13	GROUND		

FIGURE 3, F117 FRONT PANEL AND J1, J2 PINOUTS

The F117 circuitry is contained on two removable circuit boards: the VLBA Standard Interface Board and a Wire-Wrap circuit board which interfaces the Front-End circuitry to the Standard Interface Board.

Since eight F117's are currently installed in the antenna vertex room and there is a microcontroller clock oscillator (11.0592 MHz) and digital logic in the F117, the circuitry is contained in an RFI enclosure. Signals and power to the enclosure are fed through feed-through terminals with an integral by-pass filter capacitor. The front panel Front-End interface connectors (J1 and J2) are D-series connectors with integral by-pass filter capacitors on the contacts. RFI gaskets are installed on J1 and J2 to further inhibit RF feedthrough.

F117 Functional Description

Many devices at the VLBA Station are controlled by the VLBA Standard Interface Board (or a functional equivalent) that interfaces devices to the station computer via the VLBA Monitor and Control Bus (MCB). Each controlled or monitored device is tapped onto the bus. The VLBA Standard Interface Board interfaces the MCB signals to the device circuitry. The MCB carries time-serial, digital messages on two multi-drop party-lines consisting of the XMT (Transmit) line and the RCV (Receive) line.

The Standard Interface Board (SIB) in each device analyzes the message stream on the XMT line and if addressed, it executes the designated action. This will be a command to the device or it may evoke data from the device which is serially routed back to the station computer via the RCV line. Section 2.1 briefly describes the Monitor and Control Bus. Section 2.2 briefly describes the Standard Interface Board.

Like many other VLBA Station devices, the F117 contains a Standard Interface Board (version "D") which controls Front-End interface circuitry installed on a Wire-Wrap Board. The interface circuitry consists of logic to interact with the Standard Interface board, command and digital monitor data registers, an analog multiplexer to sample Front-End analog signals, and calibration control and drive circuitry. Section 2.3 describes the operation of the Wire-Wrap board circuitry.

At this point, it is important to review drawing D53510W010 which depicts the F117 internal wiring. This drawing emphasises the signal interconections between the two circuit boards and the Front-End interface connectors J1 and J2.

The Standard Interface Board provides 8 address code bits for address enables, a 16-bit parallel tri-state Command/Monitor (CON/MON) bus for command/monitor argument transfer and interactive hand-shake signals to control the Wire-Wrap board logic. The Standard Interface Board also has an 8-channel differential analog multiplexer/Sample/Hold/A-D Converter to sample and convert the Wire-Wrap board analog signals to digital values.

The Wire-Wrap board contains the following circuitry:

Address decode logic provides enables for two 8-bit command registers (Cryogenics Control and Calibration Control) and enables for four 8-bit and one 16-bit digital monitor registers.

The Cryogenics Command register controls the state of the Front-End cryogenic equipment and the Calibration Control register controls the Front-End calibration circuitry.

The digital monitor registers sample Front-End control logic states and the three Front-End status codes (described below).

Calibration Control logic controls the Calibration Drive circuitry in one of five modes. An externally-supplied switching signal (i.e. Mod, 80 Hz) drives the calibration switching logic. If the noise source drive currents exceed a pre-set level, Calibration Inhibit circuitry inhibits the Calibration Drive.

A 16-channel, single-ended analog multiplexer samples calibration drive voltages and currents and Front-End voltages for conversion by the SIB.

A power-on reset circuit clears the Cryogenics and Calibration Control registers to the zero state when power is applied to the module.[1] The cleared state of the Cryogenics control register is interpreted by the Front-End control logic as equivalent to the STRESS state (designated STRESS* in the state table on the next page).

In response to an ID Request signal from the SIB, the Wire-Wrap board asserts a block ID code on the SIB tri-state Command/Monitor bus to identify the Front-End type. The Front-End type code is the Front-End band code.

The F117 has provisions for an external 8-channel analog multiplexer. J1, the Front-End Monitor Connector, has three address bits and the multiplexer analog output connected to five J1 contacts that are not used in the Front-End circuitry. This external multiplexer is used in module F118 which controls Front-Ends that do not use cryogenic cooling.

The F117 module has an internal RFI-shielded enclosure that contains the SIB and Wire-Wrap board. This enclosure reduces the emissions from the SIB microprocessor clock and digital logic.

F117 functional specifications are tabulated below.

F117 Command and Digital Monitor Specifications

Function	Quantity	Mux Address
Cryo Command Word, 8-bits*	1	Mux 20H
Cryo Command Echo Digital Monitor, 8-bits*	1	Mux 20H
Cal Switching Command Word, 8-bits**	1	Mux 22H
Cal Switching Command Echo Digital Monitor, 8-bits**	1	Mux 22H
RCVR S/N, Band & Mod Codes Digital Monitor, 16-bits	1	Mux 23H
RCVR Discretes Monitor, 8-bits***	1	Mux 21H
F117 Serial Number Digital Monitor, 8-bits	1	Mux 24H
F117 Module ID Value, 8-bits (RCVR Band Code)***	1	

Notes: * 3 bits used, 5 spare bits
** 4 bits used, 4 spare bits
*** 6 bits used, 2 spare bits
**** see RVCR Band Code values below

[1] The Front-End contol logic interprets the cleared state of the Cryogenics Control register as the STRESS mode. STRESS is a test mode which adds an excess heat load to the Front-End to test the refrigerator cooling capacity. If the Front-End is in the computer control mode and a power dropout or glitch occurs, it should be immediately commanded to the COOL state. In normal operation, the Front-End is kept in the (manual) COOL state; this state inhibits computer control of the cryogenics modes.

F117 Analog Monitor Functions

Function		Quantity	Mux Address
Maximum Voltage to Analog Inputs	+/-	20 Volts	
Analog Voltage Measurement Range	+/-	10 Volts	
A/D Conversion Scaling		4.8828 mV/count, 2's complement code	
Number of Front-End Analog Signals Multiplexed		12	08H,.... 17H
Number of Internal Analog Signals Multiplexed		2	OCH, ODH
Number of External Analog Multiplexer Channels		8	18H, ... 1FH
Number of Spare Analog Multiplexer Channels		3	OOH, OEH, OFH,

Front-End and F117 Analog Monitor Data

Address (Hex)	Function	1 Volt =	Normal Value	Data Range
00	ANLGO, Spare, not connected	1V	*****	
01#				
02#				
03	ANLG3, External 8-channel Multiplexer			
04	ANLG4, Low Cal Current	100 mA	*	*
05	ANLG5, Hi Cal Current	100 mA	*	*
06	ANLG6, Low Cal Volts/4	1V	+7.000	+6.900 to +7.100
07	ANLG7, Hi Cal Volts/4	1V	+7.000	+6.900 to +7.100
08	VP, Pump Vacuum	**	+10.000	+9.950 to +10.000
09	ACI, Front-End AC Current Load	0.1A	***	***
OA	LED, Voltage	1V	+7.000	+5.000 to +8.000
OB	SENS, refrigerator 2nd Stage Temp	1V	****	****
OC	+7.5, F117 +7.5 Volt Reference	1V	+7.500	+7.490 to +7.510
OD	GND, F117 Analog Ground Reference	1V	0.000	-0.020 to +0.020
OE	Spare Analog Channel	1V	*****	
OF	Spare Analog Channel	1V	*****	
10	LF#1, Left FET #1 Bias	1V	-0.600	-1.000 to +1.000
11	RF#1, Right FET #1 Bias	1V	-0.600	-1.000 to +1.000
12	LF#2, Left FET #2 Bias	1V	-0.600	-1.000 to +1.000
13	RF#2, Right FET #2 Bias	1V	-0.600	-1.000 to +1.000
14	15K, 15 Deg Stage Temperature	100K	+0.150	+0/100 to +0.200
15	50K, 50 Deg Stage Temperature	100K	+0.550	+0.400 to +0.700
16	300K, 300 Deg Stage Temperature	100K	+2.900	+2.000 to +3.000
17	VD, Dewar Vacuum	**	0.000	-0.200 to +0.200

Notes:
\# SIB analog inputs ANLG1 and ANLG2 are used by the Wire-Wrap board 16 channel multiplexer. These addresses are 08 through 17.
* Calibration Noise Source currents are different for each frequency band.
** Non-linear scale, see the Data Sheets section (5) which has a vacuum vs monitor output voltage curve.
*** Front-End AC load currents depend upon the Refrigerator type.
**** Non-linear function of temperature but provides a greater sensitivity at low temperatures.
***** Not connected, may be any value, of no significance until assigned.
Left and Right FET #1 Bias voltages are the gate voltages of the cooled amplifier's first stages.
Left and Right FET #2 Bias voltages are the summed gate voltages of the sucessive stages of the cooled amplifiers. These four gate voltages should not vary from the values observed when the Front-End is installed.

Front-End Description

For a better perspective of F117 functions, a very brief functional description of the Single-Band Front-End follows. The emphasis is on the control and data aspects; RF properties are treated lightly. For additional details on the Front-Ends, refer to the NRAO Technical Reports listed in the Appendix.

A Single-Band, Front-End is a complete, independent, modular assembly consisting of a dewar, RF amplifiers, refrigerator, vacuum and cryogenic plumbing, and interface circuitry. Since it is a modular

design, differences between Front-Ends are principally in the RF circuitry. This modularity provides greater commonality among Front-Ends which reduces construction costs, eases installation and simplifies maintenance. These Front-Ends may be quickly removed from the antenna for maintenance or replacement without disturbing the other Front-Ends. In removing a Single-Band Front-End, its AC power is disconnected first. Removing the AC power will close the vacuum valve if it was open. The vacuum and cryogenic lines from the manifolds to the Front-End are disconnected next. After completing these simple operations, the Front-End may then be unbolted and replaced by another unit. This simplification of Front-End replacement reduces antenna down-time and the commonality among Front-Ends improves maintainablilty.

A waveguide polarizer on the Front-End input separates the left and right circular polarized (LCP and RCP) signal components for amplification by two cooled amplifiers. Low and High calibration signals are coupled into the Front-End inputs via a power splitter and directional couplers. After passing through the dewar walls, the signals are filtered by band-pass filters and are further amplified by room temperature post-amplifiers. The two signals are then output to the mixers-IF system. An LED in the cooled amplifiers stabilizes HEMT sensitivity. The noise source drive voltage is the same for all Front-Ends but the noise source current may differ between bands. For example, at 20 cm and 3.6 cm (L and X bands), an amplifier is required to achieve the required high noise level. The amplifier is switched by the High cal drive. Only a few few Front-Ends are equipped with a high noise source.

The Front-End is enclosed in an evacuated dewar that is cooled by a closed-cycle, Helium-cooled refrigerator. The dewar is connected to a vacuum manifold through an electrically operated vacuum valve and quick-disconnect coupling. The refrigerator is connected to Helium supply and return manifolds via Arequipt couplings and operates continuously (in the COOL state) but the vacuum pump operates only when commanded by a Front-End. When the vacuum pump is not operating, the vacuum manifold is vented to atmospheric pressure; this helps to seat the Front-End's vacuum valve. The Front-End Helium supply and return pressures should be 270 +/- 10 psi and 60 +/-15 psi, respectively. Helium supply and return pressures are monitored by F118.

Dewar vacuum, refrigeration and heating control is performed by control logic in the Front-End (described below); control bits X, C and H(L) from the F117 define the five Front-End control states as shown below.[2] (A "1" is a TTL high level.)

Front-End Cryogenics Control State Table

Control Bit	X	C	H(L)	
CRYO OFF	1	0	1	No refrigerator power, heater power, or vacuum pumping.
COOL	1	1	1	Normal cooled operation.
STRESS	1	0	0	COOL with small added heat to stress-test cryogenics.
HEAT	1	1	0	Fast warm-up of dewar, 65 Watts of heater power.
PUMP	0	1	0	No refrigerator or heater power.
STRESS*	0	0	0	Reset state of the Cryogenics Control Register

The reason for the all-1's COOL code is that in the event of an "X, C and H(L) stuck high" failure of the Front-End controller or the Front-End J5 cable is disconnected, the control logic defaults to the COOL state, the desired default condition for a Front-End. This state is also convenient for Front-End bench tests. The STRESS command causes a small amount of heat to be generated in the Dewar; the

[2] In a sense, the H(L) bit can be considered a "not-heater" bit although it is combined with X and C and temperature-dependent terms in the Front-End control logic. See VLBA Technical Report No. 1 for details.

response of the refrigerator to this additional load may be seen in the 15 and 50 degree stage temperatures. The HEAT command is a maintenance command which causes the Dewar to be heated; this permits the dewar to be warming up while Front-End maintenance personnel are on the way to the Antenna. The PUMP command causes the vacuum valve and vacuum pump to be turned on. These states are controlled by Front-End control logic described below.

The STRESS* state is not defined in the Front-End control circuitry. However, when the Cryogenics Control Register is cleared (e.g., a power reset), the Front-End cryogenic control logic reverts to the Stress state[3], a refrigerator test state (hence undesirable for sustained periods). When installing an F117 in an antenna with operational Front-Ends or when a power drop-out or glitch occurs, a COOL command should immediately be sent to the F117's when power is restored.

Dewar vacuum and temperature transducers are conditioned by a control and monitor electronics card cage attached to the dewar. A mode control switch on the card cage enables the Front-End vacuum, refrigeration and heater circuitry to be set to the CPU control mode or any of the five manual control modes tabulated above: OFF, COOL, STRESS, HEAT, and PUMP. The CPU position permits antenna computer control of these functions via F117 and the Monitor and Control System. In the CPU position, the X, C and H(L) control bits from F117 set the control states to OFF, COOL, STRESS, HEAT or PUMP. When the mode switch is set to any position other than CPU, these functions are determined by X, C and H(L) control bits from the control logic as a function of the mode control switch position. The position of the mode control switch is indicated by the M(L) discrete; if the switch is in the CPU position, M(L) is high ("1") and it is low ("0") in any other (e.g. manual control) postion. In practice, the Front-End control switch is normally set to the COOL state, a manual control condition; therefore, the antenna computer cannot control the cryogenic functions.

Control logic in the card cage controls the operation of the vacuum pump request, vacuum valve, refrigerator, and heater. The control logic inputs are the mode control switch X, C, H(L) and M(L) bits; the F117 X, C and H(L) control bits; dewar (VD) and port (VP, manifold) vacuum; dewar (15K, 15 deg stage) temperature and AC current load (ACI). Control outputs are the discretes: vacuum valve solenoid drive S, pump request P, refrigerator motor power and dewar heater power. The operations performed by the control logic are described in the next paragraph.

Vacuum valve operation is inhibited if the pump port (VP, manifold) vacuum is above 50 microns. The vacuum valve is opened if the pump port vacuum is less than the dewar vacuum (VD) and the dewar vacuum is greater than 7 microns. The discrete signal S indicates the state of the vacuum valve command. The pump request signal (P) becomes true (i.e., a "1") if dewar vacuum exceeds 5 microns and goes false ("0") if the dewar vacuum becomes less than 3 microns. The discrete monitor signal P indicates the state of the pump request signal. The refrigerator operation is inhibited if the dewar vacuum is above 50 microns. The Front-End control logic is designed to continue the refrigerator operation in the event that the J5 cable (power and control bits) from F117 is disconnected. This permits maintenance of the system electronics but does not affect the cryogenics operation. The control logic turns on the heater when the mode switch is set to HEAT or when the central computer commands the HEAT state. The control logic also protects the dewar from overheating by the heater when in the HEAT state.

Monitor circuitry in the card cage reads out the three operative control bits (X, C and H(L) from either F117 or the mode control switch (depending upon the switch position), M(L) (the mode control switch status) and control output discretes P and S. The monitor circuitry also reads out the following analog values: vacuum (VD, dewar and VP, pump port); linear temperature measurements (15K, 50K and 300K degree stages); a non-linear temperature measurement (SENS, on the 15 degree stage); AC current

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[3] VLBA Technical Report No. 10

load (ACI); HEMT and FET gate bias levels (LF#1, LF#2, RF#1, RF#2), and the LED voltage. These parameters are output to F117 analog multiplexers via monitor connector J2. The normal values and working range are tabulated above.

A 12-position manual selector switch and integral DMM on the card cage permit the analog parameters to be monitored locally.

Front-End Status Codes

The Front-Ends read out digital status code values that indicate the Front-End frequency (**Band Code**), **Front-End Serial Number**, and the **Modification Level**. These codes are hard-wired in the Front-End when it is manufactured and are output to the F117 on the Power-Control-ID connector J2. These codes are:

The **Band Code** is a four-bit binary plus parity (even) code (bits F_0 through F_3 and PA, parity), from the Front-End via the J2 (monitor) connector.

The Front-End type, WL (wavelength in cm or mm), freq (frequency, MHz or GHz) and **Band Code** (Hex) are tabulated below.

Front-End Type, Band, Band Codes and Wavelength/Frequency

FE Type	Band	WL/Freq Code		FE Type	Band	WL/Freq Code	
F101*	P	00H	400 cm/75 MHz	F102	P	01H	90 & 500 cm/330 & 610 MHz
F103	L	02H	20 cm/1.4 GHz	F104	S	03H	13 cm/2.3 GHz
F105	C	04H	6 cm/4.8 GHz	F106	X	05H	4 cm/8.4 GHz
F107*	X	06H	2.8 cm/10.7 GHz	F108	U	07H	2 cm/15 GHz
F109	K	08H	1.3 cm/23 GHz	F110	Q	09H	7 mm/43 GHz
F111*	W	0AH	3.5 mm/86 GHz				

* Not currently implemented on the VLBA

Front-End Serial Number is a six-bit binary hard-wired code (bits S_0 through S_5) from the Front-End and is unique to each Front-End. **Front-End Serial Number** ranges from 1 through 63.

The **Modification Code** is a two-bit code (M_0 and M_1) that indicates the Front-End modification level.

Two DB25 connectors on the Front-End provide the +/- 15V Front-End Power and the F117 control and monitor connections. Two shielded, 25 conductor cables connect an F117 to a Front-End. J5 (25 pin contacts) carries Front-End Power, the antenna control computer X, C and H(L) control bits, the **Band Code** code bits, the **Front-End Serial Number** code bits and Front-End **Modification Level** bits. J2 (25 socket contacts) carries analog and discrete monitor signals. Figure 3 shows the assignments of these power, control, status codes and monitor signals on the F117 front panel J1 and J2 connectors.

A dedicated (for each Front-End) Refrigerator Drive Unit (P111 for 5 GHz through 43 GHz Front-Ends or P112 for 1.5 GHz through 2.3 GHz Front-Ends) in the Antenna Vertex Room Feed Tower provides

two-phase, 150 Volts AC power for the Front-End. The refrigerator Drive Unit has an isolation transformer and phase shift network to generate the shifted phase. The unshifted phase of this 150 volt AC also powers the vacuum valves and dewar heaters. P111 (or P112) also has an AC current transducer to measure the Front-End total AC current load. This Front-End AC current load is monitored by F117 multiplexer channel 09H.

The Helium Supply and Return Pressure and vacuum pump functions are common to cooled Front-Ends. Two Helium compressors typically drive five Front-Ends; F118 monitors the output of the four pressure transducers used to monitor the two compressors' Helium supply and return manifolds. Each F117 monitors its associated Front-End's Dewer and Pump vacuum.

A-Rack power supplies provide the Front-End's +15 and -15 DC Power via F117. The B-Rack +/-15, +5 and +28 Volt DC power is monitored by F118.

In addition to the two DB25 connectors mentioned above, the Front-End has an "AUX" DE9 (9 socket contacts) J4 connector which carries the Pump Request (P) and a return. This signal is combined with eight other Pump Requests in the Vacuum Pump Controller installed in the "A" Rack. This unit functions as an eight-input OR gate; when any Front-End Pump Request becomes true (high), the controller logic turns on a solid state relay to apply AC power to the Vacuum Pump.

When an F117 is removed from the bin or the F117's J2 cable is disconnected, the associated Front-End cannot activate the Vacuum Pump Controller.

The Single-Band, Front-Ends do not have an internal transfer switch to interchange the LCP and RCP signals for test purposes. This feature is implemented in the Converter Modules (T101 through T110).

2.0 THEORY OF OPERATION

The VLBA Monitor and Control Bus (MCB) is described in Section 2.1. The Standard Interface Board interacts with the MCB and activates the Wire-Wrap board circuitry. It is described in Section 2.2. These two descriptions provide the basis for the description of the Wire-Wrap board circuitry in Section 2.3.

2.1 MONITOR AND CONTROL BUS DESCRIPTION

This MCB description is abstracted from VLBA Technical Report No. 12. Some details of the bus description have been omitted for brevity; these details are factors in the design of the SIB and are not a concern of this manual. Readers interested in a more detailed description of the MCB are referred to this Technical Report.

In the bus and SIB descriptions below, the term "Device" refers to a unit (module, etc.) containing a Standard Interface board or a functional equivalent. F117 is a typical device.

The VLBA Monitor and Control Bus (XMT and RCV) conform to the EIA RS-485 signal specification.

Interface Address Block

Each Device Interface (Standard Interface Board) is assigned a unique block of contiguous addresses to which it alone responds. The block may be any length up to 256 addresses and is disjoint with the address blocks of all other Interfaces. The last 16 addresses (described below) of each block are dedicated to storage of the ID byte value N, block start address and error counters (parity, etc.) internal to the Interface. These counters may be read out as monitor data.

The MCB consists of two differential-mode logic signals, each on a shielded twisted pair cable wired as a multi-drop party line. The bus signals are called Transmit Data (XMT) and Receive Data (RCV). The MCB Controller is the station computer which transmits messages on the XMT line and receives messages on the RCV line. The Interfaces (one at a time) are the sources of Receive Data. Data is bit-serial at a rate of 57.6 kbaud and the transmissions are byte asynchronous. Each byte consists of, in order, a start bit (binary 0), eight data bits (least significant bit first), one parity bit, and one stop bit (binary 1).

XMT and RCV bus messages are combinations of data value bytes and control function codes. The data value bytes are address and argument values: Address High (ADH), Address Low (ADL), Control Data High (CDH), Control Data Low (CDL), Monitor Out High (MOH) and Monitor Out Low (MOL). Data value bytes are transmitted with odd parity.

Control function codes (bytes) signal the start of a message or report interface-device status during the execution of control and data request messages. The Control Function codes are: Synchronization (SYN), Acknowledge (ACK), Second Acknowledge (DC1), Non-Response Acknowledge (DC2) and Negative Acknowledge (NAK). Control Function codes are transmitted with even parity.

XMT Line

Every message on the XMT line is exactly five bytes long and the bytes occur in the following sequence: SYN, Address High (ADH), Address Low (ADL), Control Data High (CDH) and Control Data Low (CDL). The SYN byte indicates the beginning of a message and is the only even bit parity byte on the XMT line (thus distinguishing it from all data bytes). The SYN byte is followed by ADH. If the most

significant bit of ADH is 1, then the message is a control message; otherwise it is a monitor request message. The remaining 15 bits of ADH/ADL form a binary address in the range of 0 through 32767.

Each Standard Interface receives ADH and ADL of every message on the XMT line and compares it with its assigned address block. If the address is within the assigned interface address block and there is no parity error, then shortly after (<382 usec) the last bit (Stop) of ADL, the interface must begin to transmit a one byte acknowledge code (ACK) on the RCV line.

A DC1 second acknowledge code is transmitted on the RCV line if the following conditions are met: SYN, ADH, ADL, CDH and CDL have valid parity, the address is within the assigned block, a control message is specified **(indicated by a 1 in the msb of the ADH)** and the device responds to the interface handshaking properly.

The Interface checks parity on all bytes received. If SYN has a parity error, an internal counter is incremented.

If ADH or ADL has a parity error, the Interface does not respond (just as if the address were outside its block), but increments an internal address parity error counter and looks for the next valid SYN.

A negative second acknowledge code NAK is transmitted on the RCV line if: SYN, ADH and ADL have valid parity, the address is within the assigned block and a control message is specified, but CDH or CDL has a parity error. In this case CDH/CDL is not passed to the device and a control data parity error counter is incremented.

A second form of negative acknowledge byte (DC2) is returned if the interface is unable to complete its handshaking with the device to which it interfaces. The device non-response condition is counted by two internal counters (one for commands and one for monitor data).

If the message is a monitor request message within the address space assigned to monitor data, the CDH and CDL byte values are ignored; they have no meaning. The parity of CDH/CDL is, however, tested and the control data parity error counter is incremented if tainted by an error. In this case, the monitor data specified by ADH/ADL is returned in the normal manner because the CDH/CDL parity error has no effect upon the validity of the monitor data.

RCV Line

Messages on the RCV line are either a two byte command acknowledgement or a two or three byte monitor data acknowledgement, as follows:

Command acknowledgement messages are: 1) ACK, DC1 (normal, no fault command execution acknowledgement), 2) ACK, NAK (CDH/CDL parity error acknowledgement), and 3) ACK, DC2 (device non-response acknowledgement).

Monitor request acknowledgement messages are: 1) ACK, MOH, MOL (normal, no fault acknowledgement followed by two bytes of monitor data obtained from the address specified by ADH/ADL); 2) ACK, DC2 (fault acknowledgement, monitor data is unavailable from the device).

The Controller also checks parity on all bytes received on the RCV line. In the event that monitor data or function codes have parity errors, the Controller application software notes the errors and disqualifies the data.

Bus Timing

The first acknowledge byte (ACK) also functions as a clear to send to the controller, granting the controller the right to begin its next message, and promising to yield the RCV line before it is needed for another interface's response. The interface will have at least 573 microseconds after the end of transmission of CDL to disconnect from RCV.

The Controller may begin transmitting another message following a control message after the receipt of the acknowledge (ACK) byte. Figure 4 (following this section) shows the XMT and RCV bus formats and maximum-speed and minimum-speed timing for sequences of control messages and monitor requests.

Note from Figure 4 that in the maximum rate mode of control message reception, the interface is transmitting the second acknowledgement (DC1) concurrent with the reception of a new control message.

Note also from Figure 4 that in the maximum rate mode of monitor request message reception, MOH/MOL are being transmitted on RCV at the same time that a new message is being received on the XMT bus.

Function Codes

The hexadecimal byte values for the control function codes are as shown below. These bytes are transmitted in even parity, which makes them unique since data bytes are odd parity.

SYN - 16, Synchronization byte which prefixes all messages from the controller.

ACK - 06, First acknowledgement byte to the controller which signifies that SYN was detected and that SYN, ADH and ADL did not have parity errors. ACK is not transmitted if there was a parity error on any of these three bytes.

DC1 - 11, Second acknowledgement byte to the controller which signifies that in the case of control messages, there were no parity errors in CDH/CDL and the device responded properly to the interface-device handshaking requirements.

NAK - 15, Negative acknowledgement byte to the controller which signifies that, for control messages, CDH/CDL was tainted by a parity error.

DC2 - 12, Second negative acknowledgement byte to the controller which signifies that the device logic did not respond to the interface handshaking within the allocated time period. This non-response acknowledgement is used for both control and monitor request messages.

Interface Internal Monitor and Control Functions

The last 16 addresses in the address block are allocated to Monitor and Control parameters internal to the Standard Interface board. The occurrence of bus fault conditions (such as parity errors, invalid SYNC, etc.) is accumulated in counters and is available for monitor data readout by the Controller. Device non-response events are also accumulated. These parameters were described above. The counters are capable of being reset or set to other values by a control message from the Controller.

Other parameters in this block are the Interface Type and Revision level, Block ID Code (N) and Address Block start address. This Block ID Code is the index for assignment of the address block by the

Controller. None of these locations (indicated by bold print) can be overwritten by the Controller. The last three addresses in the block are reserved for future assignment.

These Interface addresses are identified by the notation: BE-1, BE-2, etc. where BE designates the Block End (last) address. The assignments are as follows:

Address	Value
BE-15	Reserved for future use
BE-14	" " " "
BE-13	" " " "
BE-12	No Control Response counter (i.e, no DEV ACK from device)
BE-11	No Monitor Response counter (i.e., no DEV ACK or ANENB from device)
BE-10	**Interface Type and revision code (cannot be altered by the Controller)**
BE-9	Address of last control message received. (i.e., ADH and ADL)
BE-8	Control data for last control message received. (i.e., CDH and CDL)
BE-7	Address parity error counter, all messages
BE-6	Control data parity error counter, all messages
BE-5	Invalid SYN character
BE-4	Control data parity error counter, messages in block
BE-3	**N, ID byte value from device logic (cannot be altered by the Controller)**
BE-2	Count of correctly received control messages
BE-1	Count of correctly received monitor data request messages
BE-0	**Address of beginning of block (cannot be altered by the Controller)**

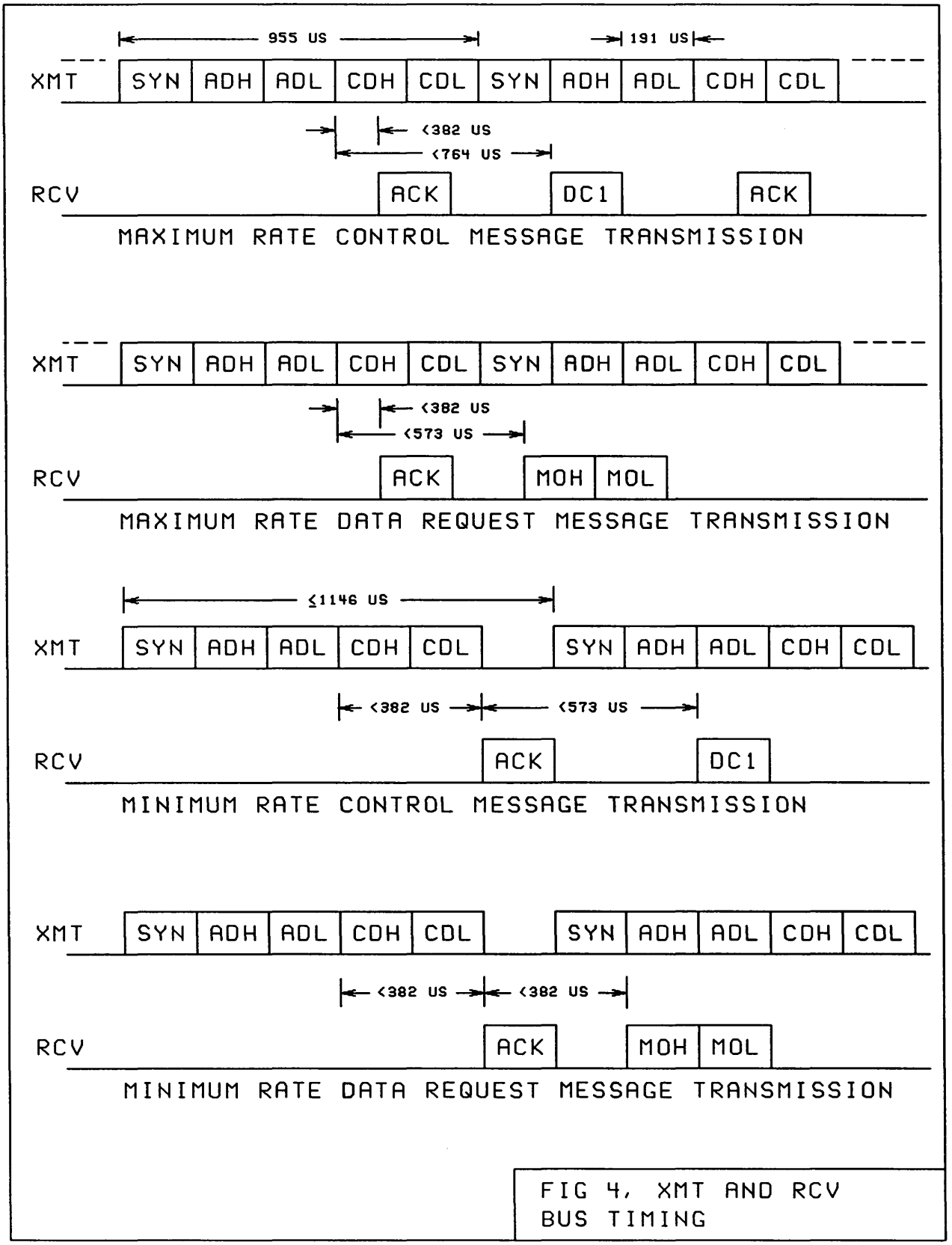


FIG 4, XMT AND RCV BUS TIMING

2.2 STANDARD INTERFACE BOARD DESCRIPTION

This section describes the VLBA Standard Interface Board, Version "D" (for differential analog signals). The previous section described the MCB bus and the bus-SIB interaction protocols. This section briefly describes the operation of the Standard Interface Board and its interactions with the Wire-Wrap board circuitry.

The material in this Section is an adapted abstract from VLBA Technical Report No. 12. The Wire-Wrap board circuitry is fully described in Section 2.3.

This section does not describe the SIB microcontroller and support chips, the microcontroller firmware and the A/D Converter. Readers interested in a more detailed description of the Standard Interface Board are referred to the Technical Report cited above.

The description is based upon the assumption that XMT line messages are error-free. In the event of a parity error, the SIB performs the operations outlined in Section 2.1 above.

SIB Functions

The Standard Interface Board (version "D") logic schematic is shown on drawing D55002S002. The reader should frequently refer to this schematic during the following description.

An Intel 8032 Microcontroller is the logic element that receives and analyzes the XMT bus messages and outputs the RCV bus messages. The 8032 firmware program execution controls all operations of the SIB with the exception of the SIB power reset. The 8032-driven SIB circuits activate the Wire-Wrap board logic to store command argument values in the designated registers and gather and format designated digital and analog monitor data from the Wire-Wrap board circuitry for output on the RCV line.

Following the successful (i.e., error-free) reception of a control or data request message, the SIB will have stored 16-bit ADH-ADL and CDH-CDL values.

The lower 15 bits of ADH-ADL is the address of some device function such as a command register or monitor data source. When the MSB of ADH is a "1", the message is a command message and when it is a "0", it is a Data Request message. The SIB block start address is subtracted from the ADH-ADL value to form an 8-bit Relative Address which is parallel-output to the Wire-Wrap board on the RA0, ... RA7 lines. The Wire-Wrap board uses only six of these addresses which are designated ADDR0, ... ADDR5 in the schematic diagrams. Decode logic in the Wire-Wrap board generates enable terms to store command arguments in the two command registers or to read monitor data to be read from digital registers.

The 16-bit CDH-CDL value is the control message argument to be stored in the address designated by ADH and ADL. These 16 bit values are asserted upon the SIB parallel tri-state CON/MON bus. The Wire-Wrap board stores the CON/MON argument in the register designated by the ADDR0, ... ADDR5 state using the SIB handshake signals (described below). CDH and CDL values have no meaning if the message is a Data Request.

Because analog signal multiplexing and A/D conversion are frequently required, the Standard Interface Board contains an analog multiplexer-A/D Converter. The converter is integrated into the logic of the interface so that it may be easily applied to analog signal monitoring applications. The analog mulitplexing capacity of the interface may be extended by additional analog multiplexers installed in the

device circuitry. On drawing D55001S002, note that the 12 A/D converter data bits are connected to the upper 12 CON/MON bus lines; the lower 4 four bus lines float, which makes them indeterminate.

The A/D Converter output is a 12-bit, 2's complement code with a resolution of 4.8828 mV/count. The 12 data bits are left-adjusted in the 16-bit data value and the four lower buts are undefined. The 16-bit formats of plus full scale, minus full scale and center scale values are tabulated below.

Value, Volts	MSB															LSB
+9.995	0	1	1	1	1	1	1	1	1	1	1	1	U	U	U	U
+0.005	0	0	0	0	0	0	0	0	0	0	0	1	U	U	U	U
0.000	0	0	0	0	0	0	0	0	0	0	0	0	U	U	U	U
-0.005	1	1	1	1	1	1	1	1	1	1	1	1	U	U	U	U
-9.995	1	0	0	0	0	0	0	0	0	0	0	1	U	U	U	U
-10.000	1	0	0	0	0	0	0	0	0	0	0	0	U	U	U	U

U Denotes undefined states.

To convert the analog data values to volts, truncate the 16-bit value to 12 bits by a fixed-point divide by 16 or a four-bit right shift and multiply the resultant (2's complement) value by 0.0048828. Dividing by 16 eliminates the four least significant bits which are undefined.

The use of HI/LO SEL logic makes the analog signal address space compact when device multiplexers are used in conjunction with the on-board analog multiplexer. This is accomplished by device address decode logic to control the state of HI/LO SEL as described below. If HI/LO SEL is low, address bits RA0, RA1 and RA2 select the on-board analog multiplexer channel and if it is high, RA5, RA4 and RA5 control the channel selection.

If no more than eight analog signals are to be multiplexed and converted to digital values, HI/LO SEL should always be low. In selecting an input signal, the on-board address multiplexer is controlled by the three lowest bits of RA: RA0, RA1 and RA2.

If the device circuitry has analog multiplexers, their outputs are connected to the inputs of the board multiplexers, ANLG-0 .... ANLG-7. RA bits RA0, RA1 and RA2 control the channel selection in these device multiplexers.

The SIB address bit multiplexer is a quad two-to-one (74LS157) multiplexer with RA0, RA1 and RA2 connected to the A inputs. The next three address bits (RA3, RA4 and RA5) are connected to the B inputs. A low on the SEL line will select the A inputs and a high will select the B inputs. The three outputs of the 74LS157 are connected to the address inputs of the SDM-854 multiplexer-S/H-A/D Converter.

Note that in the table of F117 Analog signals shown above (Section 1), some analog signals are connected directly to SIB analog inputs (e.g., ANLG4, .. ANLG7) and others are connected to multiplexers whose outputs drive ANLG1-ANLG2 and ANLG3. Note that the analog addresses are a contiguous block. Logic in the Wire-Wrap board controls the SIB address multiplexer via the HI/LO SEL line. The implementation is described in Section 2.3.

By implementing HI/LO SEL logic similar to that used on the Wire-Wrap board, up to 64 analog signals can be multiplexed using a combination of device multiplexers and the SIB multiplexer inputs with a contiguous address space.

SIB Interface Signals

The following signals interface the SIB to the Wire-Wrap board circuitry:

RA Relative Address is the difference between the 16-bit bus address (ADH-ADL) and the first address of the block. RA is 8 bits which provides 256 addresses. The F117 Wire List and Wire-Wrap board logic schematics use the notation ADDR0 (LSB), ADDR1,..... ADDR5 to designate these address terms.

CON/MON CON/MON is a 16-line, parallel tri-state bus used for message argument interchange between the SIB and Wire-Wrap board logic. During the intervals between argument transfers, the SIB tri-state drivers are disconnected. Wire-Wrap board logic connected to the CON/MON bus is also disconnected from the CON/MON bus after an argument transfer. The F117 Module Wire List, the Wire-Wrap board schematic diagrams and the module wiring diagram all use the notation C/M 0, ... C/M 15 to designate these bus lines.

R/W- R/W- (read/write-not) designates the type of interaction with the device logic. If low, it requires the Wire-Wrap board to read the data standing on the CON/MON bus. If high, it requires the Wire-Wrap board (or the SIB A/D converter) to assert monitor data on the CON/MON bus. R/W- is held low during the interval between message executions. This signal is designated R/W(L) in the F117 Module Wire List and Wire-Wrap Board logic schematics.

DEV REQ DEV REQ (Device Request) signals the Wire-Wrap board that a command or monitor operation must be performed. The Wire-Wrap board decodes the RA and executes the control or monitor data action as a function of the address. DEV REQ remains high until the Wire-Wrap board returns a DEV ACK (Device Acknowledge) or an ANENB (Analog Enable) signal which will cause DEV REQ to go low. In the event the Wire-Wrap board logic does not return a DEV ACK (or ANENB) signal within 500 usec, the SIB disconnects the CON/MON bus, drops DEV REQ and signals a no-response fault to the controller by outputting a DC2 function code on the RCV line.

DEV ACK DEV ACK (Device Acknowledge) signals that the Wire-Wrap board has (if a command) read the command argument on the CON/MON lines or (if the requested data is digital) has asserted the requested data upon the CON/MON bus.

ANENB ANENB (Analog Enable) is the DEV ACK counterpart when RA specifies an analog signal. ANENB signals the SIB that RA specifies an analog signal which is to be sampled and converted by the SIB analog multiplexer and A/D converter. ANENB is generated by the Wire-Wrap board address decode logic. When ANENB goes true, the analog multiplexer selects the RA-designated channel and the A/D conversion process is initiated. In this A/D conversion to case, the Wire-Wrap board logic holds DEV ACK low. If RA does not specify an analog address, the Wire-Wrap board logic holds ANENB low.

HI/LO SEL HI/LO SEL signals the SIB that either the lower three RA bits (RA:0,1,2) or the next three RA bits (RA:3,4,5) are to be used by the on-board analog multiplexer. HI/LO SEL controls this multiplexer. HI/LO SEL should always be low if only the SIB analog multiplexer is used. If both the on-board and device multiplexers are used in conjunction, (as is the case in F117), HI/LO SEL should be set high if the RA specificies an address for an external multiplexer whose output is connected to one of the SIB analog multiplexer inputs. Proper usage of the HI/LO SEL term enables remote analog multiplexers and SIB

analog multiplexer addresses to be contiguous in address space. (See the HI/LO SEL logic description in Section 2.3 below.)

ANLG-X ANLG-X are eight sets of differential analog signal inputs which are to be selected and converted to digital values for monitor data readout.

ID REQ ID REQ is 8032 port P1.5. When ID REQ goes low, the Wire-Wrap board logic asserts the Block ID code on the CON/MON bus as described below.

At this point, the reader should refer to the Standard Interface Block Diagram (Figure 5) on the next page to put these bus and device interface signals into context.

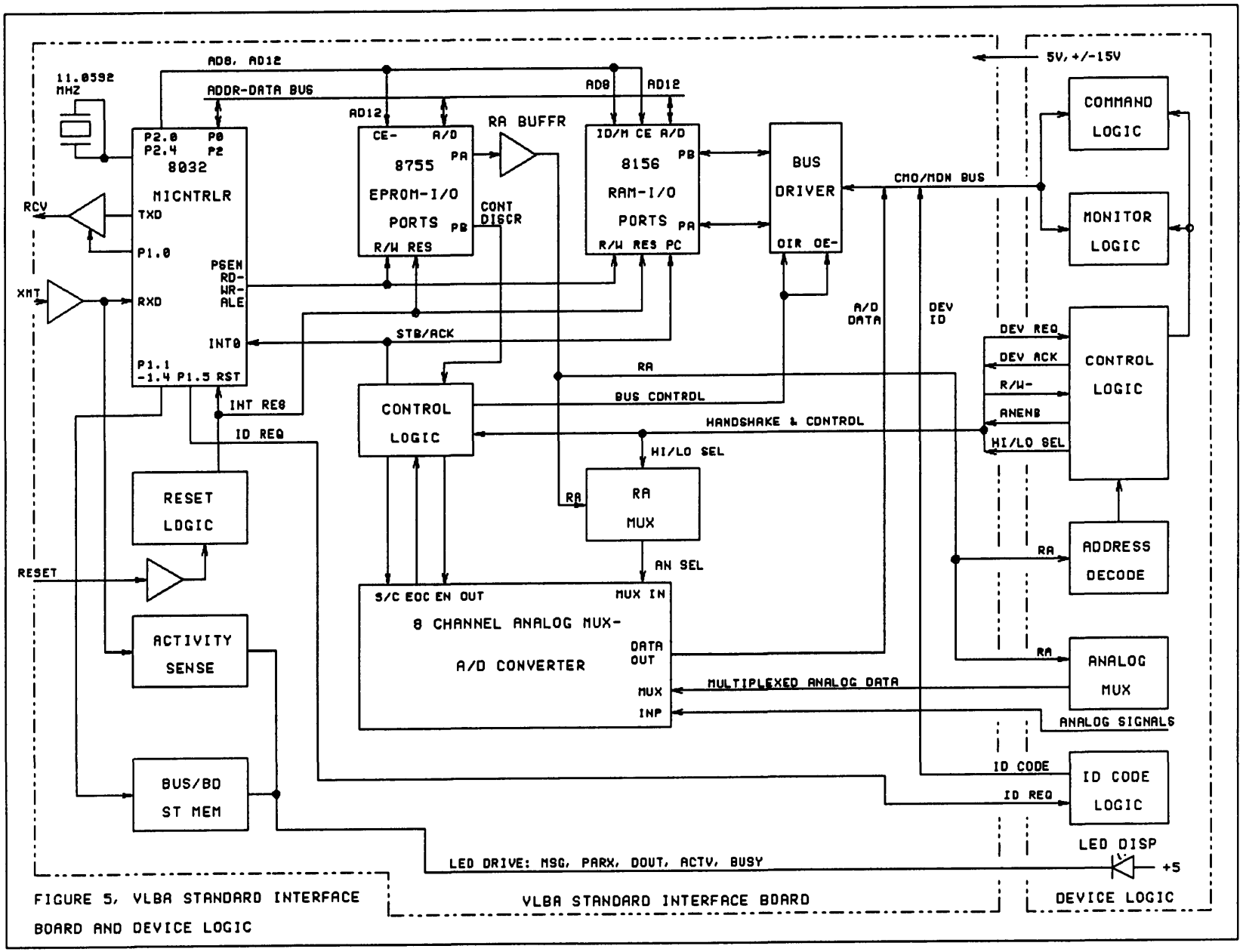


FIGURE 5, VLBA STANDARD INTERFACE BOARD AND DEVICE LOGIC

Referring to the SIB Schematic Diagram D55002S002, the reader will note that the SIB interface stimulus logic signals listed above are derived from four control discretes from Port B of U2, an Intel 8755. These glitch-free bits, BFR ENABLE, CMD RLSE, R/W- and IOR are set and cleared by the firmware during the course of interactions with the Wire-Wrap board logic. During the following discussion, the reader should refer to the SIB schematic diagram to see how these control discretes are used.

The SIB performs five types of operations, four of which are controlled by the microcontroller. After the hardware power-up reset and firmware initialization of hardware, the board operations are a response to the XMT bus signals described in Section 2.1.

The four firmware-controlled operations are: 1) Execution of a control message command to the device, 2) Acquisition of digital monitor data from the device in response to a monitor data request message, 3) Acquisition of analog monitor data from the device in response to a monitor data request message, 4) Device ID code read. These are described in this order below.

The descriptions below assume that there are no XMT line parity errors. In responding to all three types of messages, the SIB outputs an ACK to the Controller < 382 uSec after the reception of the ADH and ADL.

Execution of a Control Message

When a control message is received with an address within the assigned F117 address block, the firmware writes the eight bits of Relative Address (RA) into Port A of the 8755. RA is immediately available to the Wire-Wrap board address decode logic and precedes DEV REQ by about 24 uSec. RA remains static until changed by another message execution.

The message ADH byte MSB is a 1; this designates a control message so the firmware sets the 8156 Ports A and B to the output mode and writes the command argument into these Ports. The R/W- line is (normally) low which signals the Wire-Wrap board logic that an RA-designated command register is to be loaded. R/W- also sets the 74LS245 CON/MON Bus driver's direction to output (from the SIB) mode. At the same time that R/W- is set low, the command argument is asserted on the CON/MON Bus. These operations are completed several uSec before DEV REQ goes true (high).

DEV REQ is set high (true) which enables the Wire-Wrap board address decoder. The Wire-Wrap board responds to the DEV REQ signal with a DEV ACK signal after (about) a 20 nSec delay. After a firmware delay of several microseconds, the SIB lowers the DEV REQ signal and disconnects the 8156 Ports from the CON/MON bus. Lowering DEV REQ disables the address decoder. The trailing edge of the RA-designated decoder enable output clocks the lower eight bits of the argument on the CON/MON bus into the selected command register. About 20 nSec after DEV REQ goes low, the Wire-Wrap board lowers the DEV ACK line which completes the SIB-Wire-Wrap board command transfer.

The SIB then outputs a DC1 function code to the Controller via the RCV line to signify the completion of a control message execution.

In the event of a malfunction in the Wire-Wrap board logic that would inhibit the DEV ACK response, the firmware has a 500 usec timer which causes a DC2 (no F117 response) function code to be output to the Controller via the RCV line. In this case, the SIB lowers the DEV REQ signal.

After completion of the command, the R/W- line stays low and RA remains static until the next message execution.

Execution of a Monitor Data Request for Digital Monitor Data

When a monitor request message is received with the address within the assigned F117 address block, the firmware writes the eight bits of Relative Address (RA) into Port A of the 8755. RA is immediately available to the device address decode logic and precedes DEV REQ by about 18 uSec. RA remains static until changed by another message execution.

The following description assumes that RA specifies a digital monitor data register.

The message ADH MSB will be 0; this identifies a monitor data request. Consequently the R/W- control discrete is set high. The high state of R/W- conditions the Wire-Wrap board address decode logic to generate monitor data enables for the output of Digital Monitor data to the SIB on the CMD/MON bus. Since R/W- is high, the 74LS245 CON/MON bus drivers are set to the input (to the SIB) direction; this steers data from the device to the 8156 Ports A and B via the bus.

8156 Ports A and B are set to the input mode by the firmware.

The SIB sets DEV REQ high (true) 18 uSec after R/W- is set high. DEV REQ enables the Wire-Wrap board address decoder; the RA-designated decoder enable output holds the selected monitor data register static and causes the register outputs to be asserted onto the lower eight bits of the CON/MON bus.

The Wire-Wrap board responds to the DEV REQ signal with a DEV ACK signal after (about) a 20 nSec delay. This loads the data into the 8156 Ports A and B via the CON/MON bus. After a few uSec of firmware delay, the SIB responds to DEV ACK by reading the digital monitor data in the 8156 Ports A and B. The SIB then lowers the DEV REQ signal. When DEV REQ is lowered, the Wire-Wrap board lowers DEV ACK after about a 20 nSec delay.

After lowering DEV REQ, the SIB outputs the MDH and MDL monitor data to the Controller via the RCV line; this completes the monitor data request message sequence.

In the event that DEV ACK does not go true within 500 usec after DEV REQ has gone true, a firmware timer causes the DC2 function code to be output to the Controller on the RCV line; DEV REQ is also lowered.

Because the requested data is digital, the Wire-Wrap board address decode logic holds the ANENB line low. The HI/LO SEL line is a "don't care" case; the state of this signal does not affect the digital monitor data gathering sequence.

After the monitor data has been output to the Controller, the R/W- line reverts to the low state. RA will stay at the current message value until changed by the next message within the address block.

Execution of a Monitor Data Request for Analog Monitor Data

When a monitor request message for analog data is received with an address within the assigned address block, the firmware writes the eight bits of Relative Address (RA) into Port A of the 8755. RA is immediately available to the device address decode logic. RA remains static until changed by another message execution.

Although there are significant differences between the circuitry for digital and analog monitor data operations, both use the same 8032 firmware; the board logic makes both operations seem identical to the firmware.

The message ADH MSB is 0; this identifies a monitor data request and causes R/W- to be set high. The Wire-Wrap board logic does not use R/W- in executing a data request message for analog data.

The first steps in the execution of a request for analog data are similar to that for gathering digital monitor data.

8156 Ports A and B are set to the input mode and the CON/MON bus direction is set to input data to the 8156 Ports A and B.

The device must decode RA to determine whether the monitor data request is for digital or analog data. If analog data is specified by RA, the logic operations are quite different than for the digital data case. Instead of reading device registers on the CON/MON bus as in the digital data input case above, analog multiplexers on the board and in the Wire-Wrap board select the analog signal designated by RA. The selected analog signal is sampled by the SIB A/D converter sample-and-hold circuit and converted to a digital value. The A/D converter EOC (end-of-conversion pulse) asserts the converter data on the CON/MON bus and causes the A/D data to be loaded into 8156 Ports A and B.

Because R/W- is high, the 74LS245 CON/MON bus drivers are set to the input direction; this enables the data from the A/D converter outputs to be read by the 8156 Ports A and B.

18.4 microseconds after R/W- goes true, DEV REQ is output to the Wire-Wrap board to initiate the analog data gathering sequence.

The Wire-Wrap board address decode logic identifies an analog data mulitplexing-A/D Conversion operation; all addresses between 00H and 17H are analog data addresses.

DEV REQ and an RA less than 20H causes the Wire-Wrap board logic to feed back the ANENB signal to the SIB which initiates the A/D conversion sequence. ANENB is analagous to DEV ACK in that it is the device's response to DEV REQ but it really signals the **start** of the analog multiplexing-A/D conversion process, not the **completion** of the process as in the digital data case. ANENB is fed back to the SIB with a delay of about 20 nSec.

The HI/LO SEL feedback from the Wire-Wrap board determines the SIB analog data multiplexer address by selecting either the three least significant address bits or the next higher three address bits as described above. The Wire-Wrap board sets HI/LO SEL high if either address bit RA3 or RA4 are true (ADDR3 or ADDR4 in the Wire-Wrap board notation). The HI/LO SEL logic application to F117 analog multiplexing is described in more detail in Section 2.3. This term must be stable before ANENB goes true, but since RA is true about 18 uSec before DEV REQ becomes true, the Wire-Wrap board logic will have set HI/LO SEL to the proper state.

DEV ACK must be held low during an analog data gathering sequence; a DEV ACK glitch or sustained high DEV ACK will cause false data to be loaded into the 8156 ports.

The ANENB response from the Wire-Wrap board initiates the A/D conversion sequence; the 3-bit multiplex address determined by the HI/LO SEL logic is stored in the A/D Converter's address latches and the A/D converter sequencing circuitry initiates a 250 uSec time delay that enables the analog signal to settle in the analog multiplexers, Instrumentation Amplifier and Sample/Hold Amplifier. At the end of this 250 uSec period, the Sample/Hold Amplifier is set to the Hold mode and the A/D conversion is started.

After a conversion delay of 25 uSec, the converter EOC (End of Conversion signal, BUSY) causes the A/D data to be loaded into 8156 Ports A and B via the CON/MON bus and signals the firmware that the conversion has been completed. The firmware inputs the digital data and outputs it to the Controller as MDH and MDL on the RCV line.

The paragraphs above briefly describe operation of the Burr-Brown SDM-854 Muliplexer-A/D Converter. For a more complete description of this Multiplexer-S/H-A/D Converter, see VLBA Technical Report No. 12.

Reading the Device ID Code Value

The SIB must be able to relate the addresses of XMT bus messages to its assigned address block. Messages with addresses inside the block must be executed; messages outside the block are to be ignored. To identify messages addressed to the SIB, incoming message addresses are compared with the block starting address (in the 8032 2N+1 address) and block length (in the 8032 2N RAM address) values.

The board does not have internal address assignment logic; this function is performed by the Wire-Wrap board logic and Controller. When the board emerges from the power-on reset, 8032 initialization firmware sets the address block to 7FF0H through 7FFFH. After this initial assignment, the board reads the unique ID byte from the Wire-Wrap board ID logic on the lower byte of the CON/MON bus. The ID byte value (N), is used to establish the F117's addresses. At a later time the Controller (i.e., the Station Computer) will send a control message that will contain the Block Size value which the 8032 stores in the RAM 2N address. The Controller will then send a second control message that will contain the Block Start Address which the 8032 stores in the RAM 2N+1 address. Monitor data requests to these addresses will return the assigned values.

During the ID byte read process, the A/D converter digital outputs are disconnected and the Wire-Wrap board logic does not assert monitor data on the CON/MON bus. R/W- sets the 74LS245 bus driver to the input mode and the driver outputs are enabled which permits the Wire-Wrap board to assert the Block ID code on the CON/MON bus. The Block ID code is loaded into the 8156 A and B Ports. To read the ID byte, the 8032 firmware sets 8032 port P1.5 (ID REQ) low; this causes the Wire-Wrap board logic to assert the seven-bit ID byte on CON/MON lines 0 through 6. The Wire-Wrap board logic also sets a parity bit on CON/MON-7 so that CON/MON 0 .. 7 has odd parity. The Wire-Wrap board leaves the upper byte (i.e. CON/MON 8 .. 15) floating which makes the upper byte value indeterminate.

Note that in reading the ID Code value, only the ID REQ, R/W- and CMD/MON lines are active; DEV REQ is held low. R/W- is high to enable the ID Code value to be input to the 8156. The RA lines remain at the state used for the previous command or data request message. The Device logic must not activate DEV ACK, ANENB or assert monitor data on the CMD/MON bus.

The ID code is input from the 8156 A and B ports in the simple input mode described in Section 2.2 of VLBA Technical Report No. 12.

Periodically thereafter, a 5-second firmware timer causes the 8032 to re-read the ID byte to insure that the stored value is correct.

Interface-Device Timing

These paragraphs describe the SIB - device timing that is depicted in Figure 6 (next page). The three types of SIB - device message timing operations are shown. The firmware operations are identical for the execution of data request messages for digital and analog data but the board circuitry operations are quite different. Both cases are shown in the figure. Device non-response conditions are also shown.

To simplify the figure, the timing diagrams are not drawn to scale.

The most important term in these timing signals is DEV REQ which the device logic uses to enable device logic operations. DEV REQ goes true many microseconds after RA and R/W- are set and is cleared many microseconds before R/W- is reset. The device logic can use microprocessors and hard-wired digital logic because of the very large timing margins.

The interface timing is primarily determined by the control firmware described in VLBA Technical Report No. 12.

The operation of the 8755 and 8156 I/O ports are fully described in this VLBA Technical Report.

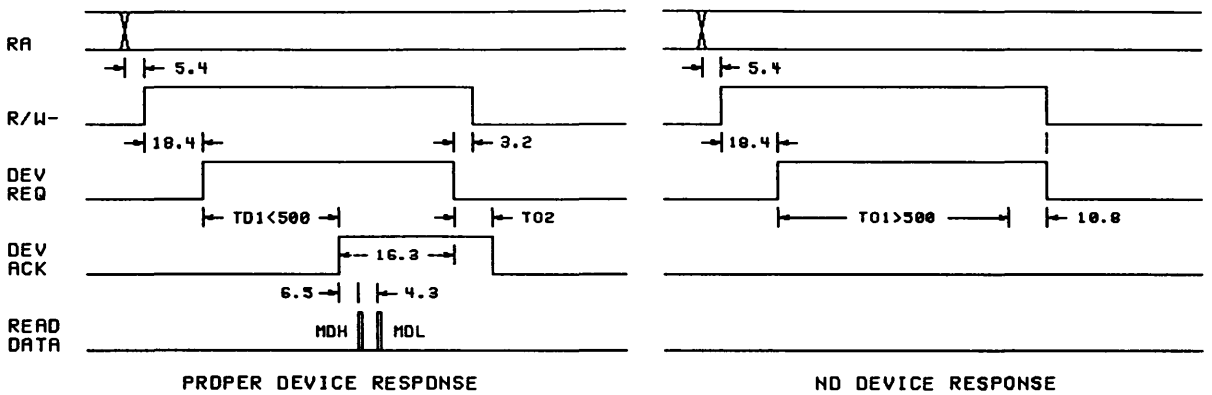
Note that RA remains set at the message value until the next message is serviced. The quiescent (i.e. between messages) state for R/W- is low.

Two device logic response times are shown: TD1 and TD2. TD1 is the DEV ACK or ANENB response time when the DEV ACK line goes true. The firmware permits device responses within 500 microseconds; the device is considered non-responsive if TD1 exceeds this period. TD2 is the device logic response time when DEV REQ returns low.

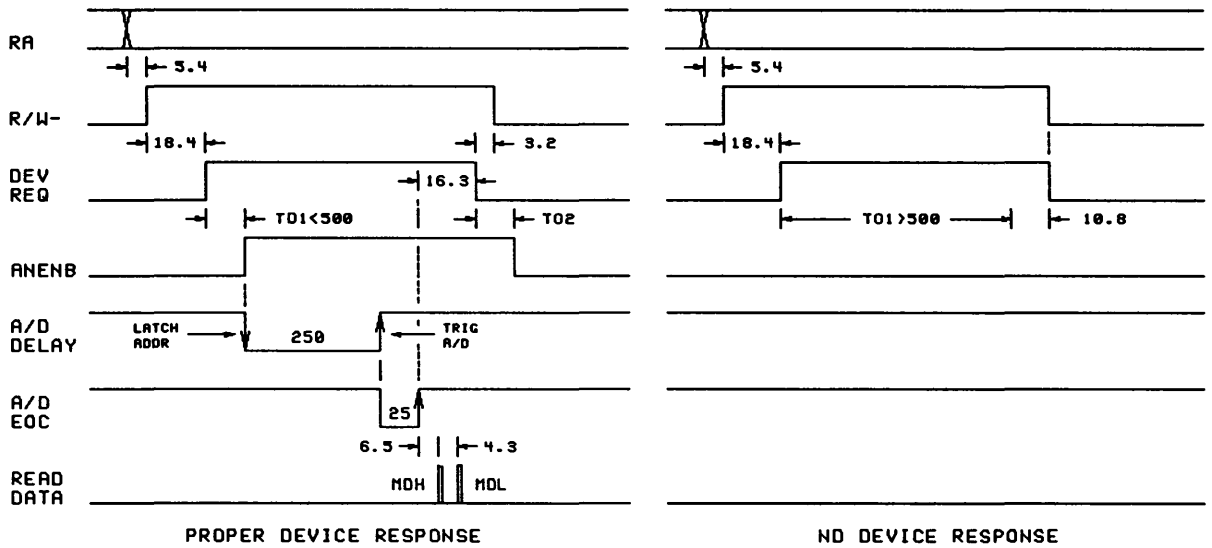
The ID code read operation is not shown on Figure 6 because it is very simple and does not involve handshaking. The ID value is sampled twice by the firmware and the total period for the Device ID code read operation is about 6.5 microseconds. For the first sample, the device logic must assert the ID value upon the CON/MON bus within approximately 2 microseconds after the interface drops the ID REQ line low. The second sample is taken about 2 microseconds after the first sample. Two microseconds are many times greater than the typical TTL device ID logic response time. The device logic should disconnect the ID Code drivers within a few microseconds after the ID REQ line returns high.

Standard Interface Board Power Reset

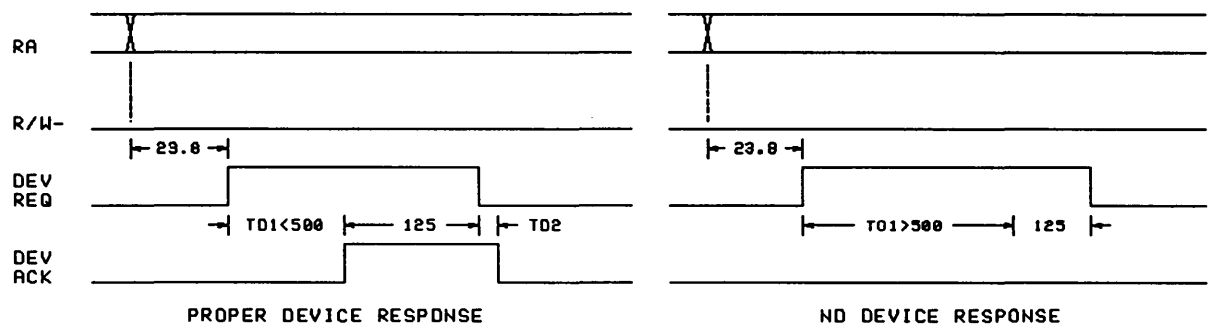
A power-on reset circuit generates a 75 mS reset pulse which initializes the 8032, 8156 and 8755. This circuit is identical to that used on the Wire-Wrap board. Section 2.3 describes the operation of this circuit.



DATA REQUEST MESSAGE EXECUTION TIMING - DIGITAL DATA



DATA REQUEST MESSAGE EXECUTION TIMING - ANALOG DATA



CONTROL MESSAGE EXECUTION TIMING

NOTES:

1. TIME IN MICROSECONDS
2. NOT TO SCALE
3. TD1 AND TD2 ARE DEVICE LOGIC RESPONSE TIMES

FIGURE 6, SIB - DEVICE LOGIC TIMING DIAGRAM

2.3 WIRE-WRAP BOARD CIRCUITRY DESCRIPTION

In this section, we first consider the F117 Command and Monitor functions. This is followed by a description of the circuits that implement these functions. During the following description, the reader should refer to Schematic diagrams D53510S004 and C53510S003. The first drawing is newer and has a more detailed representation of the circuit components.

Address Assignments

Address (ADDR0, .. ADDR5) state determines all operations performed by the Wire-Wrap board circuitry. Addresses 00H through 1FH are assigned to analog multiplexing and A/D conversion. Addresses 20H through 24H are assigned to command and digital monitor functions.

The state of ADDR5 determines whether a command-digital monitor function or an analog multiplexing function is to be performed.

ADDR5 is low (false) for addresses 00H through 1FH. This state disables DEV ACK and enables the ANENB signal to the SIB to cause the SIB analog multiplexer-A/D converter to convert the multiplexed analog signal selected by the ADDR0, ... ADDR4 address terms. The analog multiplexer functions are described below.

ADDR5 is true (high) for addresses 20H through 24H. This state enables decoder 1D (for addresses 20H, ... 23H) and the gate 1CB decoder (for address 24H). These enables permit the command and digital monitor data registers to be accessed by the SIB. The command and digital monitor data functions are described below.

Address Decode Logic

The command and digital monitor functions are selected by address enables from two sets of address decoders: 74LS138 decoder 1D generates enables 20H through 23H and a Gate Decoder (gates 1A-1C with 1B inverters) generates enable 24H. These enables are used to load commands or read digital monitor values.

Interface logic interactions are initiated by the SIB DEV REQ term when it goes high-true. For this reason, the Address Decode logic on the Wire-Wrap board is qualified by the DEV REQ term. When DEV REQ returns low after a command or monitor data transfer, the address enables all return false (high).

R/W(L) is used on the C input of the 74LS138 to produce command enables when low (i.e., Write Mode) and monitor enables when high (i.e., Read Mode). The Command Echo Monitor Enable addresses are identical to the associated command addresses but are output on different decoder outputs. This is accomplished by using R/W(L) to translate the 74LS138 decode logic by four counts. When R/W(L) is low (Write), command enables Y0 and Y1 are generated for the corresponding A0 and A1 address states. When R/W(L) is high (Read) outputs Y4 through Y7 produce monitor enables for the corresponding A0 and A1 states. The state table for this decoding logic is shown on the next page.

Decoder 1D (74LS138) Inputs and Outputs								Gate 1A-1C Decoder	
Decoder Inputs		Decoder Outputs						Signal	State
Signal	Decoder Input	Y0	Y2	Y4	Y5	Y6	Y7		
A0	A	0	0	0	1	0	1	A0	NU
A1	B	0	1	0	0	1	1	A1	NU
R/W(L)	C	0	0	1	1	1	1	R/W(L)	NU
DEV REQ	G1	1	1	1	1	1	1	DEV REQ	1
A2	G2A	0	0	0	0	0	0	A2	1
A5(L)	G2B	0	0	0	0	0	0	A5	1
Enable outputs (Low-True)		20H Cryo Cmd	22H Cal Cmd	20H Cryo Mon	21H RCVR Discr Mon	22H Cal Mon	23H Status Codes Mon		24H F117 S/N Mon

In the gate decoder table above, NU indicates that the A0, A1 and R/W(L) terms are not used in the gate decode logic.

These decoder enables are low true during the time that DEV REQ is true. When the DEV ACK from the Wire-Wrap board goes true (about 20 nS after DEV REQ goes high), the SIB lowers DEV REQ after a firmware delay of about 500 uSec. The trailing (i.e., rising) edge of these enables clock the 8-bit command argument into the command registers 3A and 3B.

In the case of readout of monitor data registers, the low-true enable holds the latches at the state of the "D" inputs at the time that the enable goes low.

Command Registers and Functions

The F117 has two command functions: Front-End Cryogenic control and Front-End Calibration control. Two (3A - Cryo Cmd and 3B - Cal Cmd) eight-bit 74LS273 Octal D registers are loaded with the state of the lower eight bits of the CON/MON bus (C/M0, ... C/M7). The upper eight bits of the CON/MON bus command argument (e.g., C/M8, ... C/M15) are not stored by the F117.

The state on the Register "D" inputs (i.e., C/M0, ... C/M7) is loaded into the addressed register when the clock input rises from a low. The register clocking term is the low-true output of an address decoder 1D, a 74LS138 which has DEV REQ on the G1 input. When gate 1AA outputs DEV ACK to the SIB, control firmware forces DEV REQ low which disables the encoder; the selected output then rises which clocks the CON/MON bus state into the selected register. The operation of the Address Decode logic is described above.

The DEV ACK feedback to the SIB is qualified by the ADDR5 term in gate 1AA. If ADDR5 is true (high), a command or digital monitor data operation is to be performed and gate 1AA returns a DEV ACK response from the Wire-Wrap logic. The Wire-Wrap board must return DEV ACK within 500uSec after DEV REQ becomes true; if not, the SIB assumes the Wire-Wrap command circuitry is non-responsive and signals a DC2 on the RCV line. The Wire-Wrap board DEV ACK response time is about 20 nS; after a firmware delay of a few uSec, the SIB lowers DEV REQ. The Wire-Wrap board analog response ANENB is inhibited by the true state of ADDR5.

The two command registers are cleared to the zero state by the Power Reset circuit which imposes a 100 mS, low-true clear pulse on the 74LS273 Clear inputs.

The three **Cryogenic Command** bits are H(L), C and X and are the three least-significant bits in the eight-bit value. H(L) is bit 0 (LSB). The upper five bits have not been assigned a control function.

These three Cryo Command bits are output to the Front-End on J2. The resultant Front-End Cryo control states are tabulated below. The Front-End Cryo functions were described in Section 1.

Front-End Cryogenics Control State Table

Register Bit	2	1	0 (LSB)	
Bit Function	X	C	H(L)	
CRYO OFF	1	0	1	No refrigerator power, heater power, or vacuum pumping.
COOL	1	1	1	Normal cooled operation.
STRESS	1	0	0	COOL with small added heat to stress-test cryogenics.
HEAT	1	1	0	Fast warm-up of dewar, 65 Watts of heater power.
PUMP	0	1	0	No refrigerator or heater power.
STRESS*	0	0	0	Reset state of the Cryogenics Control Register

The **Front-End Calibration Command** uses the four least-significant bits to control the receive calibration drive circuitry. The four bits are: LO SW, LO CONT, HI SW and HI CONT and LO SW is the least significant bit. The functions performed by these four control bits are described below.

Digital Monitor Registers

The Digital Monitor Data Registers are 74LS373 transparent octal edge-triggered D latches with tri-state outputs. When selected, registers 2A, 2B, 5E, 2E and 5D assert an eight-bit value on the lower eight bits of the CON/MON bus (i.e., C/M0, ... C/M7). Sixteen-bit register 2C-2D asserts a sixteen-bit value on the whole CON/MON bus (i.e., C/M0, ... C/M15) when selected.

When the 74LS373 Gate inputs are high, the flip-flop Q outputs follow the D inputs. When the Gate input is dropped low, the Q outputs are latched at the state of the D inputs at the time the Gate input is dropped. The register Gate inputs are driven by the low-true address enables of the address decode logic described above.

The 74LS373 Q outputs drive the tri-state CON/MON bus if the Output Enable (OE) input is low. The decoder enables drive both the Gate and Output Enable inputs. This performs two functions: the low level holds the Q outputs static as described above and enables them to drive the tri-state CON/MON bus.

The decoder enables (e.g., 20H, 21H, 22H, 23H and 24H) are low-true during the time that DEV REQ is true (high). When the DEV ACK from the Wire-Wrap board goes true (about 20 nS after DEV REQ goes high), the SIB samples the monitor data state on the CON/MON bus and lowers DEV REQ after a firmware delay of several uSec.

The addresses and formats of the Digital Monitor Data are tabulated on the next page. For convenience, the Block ID Code format (described below) is included in the table.

Digital Monitor Data Formats

	MSB															LSB
Register Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cryo Mon, 20H	NU	NU	NU	NU	NU	NU	NU	NU	CS	CS	CS	CS	CS	X	C	H(L)
Cal Mon, 22H	NU	NU	NU	MU	NU	NU	NU	NU	CS	CS	CS	CS	HC	HS	LC	LS
RCVR S/N, Mod & Freq Mon, 23H	1	1	S5	S4	S3	S2	S1	S0	1	1	M1	M0	F3	F2	F1	F0
RCVR Discr Mon, 21H	NU	NU	NU	NU	NU	NU	NU	NU	I	I	S	P	M	XM	CM	HM
F117 S/N Mon, 24H	NU	NU	NU	NU	NU	NU	NU	NU	SN7	SN6	SN5	SN4	SN3	SN2	SN2	SN0
Block ID Code (no address)	NU	NU	NU	NU	NU	NU	NU	NU	P	0	0	0	F3	F2	F1	F0

Notes: NU denotes Not Used, state indeterminate. CS's in Cryo and Cal Mon are the state commanded by the Front-End control software for these unassigned control bits. I denotes a floating register input, indeterminate state. The XM, CM and HM bits are the X, C and H(L) Front-End cryo state monitor bits. M is the M(L), Front-End manual control mode monitor bit. See the Front-End Description in Section 1 for a description of the X, C, H(L) Front-End control and the S, P and M(L) Front-End state monitor bits.

Analog Signal Multiplexing

The F117 uses seven of the eight available SIB analog multiplexer inputs; ANLG0 is not used. The F117 analog signals are multiplexed by a combination of SIB multiplexers, a Wire-Wrap board sixteen-channel multiplexer and an external eight-channel multiplexer. The selected analog signals are converted to digital values by the SIB A/D Converter and output as monitor data on the RCV line.

Four analog signals from the Wire-Wrap board are connected to SIB inputs ANLG4,...ANLG7. The external multiplexer (in F118 when used with F117) is connected to SIB input ANLG3. The sixteen channel analog multiplexer is connected to SIB inputs ANLG1 and ANLG2 and samples Front-End analog signals and two F117 reference voltages.

The Wire-Wrap board mulitplexer (4A) is a Harris HI-506A, a sixteen-channel, single-ended analog multiplexer. This input-protected multiplexer features active over-voltage protection, ESD resistance, break-before-make switching, 1.5 kOhm (typical) channel-on resistance and an output leakage current of 0.1 nA (typical, at 25° C). The HI-506A address line inputs (A0, ... A3 and Enable) require a logic high level greater than +4 volts; 1.5 kOhm pull-up resistors to V_{CC} provide this high logic level. Section 5 contains a data sheet for the HI-506A.

The sixteen channel multiplexer output is connected to the signal-high inputs (i.e., ANLG1+ and ANLG2+) of the SIB ANLG1 and ANLG2 inputs. The low side of all seven of the ANLG1, ... ANLG7 inputs are connected to analog ground at the SIB P1 connector inputs (See Wiring Diagram D53510W010). ANLG0 inputs are floating.

The SIB analog address multiplexer HI/LO SEL input is a multiplexer mode control term that is a function of the multiplexer address. OR gate 1CA, driven by ADDR3 and ADDR4, has a high output if either input is high. The usage of this term in the Wire-Wrap board multiplexer is described below. (The typical usage of HI/LO SEL is described in Section 2.2).

Note that the first operative address for the HI-506A multiplexer is 08H which selects input I9. The next seven consecutive addresses (09H, ... 0FH) select inputs I10, ... I16, respectively. Correspondingly, address 10H selects input I1 and the next seven consecutive addresses (11H, ... 17H) select inputs I2, ... I7, respectively.

The ANENB feedback to the SIB is dependant upon the state of ADDR5. For the analog data multiplexing address range, (00H, ... 1FH, ADDR5 low), ANENB is true when qualified by DEV REQ. The ANENB response from the Wire-Wrap board is used to initiate the SIB analog multiplexing and A/D Converter operations. Note that when ADDR5 is false, the DEV ACK feedback to the SIB is inhibited.

The Analog Monitor Data address space, HI/LO SEL, ANLG inputs and multiplexed signals are tabulated on the next page. Note that when either ADDR3 or ADDR4 is a 1, HI/LO SEL (from gate 1CA) is a 1 which causes the SIB analog multiplexer to be driven by ADDR5, ADDR4 and ADDR3. In this condition, the multiplexers connected to ANLG1, ANLG2 and ANLG3 are driven by ADDR2, ADDR1 and ADDR0. This HI/LO SEL scheme constrains the analog address space to 20H addresses for a multiplexer channel capacity of 1FH (31 Decimal). Three spare channels are available in the F117: ANLG0, HI-506A inputs I15 and I16 - addresses 00H, 0EH and 0FH, respectively.

Analog Multiplexer Addresses and Signals

Addr, Hex	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	ANLG Input	HI/LO SEL	Selected Signal
00	0	0	0	0	0	0	0	0	NU
-	-	-	-	-	-	-	1	-	HI-H06A Mux,
-	-	-	-	-	-	-	2	-	see below
03	0	0	0	0	1	1	3	0	Ext Mux
04	0	0	0	1	0	0	4	0	Low Cal Current
05	0	0	0	1	0	1	5	0	HI Cal Current
06	0	0	0	1	1	0	6	0	Low Cal Voltage/4
07	0	0	0	1	1	1	7	0	HI Cal Voltage/4
08	0	0	1	0	0	0	1	1	VP
09	0	0	1	0	0	1	1	1	ACI
0A	0	0	1	0	1	0	1	1	LED
0B	0	0	1	0	1	1	1	1	SENS
0C	0	0	1	1	0	0	1	1	+7.5 Ref
0D	0	0	1	1	0	1	1	1	An Gnd
0E	0	0	1	1	1	0	1	1	NU
0F	0	0	1	1	1	1	1	1	NU
10	0	1	0	0	0	0	2	1	LF1
11	0	1	0	0	0	1	2	1	RF1
12	0	1	0	0	1	0	2	1	LF2
13	0	1	0	0	1	1	2	1	RF2
14	0	1	0	1	0	0	2	1	15K
15	0	1	0	1	0	1	2	1	50K
16	0	1	0	1	1	0	2	1	300K
17	0	1	0	1	1	1	2	1	VD
18	0	1	1	0	0	0	3	1	External Mux Signal
19	0	1	1	0	0	1	3	1	" " "
1A	0	1	1	0	1	0	3	1	" " "
1B	0	1	1	0	1	1	3	1	" " "
1C	0	1	1	1	0	0	3	1	" " "
1D	0	1	1	1	0	1	3	1	" " "
1E	0	1	1	1	1	0	3	1	" " "
1F	0	1	1	1	1	1	3	1	" " "

Notes: NU denotes an unused analog input. The dashes indicate a "doesn't apply" case.

Calibration Switching Logic

The four Calibration control bits from the Calibration Command register are: LO SW, LO CONT, HI SW and HI CONT. LO SW is the least significant bit. Two sets of AND-OR gates drive the Cal and High Cal Drive circuitry (described below). These two sets of logic are independent of each other. The

state table of the Cal Switching logic is shown below.

Front-End Calibration Control State Table

Register Bit	3	2	1	0 (LSB)		
Bit Function	HI CONT	HI SW	LO CONT	LO SW	Hex Code	Cal State
Cals off	0	0	0	0	0	No drive to either noise source
High continuous	1	X	0	0	8	High (only) continuous noise source drive
Low continuous	0	0	1	X	2	Low (only) continuous noise source drive
Both continuous	1	X	1	X	9	Both noise sources on continuously
** High auto	0	1	0	0	4	80 Hz drive to High (only) noise source
* Low auto	0	0	0	1	1	80 Hz drive to Low (only) noise source
Both auto	0	1	0	1	5	80 Hz drive to both noise sources

** is the usual Solar observing condition. * is the usual Normal observing condition. X denotes a "don't care" state. The Hex code is the Calibration Monitor readout value with logic 0's for the "don't care" bits.

Although there are many additional possible states for this table, the Front-End calibration drive software in the Antenna control computer only activates the states shown above.

A continuous cal command state causes a continuous (i.e., non-switching) drive to the noise source diodes. The auto states cause the 80 Hz signal from L108 to drive the noise sources when it is a logic 1 (high).

Since gates 1CC and 1CD are OR gates, the switching drive from gates 1AD and 1AC are "don't care" inputs to the OR gates if either continuous bit is true (i.e., high). Note that there are no logic inversions through these gates.

The output of the Calibration Switching Logic drives the Calibration Drive circuitry described below.

Calibration Drive Circuitry

The calibration drive circuits consist of two sets of two-stage, direct-coupled, NPN-PNP transistor driver amplifiers that source current from the +28 Volt supply to the noise sources through 1 Ohm current measuring resistors installed on terminals 5-12 and 3-14 of dip header 3G. The four transistors are a Sprague TPQ6502 Quad transistor array that consists of two NPN and two PNP transistors. These transistors are similar to the 2N2222 (NPN) and 2N2907 (PNP) transistors. Data sheets for these devices are included in Section 5.

Noise source drive current is turned on when the 74LS32 (1CC and 1CD) outputs are high (approximately +3.4 Volts). When the gate outputs are high, the driver circuit first stage (NPN1 and NPN2) receive a base drive current of about 0.15 mA which drives it into saturation. The resultant emitter current is about 7.5 mA. The collector-current drop across the NPN stage 1000 Ohm resistor heavily forward-biases (about -7.5 volts, Base-to-Emitter) the PNP stage so that the Emitter-Collector drop is very small, typically less than 0.10 Volts at a noise current drive of 50 mA.

When the 74LS32 outputs are low (about +0.25 Volts), the NPN stage is cut off because the +0.25 Volt level is below the (about) +0.6 volt base-emitter forward bias level. Since the NPN stage is cut off, the PNP base is also cut off because the PNP base drive current is zero; that is, both the base and emitter are at +28 Volts.

Calibration Current and Drive Voltage Monitor Circuitry

Referring to the amplifier circuit on the Wire-Wrap board schematic, note that noise source drive current is measured by two LF442A differential operational amplifiers. The amplifier difference signal inputs are the voltage drop across 1 Ohm (R_D) series resistors when the noise source is being driven. There are two divide-by-three voltage dividers to ground on each side of R_D and the amplifier's + and - (positive and negative) inputs are connected to the junctions of the 10 K and 4870 Ohm resistors. When the 28 Volt noise source drive is on, these two points are about +9.2 Volts above ground; thus the LF442A amplifier's inputs have a common mode voltage of +9.2 Volts. This is not a problem because the LF442 can operate with common-mode inputs as high as +18 and -17 Volts and has a typical Common Mode Rejection Ratio of 100 dB (with a source impedance < 10 Ohms). The current flow into each divider circuit is about 28 Volts/15 kOhms or about 1.8 mA. The LF442A input impedance is greater than 10^{12} Ohms and input bias and offset currents are a few picoAmps at room temperature; therefore, the amplifier's output voltage is a simple function of the **current difference** in the two divider circuits. The two current monitor outputs are conected to the SIB ANLG 4+ and ANLG 5+ inputs (addresses 04H and 05H).

When there is a current flow through resistor R_D, the input to the divider connected to the amplifier - input is reduced by $I_{ND}R_D$ Volts. The amplifier output swings positively to produce a current through the 100 kOhm feedback resistor to null the amplifier's error input. Since the feedback resistor is 100 kOhm (the divider current comes through a 10 kOhm resistor), the output voltage must swing ten times the voltage drop across R_D to drive an equivalent current into the amplifier's - input node. Another way of stating this is to note that the amplifier has a gain of 10: $R_{FB}/R_{INPUT} = 10$.

Since R_D is 1 Ohm, the current-voltage scaling of this amplifier is 100 mA/Volt. To obtain the value of noise source current, multiply the amplifier output voltage by 100 mA/Volt.

The - (negative) input divider has a 200 Ohm zero-adjustment pot to set the amplifier output to zero volts with the noise source voltage drive on but no load current.

Section 5 has a data sheet for the LF442A amplifier.

The noise source drive voltage is monitored by a 40 kOhm, 4:1 voltage divider connected to the output side of R_D. The divider output is thus +7.00 Volts when the drive is active. (Note that the 0.7 mA current into this divider goes through the 1 Ohm resistor; thus the amplifier's input difference includes the effect of this current. The divider outputs are connected to the SIB ANLG 6+ and ANLG 7+ inputs (addresses 06H and 07H).

In checking these monitor values when the antenna is observing, it is important to remember that the calibration circuitry is normally in the auto mode; values read in this mode will vary because the data sampling time and switching signal are not concurrent. Correct values may be read by setting the calibration command to the continuous-on states shown in the table above.

Calibration Drive Inhibit Circuitry

A drive inhibit circuit protects the noise sources from excess current drive. Two LM393A analog comparators force the drive to the NPN-PNP driver circuit (described above) to ground if the output of the current monitor circuit (described above) exceeds +1.9 volts. This level is determined by the tap on the R53-R54 voltage divider connected to the + (plus) inputs of the LM393A's.

When an analog comparator's + (plus, noninverting) input is more positive than the - (minus) input, the output is positive (high) and when the + input is more negative than the - input, the output

is negative (low). Typically, only a few millivolts are required to cause the switching transitions because an analog comparator is essentially a high-gain operational amplifier without feedback.

In the inhibit circuit, the - input is connected to the current monitor amplifier's output and the + input is connected to the +1.9 Volt tap on the voltage divider. When the voltage from the current monitor is less than +1.9 Volts, the comparator output is high; this enables the driver circuit to output current to the noise sources. If the voltage from the noise source monitor circuit exceeds the +1.9 Volt level, the comparator output drops to ground. This inhibits the driver circuits because the 74LS32 base drive current for the NPN1 and NPN2 transitors is diverted to ground.

The LM393A comparator has an open-collector output; when high, it assumes the level of the NPN-PNP transistor driver circuit input. When low, the level is about 10 mVolts when sinking the 0.15 mA drive from the 74LS32 gate. This low level imposes a hard limit on the input to the NPN-PNP transistor driver circuit.

Section 5 contains a data sheet for the LM393A.

A 75141 dual, single-ended line Front-End is used to detect the 80 Hz Mod signal from L108. This Front-End can function as a level comparator by connecting the Common Reference input to a reference voltage, in this case the +1.9 Volts used by the inhibit circuitry described above. +1.9 volts is slightly less than the typical 74LS 2 Volt V_{IH}. The 75141 output is inverted relative to the input; if the MOD signal is high (and 100 mV above +1.9 Volts), the output is low and the cal switching logic outputs are low (if set to the switching mode). If the Mod signal is about 100 mV less than +1.9 V, the output is high and the switching logic output is also high. The 75141 outputs are TTL-compatible.

Section 5 contains a data sheet for the 75141.

Device ID Code Register

Register 5E, a 74LS373 octal latch, performs the function of asserting the Block ID code on the lower eight bits of the CON/MON bus when the ID REQ line from the SIB drops low. The Block ID code bits are the Front-End Band Code (bits F3, .. F0) and the even parity bit PA(L) (shown as P in the table above) and are stored in the register Q outputs when the ID REQ line is high. Three of the eight bits are set to logic 0's and Inverter 1BB makes the parity odd as required by the MCB specifications. The usage of the Block ID code was described in the MCB description above.

Power Reset Circuitry

A power reset circuit clears the command registers when +5 Volt power is applied to the module. The circuit is identical to that used on the SIB and uses a 74LS221 Schmidt input one-shot. When power is applied, the 22 uF capacitor charges to +5 Volts through the 1 kOhm resistor; the one-shot triggers when the capacitor voltage reaches the B input 1 Volt (typical) threshold. The time delay to the trigger threshold is about 32 ms (assuming that the 5-Volt power is a step). The 74LS221 triggers reliably on input signals having slopes as low as 1 Volt/second. A dV/dt, this low permits the RC delay circuit to have a large time constant so that a long delay is realized after power is applied. The one-shot delay time is about 100 ms which clears the two 74LS273 command registers. The diode across the charging resistor protects the one-shot input from being forced to -5 Volts by the charged capacitor when the power is removed.

Module Serial Number Register Encoding

The F117 module serial number is read from register 5D, a 74LS373 transparent octal latch. The register loading process was described above. When the module is manufactured, a high-true binary module serial number code is wired onto the Wire-Wrap connector pins. 1's code bits are set by connecting the associated pins to +5 Volts on pin W28. 0's code bits are set by connecting the associated pins to logic common on pin W27.

7.5 Volt Reference

Two reference voltages connected to inputs on the 16-channel analog multiplexer provide a means of checking the SIB analog multiplexer and A/D Converter gain and zero drift. These two voltages are analog common and +7.5 Volts. The +7.5 Volt reference is provided by an Analog Devices AD584JH pin-programmable voltage reference installed on a transistor adaptor at location 3C. AD584 pins 1 and 2 are jumpered to program a +7.5 Volt output. The maximum error of this output over the 0 to 70° C temperature range is +/- 30 mV. Section 5 contains a data sheet for the AD584.

3.0 BENCH TEST AND ALIGNMENT

This section describes the F117 Bench Test and Alignment system used at the AOC Front-End Laboratory; this is the primary maintenance and alignment facility for the F117 module. The system consists of the Test Environment, the Test Fixture and the the Test Program.

F117 Test Environment

The Test Environment simulates the F117 operating environment and consists of an IBM-compatible PC to execute the test program, an RS-232/RS-485 line signal converter to adapt the PC's RS-232 serial I/O levels to the SIB's RS-485 levels, the F117 Loop-Back Unit for both digital and analog simulation and +5, +/-15 and +28 Volt power supplies. The F117 Test Environment is depicted on Figure 7 (this page).

F117 Test Fixture

The F117 Loop Back Unit schematic diagram is drawing C53510S005 and the assembly drawing is C53510A007. This test fixture has two cables that terminate in 25-contact "D" connectors that are plugged into F117 front panel connectors J1 (Front-End monitor) and J2 (Front-End control). A single wire from the Loop Back unit (RTP7, X Cmd) connects to the F117 module rear panel (J11- 12, MOD signal input). Under test program control, this X command simulates the MOD calibration switching command to the F117. The Loop Back unit's circuitry is powered by + and - 15 volts from J2, the Front-End control connector.

The F117 Loop Back unit's stimulus inputs are the F117's three multiplexer address lines (ADDR0, ADDR1, ADDR2) and the three Front-End cryogenic control bits X, C and H(L). (H is used to designate H(L) in the following discussion.) These six signals exercise the F117 Loop Back unit circuitry.

The Loop Back provides Front-End Band Code and Parity Bit (even), hard-wired to logic common; this designates a Block IDN code (N in SIB terminology) of 0 which designates an FE101 (75 MHz) Front-End. (See the table of Band Codes in Section 1.0 and the Block IDN code format in Section 2.3. Schematic Diagram D53510S004 depicts the F117's Band Code and Block IDN logic circuitry.)

The state of X (one of the three cryogenic control bits) controls the selection of the analog signal level input to the Front-End analog inputs on J1. When X is a "1" (high), zero volts are input to all analog inputs via unity-gain buffers; when X is a "0", +8.3 volts are input to the analog inputs. The external analog multiplexr, ANLG3 (also on J1) is also driven by the X-controlled zero and +8.3 volts. As noted above, X is also fed back to the F117 module MOD input to simulate the MOD signal for the Cal Switching tests.

The X, C and H cryogenic control bits are also connected to the X Mon, C Mon and H Mon

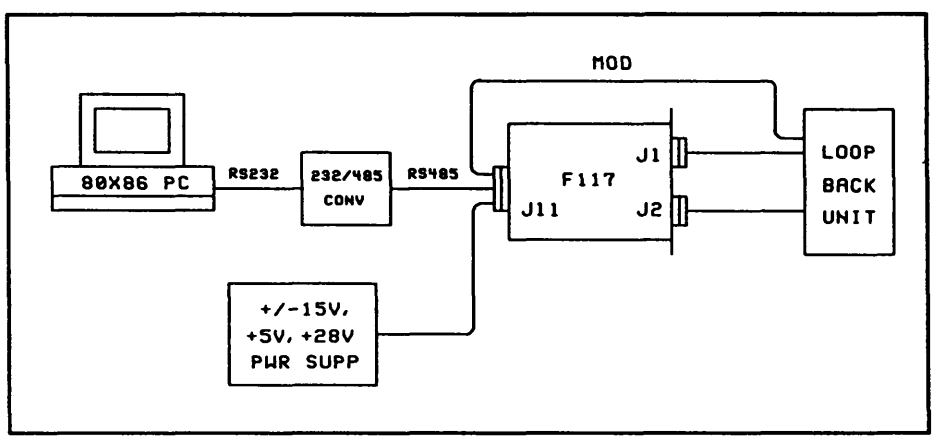


Figure 7, F117 Test Environment

inputs to simulate these three Front-End state discretes.

The inverse of the states of the C and H bits are connected to the Front-End Serial Number and Modification Level inputs on J2. The truth table for these inputs as a function of the C and H bits is shown below.

Cmd Bits		Front-End Serial Number Code Bits						Rcvr Code, Hex	Mod Lvl Bits		Mod Lvl, Hex
C	H	S5	S4	S3	S2	S1	S0		M1	M0	
0	0	1	1	1	1	1	1	3F	1	1	3
0	1	1	0	1	0	1	0	2A	1	0	2
1	0	0	1	0	1	0	1	15	0	1	1
1	1	0	0	0	0	0	0	00	0	0	0

F117 Multiplex Address bits ADDR0, ADDR1 and ADDR2 are connected to the J1 Front-End control and status monitor discretes M Mon (Front-End Control in Manual Control Mode), P (Pump Request) and S (Vacuum Solenoid Monitor), respectively.

Resistors 1 and 2 (R1 and R2, both 1000 Ohms, 2 Watt) are loads for the High Calibration and Calibration drive circuitry in J117.

F117 Test Program

The following text is a narrative description of the operations performed by the F117 test progam in exercising an F117 connected to the F117 Loop Back Unit or the F117 connected to a Front-End for Front-End monitoring (described below). Since the text emphasis is on a description of the test functions, it is too long and detailed to be a convenient test procedure although it does include some operator-program interactions. During the course of program execution, several CRT dislays show the states of the F117 tests or Front-End being monitored. The text includes samples that were printed by the test systen.

Secondly, it is **not** a description of the program or its mechanics but there are some program references. For example, the notation Page 5B refers to an operation performed on the bottom of Page 5 in the source code listing (in Section 6). Some variables such as MONCHAR$(XX, Z), constants like &HF0 or a flag like FLAGER3 are mentioned where it seems appropriate to do so. Although this text is not a program description, it may be a useful reference for modifications to the program or an adaptation of some elements of the program to another test application involving the SIB.

The F117 test program is F117.EXE and the source code is F117_2.BAS (described below). The program's initial operation is a test of the SIB; if problems are detected, the SIB board should be replaced. If the SIB passes these initial tests, the program proceeds to perform a comprehensive functional test of the F117 module.

The F117_2.BAS Test Program is written in Microsoft Basic and then compiled to F117.EXE. The program description is based upon the February 1, 1993 version but there may be future changes to implement more extensive analyses of the F117's or Front-End's performance.

The program may be run from the DOS root directory by typing F117 followed by ENTER.

The test program has three operating modes: 1) The **Auto-Loop** mode in which test program functions proceed automatically and provide a go/no-go test result at the completion of the test. 2) The **Man-Loop** mode performs the same test operations as 1) above, but there are pauses at important points in the program to permit direct manual measurements of F117 states; the test sequence may be resumed after the pauses. In the Auto-Loop mode, failure of certain tests forces a transition to the Man-Loop

mode to enable the operator to make manual F117 adjustments or measurements. It is not possible to make a transition from the Man-Loop mode to the Auto-Loop mode. 3) The **Front-End Monitor** mode in which a Front-End (instead of the F117 Test Fixture) is connected to the F117's J1 and J2 connectors with 25-conductor cables. The Front-End (not the F117) is the focus of this test mode and a fully-functional F117 is required to avoid ambiguities in the tests. The Front-End's RF inputs are the ambient RF levels of the lab environment; the RF output signals are not tested but the calibration noise sources are powered. The Front-End's Calibration drive and Cryogenic control inputs are exercised and its analog and digital outputs are monitored via the F117 circuitry. This mode provides a convenient way to systematically exercise the Front-End's cryogenics and calibration circuitry, monitor the Front-End's analog and digital signals and trouble-shoot Front-End signal and wiring problems. The Front-End Monitor mode performs the same test operations as 1) above, but permits the operator to enter cryogenic and calibration command states. Once entered, there are no transitions from the Front-End Monitor mode to the other test modes.

The F117 test program is a single entity, not three separate sub-programs; program flow is a function of the operating modes. A third-party serial I/O subroutine is called to control the serial port operations.

In the text below, all operator interactions and test result messages are indicated by **BOLD CAPS TEXT.** The operator interacts with the program execution by inputting manual commands at certain points during the execution when prompted by messages on the CRT. These manual command inputs are all cited in **BOLD CAPS TEXT.** Test result messages and data are also displayed on the CRT as **BOLD CAPS TEXT.** These messages are sometimes single lines, other times a part of a CRT display. Samples of these displays are pictured in the text below.

Before starting the program execution, the **OPERATOR SHOULD TURN OFF THE F117 + 5 AND +/- 15 VOLT POWER SUPPLIES FOR AT LEAST 5 SECONDS.** This permits the SIB power reset circuit capacitors to discharge; when power is reapplied, the power reset circuit initiates a processor reset which activates initialization firmware. The initialization firmware reads the Block IDN value and sets the address block start address and block size parameters to default values. The first operations of the test program evaluate the reset conditions. If the CRT displays the message **"MONCHAR$(number) SUBSCRIPT OUT OF RANGE"**, it indicates that either the SIB power had not been turned off, or the off period was too short or that the SIB initialization is not working.

When the program is started, the CRT displays a box showing: **"VLBA F117 MODULE TEST PROGRAM & FE MONITOR by LDM MAR 92"** followed by **"needs: F117, F117 test box / pwr supply, F117 cables & RS232 cable"**.

The CRT then displays a sequence of four messages that prompt the operator to make the following cable connections; the operator should respond to each of these messages by pressing ENTER. These messages are: **"Connect F117 rear cables to Willy box, press ENTER when ready"**. **"Connect RS232 cables to Willy box & PC, press ENTER when ready"**. **"Connect F117 front jumpers, press ENTER when ready"**. **"Connect ac power to F117 & turn ON, press ENTER when ready"**.

A program control flag, FLAGER3 (evoked from the operator), determines the program's operating mode (described below). This flag is tested at strategic locations in the program and determines the program flow as a function of the operating mode. If the operator FLAGER3 = 1, the Man-Loop mode is specified; if FLAGER3 = 2, the Auto-Loop mode is specified; and finally, if FLAGER3 = 3, the FE Monitor mode is specified. FLAGER3 is input on page 2T (T for Top of page). The CRT displays a mode selection menu in a box which has a **"SELECT"** designator, **"1, 2, 3 or Q"** to be input by the operator to designate the **"F117 MAN LOOP TEST, F117 AUTO LOOP TEST OR FRONT END MONITOR"** modes, respectively. The SELECT value (1, 2 or 3) is FLAGER3 in the program. "Q" designates Quit for stop

program execution.

The operator is next prompted to verify that the cable configuration is correct for the selected mode (Page 2T). In the Man-Loop or Auto-Loop modes, the CRT displays **"BE SURE TO CONNECT FRONT LOOP BACK TEST JUMPER ON F117"** followed by **"PRESS ENTER TO CONTINUE"**. In the FE Monitor mode, the CRT displays **"BE SURE TO CONNECT FE CABLES TO F117"** followed by **"PRESS ENTER TO CONTINUE"**.

Since the SIB is the control-data interface to the F117, it is tested first in all three modes. A delay subroutine, DELAY1 (page 36M) is frequently called to insert time delays in the program execution to provide sufficient time for the serial I/O operations to be completed.

The first operation of the program (common to all three modes) is a readout of the 16 (MDH and MDL) monitor data values stored in the SIB's last 16 data addresses (see the description of these values in Section 2.2) The CRT displays **"PRECHEK MON WORDS"**. This operation begins on page 2M. These values are intialized by the 8032 Microcontroller firmware when the SIB is powered up (mentioned above). Important parameters are N (labelled IDN in the program), the Block IDN Code read from the Device (i.e. F117), the SIB Type and Revision (Version "D", Rev "B") and the Block Start Address. The Block Start Address is initialized to 7FF0H and remains set at this value until set to another value by the MCB Controller (i.e. the Station Computer, in this case the F117 Test System). The Block Size is initialized to 16 to permit these 16 monitor data values to be read out.

For convenience in the following discussion, these initial end-of-block parameters are as follows:

BE-X Addr	EOB AddrH	Function
BE-15	7FF0	Reserved for future use, 7FF0H is the Block Start Address
BE-14	7FF1	" " " "
BE-13	7FF2	" " " "
BE-12	7FF3	No Control Response Counter (i.e., no DEV ACK from Device)
BE-11	7FF4	No Monitor Response Counter (i.e., no DEV ACK or ANENB from Device)
BE-10*	7FF5	Interface Type and Revision Code. For F117 should be D and B (Version D, Rev B)
BE-9	7FF6	Address of most recent control message (i.e., ADH and ADL)
BE-8	7FF7	Control Data for most recent control message (i.e., CDH and CDL)
BE-7	7FF8	Address parity error counter, all messages
BE-6	7FF9	Control data parity error counter, all messages
BE-5	7FFA	Invalid SYN character counter, all messages
BE-4	7FFB	Control Data parity error counter, messages in block
BE-3*	7FFC	IDN (Block ID code value from F117, 0, for F117 Test Fixture)
BE-2	7FFD	Count of correctly received control messages
BE-1	7FFE	Count of correctly received monitor data request messages
BE-0	7FFF	Address of beginning of block (0100H for the F117 test fixture)

* Cannot be altered by the Controller or F117 test program

The monitor data read process stores these data values in the MONCHAR$ array (16 elements, 3 bytes/element, i.e. for ACK, MDH and MDL) during the first phases of program execution. Since these memory locations in the SIB RAM are initialized to specific states during the processor power-up initialization, the test program reads and tests the values to verify that the SIB is responding properly to monitor data request messages and to evaluate the quality of the SIB-MCB interactions.

The other values in the table (three are unassigned) are address and data values (of the most recent control and data messages) and several error counters. These parameters are not important at this stage of the test program but are printed out (page 3T) for the operator's information (the error counters should all be zero). Note that the count values in locations BE-2 and BE-1 are not errors and will increase

during the course of program execution. The program analyzes this data and constructs the SIB EOB monitor display shown in Figure 8, next page. This display is a summary of the contents of these first EOB monitor values and also shows evaluations of this data; the details of the evaluations are described below.

The ACK response preceding the MDH, MDL values for the address 77HFH is tested next (page 3T, T for Top). This monitor data is the Block ID value IDN, which is a very important parameter. If the ACK code is correct, an **"ID ACK OK FIRST PASS"** message is displayed on the CRT display (see Figure 8 below). This is followed by **"ID + ODD PARITY - OK"** if it is correct or **"ID = EVEN PARITY - BAD"** if it is incorrect.

The next display line shows **"ID PARITY = 1, ID VALUE = (IDN value read), BAND MUST BE = (band label)"**. In the case of the F117 Loop Back test fixture (Man and Auto-Loop modes), the **IDN = 0, ID PARITY** is **1** and the band label is **"75 MHz"**. In the FE Monitor mode, the Front-End's IDN, ID parity and associated band label will be displayed.

If the ACK value for the IDN monitor data address (BE-3, 7FFCH) is correct, the CRT displays the message **"ID ACK OK FIRST PASS"** and control is passed forward to decode the Front-End band, the IDN and associated parity.

If the ACK value tested above is erroneous, the IDN monitor data address (BE-3, 7FFCH) is read out another 99 times and tested on each pass. Erroneous ACK's are counted and at the conclusion of the sequence, a **"PERCENT ID NAK OUT OF 100 TRIES"** message (page 3B) is displayed on the CRT. Note that this message denotes an erroneous ACK character (code 06H), not the NAK character (15H) which is entirely different.

If the 77FCH address ACK is erroneous after the 99 cycle ACK test, the test program is halted (page 3B) because additional test operations would be meaningless.

If the 77FCH address ACK (tested above) is correct, the IDN value (i.e. Block ID Code) stored in array MONCHAR$(12,3) is value-tested (page 4T). If greater than 127D (D for decimal), the ID Parity Bit is a "1" and the IDP flag is set to "1" (see the Block ID format in Section 2.3 above). In this event, the value is subtracted from 128 to obtain the true IDN. This IDN is value-tested (Pages 4 & 5) to identify the Front-End type so that the SIB's block start address and block size can be set to the value appropriate for the Front-End under test in the FE Monitor mode. The test fixture has a hard-wired IDN of 0 so the SIB block start address parameters BLKSTHI and BLKSTLO are set to 01 and 00 respectively, designating a SIB block start address of 0100H. This address will be sent to the SIB as a control message on page 6M.

Associated with each IDN value and associated band display message on Pages 5 and 6 are the following Front-End-specific constants: the Block Start Address BLKSTHI (ADH), BLKSTLO (ADL) and BELO, the ADL of the Block End Address, 40H counts above the Block Start Address.

During the IDN value tests, a parameter Par is set to either 1 or 0, as appropriate for the IDN code value. Also during these tests, a band designation message is stored to display the Front-End's band at the end of the tests.

At the conclusion of the IDN value test sequence if the IDN is greater than 10H, the IDN value read is erroneous; the largest Front-End IDN is 0AH (for the 4 mm Front-End). In this case, the message **"NO BAND"** is displayed on the CRT and program execution is halted. The Par parameter is compared with the IDP parameter stored on Page 4; if they are not identical (i.e., both 1's or 0's), the message **"ID = EVEN PARITY - BAD"** is displayed on the CRT. If they are identical, the message **"ID = ODD PARITY -**

OK" is displayed. The band designation message (e.g., "75 MHz" for the test fixture IDN) is also displayed.

If the program did not halt as a result of a failure of the test immediately above, the ACK character for all 16 monitor data readout values in the MONCHAR$ array are tested (page 7B). If any of the 16 ACK codes is incorrect, the message "NO ACK ONE OR MORE INITIAL MON WORDS" is displayed. If they are all correct, the message "ALL ACK OK IN FIRST PASS" is displayed.

Following the test of the 16 ACK values above, the error counter values (bytes 2 and 3) in the first 14 sets of the MONCHAR$ array are tested for a zero value (Page 5); the SIB should have initialized these counters to zero. The BE-10 (address 7FF5H, SIB Version and Rev values, D and B respectively) and BE-3 (8032 address 7FFC, IDN) are excluded from the zero-value test because they are never zero. If all of the 12 sets of MDH and MDL values tested are zero, the message "ALL MON WORDS THAT SHOULD BE ZERO - ARE ZERO". If any of the 12 sets of MDH and MDL values tested are not zero, the message "ONE OR MORE MON WORDS NOT ZERO THAT SHOULD BE" is displayed on the CRT. If these words are not all zero, program operation still continues to the 99-cycle loop below.

The final test in this part of the program is to read and display the SIB Version and Revision level (Page 6T). MONCHAR$(5,2) contents are the SIB Version (should be "D") and MONCHAR$(5,3) contents are the SIB Revision (should be "B"). These were read from BE-5 location and are displayed on the CRT with the messages "INTERFACE TYPE = D INTERFACE REVISION = B". The program does not test these values; THE OPERATOR SHOULD VERIFY THEM.

The tests above showed that if successful for at least 16 monitor data requests, the SIB response was correct for its initialized state. The next test (page 6T) is a more extensive exercise of the SIB that reads and evaluates these 16 Block-End monitor values in a 99-cycle loop. The 99-cycle loop test repeats the 16-address, single-pass operation described above. The objective of this 99-cycle loop test is to request a lot of monitor data (1584 monitor data readouts) and to test the known values (ACK, IDN, SIB Version and Rev), and to assess the error counter accumulations. If the test environment power is glitch-free and the MCB is not faulty, the SIB error rates should be zero and all the fixed values such as ACK, IDN and SIB Version and Rev should never be incorrect.

Much of the 99-cycle loop code is a replica of the operations described above. During each pass the CRT displays "CHECKING ALL FIRST 16 SIB MON WORDS 100 TIMES - CHECK # (pass number)".

The first operation in the 99-cycle FOR-NEXT loop reads the 16 three-bytes sets of End-Block monitor data and loads it into the MONCHAR$ array in a 16-cycle FOR-NEXT loop. Unlike the comparable portion of the code above, the 16 sets of data are not printed. This code (Page 6) is virtually a replica of the Page 3 code.

After this data has been stored in the MONCHAR$ array, the next operation in the 99-cycle loop is to test the 16 ACK characters in the MONCHAR$ array (page 10T). Each set consists of three bytes; ACK is the first byte in each set. If any of the 16 ACK characters is erroneous, a "NO ACK ONE OR MORE SUBSEQUENT MON WORDS" message is displayed on the CRT. This code is virtually a replica of the Page 5 code.

The next operation in the 99-cycle loop is to test the 13 error counters to verify that they are all zero (Page 7). If one or more error counter values are not zero, the "ONE OR MORE MON WORDS NOT ZERO THAT SHOULD BE" message is displayed on the CRT. This code is virtually a replica of the comparable Page 5 code.

The 99-cycle loop will increment the BE-1 counter which contains a count of the number of

correctly received monitor data request messages.

At the conclusion of the 99-cycle loop (page 7M), the FLAGER3 (test mode) is tested. If a 1 or 3 (Man-Loop or FE Monitor Mode), the operator is prompted by the CRT display message "SIB FIRST 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE". If FLAGER3 is a 2 (Auto-Loop mode) the CRT display message is "SIB FIRST 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE". No program branching occurs as a result of the test of FLAGER3.

Having completed the 99-cycle loop and displayed the test result messages, the next operation (Page 7B) is to load the IDN-designated Block Size and Block Start Address parameters into the SIB RAM memory. These Front-End-specific addresses enable the SIB to detect command and data request messages addressed to the F117 under test.

Figure 8 (below) shows the CRT display developed by the program operations described above.

At this point an important digression is to describe the SIB address conventions and the role of the Controller (or F117 Test System) in assigning address space to the SIB. The SIB's command-data address space ranges from 0000 to 7FFFH. The first 100H addresses (00 to FFH) are dedicated to the VLBA Monitor and Control System's SIB 2N and 2N+1 values; each SIB is assigned a pair of these addresses. Each SIB reads and stores a hard-wired, unique Block IDN Code (N in the SIB documentation terminology). The IDN value is used by the SIB firmware as an address reference. Two unique values, output as commands by the Controller (or F117 Test System), are directed to addresses 2N and 2N+1 in each SIB. The 2N value (issued first) specifies the SIB's address Block Size and the 2N+1 value is the Start Address of the SIB's Address Block. Each SIB identifies these values by relating an incoming command addressed to its 2N and 2N+1 addresses and stores the two command arguments in its Block Size and Block Start Adddress locations in RAM. The Controller may reassign the SIB's address space at any time by setting new values in these RAM locations. The time interval between the Controller's transmission of these two parameters is not specified but the SIB cannot perform device control or monitor data operations until both these parameters have been loaded. The 8032 firmware requires the Block Size

```
ADR #BE- 15  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 14  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 13  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 12  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 11  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 10  =DB  CHAR 1 = 6   CHAR 2 = 68   CHAR 3 = 66
ADR #BE- 9   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 8   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 7   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 6   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 5   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 4   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 3   =  CHAR 1 = 6   CHAR 2 = 255   CHAR 3 = 128
ADR #BE- 2   =   CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 2
ADR #BE- 1   =^  CHAR 1 = 6   CHAR 2 = 6   CHAR 3 = 94
ADR #BE- 0   p  CHAR 1 = 6   CHAR 2 = 127   CHAR 3 = 240
ID ACK OK FIRST PASS     ID = ODD PARITY - OK
ID PARITY =  1     ID VALUE =  0     BAND MUST BE = 75 mHz
ALL ACK OK FIRST PASS
ALL MON WORDS THAT SHOULD BE ZERO - ARE ZERO
Interface Type = 68
Interface revision code = 66
SIB FIRST 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE?
```

Figure 8, SIB EOB Monitor Data, Initial Addresses

value before the Block Start Address.

Consider some examples: the 75 MHz Front-End's IDN is 0, the 2N address is thus 00H and the 2N+1 address is 01H. The Controller sends 40H (the Block Size) to address 00 (2N address) and 0100H (the Block Start Address) to address 01 (2N+1 address). The 2.3 GHz Front-End's IDN is 3, the 2N address is 06H and the 2N+1 address is 07H. The Controller sends 40H to address 06H (2N) and sends 280H (the Block Start Address) to address 07H (2N+1). The IDN values for each band are tabulated in Section 1.

The ADH for these two commands is 80H; the most-significant bit is a "1" to designate a command message.

When the SIB is powered up, as described above, the 8032 firmware exercises the initialization code which stores a default block size (10H) and block start address (7FF0H) in the 2N and 2N+1 RAM locations. The usage of these last 16 addresses was described above.

The first operation in sending the Block Size and Block Start Address values is to set 1's in all locations of the MONCHAR$ array (Page 7B).

The page 7B code is general in that it will enable all possible Front-End Block Start address values to be loaded into the SIB as a function of the IDN. In the Man-Loop and Auto-Loop modes, the IDN for the F117 Test Fixture is a hard-wired code of 0 so the Block Start address is commanded to 0100H. If a front-end is connected to the F117 (for the FE Monitor mode tests), the Block Start address will be set to the appropriate value as a function of the IDN value. The Block Size for all Front-Ends is 40H.

Page 7B assigns values to the ADL portions of the 2N and 2N+1 addresses for each IDN. They are labelled CADR1LO and CADR2LO and are used in sending these values to the SIB on Pages 8 and 9. The IDN, CADR1LO and CADR2LO values are displayed on the CRT with these labels (Page 8M).

After sending the Block Size (2N) command to the SIB, the Com Routine sends out a monitor data request to the 2N address to read back the 2N address data to confirm that it has been loaded. A message **"BLOCK SIZE COMMAND RESPONSE = (block size)"** is displayed on the CRT. This is followed by the CRT message **"JUST SENT BLOCK SIZE COMMAND"**.

The Block Start Address must now be sent to the SIB (Page 9T). Following this transmission, the value is read from the SIB and the CRT displays the message **"BLOCK START ADDRESS RESPONSE = (block start address)"**.

The error counter PERROR is cleared (Page 9B), the MONCHAR$ array is cleared to 0's and the message **"STARTING RECHECK OF RELOCATED MON WORDS"** is displayed on the CRT (Page 10T). This operation will read back all 16 end-of-block monitor values in a 16-cycle For-Next loop.

The ADH (BLKSTHI, from Page 4) for this set is transmitted next (Page 10M). The ADL for the first address is 30H, 10H counts less than 40H, so the ADL (for IDN = 0) is H30; this is transmitted next. Note that there are two possible values for ADL as a function of the Block Start Address intervals (80H). If the intervals were 100H, the end-block ADL addresses would be identical. CDH and CDL values of 00H are transmitted following ADL. The data values are loaded into the MONCHAR$ array.

The 16 end-of-block monitor values read back in the 16-cycle For-Next loop are printed out in the format shown in Figure 9, next page. Note that this data display is very similar to that shown in Figure 8, above. The operations described immediately below generate and display this data.

After storage and print-out of the 16 sets of values, the ACK character for the IDN address (ADL = HFC) is checked; this operation is identical to that on Page 3. If it is correct, the message **"Relocated ID ACK OK FIRST PASS"** is displayed on the CRT.

If the IDN message ACK is bad, this message element (for the 13th value) is read in a 99-cycle FOR-NEXT loop (Page 11M). This test is similar to that performed on Page 3B but does not read the whole 16-value set. Before this loop is started, the MONCHAR$ array is cleared to 0's. At the completion of this 99-cycle loop, the message **"relocated PERCENT ID NAK OUT OF 100 TRIES = (percent value)"** is displayed on the CRT screen. This is a test of the ACK character 06H, not NAK which is 15H.

Following this ACK error analysis (if it was entered) or if the single IDN ACK test of two paragraphs above was passed, the IDN parity (of the single-pass or the last IDN message tested in the 99-pass try) is determined (Page 12B). The BAND$ value is set to indicate the Front-End's frequency band (75 MHz for the F117 Test Fixture) and the two parameters CBLKSTHI and MBLKSTHI (for the first addresses of the Wire-Wrap board control and monitor data addresses) are set for subsequent use in the program.

If the IDN is greater than 10, the BAND$ parameter is set to "NO BAND" (an erroneous state) and if Par is not equal to IDP, the message **"ID = EVEN PARITY - BAD"** is displayed on the CRT (Page 12B). If the IDP parity is not erroneous, the messages **"ID PARITY = (Value), ID VALUE = (Value)** and **BAND MUST BE = (Value)** are displayed. (The Par parameter test was described in the Page 5B code above).

On Page 13T, all 16 ACK characters in the MONCHAR$ array are tested; these were loaded by the single pass end-of-block data read operation on Page 11T. If any ACK's are missing, the message **"NO ACK ONE OR MORE relocated INITIAL MON WORDS"** is displayed on the CRT. If all ACK's are correct, the message **"ALL relocated ACK OK FIRST PASS"** is displayed on the CRT.

On Page 13M, the error counters are tested for 0's; if any of these twelve counter contents are not zero, the message **"ONE OR MORE relocated MON WORDS NOT ZERO THAT SHOULD BE"** is displayed on the CRT. If these counter contents are all zero, the message **"ALL relocated MON WORDS THAT SHOULD BE ZERO - ARE ZERO"** is displayed on the CRT.

Following these analyses, on Page 13B the message **"relocated Interface Type = (Type), relocated Interface revision code = (Rev)"** is displayed on the CRT.

The analyses above are based upon a single pass through the 16 monitor data messages. On Page 13B, these 16 values are tested in a 100-cycle loop. This test is similar to that performed on Page 6T for the initialized set of addresses (i.e. 7FF0H to 7FFF). The purpose of this test is to evaluate the SIB's performance when it is subjected to 1600 monitor data request messages. Here again, the contents of these addresses are known (if there are no errors), and the ACK and counter contents = 0's tests are repeated on each pass through the 100 pass loop. During the pass through the loop, the messages **"NO ACK ONE OR MORE SUBSEQUENT relocated MON WORDS"**, **"ONE OR MORE relocated MON WORDS NOT ZERO THAT SHOULD BE"** and **"CHECKING ALL relocated 16 SIB MON WORDS 100 TIMES - CHECK (pass number)"** are displayed on the CRT (Page 15T). The two fault messages result from errors discovered in the ACK and zeros tests. The third message identifies the pass and informs the operator that the test is still in progress.

The tests above have exercised the SIB monitor data readout for about 3000 cycles. The tests have also demonstrated that commands to change the SIB's Block Size and Block Start Addresses were properly executed.

On Page 15T, the operator is queried by one of two messages. If FLAGER3 is a 1 (Man-Loop Mode), the message "SIB relocated 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE". If FLAGER3 is a 2 (Auto-Loop Mode) or 3 (FE Monitor mode), the message "SIB relocated 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE". In either case, the OPERATOR MUST PRESS "ENTER" TO CONTINUE.

Figure 9 (below) shows the CRT display developed by the program operations described above.

The foregoing tests were focused on the SIB; the only circuit exercised on the Wire-Wrap board was the Block IDN and IDN parity bit circuitry. The next set of test operations involves the Wire-Wrap board command, digital monitor and analog monitor circuitry.

In the Auto-Loop and Man-Loop modes, a large 12-pass FOR-NEXT loop (Page 15T to 35M) sends commands to the Wire-Wrap board command registers, reads digital data from the monitor registers, selects and converts the analog signals, evaluates the data and drives the test displays.

Since the analog levels from the Test Fixture are dependent upon the state of the X Cryogenic control bit (described above), it is convenient to test the F117 analog signals in this loop. N6 is the FOR-NEXT loop control index which increments from 1 to 12. Each pass through the N6 loop loads a different state into the Cryo and Cal Control registers, reads and stores the states of the five monitor data registers and samples and converts all 28 analog signals. The digital and analog monitor data is evaluated next and the result of each test comparison is displayed on the CRT in one of four display formats; they are described below.

Some operations in this loop are dependant upon the mode. These differences are described below.

In the Man-Loop and Auto-Loop modes the Cryo and Cal command register states are commanded in a programmed sequence as a function of N6, the loop control variable; in the FE Monitor mode the command states are incremented through the same sequence after a pause to permit the operator to

```
ADR #BE- 15  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 14  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 13  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 12  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 11  =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 10  =DB  CHAR 1 = 6   CHAR 2 = 68   CHAR 3 = 66
ADR #BE- 9   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 8   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 7   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 6   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 5   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 4   =    CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 0
ADR #BE- 3   =  CHAR 1 = 6   CHAR 2 = 255   CHAR 3 = 128
ADR #BE- 2   =   CHAR 1 = 6   CHAR 2 = 0   CHAR 3 = 2
ADR #BE- 1   =^  CHAR 1 = 6   CHAR 2 = 6   CHAR 3 = 94
ADR #BE- 0   p  CHAR 1 = 6   CHAR 2 = 127   CHAR 3 = 240
ID ACK OK FIRST PASS    ID = ODD PARITY - OK
ID PARITY =  1     ID VALUE =  0    BAND MUST BE = 75 mHz
ALL ACK OK FIRST PASS
ALL MON WORDS THAT SHOULD BE ZERO - ARE ZERO
Interface Type = 68
Interface revision code = 66
SIB FIRST 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE?
```

Figure 9, SIB OEB Monitor Data, Relocated Addresses

manually advance the sequence. The operator is prompted by the CRT display message "PRESS ENTER TO CONTINUE". The reason for this pause in the FE Monitor mode is to avoid rapid Front-End Cryogenics state changes resulting from an uninterrupted state-change loop.

The FE Monitor mode initializes the Front-End cryogenics to the COOL (the normal state) and does not auto-sequence as in the Auto-Loop or Man-Loop modes; the operator must press ENTER to start the next pass. In addition, the N6 loop is a 3-pass loop that sequences the cal commands through three states: 1) COOL & CAL OFF & MOD OFF; 2) COOL & LO CAL MOD ON; and 3) COOL & HI CAL MOD ON. This mode permits entry of a cryogenics state command using "C" (for cryo) to enter a command code. In a similar manner, "N" (for NEXT) is used to enter the next N6 state. These functions are described in more detail during the test sequence description below.

The X, C and H bits exercise a number of functions in the F117 Test Fixture; these were described above. The reader should refer to the schematic diagram (C53510S005) during the following discussion.

The F117 Test Fixture uses the X Cryogenic Control bit to select the analog signal level to be fed into the F117 analog inputs. With the exception of the F117 internal signals (+7.5 V and Analog Ground), when X is a 1 (high), the F117 analog inputs are all zero volts and when X is a 0, the analog inputs are all (about) +8.3 volts.

The 12 states exercise the Cryogenic Control X, C and H bits in the XCH variable and the Calibration Control bits in the CALCON variable. Remember that the F117 Test Fixture feeds the X control bit back to the F117 MOD signal input as a simulated MOD signal; this makes the calibration tests dependent upon the state of the Cryo Commands. The line receiver (75141) on the Wire-Wrap board has an inverting output; when the X bit (i.e. MOD) is a 1 (high), the driver output is a 0 so that when the calibration command is set to a switching mode, the X bit must be **low ("0")** to turn on the switching drive to the noise source drive logic. Therefore, in order to read the calibration drive circuit's voltage and current levels, MOD (i.e. X) must be a 0. These signal levels are zero when the calibration drive is off. (See the Calibration circuitry on the Wire-Wrap board schematic diagram.)

Since the Calibration Control circuitry is dependent upon the Test Fixture's usage of X as a psuedo-MOD signal, the Calibration and Cryo commands must be exercised in conjunction during the 12-cycle loop tests. These 7 bits can be set to many Test States but only a few are meaningful; these are tabulated below. In the Cal State column, MOD=0 (referring to the MOD signal) indicates that the switching drive to the Calibration Drive circuit switching is active. The two columns on the right indicate the two drive states. The drive currents are evaluated in the N6 passes in which the drive is active.

N6, Test State	X (MOD)	C	H	Hi Cal Cont	Hi Cal Mod	Lo Cal Cont	Lo Cal Mod	Cal State	Lo Cal Drive	Hi Cal Drive
1	0	1	1	0	0	0	0	Cals Off & MOD=0	OFF	OFF
2	0	0	1	0	0	0	1	Lo Cal Mod & MOD=0	ON	OFF
3	1	1	0	0	0	0	1	Lo Cal Mod & MOD=1	OFF	OFF
4	1	0	0	0	0	1	0	Lo Cal Cont & MOD=0	ON	OFF
5	0	1	1	0	0	0	0	Cals Off & MOD=0	OFF	OFF
6	0	0	1	0	1	0	0	Hi Cal Mod & MOD=0	OFF	ON
7	1	1	0	0	1	0	0	Hi Cal Mod & MOD=1	OFF	OFF
8	1	0	0	1	0	0	0	Hi Cal Cont & MOD=0	OFF	ON
9	1	1	1	0	0	0	0	Cal Off & MOD=1	OFF	OFF
10	1	0	1	0	0	0	0	Cals Off & MOD=0	OFF	OFF
11	0	1	0	0	0	1	0	Lo Cal Cont & MOD=0	ON	OFF
12	0	0	0	0	1	0	0	Hi Cal Mod & MOD=0	OFF	ON

To test the F117's Front-End Cryo monitor discretes inputs, the Test Fixture routes the X, C and H Cryogenic Control bits to the X Mon, C Mon and H Mon pins on J1; therefore these monitor bits should always reflect the state of the command bits. In the following discussion X, C and H designates these three control bits; if the X Mon, C Mon and H Mon bits are referenced, they will have this designation.

The Test Fixture jumpers the F117 multiplex address bits ADDR0, ADDR1 and ADDR2 to the Front-End's control logic output discretes: M - Manual Mode monitor, P - Pump Request, and S - Solenoid state, respectivley. These multiplex address bits cycle the three discretes through 8 states.

When a fault condition is detected in the Auto-Loop mode, FLAGER3 is forced to 1, the Man-Loop mode. This transition enables the operator to make adjustments or measurements. After this transition, program execution continues in the the Man-Loop mode when resumed by the operator; it is not possible to return to the Auto-Loop mode during the balance of the program execution. There are no transitions between FE Monitor mode and the other two modes.

During the digital monitor portion of the loop (Page 16T), the states of the five (addresses H20, .. H24) F117 Monitor Data registers are loaded into the DIGCHAR$ array. The MONCHAR$ array is defined by the DIM MONCHAR$(&H24, 3, 16) statement on Page 1T. The &H24 dimension is 36D. During each N6 pass, the array is loaded with 3 bytes x 5 addresses (ACK, MDH and MDL for H20,... H24) or 15 bytes/pass. Thus, the 12 N6 passes load 180 bytes into the array.

In the digital command portion of the loop (Page 15T), the Cryo and Calibration command registers will be set to one of 12 sets of states. The readout of the associated digital monitor registers (addresses H20 and H22) should match the command register states. The contents of the address 23H register (Band Code, Mod Level, and Front-End Serial Number) should reflect the state set by the Test Fixture logic circuits and the X, C and H Cryo command bits. These states are tabulated in the preceding description of the Test Fixture. X Mon, C Mon, H Mon in the Front-End discretes monitor register (address 21H) should be identical to the X, C and H Cryogenic Control bits and discretes M, P and S should reflect the states of the ADDR0, ADDR1 and ADDR2 multiplex address bits. The F117 module Serial Number readout should be the value hard-wired on the Wire-Wrap connector pins.

In the FE Monitor mode, the Front-End's cryogenic state monitor bits (X Mon, C Mon and H Mon from address H20) reflect the state of the Front-End's cryogenic control logic. If the Front-End's manual control switch is in any position other than Computer, the F117 Test System cannot change the Front-End's cryogenic state. If the switch is in the Computer position, the cryogenic state will be controlled by the F117 Test System. Secondly, in this mode the Front-End's M, P and S discrete bits are controlled by the Front-End control logic and reflect the state of this logic, not the test program's commands or states. Finally, in the FE Monitor mode, the ANLG3 inputs on J1 are floating and can assume any value. The J1 pins assigned to ANLG3 are not connected in the Front-End; the ANLG3 analog values in this mode are the result of minute leakage currents driving the A/D's high input impedance. The leakage currents are mulitplexer leakage currents and bias currents in the A/D converter's input amplifier.

The acquistion and storage of analog monitor data is not dependent upon mode but the evaluation (described below) is. The analog data is stored in the ANLGCHAR$ array which is defined by the DIM ANLGCHAR$(&H1F, 3, 16) statement on Page 1T. The first 12 x 16 x 3 sets of locations are cleared to 0's (Page 17T).

The address range of the analog data is 28D (1FH minus 3H) which covers all analog addresses. This includes the 8 external multiplexer (ANLG3) addresses (18H - 1FH). The analog data addresses were tabulated in Sections 1 and 2 above. During each pass of the N6 loop, 28 analog values for this address range are read and stored in the ANLGCHAR$ array. The first address assigned to the F117-Front-End set is 4H for the Low Cal Current and the last is 17H for the Dewar Vacuum. The Test Fixture connects the

8 ANLG3 inputs to one of the unity-gain buffers so that in the Auto-Loop or Man-Loop modes, the inputs are 0 volts or +8.3 volts as a function of the X command bit. The evaluation of this data in these two modes is dependent upon the state of the X command bit. In the FE Monitor mode, the ANLG3 inputs float and can assume any value in the analog signal range; there is no basis for evaluation of this data in this mode.

In all three modes for each N6 pass, after completing the readout and storage of all digital and analog data (Page 17B), the program pauses and displays the message "PRESS TO GO ON". THE OPERATOR MUST PRESS A KEY TO CONTINUE PROGRAM EXECUTION.

The evaluation of the digital and analog monitor data starts on Page 17B and is inside the 12-cycle N6 FOR-NEXT loop following the acquisition of the analog data.

The test results are displayed on the CRT in four formats which are briefly described below. The reader should compare Figures 10, 11, 12 and 13 (shown below); these are sample print-outs of the (approximate) evaluation CRT display formats for the three test modes. Note that the displays shown in Figure 10 and 11 are virtually identical; the difference is the smile used to indicate a test result GO (Figure 10) or a frown to indicate a NO GO (Figure 11) test result. These two displays are used for the Man-Loop and Auto-Loop modes. The FE Monitor mode uses the display shown in Figure 13 which is very similar to the previous two; the difference is the set of Cryo control codes that the operator can input when prompted to do so.

Note that the upper right half of the three displays (Figures 10, 11 and 12) are dedicated to the FE CRYO and the upper left half is dedicated to the FE ELEC (Calibration) function. Each portion displays states and analog values associated with these two functions. The F117 register states were described in Section 2 above and the character of the test fixture analog signals were described above in this Section.

The Cryo command state (COOL, OFF, etc. from the readback of the H20 monitor register) is

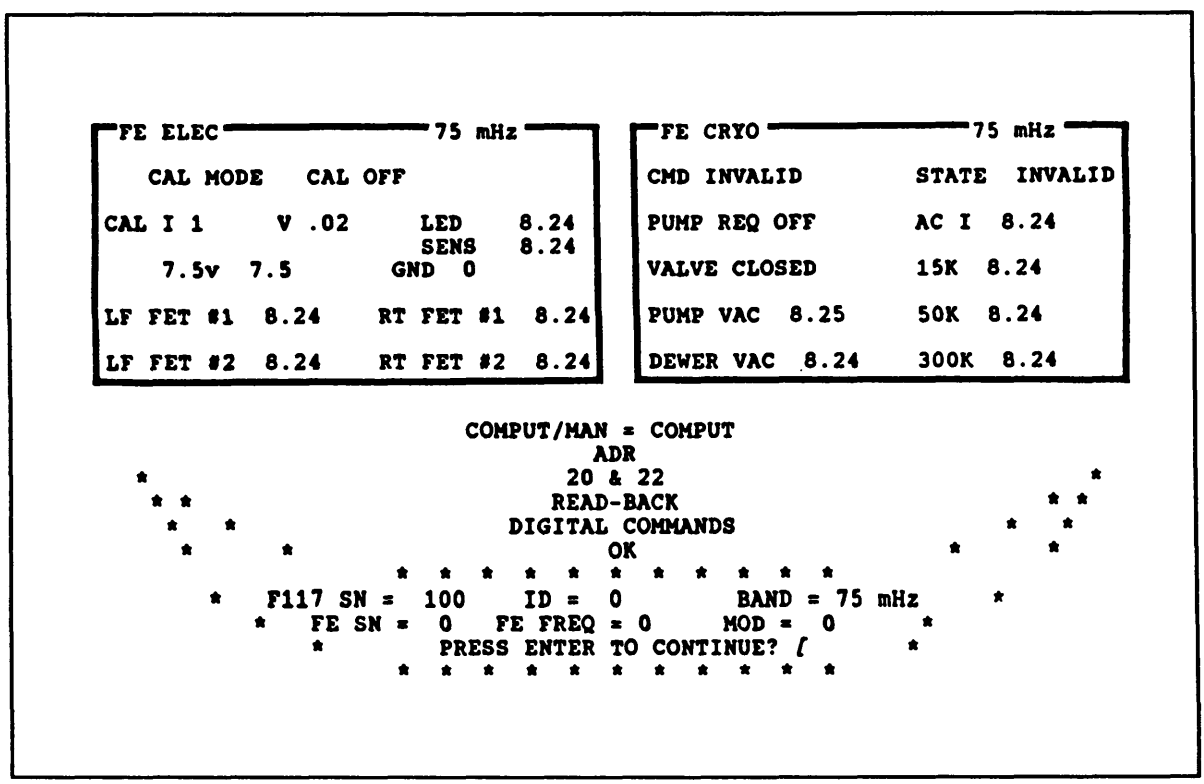


Figure 10, Successful Test Display

displayed adjacent to the CMD label. The Front-End cryo response state read from the H21 register (e.g. COOL, STRESS, etc. from X Mon, C Mon and H MON) is displayed adjacent to the STATE label. The state of two other discretes, P and S, are displayed with the labels and states PUMP REQ OFF (or ON) and VALVE OPEN (or CLOSED) displayed below the mode states. Analog values also displayed in this field are a function of the N6 loop index and should be either 0 volts or about +8.3 volts (if not erroneous).

Calibration command state (e.g. LO CAL SW, etc.) read from the H22 monitor register is displayed adjacent to the CAL MODE label. The associated analog values of calibration current and voltage are displayed below the mode states. These values are a function of the N6 loop index value and should be either 0 volts or about +8.3 volts.

The fourth display is used only in the Manual-Loop and FE Monitor modes. The analog data is a tabular display of hex addresses and values. Note that the ANLG3 data is displayed; it is not included in the other three displays. The digital data is labeled by a functional label (e.g. CAL) and the hex address. The data is presented as decimal and binary 8-bit values (remember that the H20, H12, H22 and H24 monitor data registers are 8 bit registers). ID1 and ID2 values are the two halves of the 16-bit, H23 register's Front-End Band Code, Mod Code and Serial Number. The top line indicates test conditions. The TEST STATE label indicates the N6 loop index value (tabulated above); ANALOG indicates the 0 or +8.3 volts analog stimulus value; MOD shows the state of the MOD bit and noise source drive currents; the EVEN BITS = (1 or 0) and ODD BITS = (0 or 1) indicates the states of the four calibration control bits.

The text below does not describe how the formats are generated or the display color assignments (the text is monochrome). The reader should note that Figures 10, 11 and 12 are not exact replicas of the actual CRT displays; the difference is small and is the result of the printer's response to the CRT's display code values. These displays were obtained by using the computer's "Print Screen" key; the program does not print a hard copy of the data evaluation.

During each pass through the data evaluation portion of the program, the data values are related to the conditions under which they were stored (tabulated above); these conditions are the basis for the GO/NO-GO evaluation. In the Man-Loop and Auto-Loop modes during the data evaluation, an error flag

```
FE ELEC ---------- 75 mHz          FE CRYO ---------- 75 mHz
  CAL MODE   LO CAL SW             CMD PUMP          STATE  COOL
CAL I 3     V 27.4    LED   8.13   PUMP REQ ON       AC I  8
                      SENS  8.2
   7.5v  7.5        GND  0         VALVE OPEN        15K  7.99
LF FET #1  6.03    RT FET #1  7.89  PUMP VAC  6.04    50K  8.01
LF FET #2  8.01    RT FET #2  8.01  DEWER VAC  7.96    300K  8.01

                    COMPUT/MAN = COMPUT
                           ADR
                         20 & 22
                       READ-BACK
                    DIGITAL COMMANDS
                           OK
              * * * * * * * * * * * * * * * *
          *   F117 SN =  100    ID =  0      BAND = 75 mHz  *
     *          FE SN =  0   FE FREQ = 0     MOD =  0              *
  *                  PRESS ENTER TO CONTINUE? [                      *
** * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * **
```

Figure 11, Failed Test Display

THISCHK is set when an erroneous condition is detected. If the program is executing in the Auto-Loop mode, the mode is switched to Man-Loop when THISCHK = 1. The error counter SUMCHECK is incremented each time an error is encountered.

The following is a description of the sequence of data evaluation operations performed in the passes through the N6 loop. Some operations (e.g. High and Low Cal current and Voltage evaluations) are performed on selected passes; others are performed on every pass.

The first data evaluated (Page 18T) is the calibration command mode read from monitor address 22H and stored in the DIGCHAR$ array. The stored state is compared with the value commanded earlier (Page 15M). One of the the following messages will be displayed adjacent to the CAL MODE label as a function of the state: "CAL OFF", "LO CAL SW", "LO CAL CONT", "HI CAL SW" or "HI CAL CONT". If the stored state differs from the commanded state, THISCHK is set to 1, the mode is shifted to Man-Loop and SUMCHECK is incremented. This Cal Mode evaluation drives all three types of displays and is not dependent upon test mode.

The next data evaluated (Page 18M) is the Cryo command state read from monitor address H20 and stored in the DIGCHAR$ array. The stored value is compared with the value commanded earlier in (Page 15M) the N6 loop. If they differ, THISCHK is set to 1, the mode is shifted to Man-Loop and SUMCHEK is incremented. One of the following messages will be displayed adjacent to CMD label as a function of the state: "START", "HEAT", "STRESS", "OFF", "PUMP", or "COOL". If an invalid mode is detected, the CRT displays "INVALID".

The Front-End discretes monitor data (address H21) is evaluated next (Page 19M). This data contains the Front-End's Cryo state monitor bits X Mon, CMon and H Mon and three Front-End discretes, S (vacuum solenoid valve command monitor), P (vacuum pump request) and M (Cryo control in Manual mode).

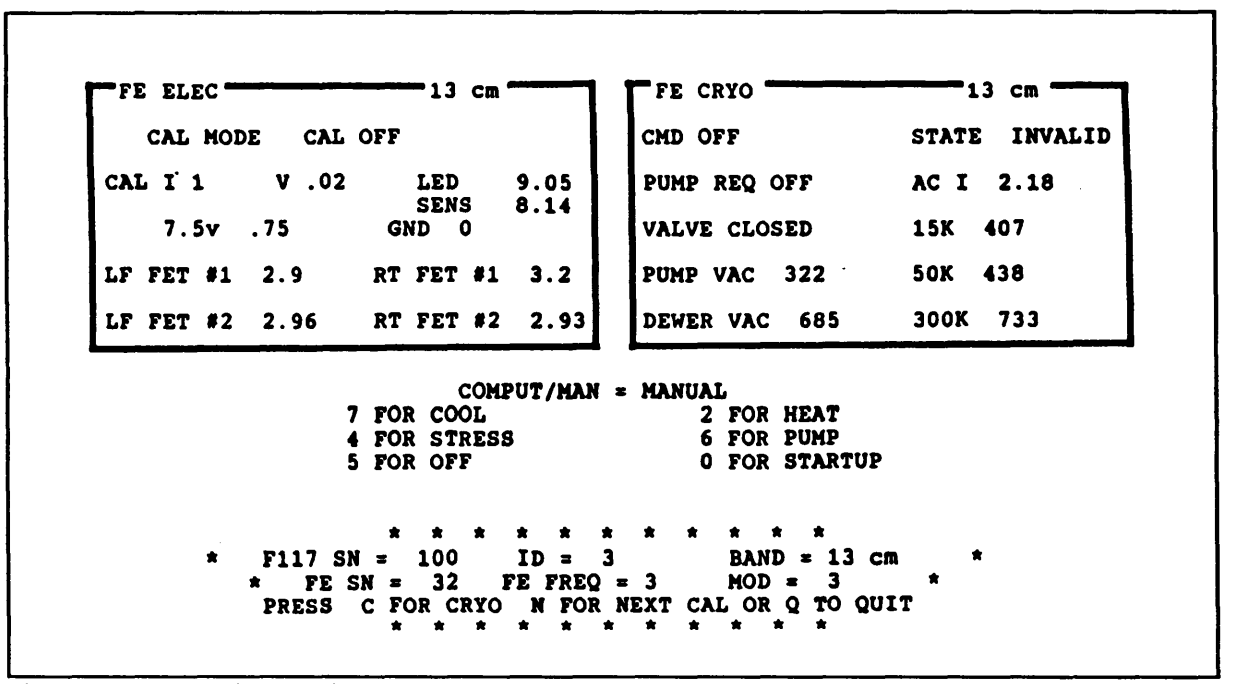


Figure 12, FE Monitor Mode Display

The Front-End's cryo state (X Mon, C Mon and H Mon) is evaluated and one of the following messages is displayed adjacent to the STATE label: "START", "HEAT", "STRESS", "OFF", "PUMP", or "COOL". If an invalid mode is detected, the CRT displays "INVALID".

The Front-End's S, P and M discretes are generated by the Front-End control logic. One of the text messages "OPEN or CLOSED", "ON or OFF" will be displayed adjacent to the VALVE and PUMP REQ labels, respectively, to indicate the state of these discrete bits (Page 19M). The M bit indicates the state of the Front-End's cryogenic mode control switch. Either a "MANUAL" or "COMPUT" message will be displayed adjacent to the COMPUT/MAN label as a function of this switch position.

If the program is executing in the Auto-Loop or Man-Loop modes, the test fixture's simulated values are read from H21. Remember that X Mon, C Mon and H Mon follow the cryogenic control bits X, C and H. If an error is detected, THISCHK is set to 1 (forcing a transition to the Man-Loop mode) and incrementing SUMCHECK.

When the program is executing in the Auto-Loop or Man-Loop mode with the F117 Test Fixture, these discretes are determined by the fixture circuitry that connects these bits to the three lower mux address bits. In these two modes, the Front-End S, P and M discretes data is determined by the state of mux address H21 (binary 0010 0001). Since S, P and M follow the address bits, then S = 0 (Addr2), P = 0 (Addr1) and M = 1 (Addr0); any other state is an error in the Auto-Loop or Man-Loop mode.

In the Auto-Loop and Man-Loop modes, Low and High Calibration currents through the two 1000 Ohm resistors in the Test Fixture are evaluated next (Page 20T). As noted in the calibration states table above, the Low Calibration drive is on during N6 passes 2 and 11; the High Calibration drive is on during passes 6 and 12. The drive currents and voltages are evaluated on these passes. The calibration drive values (in mA) are displayed adjacent to the CAL I label. The Calibration current data display is identical for all three program modes. If the drive current exceeds +/- 50 mA in any pass, THISCHK is set to 1, SUMCHECK is incremented and the program execution mode is set to Man-Loop. The data display is

```
TEST STATE  3   ANALOG = 0 v   MOD = OFF/1   EVEN BITS = 1   ODD BITS = 0

ADR  4   .03 ma          ADR  10   6.03 V
ADR  5   0 ma            ADR  11   7.89 V          ADR  18   4.02 V
ADR  6   27.4 V          ADR  12   8.01 V          ADR  19   4.02 V
ADR  7   0 V             ADR  13   8.01 V          ADR  1A   4.02 V
ADR  8   6.04 V          ADR  14   7.99 K          ADR  1B   4.02 V
ADR  9   8 A             ADR  15   8.01 K          ADR  1C   4 V
ADR  A   8.13 V          ADR  16   8.01 K          ADR  1D   4 V
ADR  B   8.2 V           ADR  17   7.96 V          ADR  1F   4 V
ADR  C   7.5 V
ADR  D   0 V

CMD    MONIT WORD &H20 = 6        0  0  0  0  0  1  1  0
CAL    MONIT WORD &H21 = 255      1  1  1  1  1  1  1  1
STATE  MONIT WORD &H22 = 1        0  0  0  0  0  0  0  1
ID1    MONIT WORD &H23 = 255      1  1  1  1  1  1  1  1
ID2    MONIT WORD &H23 = 255      1  1  1  1  1  1  1  1
FE     MONIT WORD &H24 = 100      0  1  1  0  0  1  0  0


PRESS ENTER TO CONTINUE? [
```

13, Backup Display

identical for all three modes of program execution.

Low and High Calibration voltages across the 1000 Ohm resistors or Front-End's noise sources (scaled to 28 volts) are displayed adjacent to the V label (Page 20M). If the drive voltage is less than +27 volts or greater than +28.5 volts in the N6 passes when the drive is on or exceeds +/- 0.50 volts in the N6 passes when the drive is off, THISCHK is set to 1, SUMCHECK is incremented and the program execution mode is set to Man-Loop. The data display is identical for all three modes of program execution and is displayed adjacent to the V label.

The LED drive voltage is evaluated next (Page 21T). The data value is displayed adjacent to the LED label. A subroutine CHECKUM is called to evaluate this data; from this point on, CHECKUM is frequently called for evaluations of analog data. CHECKUM uses fixed limits of +/- 25 mV and +8.0 to +8.5 V as a function of the N6 index value. CHECKUM sets THISCHK = 1 and increments SUMCHECK for values outside these limits.

The SENS voltage is evaluated next (Page 21M). CHECKUM is called to evaluate the data. The data value is displayed adjacent to the SENS label.

The Front-End's AC current load monitor voltage (ACI) is evaluated next (Page 21B). CHECKUM is called to evaluate the data. The data value is displayed adjacent to the AC I label.

The F117's +7.5 volt reference voltage is evaluated next (Page 22T). CHECKUM is called to evaluate the data. The data value is displayed adjacent to the 7.5 V label. If the program is operating in the FE Monitor mode, the value printed is 1/10 the measured value.

The analog ground voltage is evaluated next (Page 22M). Since it is an F117 internal function, it has a constant value and is therefore independent of the N6 value. The tolerance range for this signal is +/- 0.25 volts and it is tested on all passes through the 12-cycle loop. The value is displayed adjacent to the GND label and is not dependent upon the program execution mode. When it is outside this tolerance range, THISCHK is set to 1, SUMCHECK is incremented and the program execution mode is set to Man-Loop. In the FE Monitor mode the value printed is 1/10 the measured value.

The 15K voltage is evaluated next (Page 22B). CHECKUM is called to evaluate the data. The value is printed adjacent to the 15K label. In the FE Monitor mode the value printed is 100 times the measured value.

The LF FET #1 voltage is evaluated next (Page 23T). CHECKUM is called to evaluate the data. The value is printed adjacent to the LF FET #1 label.

The RT FET #1 voltage is evaluated next (Page 23M). CHECKUM is called to evaluate the data. The value is printed adjacent to the RT FET #1 label.

The PUMP VAC is evaluated next (Page 23B). CHECKUM is called to evaluate the data. The value is printed adjacent to the PUMP VAC label. In the FE Monitor mode the value printed is 100 times the measured value.

The 50K voltage is evaluated next (Page 24T). CHECKUM is called to evaluate the data. The value is printed adjacent to the 50K label. In the FE Monitor mode the value printed is 100 times the measured value.

The LF FET #2 voltage is evaluated next (Page 24M). CHECKUM is called to evaluate the data. The value is printed adjacent to the LF FET #2 label.

The RT FET #2 voltage is evaluated next (Page 24B). CHECKUM is called to evaluate the data. The value is printed adjacent to the RT FET #2 label.

The DEWER VAC voltage is evaluated next (Page 25T). CHECKUM is called to evaluate the data. the value is printed adjacent to the DEWER VAC label. In the FE Monitor mode the value printed is 100 times the measured value.

The 300K voltage is evaluated next (Page 25M). CHECKUM is called to evaluate the data. The value is printed adjacent to the 300K label. In the FE Monitor mode the value printed is 100 times the measured value.

The Band Code, Front-End Serial Number and Mod level codes are extracted from H23 (Page 25M) for printout (described below).

The eight ANLG3 external multiplexer voltages are evaluated next (Page 26T). The values are loaded into the ANVAL array and evaluated by CHECKUM. If outside the CHECKUM tolerances, the message **"BAD AUX ANALOG"** is displayed. In the Man-Loop and Auto-Loop modes, the ANLG3 lines are driven by the Test Fixture's 0 and +8.3 signals. In the FE Monitor mode the ANLG3 lines float.

The operations described above are the data evaluation and display functions. The next steps in program execution are the final test decisions and generation of the GO (smile) or NOGO (frown) display symbols.

In the Man-Loop and Auto-Loop modes, a final summary message **"ADR 20 & 22 READ BACK DIGITAL COMMANDS OK"** is displayed (Page 27) for either case of SUMCHECK (either 0 or not 0).

Enclosed within the smile or frown, the Figures 10, 11 and 12 displays show the IDN and the H23-H24 monitor data values displayed adjacent to the following labels: F117 SN = **(serial number)**, ID = **(ID value)**, BAND = **(band name)**, FE SN = **(serial number)**, FE FREQ = **(band code)**, MOD = **(mod level)**. These display values are followed by the prompt: **"PRESS ENTER TO CONTINUE"**.

In the FE Monitor mode, the display shows a set of Cryo control codes and a prompt **"PRESS C FOR CRYO N FOR NEXT CAL OR Q TO QUIT"**. If the operator presses C, he may enter any of the displayed codes to command the associated cryo modes. If the operator presses N, the next FE Monitor cal state (e.g. CAL OFF, LO CAL and HI CAL) in the N6 sequence is commanded and control reverts to the start of the N6 loop (Page 15T). If he presses Q, the Backup display (Figure 13, described above) is entered. This display is also entered in the Man-Loop mode after completing the **"PRESS ENTER TO CONTINUE"** response of the previous paragraph.

In the FE Monitor mode, after displaying the Backup display (Page 35), the prompt **"PRESS ENTER TO CONTINUE"** ends the program execution when the operator presses **ENTER**. This prompt is also displayed in the Man-Loop and Auto-Loop modes; when the operator responds by pressing **ENTER**, the flag GONO is set to the SUMCHECK value. If GONO is 0, the message **"F117 PASSED PASSED TESTING"** and the F117 serial number is printed adjacent to the F117 SN = label. If GONO is not 0, the message **"F117 FAILED TESTING"** and the F117 serial number is printed adjacent to the F117 SN label.

This final **ENTER** response ends program execution.

Alignment Adjustments

The SIB alignment should be done in the Maxtester system; the F117 module is not an adequate test environment for this board. SIB features that are not testable in the F117 test environment are the

CDH output on the upper byte of the CMD/MON bus, the two upper address bits and the SIB state LED drive circuitry. Secondly, the F117 analog circuitry does not provide adequate negative and positive reference voltages for a comprehensive SIB analog alignment and the ANLG-0 input is not testable.

The only alignment adjustments on the Wire-Wrap board are the calibration current monitor zero-adjustment potentiometers, R55 and R56. To adjust these two potentiometers, use a test fixture that approximately simulates a Front-End (i.e. an IDN code, etc.). The test fixture should have two 1000 Ohm resistors to simulate noise source loads with manual switches (or clip leads, etc.) to connect or disconnect the two loads. In the FE Monitor mode, set the calibration drives active (i.e. the calibration drive outputs at +28 volts). With the loads disconnected, adjust the two potentiometers for zero volt outputs on amplifiers 3DA-1 and 3DA-7. Connect the two loads by actuating the switches; the amplifier outputs should be + 0.280 volts since the amplifier scaling is 100 mA/volt.

4.0 DRAWINGS

The F117 Functional and Reference drawings, the Standard Interface Schematic Diagram and Loop-Back test fixture drawings listed below are included in this section. F117 and Standard Interface Fabrication drawings are listed but not included. F117 Module and Wire-Wrap board fabrication drawings are listed in the associated BOM's.

F117 Functional Drawings

D53510A001 F117, Front-End Interface Assembly
D53510W010 F117 Front-End Control Module Wiring Diagram
A53510B001 F117 Front-End Interface Module BOM

D53510S004 Wire-Wrap Board Circuit Schematic Diagram
A53510A004 F117 Wire-Wrap Printed Circuit Board Component Layout
A53510B002 Wire-Wrap Printed Circuit Board BOM

D55002S002 Standard Interface Board Model "D" Schematic Diagram

F117 Reference Drawings

C53510S003 Front-End Interface - F117 Module (Wire-Wrap Board Schematic)
A53510W007 Wire List

F117 Fabrication Drawings

D53510A001 Front-End Interface Assembly
C53510W001 Wiring Harness Diagram
A53510W007 Wire List
A53510W006 F117 Internal Wiring Harness

Standard Interface Board Fabrication Drawings

D55002A002 Assembly Drawing, Model "D"
A55002B002 Assembly Bill of Materials, Model "D" (not included in this manual)
D55002Q002 Printed Circuit Artwork Master, Model "D"
D55002P002 PCB Drill Drawing, Model "D" (not included in this manual)

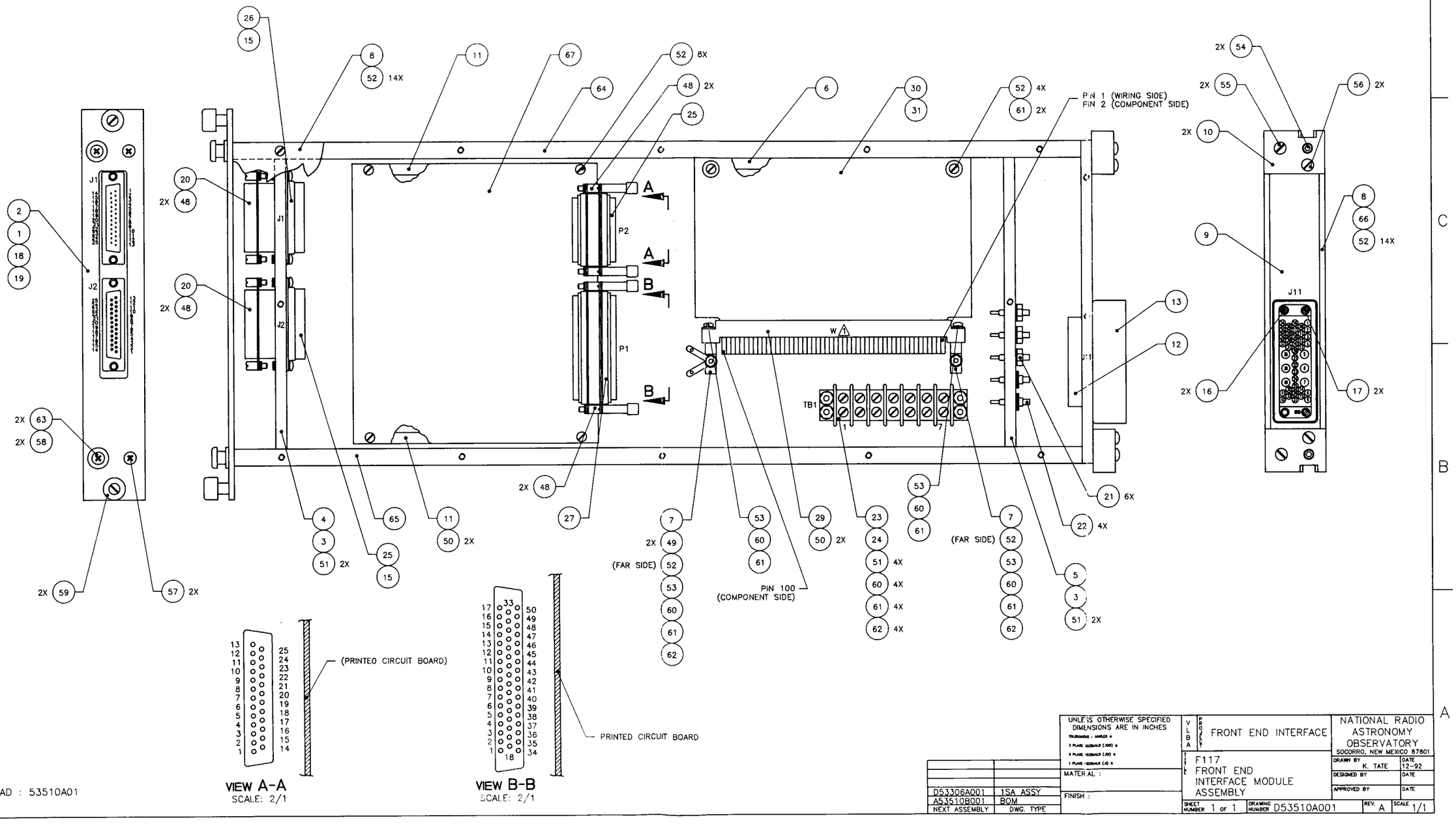
F117 Test Fixture Drawings

C53510S005 F117 Loop Back Schematic
C53510A007 F117 Loop Back Test Fixture Assembly

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12-92	K. TATE		REVISED & REDRAWN ON ACAD

NOTES:

1. CONNECTOR "W" CONTACT LOCATIONS:
   EVEN NUMBERED CONTACTS ON TOP (COMPONENT) SIDE
   000 NUMBERED CONTACTS ON FAR (WIRING) SIDE



VIEW A-A
SCALE: 2/1

VIEW B-B
SCALE: 2/1

ACAD : 53510A01

D53306A001	1SA ASSY
A53510B001	BOM
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMAL (.000) ±
2 PLACE DECIMAL (.00) ±
1 PLACE DECIMAL (.0) ±
MATERIAL :
FINISH :

PROJECT: VLBA — FRONT END INTERFACE

TITLE: F117 FRONT END INTERFACE MODULE ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY: K. TATE	DATE: 12-92
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D53510A001 | REV. A | SCALE 1/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

RFI ENCLOSURE

GND J11-34 FT1 — TB1 1 — REF GND
+5V J11-10 FT2 — TB1 4
−15V J11-17 FT3 — TB1 5
+15V J11-16 FT4 — TB1 6
+28V J11-29 FT5 — TB1 7

5 WW BOARD +5, ±15, +28V
2 FE ±15

XMT
+ J11-9 RED FT8 — RED — 21 XMT+
− J11-8 BLK FT10 — BLK — 22 XMT−
TW PR
M & C BUS SIGNALS

RCV
+ J11-14 WHT FT7 — WHT — 19 RCV+
− J11-15 BLK FT9 — BLK — 20 RCV−
TW PR

NOT USED IN F117
5 SYSRST+
6 SYSRST−
23 RSTSW
25 DIG GND
7 P1.7
8 P1.6
18 XACT
10 DOUT
11 PARX
24 BUSY
12 MSG
25 DIG GND
1 +5V
17 ANALOG GND

P2 15 16 14 13 +15V −15V +5V DIG GND
P2 P1 34 50 40 39 DIG GND +5V +15V −15V
W 99 2 100 94 95 96 W REF GND +5V +5V −15V +15V +28V

P1 ANLG 2+ 3 — BUS 1 ANALOG MUX SIGNALS
ANLG 1+ 2
ANLG 4+ 5 — 4 ANALOG MUX SIGNALS
ANLG 5+ 6
ANLG 6+ 7
ANLG 7+ 8
ANLG 1− 19 — BUS
ANLG 2− 20
ANLG 4− 22
ANLG 5− 23
ANLG 6− 24
ANLG 7− 25
ANLG GND 38
C/M 0 33 — 16 TRI-STATE CMD/MON BUS
C/M 1 16
C/M 2 32
C/M 3 15
C/M 4 31
C/M 5 14
C/M 6 30
C/M 7 13
C/M 8 29
C/M 9 12
C/M 10 28
C/M 11 11
C/M 12 27
C/M 13 10
C/M 14 26
C/M 15 9

STANDARD INTERFACE BOARD VERSION "D"
ASSEMBLY: D55002A002
SCHEMATIC: D55001S002

P2 1 ANLG 0+
18 ANLG 0−
P1

P2 ID REQ 9 — 1 — 16 ID REQ
P1

P1 ADDR0 48 — 6 ADDRESS BUS — 29 ADDR0
ADDR1 47 — 30 ADDR1
ADDR2 46 — 31 ADDR2
ADDR3 45 — 32 ADDR3
ADDR4 44 — 33 ADDR4
ADDR5 43 — 34 ADDR5
ADDR6 42 NOT USIED
ADDR7 41 NOT USIED
ANLG3+ 4 — 3
ANLG3− 21
R/W(L) 49 — 5 DEVICE CONTROL — 11 R/W(L)
REV REQ 35 — 12 REV REQ
DEV ACK 36 — 15 DEV ACK
ANEN B 37 — 18 ANEN B
H/L(L)SEL 17 — 17 H/L(L)SEL
93 MOD

W 10 ANLG1+, ANLG2+
ANLG 4+ 5
ANLG 5+ 6
ANLG 6+ 13
ANLG 7+ 14
C/M 0 35
C/M 1 36
C/M 2 37
C/M 3 38
C/M 4 39
C/M 5 40
C/M 6 41
C/M 7 42
C/M 8 43
C/M 9 44
C/M 10 45
C/M 11 46
C/M 12 47
C/M 13 48
C/M 14 51
C/M 15 52

WIRE-WRAP CIRCUIT BOARD
ASSEMBLY: D53540A004
SCHEMATIC: C53510S003
SCHEMATIC: D53510S004

SN0 SN1 SN2 SN3 SN4 SN5 SN6 SN7 GND +5V
W 19 20 21 22 23 24 25 26 27 28 W
TO ENCODE MODULE SERIAL NUMBER, CONNECT SN0 – SN7 PINS TO: PIN 28 FOR A "1", PIN 27 FOR A "0"

W PA(L) 69 — 5 BAND I/D CODE
F3 84
F2 83
F1 82
F0 81
S5 92 — 6 RCVR SERIAL NUMBER CODE
S4 91
S3 90
S2 89
S1 88
S0 87
M1 86 — 2 RCVR MOD CODE
M0 85
CAL 55 — 2 CAL DRIVE
HI CAL 56
X 72 — 3 CRYO CMD
C 71
H(L) 70
3 EXT MUX ADDR
13 RCVR ANALOG MONITOR SIGNALS
VP 65
VD 64
15K 61
50K 62
300K 63
ACI 66
RF1 58
RF2 60
LF1 57
LF2 59
LED(L) 67
Q GND 8
SENS 68
2 EXT MUX
6 RCVR STATE MONITORS
S 80
P 79
M(L) 78
X MON 77
C MON 76
H MON(L) 75
W

J2 (CONTROL)
13 REF GND
1 REF GND
4 NOT USED
2 +15V
3 −15V
5 NOT USED
9 PA(L)
17 F3
16 F2
15 F1
14 F0
23 S5
22 S4
21 S3
20 S2
19 S1
18 S0
10 NOT USED
25 M1
24 M0
11 CAL
12 HI CAL
6 X
7 C
8 H(L)
FRONT END CONTROL CONNECTOR
J2 (CONTROL) J1 (MONITOR) ⚠1
17 ADDR0
18 ADDR1
19 ADDR2
1 VP
2 VD
3 15K
4 50K
5 300K
6 ACI
7 RF1
8 RF2
9 LF1
10 LF2
11 LED(L)
13 Q GND
14 SENS
15 ANLG3+
16 ANLG3−
20 S
21 P
22 M(L)
23 X MON
24 C MON
25 H MON(L)
12 NOT USED
J1 (MONITOR)
FRONT END MONITOR CONNECTOR

NOTES:
⚠1 CONNECTORS J1 & J2 HAVE RFI FILTER CONTACTS
2. DRAWN USING NRAO WIRE LIST #A53510W008

MOD J11-12 FT6
2 INPUT FROM EXTERNAL ANALOG MULTIPLEXER

ACAD : 53510W10

D53510A001	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.000) ±
2 PLACE DECIMALS (.00) ±
1 PLACE DECIMALS (.0) ±
MATERIAL
FINISH :

PROJECT: VLBA — FRONT END INTERFACE

TITLE: F117 FRONT END CONTROL MODULE WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY K. TATE	DATE 11-92
DESIGNED BY	DATE
APPROVED BY	DATE
SHEET NUMBER 1 OF 1	DRAWING NUMBER D53510W010
REV. –	SCALE NONE

REVISIONS				
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY K. TATE	DATE 11-92			
DESIGNED BY	DATE			
APPROVED BY	DATE		D53510A001	ASSEMBLY
			NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLBA

PROJECT: FRONT END INTERFACE

TITLE: F117 FRONT END INTERFACE MODULE BOM

DWG NO. A53510B001 SHEET 1 OF 5

NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A53510B001 REV A DATE 11-02-92 PAGE 2 OF 5

MODULE F117 NAME FE INTERFACE MODULE DWG# D53510A001 SUB ASSY _____ DWG# _____

SCHEM. DWG# D53510S004 LOCATION _____ QUA/SYS. _____ PREPRD BY K.F. TATE APPRVD BY D. WEBER

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		NRAO	C53306M021	PANEL, FRONT	1
2		NRAO	B53510M006	MODIFICATION, FRONT PANEL	1
3		NRAO	B53306M027-1	SHIELD	2
4		NRAO	B53510M010	REWORK, FRONT SHIELD	1
5		NRAO	B53510M011	REWORK, REAR SHIELD	1
6		NRAO	A53510M012	MOUNT, WIRE-WRAP PCB	1
7		NRAO	A53510M014	STANDOFF, WIRE-WRAP PCB	2
8		NRAO	D53306M005	PLATE, SIDE	2
9		NRAO	C53306M022	PANEL, REAR	1
10		NRAO	B53306M018	GUIDE	2
11		NRAO	A53510M013	MOUNT, PCB	2
12		AMP	204186-5	BLOCK, 42-PIN	1
13		AMP	202394-2	COVER, CONNECTOR	1
14		AMP	201578-1	PIN, CRIMP, #24-20 GA.	12
15		AMP	745776-3	GASKET, EMI, 25-PIN D-SUB	2
16		AMP	200833-1	PIN, GUIDE	2
17		AMP	203964-9	SOCKET, GUIDE	2
18		NRAO	A53306N002	PAINT ITEM 2 PER NRAO SPEC	1
19		NRAO	B53510I001	SILKSCREEN ITEM 18	1
20		SPECTRUM	56-725-005	FEEDTHRU, EMI 25-PIN D-SUB	2

NATIONAL RADIO ASTRONOMY OBSERVATORY

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		SPECTRUM	51-744-001/002	FEEDTHRU, EMI #8-32	6
22		MIDLAND ROSS	570-2642-01-01-19	FEEDTHRU, #6-32	4
23		CINCH/TRW	7-140	BLOCK, 7-LUG TERMINAL	1
24		CINCH/TRW	MS-7-140 Y	STRIP, MARKER	1
25		CINCH/TRW	DBMS-25S	CONNECTOR, 25-SOCK., D-SUB	2
26		CINCH/TRW	DBM-25P	CONNECTOR, 25-PIN, D-SUB	1
27		CINCH/TRW	DBM-50S	CONNECTOR, 50-SOCK., D-SUB	1
28		PANDUIT	PLT.7M	TIE-WRAP, CABLE, 3.5"	40
29		VIKING	3VH50/1JN5	CONNECTOR, CARD EDGE	1
30		NRAO	D13520M2-B	PCB, WIRE-WRAP	1
31		NRAO	A53510A004	PCB, WW, COMPONENT LAYOUT	1
32		ALPHA	7053	WIRE, WHT/RED, #26 GA.	15'
33		ALPHA	7053	WIRE, WHT/VIO, #26 GA.	15'
34		ALPHA	7053	WIRE, WHT/BLU, #26 GA.	15'
35		ALPHA	7053	WIRE, WHT/GRN, #26 GA.	15'
36		ALPHA	7053	WIRE, WHT/YEL, #26 GA.	15'
37		ALPHA	7053	WIRE, WHT/ORG, #26 GA.	15'
38		ALPHA	7053	WIRE, WHT/BLK, #26 GA.	15'
39		ALPHA	7053	WIRE, WHT/BRN, #26 GA.	15'
40		ALPHA	7053	WIRE, BLK, #26 GA.	15'
41		ALPHA	7055	WIRE, BLK, #22 GA.	6'
42		ALPHA	7055	WIRE, ORG, #22 GA.	3'

NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A53510B001 REV A DATE 11-02-92 PAGE 4 OF 5

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
43		ALPHA	7055	WIRE, RED, #22 GA.	3'
44		ALPHA	7055	WIRE, YEL, #22 GA.	3'
45		ALPHA	7055	WIRE, GRY, #22 GA.	3'
46		ALPHA	FIT-221-1/8"	TUBING, SHRINK	1'
47		ALPHA	FIT-221-1/16"	TUBING, SHRINK	6'
48		AMPHENOL	17-895	KIT, JACKSCREW, D-SUB	8
49		H.H. SMITH	1411-4	LUG, SOLDER, #4	2
50		PANDUIT	TA1S8	TIE, ANCHOR	4
51				SCREW, PN HD, SS, #4-40x.5	8
52				SCREW, PN HD, SS, #4-40x.25	42
53				SCREW, PN HD, SS, #4-40x.69	4
54				SCREW, SOC HD,SS, #6-32x1.0	2
55				SCREW, PN HD, SS, #6-32x.75	2
56				SCREW, PN HD, SS, #6-32x.50	2
57				SCREW, FLT HD, SS, #6-32 x .38, HP GREY	2
58				SCREW, PN HD, SS, #6-32x.75	2
59		SOUTHCO	47-11-204-10	SCREW, CAPTIVE	2
60				WASHER, FLAT, #4-40	8
61				WASHER, LOCK, #4-40	10
62				NUT, #4-40	6
63		NRAO	A53306M038	BRACKET, HANDLE	2
64		NRAO	D53306M004-2	SUPPORT, TOP BAR	1

NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A53510B001 REV A DATE 11-02-92 PAGE 5 OF 5

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
65		NRAO	D53306M004-1	SUPPORT, BOTTOM BAR	1
66		NRAO	D53510M009	REWORK, SIDE PLATE	1
67		NRAO	D55002A002	PCB, STANDARD INTERFACE, VERSION "P"	1
68					
69					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
80					
81					
82					
83					
84					
85					
86					

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. CHIP LOCATION DESIGNATORS ARE UNDERLINED. SEE ASSEMBLY DRAWING A53510A004 FOR PHYSICAL LOCATION ON WIRE-WRAP BOARD.
2. THE THIRD CHARACTER IN CHIP LOCATION DESIGNATORS DESIGNATES 1ST, 2ND, ETC. CIRCUIT IN CHIP. E.G. 1CA DENOTES GATE A IN CHIP 1C.
3. *R52, *R53, & *R54 LEADS ARE DIRECTLY INSERTED INTO BOARD SOCKETS SHOWN.
4. R55 & R56 ARE DIP-FORMAT POTENTIOMETERS AND HAVE NO LOCATION DESIGNATORS.
5. LOW-TRUE SIGNAL HAVE AN (L) SUFFIX, E.G. HMON(L)
6. R/W(L) IS LOW-TRUE FOR WRITE. IF HI/LO IS HIGH, STANDARD INTERFACE BOARD ANALOG MULTIPLEXER IS CONTROLLED BY ADDR5, ADDR4, & ADDR3
7. REDRAWN FROM NRAO DRAWING #C53510S003
8. ASSEMBLY DRAWING: A53510A004

STD. INT. BD. SIGNALS

W35 ← C/M0
W38 ← C/M1
W37 ← C/M2
W38 ← C/M3
W39 ← C/M4
W40 ← C/M5
W41 ← C/M8
W42 ← C/M7
W43 ← C/M8
W44 ← C/M9
W45 ← C/M10
W46 ← C/M11
W47 ← C/M12
W48 ← C/M13
W51 ← C/M14
W52 ← C/M15

SI8 TRI-STATE BUS

W29 ← ADDR0
W30 ← ADDR1
W31 ← ADDR2
W32 ← ADDR3
W33 ← ADDR4
W34 ← ADDR5

SI8 ADDRESS BUS

W12 ← REV REQ
W15 ← DEV ACK
W18 ← ANEN8
W17 ← HI/LO SEL (L)
W11 ← R/W(L)
W16 ← ID REQ

SI8 DEVICE CONTRDL

W10 ← ANLG1+ & ANLG2+
W5 ← ANLG4+
W8 ← ANLG5+
W13 ← ANLG8+
W14 ← ANLG7+

SI8 ANALOG DATA

COMMAND AND MONITOR DATA REGISTERS

CRYO CMD 3A — 20H EN (CMD)
CRYO MON 2A — 20H EN (MON)
CAL CMD 3B
CAL MON 2B — 22H EN (MON)
FREQ & MOD MON 2C — 23H EN (MON)
IO CODE READ 5E — IO REQ
RCVR S/N MON 2D
RECR DISCR MON 2E — 21H EN (MON)
MOD S/N MON 5D — 24H EN (MON)

PWR RESET

ADDRESS DECODE

74LS138 (10)
ADDR0, ADDR1, R/W(L), DEV REQ, ADDR2, G1, G2A, G2A
Y0 20H EN (CMD)
Y1
Y2 22H EN (CMD)
Y3
Y4 20H EN (MON)
Y5 21H EN (MON)
Y6 22H EN (MON)
Y7 23H EN (MON)

ADDR5 → 74LS04 1BA → 74LS08 1AA (DEV REQ) → 74LS04 1BC → 74LS32 1C8 → 24H EN (MON)
ADDR2 → 74LS04 1BO
74LS08 1AB → ANEN8
DEV ACK

CAL SWITCHING LOGIC

COUNT CAL
HI CAL MOD
HI CAL CONT
74LS08 1AD, 1AC
74LS32 1CD, 1CC
20K

CAL DRIVE CIRCUITS

5.6K, 5.6K, 1K, +28
NPN2, NPN1, PNP2, PNP1
4C TPQ8502 QUAD TRANSISTOR ARRAY

HI CAL MONITOR

6.2K, 10K, 4870, LF442A (3D)
4990, 200, L8, L7, L9, R55
10K, 30.1K, 100K
ANLG 5+, HI CAL CURRENT
ANLG 7+, HI CAL VOLTAGE/4
HI CAL

LOW CAL MONITOR

6.2K, 10K, 4870, LF442A (3A)
4990, 200, L12, L11, L13, R56
10K, 30.1K, 100K
ANLG 4+, LOW CAL CURRENT
ANLG 6+, LOW CAL VOLTAGE/4
CAL

CAL INHIBIT LOGIC

LM393A (3EA, 3EB)

CAL DRIVE MODULATION

3.9K *R53, +1.9V, H17, 2.4K *R54, J17, MOD
74LS32 (OUT 2, OUT 1)
5A 75141 DUAL LINE RECEIVER

POWER RESET

1N914, 1K, 2.2µf, 51K, 22µf, 74LS221 (1FA), 74LS08
~100 µS PWR RESET

+7.5 VOLT REFERENCE

+1.215V, ADS84, LF442A, 16K, 8K, 4K, 4K, V8G
+15V, +7.5V REF
DIP HEADER 3C

ANALOG MULTIPLEXER

HI506A (4A)
LF1, RF1, LF2, RF2, 15K, 50K, 300K, VD, VP, ACI, LED(L), SENS, +7.5V REF, Q GND, *Q GND
+15V, GND, -15V, OUT, VREF, EN, AD, A1, A2, A3
ANLG1&ANLG2, HI/LO(L) SEL, H15, R52 1K, J15, R31, R30, R28, R29, 1CA
ADDR0, ADDR1, ADDR2, ADDR3, ADDR4
FE ANALOG SIGNALS

PULL-UP RESISTOR NETWORK

4D: R11–R25, R2X — 4.7K TYPICAL
4E: R26–R31 — 4.7K TYPICAL
VCC

FRONT END SIGNALS

FE 8AND CODE: PA(L) W89, F3 W84, F2 W83, F1 W82, F0 W81
FE SERIAL NUMBER: S5 W92, S4 W91, S3 W90, S2 W89, S1 W88, S0 W87
FE MDD LEVEL: M1 W86, M0 W85
FE CAL DRIVE: CAL W55, HI CAL W56
FE CRYO CONTROL: X W72, C W71, H(L) W70
FE ANALOG MONITORS: VP W65, VO W84, 15K W61, 50K W62, 300K W63, ACI W88, RF1 W58, RF2 W8D, LF1 W57, LF2 W59, LED(L) W87, Q GND W8, SENS W88
FE STATE MONITORS: S W8D, P W79, M(L) W78, XMDN W77, CMON W78, HMON(L) W75

BOARD POWER INPUTS

VCC PLANE: W2, W4, W98, W100 — +5, VCC
GND PLANE: W1, W3, W27, W49, W73, W97, W99 — COMMON
+28V DIST W96, +15V DIST W95, -15V DIST W94, MOD W93 — +28V +15V -15V

MODULE SERIAL NUMBER ENCODING

SN0 W19, SN1 W20, SN2 W21, SN3 W22, SN4 W23, SN5 W24, SN6 W25, SN7 W26, GND W27, +5V W28
TO ENCODE MODULE SERIAL NUMBER, CONNECT SN0 – SN7 PINS TO: PIN 28 FOR A "1", PIN 27 FOR A "0"

ACAD : 53510S04

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.000) ±
2 PLACE DECIMALS (.00) ±
1 PLACE DECIMALS (.0) ±
MATERIAL:
FINISH:

A53510A004 ASSEMBLY
NEXT ASSEMBLY | DWG. TYPE

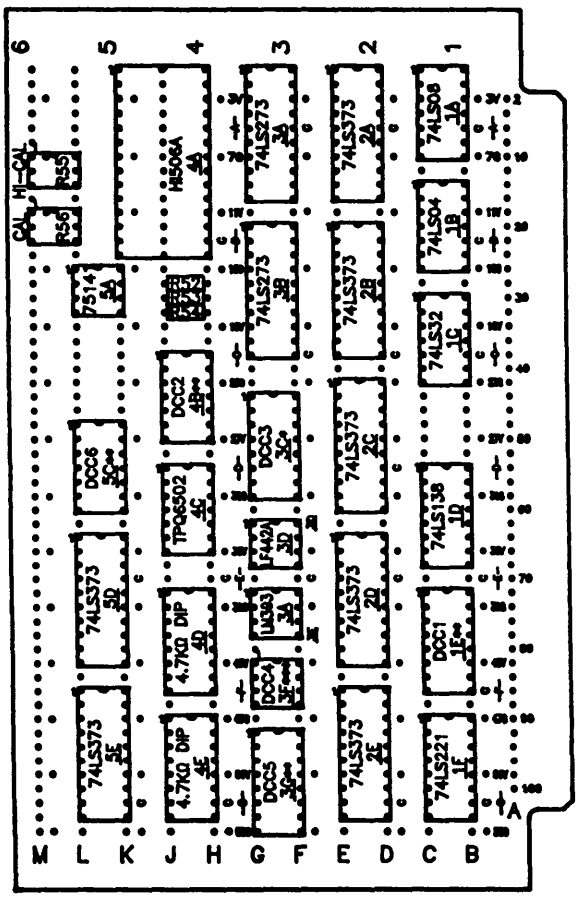
VLBA — FRONT END INTERFACE
TITLE: F117 WIRE-WRAP BOARD CIRCUIT SCHEMATIC DIAGRAM

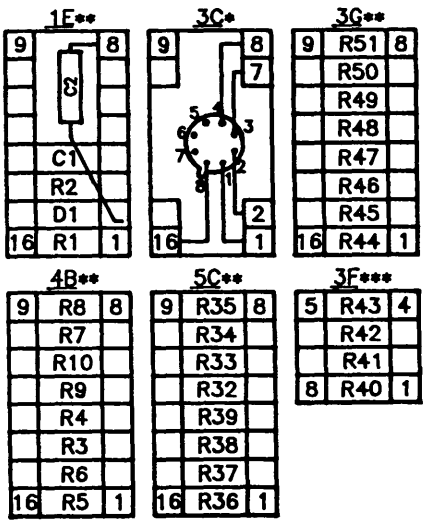
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY K. TATE	DATE 12-92
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D53510S004 | REV. – | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12-92	K. TATE	D.WEBER	REVISED AND REDRAWN ON ACAD





* AD584JH INSTALLED ON AUGAT 608-AG21 TRANSISTOR ADAPTOR
** AUGAT 606-CG1 DIP HEADER
*** AUGAT 608-CG1 DIP HEADER

ACAD : 53510A04

D53510S004	SCHEMATIC
C53510S003	SCHEMATIC
A53510B002	BOM
D53510A001	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

VLBA PROJECT: FRONT END INTERFACE

TITLE: F117 WIRE-WRAP PRINTED CIRCUIT BOARD COMPONENT LAYOUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY K. TATE	DATE 12-92
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
1 OF 1	A53510A004	A	NONE

REVISIONS				
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY K. TATE	DATE 11-92			
DESIGNED BY	DATE		A53510A004	ASSEMBLY
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLBA

PROJECT: FRONT END INTERFACE

TITLE: F117 WIRE-WRAP PRINTED CICUIT BOARD BOM

DWG NO. A53510B002 SHEET 1 OF 4

NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A53510B002 REV - DATE 11-02-92 PAGE 2 OF 4

MODULE F117 NAME WIRE-WRAP CIRCUIT BD. DWG# A53510A004 SUB ASSY _____ DWG# _____

SCHEM. DWG# D53510S004 LOCATION _____ QUA/SYS. _____ PREPRD BY K.F. TATE APPRVD BY D. WEBER

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		NRAO	A53510W007	WIRE LIST, WIRE-WRAP PCB	1
2		AUGAT	616-CG1	HEADER, 16-PIN DIP	4
3		AUGAT	608-CG1	HEADER, 8-PIN DIP	1
4		AUGAT	608-AG21	PLUG, TRANSISTOR ADAPTOR	1
5			74LS08	IC, DUAL-IN-LINE	1
6			74LS04	IC, DUAL-IN-LINE	1
7			74LS32	IC, DUAL-IN-LINE	1
8			74LS138	IC, DUAL-IN-LINE	1
9			74LS221	IC, DUAL-IN-LINE	1
10			74LS373	IC, DUAL-IN-LINE	7
11			74LS273	IC, DUAL-IN-LINE	2
12		HARRIS	HI506A-5	IC, DUAL-IN-LINE	1
13		SPRAGUE	TPQ6502	IC, DUAL-IN-LINE	1
14			75141	IC, DUAL-IN-LINE	1
15			761-1-R4.7K	RESISTOR PACK, CTS DIP, 4.7K OHM	2
16			CF141K5%	RESISTOR, 1K, 1/4W, 5%	2
17			CF184.7K5%	RESISTOR, 4.7K, 1/8W, 5%	1
18			CF1851K5%	RESISTOR, 51K, 1/8W, 5%	1
19			CF145.6K5%	RESISTOR, 5.6K, 1/4W, 5%	4
20			CF182K5%	RESISTOR, 20K, 1/8W, 5%	2

NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A53510B002 REV - DATE 11-02-92 PAGE 3 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21			CF146.2K5%	RESISTOR, 6.2K, 1/4W, 5%	4
22			RN55C3012E	RESISTOR, 30.1K, 1/8W, 1%	2
23			RN55C103F	RESISTOR, 10K, 1/8W, 1%	6
24			RN55C4991F	RESISTOR, 4990, 1/8W, 1%	2
25			RN55C1003F	RESISTOR, 100K, 1/8W, 1%	2
26			RN55C4871F	RESISTOR, 4870, 1/8W, 1%	2
27			RN55C1R00F	RESISTOR, 1, 1/8W, 1%	2
28		BOURNES	3386T-01-201	POTENTIOMETER, 200Ω, 1/8W	2
29		MALLORY	CS13BD226K	CAPACITOR, 22μf, 15V, 10%	1
30		ERIE	RPE114Z5U225M	CAPACITOR, 22μf, 50V, 10%	1
31			1N914	DIODE	1
32			CF181K5%	RESISTOR, 1K, 1/8W, 5%	1
33			CF183.9K5%	RESISTOR, 3.9K, 1/8W, 5%	1
34			CF182.2K5%	RESISTOR, 2.2K, 1/8W, 5%	1
35		CORNING	CAC03Z5U273M100A	CAPACITOR, .027μf, 100V	19
36		TI	TL082BCP	IC, DUAL-IN-LINE	1
37		MOTOROLA	LM393AN	IC, DUAL-IN-LINE	1
38		ANALOG DEVICES	AD584JH	10V REFERENCE IN TO-5 CASE	1
39		ALPHA	7053	WIRE, WHT/GRY, #26 GA.	15'
40		ALPHA	7055	WIRE, BLU, #22 GA.	3'
41		ALPHA	7055	WIRE, VIO, #22 GA.	3'
42		ALPHA	7056/19	WIRE, ORG, #20 GA.	2'

NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A53510B002 REV - DATE 11-02-92 PAGE 4 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
43		ALPHA	7056/19	WIRE, RED, #20 GA.	2'
44		ALPHA	7056/19	WIRE, GRY, #20 GA.	2'
45		ALPHA	7056/19	WIRE, YEL, #20 GA.	2'
46		ALPHA	7056/29	WIRE, BLK, #20 GA.	2'
47		ALPHA	411755	WIRE, GRN/BLK, #26 GA. TWISTED PAIR	3'
48		ALPHA	411755	WIRE, RED/BLK, #26 GA. TWISTED PAIR	3'
49		ALPHA	411755	WIRE, WHT/BLK, #26 GA. TWISTED PAIR	3'
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
60					
61					
62					
63					

REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
C	1-91	ANDREATTA		REDRAWN WITH ACAD ;

CPU ADDRESS/DATA BUS

CONTROL/MONITOR LINE BUFFERS

PARALLEL I/O P1

SERIAL I/O P2

U1 INTEL P8032AH uCONT — CONTROL PROCESSOR

U2 INTEL D8755A-2 — EPROM PROGRAM MEMORY

U5 INTEL P8156H-2 — RAM-I/O

U10 74LS245

U11 74LS245

U8 75174 DIFF DRIVER

U9 75175 DIFF RECEIVER

U12B 96LS02

U7A 74LS221

U7B 74LS221

U3 74LS173

U18 LS04

U15 LS00

U17 LS10

U16 LS04

RELATIVE ADDR TO ADDR BUS DRIVER U4 (SHT 2)

STB/ACK FROM U12-7 (SHT 2)

R/W U13-1 (SHT 2)

IOR U17-4 (SHT 2)

12 BIT ANALOG CONV. FROM U14 (SHT 2)

RESET LINK

R to D - FOR SYSTEM RESET INPUT (P2-5,6)
R to G - FOR EXTERNAL RESET INPUT (P2-23)

WARNING :
CPU U1 WILL NOT RUN IF LINK "R" IS LEFT FLOATING. IT MUST BE TERMINATED TO LINK "G" OR "D".

INSTALL HAND WIRE LINK TO P1.7 OR DESIRED SIGNAL

EXTERNAL INDICATOR DRIVER

ACTIVITY INDICATORS (EXTERNAL)

(EXTERNAL) P/O USERS DEVICE

RESET SWITCH

NOTES :

1. ALL IC's ARE 'LS' LOGIC UNLESS OTHERWISE INDICATED.
2. USE EXACT PART NUMBERS ONLY ON U1, U2, AND U5. DO NOT SUBSTITUTE.
3. BYPASS CAPACITORS (.01 'Cx' ON ASSEMBLY DWG.) NOT SHOWN.
4. * = NOT USED.
5. ALL RESISTOR VALUES ARE IN OHMS.

ACAD : SIBDSK-1

A55002B002	BOM
D55002A002	ASSEMBLY
D55002P002	DRILL DWG.
D55002Q002	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±
MATERIAL :
FINISH :

VLBA PROJECT : STANDARD INTERFACE BOARD

TITLE : STANDARD INTERFACE BOARD MODEL 'D' SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY HARDEN	DATE 12-85
DESIGNED BY WEBER	DATE 5-84
APPROVED BY	DATE

SHEET NUMBER 1 of 2 | DRAWING NUMBER D55002S002 | REV. C | SCALE —

REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
C	1-91	ANDREATTA		REDRAWN WITH ACAD ;

PARALLEL I/O P1

+5V 50 → +5V DISTR
5V COMM 34 → DIGITAL GND
+15V 40 → +15V DISTR
HIQ GND 38 → ANALOG GND
-15V 39 → -15V DISTR
DEV ACK 36 ← DEVICE ACKNOWLEDGE
ANENB 37 ← ANALOG ENABLE
HI/LO SEL 17

R/W U16-12 (SHT 1)
IOR U2-39 (SHT 1)
PU1
R7 1K
74LS74 U13
LS10 U17
LS00 U15
U16 LS04
U12A 96LS02
R6 15K
C6 220pF
STRB/ACR → TO U1-12 CPU INTR-0 (SHT 1)

H = D0-D11 IS IN HI-Z STATE
L = D0-D11 DUMPED ON BUS

(25 uS) (500 uS)

S/H CONT (66) BUSY (24) STRB (48) EN1 EN2 EN3 (54 56 53) D11 EN (41)
(L = CONVERSION IN PROGRESS)
OUTPUT D0-D11
SHORT CYCLE (26)

+5V C10 1 uF, C9 .01 uF
-15V C15 1 uF, C14 .01 uF
ANALOG GND
+15V C13 1 uF, C12 .01 uF
ANALOG COMM (63)

U14
SDM854BG (BURR-BROWN)
ANALOG DATA ACQUISITION SYSTEM

CONFIGURED FOR

8-CHAN DIFFERENTIAL INPUTS
BIPOLAR OPERATION (±10V RANGE)
12-BIT RESOLUTION (4.8828 mV/BIT)
2's COMPLIMENT OUTPUT CODING
OUTPUT IS ONE 12-BIT WORD, HI-Z DRIVERS

DIFFERENTIAL ANALOG INPUTS

ANLG-0 H 1 / L 18 → CH1+ (11) / CH1- (70)
ANLG-1 H 2 / L 19 → CH2+ (10) / CH2- (71)
ANLG-2 H 3 / L 20 → CH3+ (9) / CH3- (72)
ANLG-3 H 4 / L 21 → CH4+ (8) / CH4- (73)
ANLG-4 H 5 / L 22 → CH5+ (7) / CH5- (74)
ANLG-5 H 6 / L 23 → CH6+ (6) / CH6- (75)
ANLG-6 H 7 / L 24 → CH7+ (5) / CH7- (76)
ANLG-7 H 8 / L 25 → CH8+ (4) / CH8- (77)

D0 (29 LSB) → CON/MON-4
D1 (30) → CON/MON-5
D2 (31) → CON/MON-6
D3 (32) → CON/MON-7
D4 (33) → CON/MON-8
D5 (34) → CON/MON-9
D6 (35) → CON/MON-10
D7 (36) → CON/MON-11
D8 (37) → CON/MON-12
D9 (38) → CON/MON-13
D10 (39) → CON/MON-14
D11 (40)
D11 (44 MSB) → CON/MON-15

CON/MON BUS (12-BIT ANALOG CONVERSION) TO P1 (SHT 1)

MUX EN1 (12)
MUX EN2 (13)
CLR (18) +5V
S/H OFFSET (67) RV3 1K, R9 24K — FINE OFFSET ADJ

A0 (19) A1 (20) A2 (21) A3 (22) DIG GND (25) LOAD (23) DLY OUT (45) TRIG (46) DLY ADJ (47) BPO (59) 2.5V REF OUT (55) IN (57) MUX OUT - (78) + (2) 20V RANGE (58) S/H OUT (62) S/H IN (68)

+5V 470 → HI/LO SEL
U6 74LS157 (1Y 2Y 3Y 4Y; SEL; G (15); 1A 1B 2A 2B 3A 3B 4A 4B)
ADDR-0 (11) ADDR-3 (10) ADDR-1 (2) ADDR-4 (3) ADDR-2 (14) ADDR-5 (13) (5) (6)
250 uS — LOAD REG, TRIG A/D
C11 .01 uF (250 uS)
RV2 50 ZERO, RV1 100 GAIN
R10 240

FOR 4.8828 mV/bit INSTALL JUMPER IN LIEU OF R10
FOR 5.0 mV/bit INSTALL 240 OHM WW RESISTOR PER BURR-BROWN SPECS

RG1 (1) RG2 (4) (5) (10) (8)
NC (2) (3) OFFSET (6) (7) (9)
-15V +15V

U19
BURR-BROWN INA101CM INSTR. AMPL.
U19 PIN OUT (TOP VIEW)

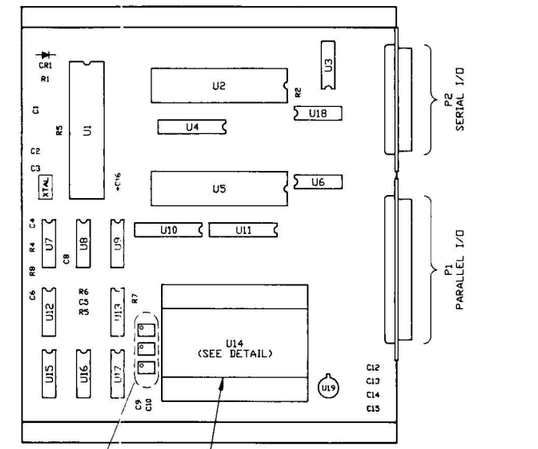
+5V 470 → PU2
FROM U2 (SHT 1)
74LS245 ADDR BUS DRIVER
U4 (20)
RA0 (9) RA1 (8) RA2 (7) RA3 (6) RA4 (5) RA5 (4) RA6 (3) RA7 (2) DIR (1) (10)
A0 A1 A2 A3 A4 A5 A6 A7
B0 (11) B1 (12) B2 (13) B3 (14) B4 (15) B5 (16) B6 (17) B7 (18) G (19)
ADDR-0 ADDR-1 ADDR-2 ADDR-3 ADDR-4 ADDR-5 ADDR-6 ADDR-7
ADDRESS BUS

PARELLEL I/O P1
ADDR-0 (48) → RA-0
ADDR-1 (47) → RA-1
ADDR-2 (46) → RA-2
ADDR-3 (45) → RA-3
ADDR-4 (44) → RA-4
ADDR-5 (43) → RA-5
ADDR-6 (42) → RA-6
ADDR-7 (41) → RA-7

SERIAL I/O P2

+5V DISTR → 1, 14 → +5V
DIGITAL GND → 13, 25 → LOGIC COMM
+15V DISTR → 15 → +15V
ANALOG GND → 17 → ±15V COMM
-15V DISTR → 16 → -15V

EXTERNAL ACCESSORY DC POWER AVAILABLE FOR TEST AND ALIGNMENT PURPOSES



ACAD : SIBDSK-2

A55002B002	BOM
D55002A002	ASSEMBLY
D55002P002	DRILL DWG.
D55002Q002	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: 2 PLACE DECIMALS (.XX) ±
3 PLACE DECIMALS (.XXX) ±
4 PLACE DECIMALS (.XXXX) ±
MATERIAL :
FINISH :

ANALOG CIRCUITRY

VLBA PROJECT: STANDARD INTERFACE BOARD

TITLE: STANDARD INTERFACE BOARD MODEL 'D' SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

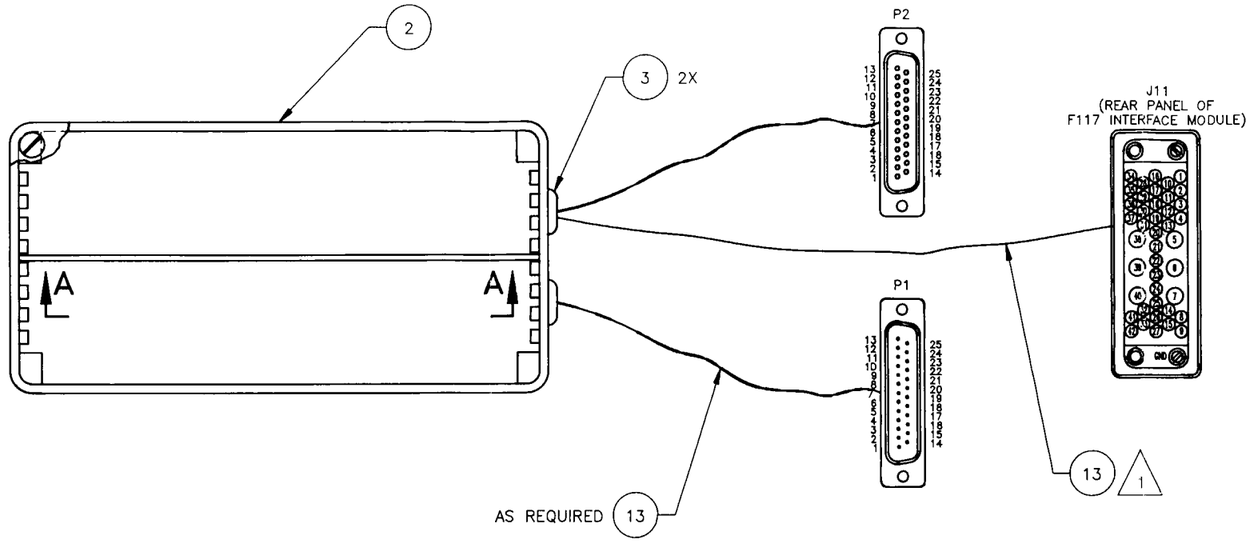
DRAWN BY HARDEN	DATE 12-85
DESIGNED BY WEBER	DATE 5-84
APPROVED BY	DATE

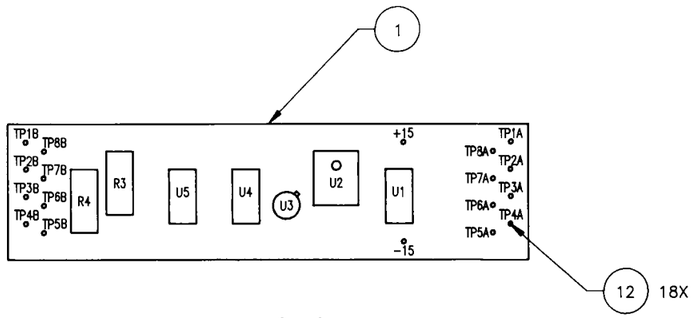
SHEET NUMBER 2 of 2 | DRAWING NUMBER D55002S002 | REV. C | SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. ONE WIRE ATTACHES TO J11, PIN 30 ON REAR PANEL OF F117 INTERFACE MODULE, NRAO DRAWING #D53510A001





VIEW A-A
COMPONENT SIDE

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
13				WIRE	AR
12				PIN, WIRE WRAP	18
11	U5		LM324	INTEGRATED CIRCUIT	1
10	U4		DG200	INTEGRATED CIRCUIT	1
9	U3		AD581LH	INTEGRATED CIRCUIT	1
8	U2		MC7805CT	INTEGRATED CIRCUIT	1
7	U1		74S04	INTEGRATED CIRCUIT	1
6	R3, R4		RC42GF102J	RESISTOR, 1K, 2W, 5%	2
5	P2		DB-25S	CONNECTOR	1
4	P1		DB-25P	CONNECTOR	1
3				GROMMET	2
2				BOX, ENCLOSURE	1
1				PERFBOARD	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.000) ±
2 PLACE DECIMALS (.00) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLBA PROJECT

FRONT END INTERFACE

TITLE
F117
LOOP BACK TEST
FIXTURE ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY K. TATE	DATE 12-92
DESIGNED BY L.D. MAY	DATE 12-92
APPROVED BY	DATE

C53510S005	SCHEMATIC
NEXT ASSEMBLY	DWG. TYPE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C53510A007 | REV. — | SCALE NONE

ACAD : 53510A07

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

P2. CONTROL (PINS)

GND 1
+15v 2
-15v 3
NC 4
NC 5
X CMD 6
C CMD 7
H CMD 8
F PARITY 9
NC 10
NCAL OUT 11
HCAL OUT 12
GND 13
F0 14
F1 15
F2 16
F3 17
S0 18
S1 19
S2 20
S3 21
S4 22
S5 23
M0 24
M1 25

U2 MC7805CT (IN, OUT, GND) → +5V TO 74904, PIN 14
GND TO 74904, PIN 7

U3 AD581LH (+VS, VOUT, GND)

R1 220
R2 1K → +8.3V

U4 DG200 (IN1, IN2, V+, V-, GND)

U1A, U1B, U1C, U1D, U1E, U1F — 74904

TP1A TP1B TP2A TP2B TP3A TP3B TP4A TP4B TP5A TP5B TP7A TP7B TP8A TP8B

U5A, U5B, U5C, U5D — LM324 (+15 / -15)

R3 1K/2W TP6B
R4 1K/2W TP5B

TP+15 → +15
C1 100 MFD/ 100V
TP-15 → -15

P1. MONITOR (SOCKETS)

1 PUMP VAC
2 DEWAR VAC
3 15 K
4 50 K
5 300 K
6 AC CURRENT
7 RCP1 BIAS
8 RCP2 BIAS
9 LCP1 BIAS
10 LCP2 BIAS
11 LED V
12 NC
13 Q GROUND
14 VAC SENS
15 ANLG 3+
16 ANLG 3-
17 ADDR 0
18 ADDR 1
19 ADDR 2
20 SOL MON
21 PUMP MON
22 H MON
23 X MON
24 C MON
25 H MON

ORCAD : 53510S05

PROPERTY OF NRAO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

853510A007	ASSEMBLY
NEXT ASSEMBLY	DWG TYPE

VLBA PROJECT

TITLE: F117 LOOP BACK SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY L.D. MAY	DATE 12/92
DESIGNED BY L.D. MAY	DATE 12/92
APPROVED BY	DATE

SHEET NUMBER 1 OF 1	DRAWING NUMBER C535109005	REV. -	SCALE -

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
G	12-92	K. TATE		UPDATED TO NRAO STANDARDS

STATE COMMAND WRT. RD.

CAL COMMAND WRT. RD.

DIGITAL ID WORD RD.

IDREAD

DIGITAL ID WORD RD.

DIGITAL ADDR.

DIGITAL MON. WORD

ANALOG ADDR.

CAL/HI-CAL DRIVER

MODULATOR FREQ.

SINGLE ENDED LINE RCV

POWER-UP RESET

NOTE: C1 IS NON-POLARIZED

CAL CURRENT MONITOR

HI-CAL CURRENT MON.

SERIAL #

C2 IS CONNECTED WITH THE POSITIVE SIDE TO PIN 2 AND NEG. TO 8.

MOUNT AD584 WITH PIN 8, THE TAB, CONNECTED TO THE HEADER PIN 16.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES: ANGLES ±

3 PLACE DECIMALS (.XXX): ±

2 PLACE DECIMALS (.XX): ±

1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSEMBLY | DWG TYPE

VLBA PROJECT

FRONT END INTERFACE

TITLE: F117 MODULE SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY

SOCORRO, NEW MEXICO 87801

DRAWN BY: K. TATE	DATE: 12-82
DESIGNED BY	DATE
APPROVED BY	DATE
SHEET NUMBER: 1 OF 1	DRAWING NUMBER: C53510S003 REV. G SCALE -

ORCAD : 53510S03

This wire list was abstracted from "Technical Manual, F117, FRONT END CONTROL MODULE " by E. Schlecht, July 1990.

VLBA FRONT END MODULE F117 INTERNAL WIRING HARNESS JULY,7,1987
DRAWING:A53510W006 WILLIAM WIREMAN
NOTE: (L) INDICATES THE SIGNAL IS LOW TRUE, EX. HI-LO(L) LO=LOW SIGNAL

PART I-WIREWRAP CONNECTOR WIRING

PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1.	GND	REF GND	BLK	22	2.	5V	TB1-4	ORG	22
3.	GND				4.	5V			
5.	ANLG 4+	P1-5	WHT/GRY	26	6.	ANLG 5+	P1-6	WHT/VIO	26
7.					8.	Q GND	J1-13	BLK	22
9.	*Q GND	P1-19	BLK	26	10.	ANLG 1 & 2+	P1-2	WHT/GRN	26
11.	R/W(L)	P1-49	WHT/BLU	26	12.	DEV REQ	P1-35	WHT/BRN	26
13.	ANLG 6+	P1-7	WHT/YEL	26	14.	ANLG 7+	P1-8	WHT/BLK	26
15.	DEV ACK	P1-36	WHT/GRY	26	16.	ID READ	P2-9	WHT/ORG	26
17.	HI-LO(L)SEL	P1-17	WHT/GRN	26	18.	ANENB	P1-37	WHT/VIO	26
19.	S/N 0	GND/5V	BUSS	26	20.	S/N 1	GND/5V	BUSS	26
21.	S/N 2	GND/5V	BUSS	26	22.	S/N 3	GND/5V	BUSS	26
23.	S/N 4	GND/5V	BUSS	26	24.	S/N 5	GND/5V	BUSS	26
25.	S/N 6	GND/5V	BUSS	26	26.	S/N 7	GND/5V	BUSS	26
27.	GND	WW BD	BUSS	26	28.	5V	WW BD	BUSS	26

NOTE: STRAP SERIAL/NUMBER TO PIN 27 FOR ZERO AND PIN 28 FOR A ONE. EX. S/N=18
STRAP S/N 0,2,3,5,6&7 TO GND PIN 27, AND S/N 1&4 TO +5V PIN 28

29.	ADDR 0	P1-48,J1-17	WHT/VIO	26	30.	ADDR 1	P1-47,J1-18	WHT/YEL	26
31.	ADDR 2	P1-46,J1-19	WHT/BLK	26	32.	ADDR 3	P1-45	WHT/RED	26
33.	ADDR 4	P1-44	WHT/BLK	26	34.	ADDR 5	P1-43	WHT/YEL	26
35.	C/M 0	P1-33	WHT/ORG	26	36.	C/M 1	P1-16	WHT/ORG	26
37.	C/M 2	P1-32	WHT/BLU	26	38.	C/M 3	P1-15	WHT/BLU	26
39.	C/M 4	P1-31	WHT/RED	26	40.	C/M 5	P1-14	WHT/RED	26
41.	C/M 6	P1-30	WHT/BLK	26	42.	C/M 7	P1-13	WHT/BLK	26
43.	C/M 8	P1-29	WHT/YEL	26	44.	C/M 9	P1-12	WHT/YEL	26
45.	C/M 10	P1-28	WHT/VIO	26	46.	C/M 11	P1-11	WHT/VIO	26
47.	C/M 12	P1-27	WHT/GRY	26	48.	C/M 13	P1-10	WHT/GRY	26
49.	GND				50.				
51.	C/M 14	P1-26	WHT/BRN	26	52.	C/M 15	P1-9	WHT/BRN	26
53.					54.				
55.	CAL	J2-11	BLU	22	56.	HI-CAL	J2-12	VIO	22
57.	LF1	J1-9	WHT/RED	26	58.	RF1	J1-7	WHT/YEL	26
59.	LF2	J1-10	WHT/BLU	26	60.	RF2	J1-8	WHT/BLK	26
61.	15 K	J1-3	WHT/GRN	26	62.	50 K	J1-4	WHT/BRN	26
63.	300 K	J1-5	WHT/GRY	26	64.	VD	J1-2	WHT/ORG	26
65.	VP	J1-1	WHT/BLU	26	66.	ACI	J1-6	WHT/VIO	26
67.	LED(L)	J1-11	WHT/ORG	26	68.	SENS	J1-14	WHT/GRN	26
69.	PA	J2-9	WHT/RED	26	70.	H(L)	J2-8	WHT/BLK	26
71.	C	J2-7	WHT/YEL	26	72.	X	J2-6	WHT/VIO	26
73.	GND				74.				
75.	H-MON(L)	J1-25	WHT/GRY	26	76.	C-MON	J1-24	WHT/BRN	26
77.	X-MON	J1-23	WHT/GRN	26	78.	M(L)	J1-22	WHT/ORG	26
79.	P	J1-21	WHT/BLU	26	80.	S	J1-20	WHT/RED	26
81.	F 0	J2-14	WHT/BLK	26	82.	F 1	J2-15	WHT/RED	26
83.	F 2	J2-16	WHT/BLU	26	84.	F 3	J2-17	WHT/ORG	26
85.	M 0	J2-24	WHT/RED	26	86.	M 1	J2-25	WHT/BLU	26
87.	S 0	J2-18	WHT/GRN	26	88.	S 1	J2-19	WHT/BRN	26
89.	S 2	J2-20	WHT/GRY	26	90.	S 3	J2-21	WHT/VIO	26
91.	S 4	J2-22	WHT/YEL	26	92.	S 5	J2-23	WHT/BLK	26
93.	MOD	FT-6	WHT/RED	26	94.	-15V	TB1-5	YEL	22
95.	15V	TB1-6	RED	22	96.	28V	TB1-7	GRY	22
97.	GND				98.	5V			
99.	GND	REF GND	BLK	22	100.	5V	TB1-4	ORG	22

PART II-STANDARD INTERFACE BOARD WIRING

JACK P1					JACK P2			
PIN	FUNCTION	SOURCE	COLOR	GA	PIN	FUNCTION	SOURCE	COLOR	GA
1.					1.	5V			
2.	ANLG 1+	W-10	WHT/GRN	26	2.				
3.	ANLG 2+	P1-2	BUSS	26	3.				
4.	ANLG 3+	J1-15	WHT/BRN	26	4.				
5.	ANLG 4+	W-5	WHT/GRY	26	5.				
6.	ANLG 5+	W-6	WHT/VIO	26	6.				
7.	ANLG 6+	W-13	WHT/YEL	26	7.				
8.	ANLG 7+	W-14	WHT/BLK	26	8.				
9.	C/M 15	W-52	WHT/BRN	26	9.	ID READ	W-16	WHT/ORG	26
10.	C/M 13	W-48	WHT/GRY	26	10.				
11.	C/M 11	W-46	WHT/VIO	26	11.				
12.	C/M 9	W-44	WHT/YEL	26	12.				
13.	C/M 7	W-42	WHT/BLK	26	13.	GND	REF GND	BLK	22
14.	C/M 5	W-40	WHT/RED	26	14.	5V	TB1-4	ORG	22
15.	C/M 3	W-38	WHT/BLU	26	15.	15V	TB1-6	RED	22
16.	C/M 1	W-36	WHT/ORG	26	16.	-15V	TB1-5	YEL	22
17.	HI-LO(L)SEL	W-17	WHT/GRN	26	17.				
18.					18.				
19.	*Q GND	W-9	BLK	26	19.	RCV+	FT-7	WHT-PR	26
20.	*Q GND	P1-19	BUSS	26	20.	RCV-	FT-9	BLK-PR	26
21.	ANLG 3-	J1-16	WHT/GRY	26	21.	XMIT+	FT-8	RED-PR	26
22.	ANLG 4-	P1-38	BUSS	26	22.	XMIT-	FT-10	BLK-PR	26
23.	ANLG 5-	P1-38	BUSS	26	23.				
24.	ANLG 6-	P1-38	BUSS	26	24.				
25.	ANLG 7-	P1-38	BUSS	26	25.	GND			
26.	C/M 14	W-51	WHT/BRN	26					
27.	C/M 12	W-47	WHT/GRY	26					
28.	C/M 10	W-45	WHT/VIO	26					
29.	C/M 8	W-43	WHT/YEL	26					
30.	C/M 6	W-41	WHT/BLK	26					
31.	C/M 4	W-39	WHT/RED	26					
32.	C/M 2	W-37	WHT/BLU	26					
33.	C/M 0	W-35	WHT/ORG	26					
34.	GND	REF GND	BLK	22					
35.	DEV REQ	W-12	WHT/BRN	26					
36.	DEV ACK	W-15	WHT/GRY	26					
37.	ANENB	W-18	WHT/VIO	26					
38.	GND	P1-22,23,24,25	BUSS	26					
39.	-15V	TB1-5	YEL	22					
40.	15V	TB1-6	RED	22					
41.									
42.									
43.	ADDR 5	W-34	WHT/YEL	26					
44.	ADDR 4	W-33	WHT/BLK	26					
45.	ADDR 3	W-32	WHT/RED	26					
46.	ADDR 2	W-31	WHT/BLK	26					
47.	ADDR 1	W-30	WHT/YEL	26					
48.	ADDR 0	W-29	WHT/VIO	26					
49.	R/W(L)	W-11	WHT/BLU	26					
50.	5V	TB1-4	ORG	22					

PART III-REAR PANEL CONNECTOR WIRING

JACK 11 (AMP 42 PIN)

PIN	FUNCTION	SOURCE	COLOR	GA	PIN	FUNCTION	SOURCE	COLOR	GA
1.					2.				
3.					4.				
5.					6.				
7.					8.	XMIT+	FT-8	RED-PR	26
9.	XMIT-	FT-10	BLK-PR	26	10.	5V	FT-2	ORG	20
11.					12.	MOD	FT-6	WHT/RED	26
13.					14.	RCV+	FT-7	WHT-PR	26
15.	RCV-	FT-9	BLK-PR	26	16.	15V	FT-5	RED	20
17.	-15V	FT-3	YEL	20	18.				
19.					20.				
21.					22.				
23.					24.				
25.					26.				
27.					28.				
29.	28V	FT-4	GRY	20	30.				
31.					32.				
33.					34.	GND	FT-1	BLK	20
35.					36.				
37.					38.				
39.					40.				
41.					42.				

PART VI-FRONT PANEL CONNECTOR WIRING

J1-MONITOR

PIN	FUNCTION	SOURCE	COLOR	GA
1.	VP	W-65	WHT/BLU	26
2.	VD	W-64	WHT/ORG	26
3.	15 K	W-61	WHT/GRN	26
4.	50 K	W-62	WHT/BRN	26
5.	300 K	W-63	WHT/GRY	26
6.	ACI	W-66	WHT/VIO	26
7.	RF1	W-58	WHT/YEL	26
8.	RF2	W-60	WHT/BLK	26
9.	LF1	W-57	WHT/RED	26
10.	LF2	W-59	WHT/BLU	26
11.	LED	W-67	WHT/ORG	26
12.				
13.	Q GND	W-8	BLK	22
14.	SENS	W-68	WHT/GRN	26
15.	ANLG 3+	P1-3	WHT/BRN	26
16.	ANLG 3-	P1-20	WHT/GRY	26
17.	ADDR 0	W-29	WHT/VIO	26
18.	ADDR 1	W-30	WHT/YEL	26
19.	ADDR 2	W-31	WHT/BLK	26
20.	S	W-80	WHT/RED	26
21.	P	W-79	WHT/BLU	26
22.	M(L)	W-78	WHT/ORG	26
23.	X MON	W-77	WHT/GRN	26
24.	C MON	W-76	WHT/BRN	26
25.	H MON(L)	W-75	WHT/GRY	26

J2-CONTROL

PIN	FUNCTION	SOURCE	COLOR	GA
1.	GND	REF GND	BLK	22
2.	15V	TB1-6	RED	22
3.	-15V	TB1-5	YEL	22
4.				
5.				
6.	X	W-72	WHT/VIO	26
7.	C	W-71	WHT/YEL	26
8.	H(L)	W-70	WHT/BLK	26
9.	PA(L)	W-69	WHT/RED	26
10.				
11.	CAL	W-55	BLU	22
12.	HI-CAL	W-56	VIO	22
13.	GND	REF GND	BLK	22
14.	F 0	W-81	WHT/BLK	26
15.	F 1	W-82	WHT/RED	26
16.	F 2	W-83	WHT/BLU	26
17.	F 3	W-84	WHT/ORG	26
18.	S 0	W-87	WHT/GRN	26
19.	S 1	W-88	WHT/BRN	26
20.	S 2	W-89	WHT/GRY	26
21.	S 3	W-90	WHT/VIO	26
22.	S 4	W-91	WHT/YEL	26
23.	S 5	W-92	WHT/BLK	26
24.	M 0	W-85	WHT/RED	26
25.	M 1	W-86	WHT/BLU	26

PART V-POWER DISTRIBUTION TERMINAL BLOCK

POWER SUPPLY INPUT					POWER DISTRIBUTION		
PIN	FUNCTION	SOURCE	COLOR	GA	SOURCE	COLOR	GA
TB1-1	GND	FT-1	BLK	20	GND REF	BLK	22
TB1-2							
TB1-3							
TB1-4	5V	FT-2	ORG	20	P1-50, P2-14, W-2, W-100	ORG	22
TB1-5	-15V	FT-3	YEL	20	P1-39, P2-16, W-94, J2-3	YEL	22
TB1-6	15V	FT-5	RED	20	P1-40, P2-15, W-95, J2-2	RED	22
TB1-7	28V	FT-4	GRY	20	W-96	GRY	22

PART IV-REAR SHIELD PANEL, FILTER FEEDTHRU

INTERNAL CONNECTIONS				REAR PANEL CONNECTIONS			
PIN SOURCE	SOURCE	COLOR	GA	PIN SOURCE	SOURCE	COLOR	GA
1. GND	TB1-1	BLK	20	1. GND	J11-34	BLK	20
2. 5V	TB1-4	ORG	20	2. 5V	J11-10	ORG	20
3. -15V	TB1-5	YEL	20	3. -15V	J11-17	YEL	20
4. 28V	TB1-7	GRY	20	4. 28V	J11-29	GRY	20
5. 15V	TB1-6	RED	20	5. 15V	J11-16	RED	20
6. MOD	W-93	WHT/RED	26	6. MOD	J11-12	WHT/RED	26
7. REC +	P2-19	WHT-PR	26	7. REC +	J11-14	WHT-PR	26
8. XMIT +	P2-21	RED-PR	26	8. XMIT +	J11-8	RED-PR	26
9. REC -	P2-20	BLK-PR	26	9. REC -	J11-15	BLK-PR	26
10. XMIT -	P2-22	BLK-PR	26	10. XMIT -	J11-9	BLK-PR	26

NOTE:WIRES ON FEEDTHRU'S 7 & 9, 8 & 10 ARE TWISTED PAIRS

5.0 DATA SHEETS

This section contains the following data sheets:

Front-End Data Sheets

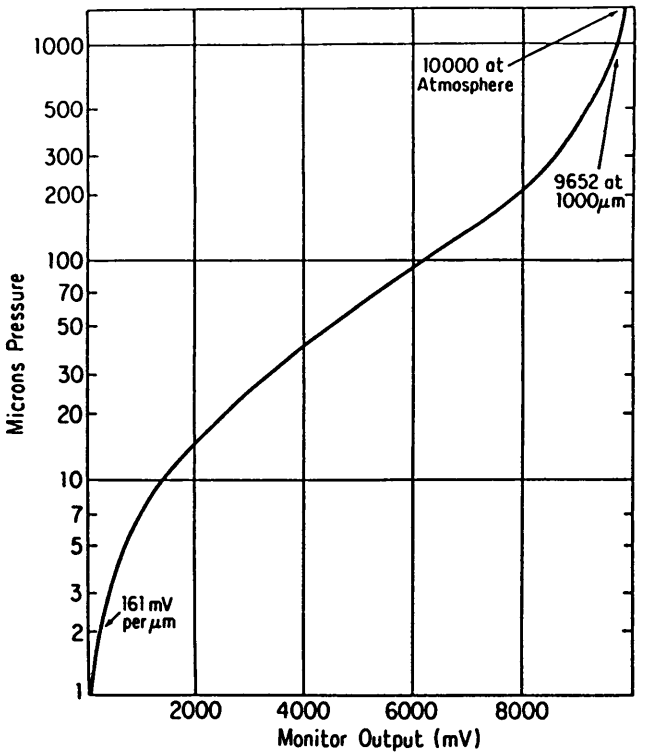
Front-End Vacuum Pressure as a function of Monitor Output Voltage
Front-End Card Cage Assembly, D53203A004

F117 Data Sheets

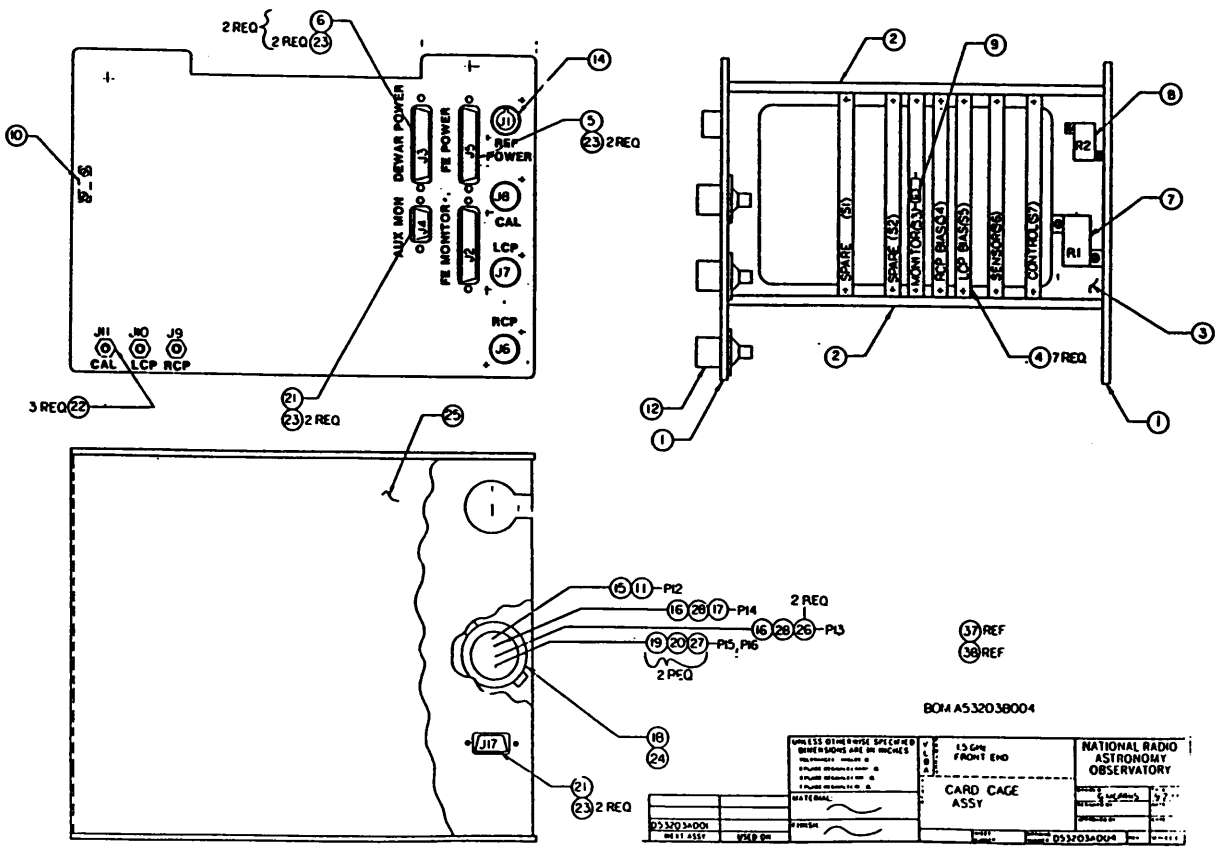
HI506A Harris Analog Multiplexer
LF442A National Semiconductor Operational Amplifier
LM393 National Semiconductor Analog Comparator
AD584 Analog Devices Pin-Programmable Voltage Reference
TPQ6502 Sprague Quad Transistor Array
75141 Texas Instruments Dual, Single-Ended Line Receiver

F117 Loop Back Test Fixture Data Sheets

AD581 Analog Devices High Precision 10 V IC Reference
LM324 National Semiconductor Low Power Quad Operational Amplifier
HI200 Harris Dual SPST CMOS Analog Switch



Vacuum Pressure as a Function of Monitor Output Voltage



HARRIS HI-506A/507A

Single 16/Differential 8 Channel CMOS Analog Multiplexer with Active Overvoltage Protection

Features

- Analog Overvoltage Protection.....70 Vpp
- No Channel Interaction During Overvoltage
- ESD Resistent.....>4,000 Volts
- 44 V Maximum Power Supply
- Fail Safe with Power Loss (No Latchup)
- Break-Before-Make Switching
- Analog Signal Renge.....±15 V
- Access Time (Typicel).....500 ns
- Standby Power (Typicel).....7.5 mW

Applications

- Data Acquisition
- Indue trial Controls
- Telemetry

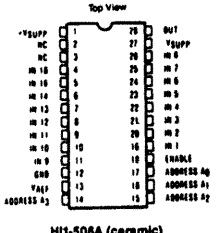
Description

The HI-506A and HI-507A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-506A and HI-507A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 506A is a 16 channel device and the 507A is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

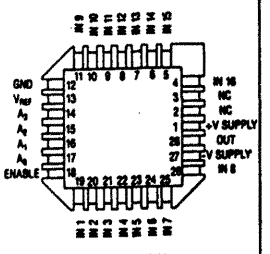
Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC package.

The HI-506A/507A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "-8" suffix.

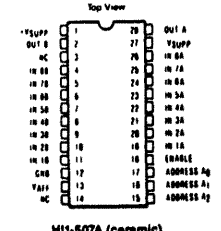
Pinouts



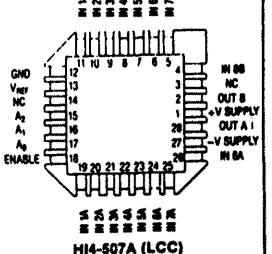
HI1-506A (ceramic)
HI3-506A (plastic)



HI4-506A (LCC)

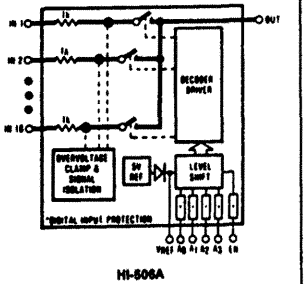


HI1-507A (ceramic)
HI3-507A (plastic)

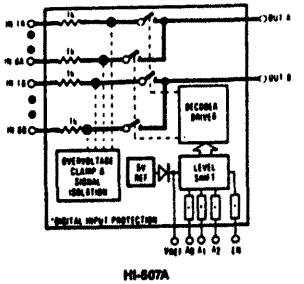


HI4-507A (LCC)

Functional Diagrams



HI-506A



HI-507A

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supply Pins	44 V
V_{REF} to Ground, V+ to Ground	22 V
V− to Ground	25 V
Digital Input Overvoltage:	
V_{EN}, V_A { VSupply(+)	+4 V
V_{EN}, V_A { VSupply(−)	−4 V
or 20 mA, whichever occurs first.	
Analog Input Overvoltage:	
V_S { VSupply(+)	+20 V
V_S { VSupply(−)	−20 V

Continous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 msec, 10% duty cycle max):	40 mA
Power Dissipation* (Cerdip)	2.0 W
Operating Temperture Range:	
HI-506A/507A-2,-8	−55°C to +125°C
HI-506A/507A-5	0°C to +75°C
Storage Temperture Range	−65°C to +150°C

*Derate 20.0 mW/°C above T_A =75°C

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified:

Supplies = +15 V, −15 V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0 V; V_{AL} (Logic Level Low) = + 0.8 V. For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/HI-507A -2, -8 MIN.	TYP.	MAX.	HI-506A/507A -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
*I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				µA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-507A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
*V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH}	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low) (Note 8)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		µs
(0.01%)	+25°C		3.5			3.5		µs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I−, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = −100 µA.
3. Test nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 10 kHz. Worst case isolation occurs on channel as due to proximity of the output pins.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1 kΩ pull-up resistors to +5.0 V supply are recommended.
9. V_{REF} = +10 V.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

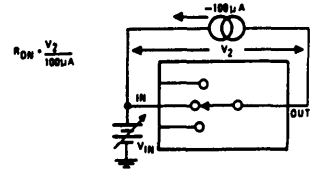
A_2	A_1	A_0	EN	ON CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Performance Characteristics and Test Circuits

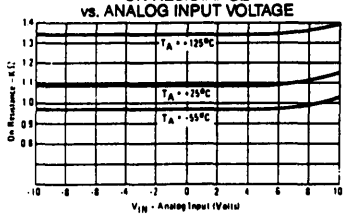
Unless Otherwise Specified: T_A = 25°C, VSupply = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

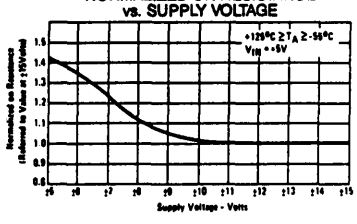
TEST CIRCUIT NO. 1



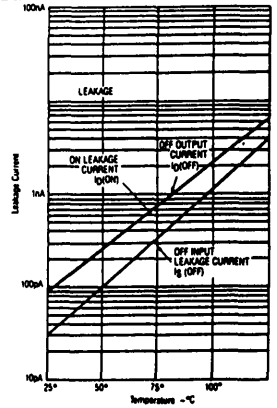
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



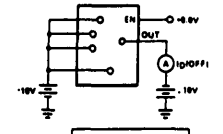
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



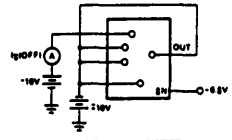
LEAKAGE CURRENT VS. TEMPERATURE



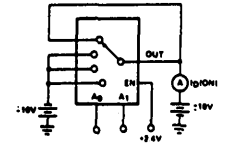
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

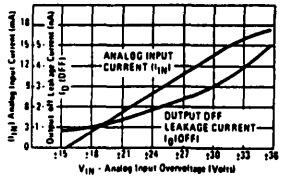


TEST CIRCUIT NO. 4*



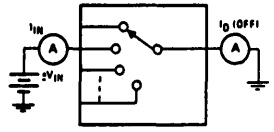
*Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for I_D(OFF): +10 V/−10 V and −10 V/+10 V.)

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



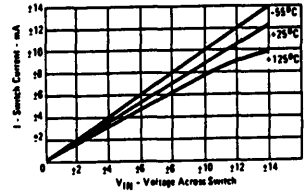
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



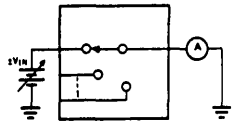
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

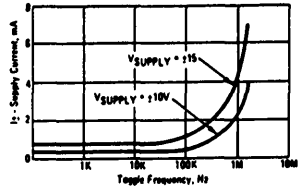


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

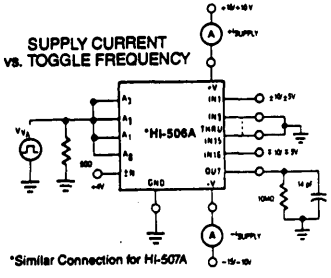


SUPPLY CURRENT vs. TOGGLE FREQUENCY

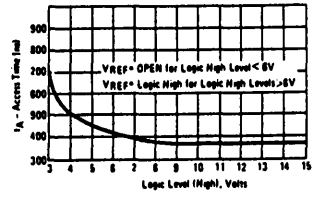


TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY

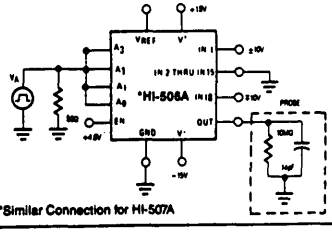


ACCESS TIME VS. LOGIC LEVEL (HIGH)

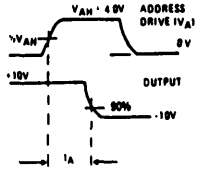


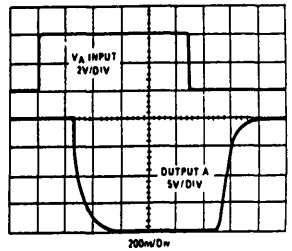
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)



Switching Waveforms

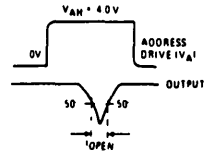


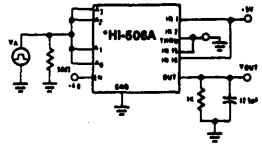


Switching Waveforms (continued)

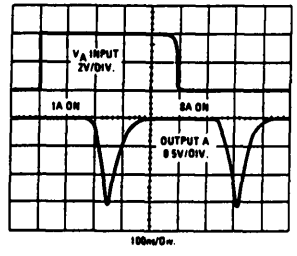
TEST CIRCUIT NO. 9

BREAK-BEFORE-MAKE DELAY (tOPEN)





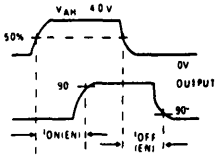
BREAK-BEFORE-MAKE DELAY(tOPEN)



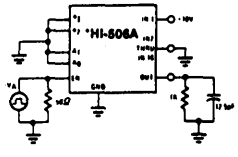
*Similar Connection for HI-507A

TEST CIRCUIT NO. 10

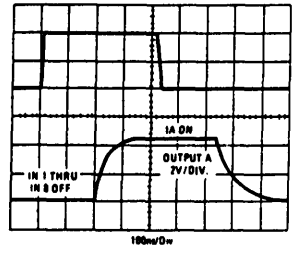
ENABLE DRIVE



ENABLE DELAY (tON(EN),tOFF(EN))

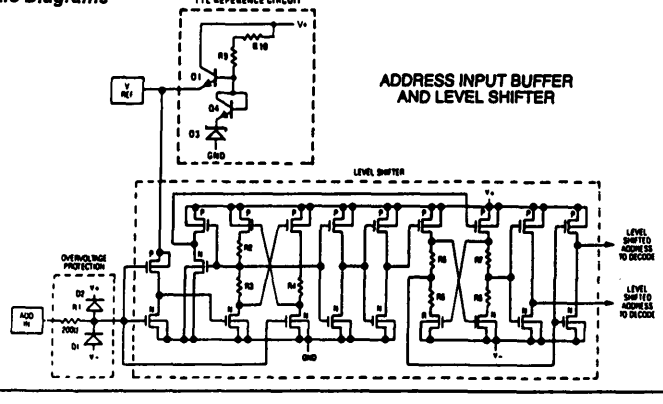


ENABLE DELAY (tON(EN),tOFF(EN))

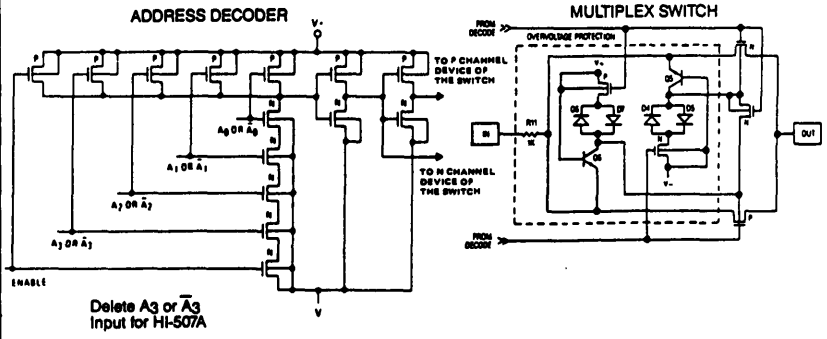


*Similar Connection for HI-507A

Schematic Diagrams



Schematic Diagrams (continued)



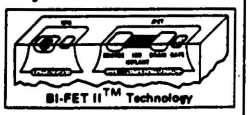
Delete A_3 or $\overline{A_3}$ Input for HI-507A

Die Characteristics

Transistor Count		485	
Die Size		161 x 85 mils	
Thermal Constants	θ_{ja}	50°C/W	For Ceramic DIP
	θ_{jc}	18°C/W	For Ceramic DIP
Tie Substrate to:		-VSupply	
Process:		CMOS-DI	

National Semiconductor

Operational Amplifiers/Buffers



LF442A/LF442 Dual Low Power JFET Input Operational Amplifier

General Description

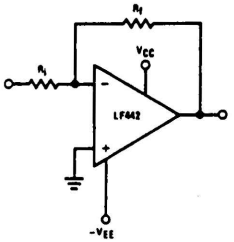
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM1458	400 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	1 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	10^{12} Ω
■ High gain V_O = ± 10V, R_L = 10k	50k (min)

Typical Connection



Ordering Information

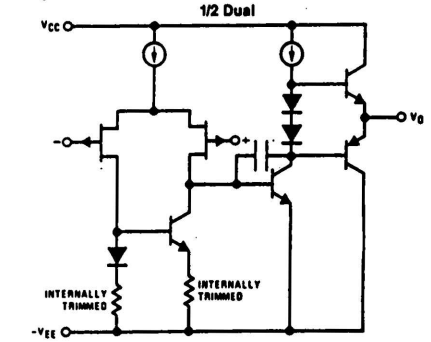
LF442XYZ

X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Simplified Schematic



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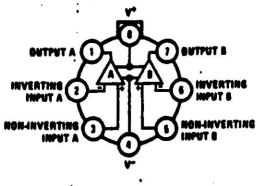
Connection Diagrams

LF442AMH, LF442ACH, LF442CH
Metal Can Package

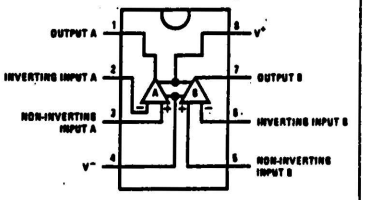


TOP VIEW

Note. Pin 4 connected to case.

Order Number LF442AMH, LF442ACH or LF442CH
See NS Package H08B

LF442ACN, LF442CN
Dual-In-Line Package



TOP VIEW

Order Number LF442ACN or LF442CN
See NS Package N08A

Absolute Maximum Ratings

	LF442A	LF442
Supply Voltage	± 22V	± 18V
Differential Input Voltage	± 38V	± 30V
Input Voltage Range (Note 1)	± 19V	± 15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 3)	670 mW	500 mW
T_j max	150°C	115°C
θ_{jA}	150°C/W	160°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF442A Min	LF442A Typ	LF442A Max	LF442 Min	LF442 Typ	LF442 Max	Units
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ			7	10		7		μV/°C
I_{OS}	Input Offset Current	V_S = ± 15V (Notes 5 and 6)	T_j = 25°C		5	25		5	50	pA
			T_j = 70°C			1.5			1.5	nA
			T_j = 125°C			10				nA
I_B	Input Bias Current	V_S = ± 15V (Notes 5 and 6)	T_j = 25°C		10	50		10	100	pA
			T_j = 70°C			3			3	nA
			T_j = 125°C			20				nA
R_{IN}	Input Resistance	T_j = 25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ± 15V, V_O = ± 10V, R_L = 10 kΩ, T_A = 25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S = ± 15V, R_L = 10 kΩ		± 12	± 13		± 12	± 13		V
V_{CM}	Input Common-Mode Voltage Range			± 16	+18 −17		± 11	14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le$ 10 kΩ		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF442A Min	LF442A Typ	LF442A Max	LF442 Min	LF442 Typ	LF442 Max	Units
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	V_S = ± 15V, T_A = 25°C	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	V_S = ± 15V, T_A = 25°C	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1 kHz		35			35		nV/√Hz
i_n	Equivalent Input Noise Current	T_A = 25°C, f = 1 kHz		0.01			0.01		pA/√Hz

Notes

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

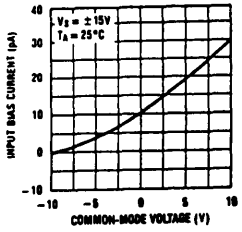
Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442 V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

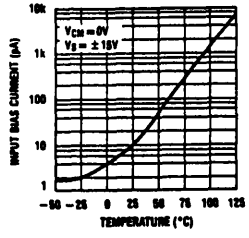
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

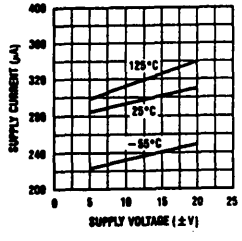
Input Bias Current



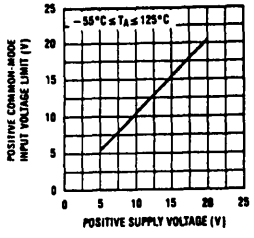
Input Bias Current



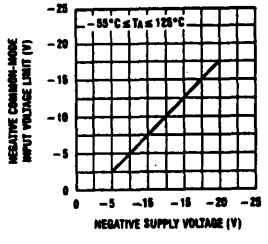
Supply Current



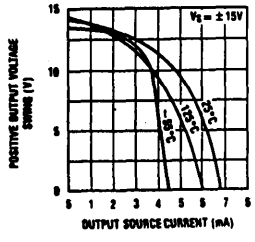
Positive Common-Mode Input Voltage Limit



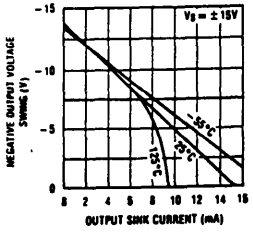
Negative Common-Mode Input Voltage Limit



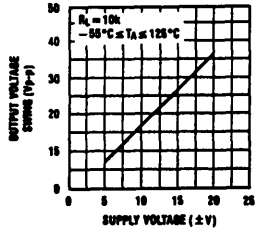
Positive Current Limit



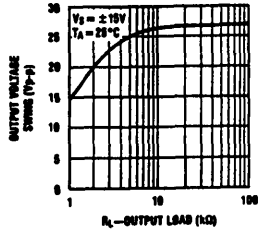
Negative Current Limit



Output Voltage Swing

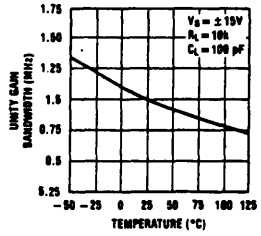


Output Voltage Swing

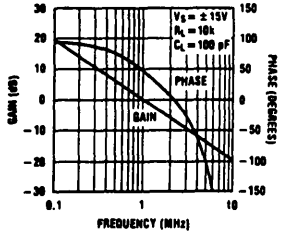


Typical Performance Characteristics (Continued)

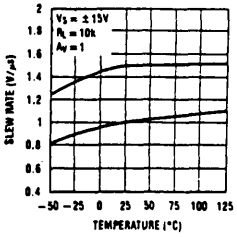
Gain Bandwidth



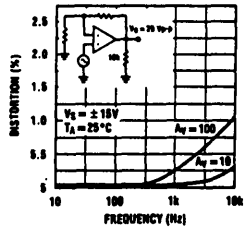
Bode Plot



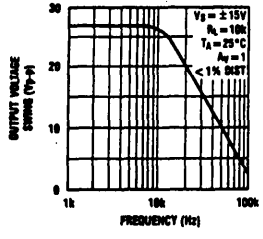
Slew Rate



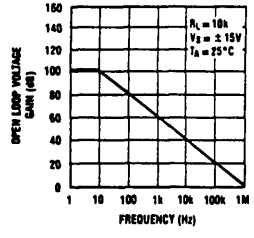
Distortion vs Frequency



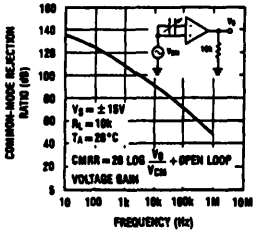
Undistorted Output Voltage Swing



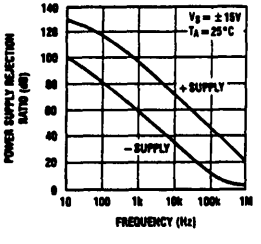
Open Loop Frequency Response



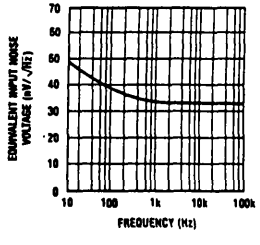
Common-Mode Rejection Ratio



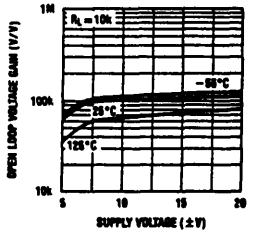
Power Supply Rejection Ratio



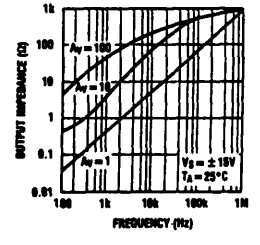
Equivalent Input Noise Voltage



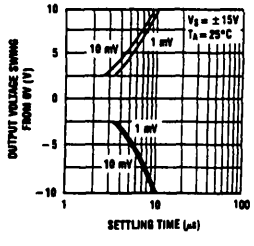
Open Loop Voltage Gain



Output Impedance



Inverter Settling Time

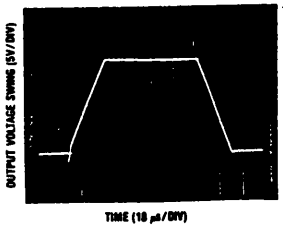


Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

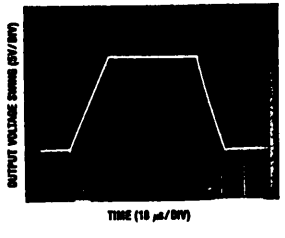
Small Signal Inverting

Small Signal Non-Inverting

Large Signal Inverting



Large Signal Non-Inverting



Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

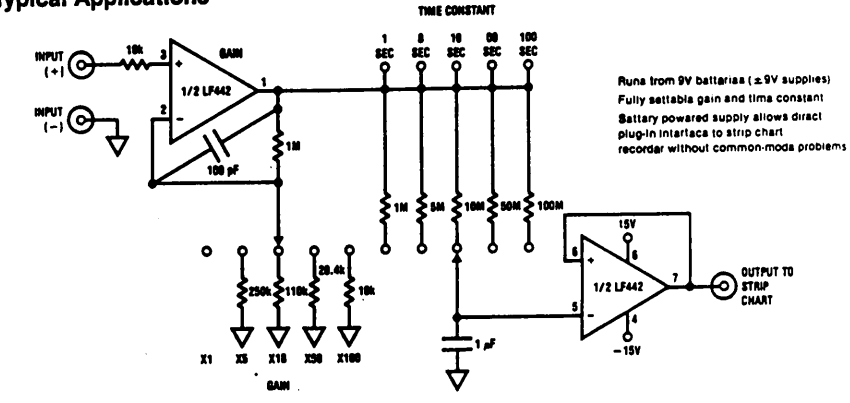
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

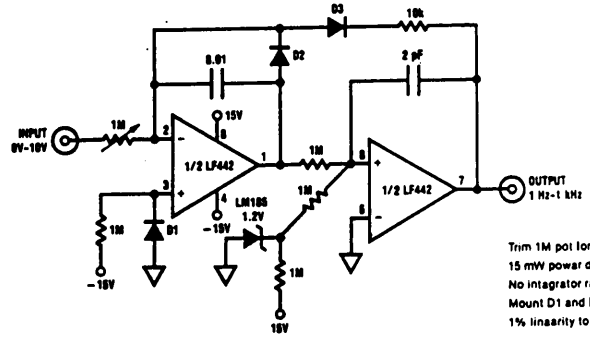
Typical Applications

Battery Powered Strip Chart Preamplifier



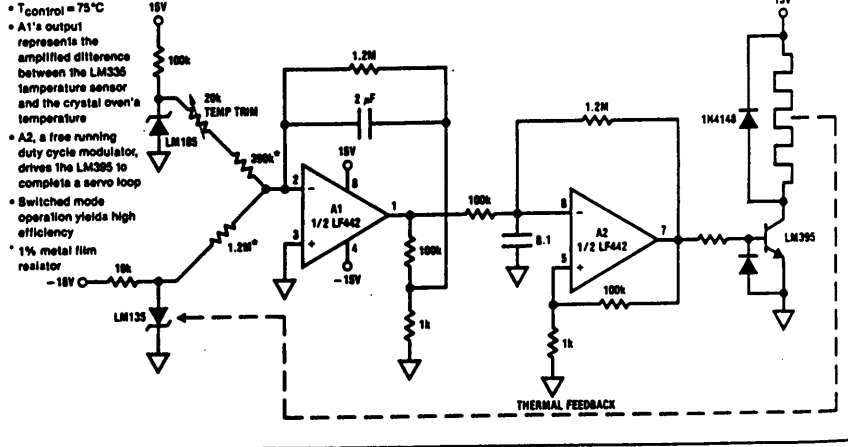
Runs from 9V batteries (±9V supplies)
Fully settable gain and time constant
Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

"No FET" Low Power V–F Converter



Trim 1M pot for 1 kHz full-scale output
15 mW power drain
No integrator reset FET required
Mount D1 and D2 in close proximity
1% linearity to 1 kHz

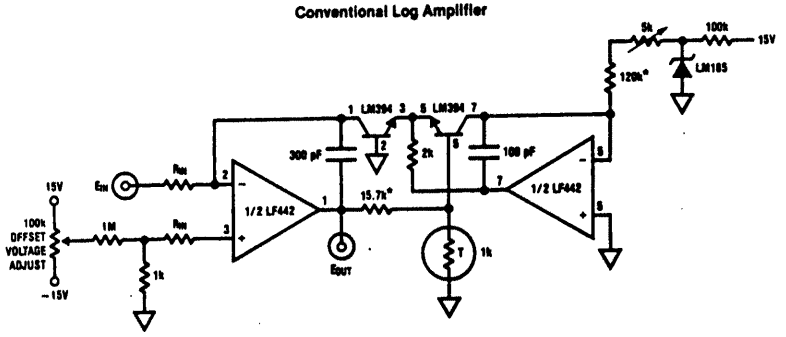
High Efficiency Crystal Oven Controller



- $T_{control} = 75°C$
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- * 1% metal film resistor

Typical Applications (Continued)

Conventional Log Amplifier



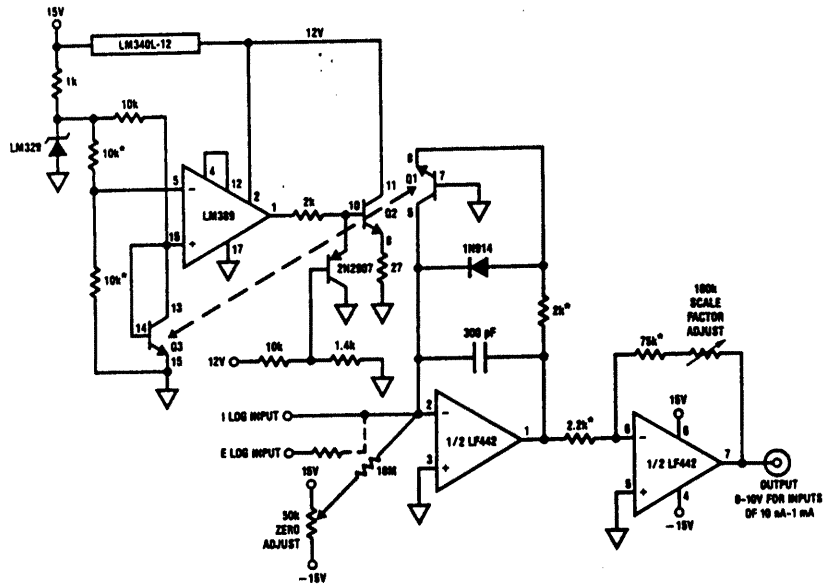
$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

(RT) = Tel Labs type QB1

Trim 5k for 10 μA through the 5k-120k combination

*1% film resistor

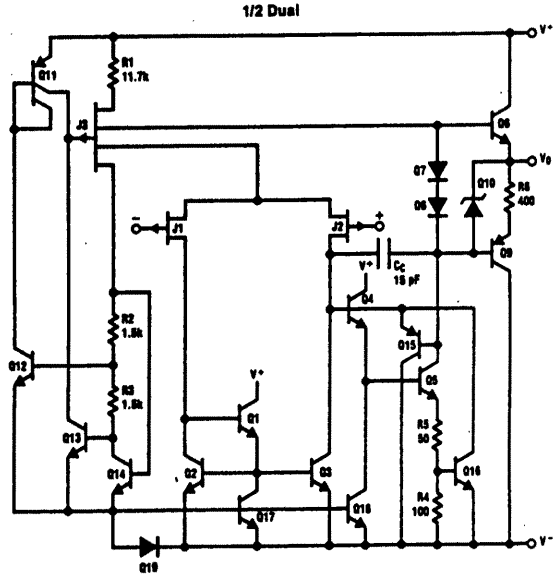
Unconventional Log Amplifier



Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair. Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.

Detailed Schematic

1/2 Dual



National Semiconductor

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparetors also have a unique characteristic in that tha input common-mode voltage range includas ground, even though operated from a single power supply voltaga.

Application areas include limit comparators, simple analog to digital converters; pulse, squerewave and time dalay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drein is a distinct advantage over standard comparators.

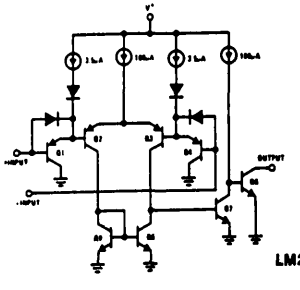
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

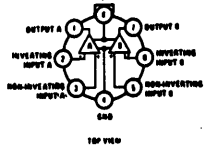
Features

- Wide single supply
  Voltage renge 2.0 V_{OC} to 36 V_{DC}
  or duel supplies ±1.0 V_{OC} to ±18 V_{DC}
- Very low supply current drain (0.8 mA)—independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA
  saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

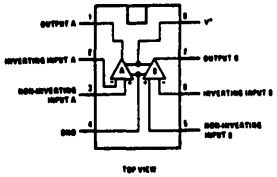


Metal Can Package



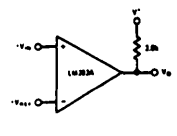
Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

Dual-In-Line Package

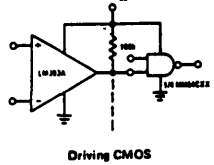


Order Number LM393N, LM393AN, or LM2903N
See NS Package N08B

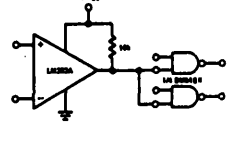
Typical Applications (V^+ = 5.0 V_{OC})



Basic Comparator



Driving CMOS



Driving TTL

Absolute Maximum Ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP	570 mW
Metal Can	830 mW
Output Short-Circuit to Ground, (Note 2)	Continuous
Input Current (V_{IN} < −0.3 V_{DC}), (Note 3)	50 mA
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V^+ = 5 V_{DC}) (Note 4)

PARAMETER	CONDITIONS	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C, (Note 8)		±1.0	±2.0		±1.0	±2.0		±1.0	±5.0		±1.0	±5.0		±2.0	±7.0	mVDC
Input Bias Current	$I_{(IN^+)}$ or I_{IN^-} with Output in Linear Range, T_A = 25°C, (Note 5)		25	100		25	250		25	100		25	250		25	250	nADC
Input Offset Current	$I_{IN^+} - I_{IN^-}$, T_A = 25°C		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5.0	±50	nADC
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		V^+ − 1.5	0		V^+ − 1.5	0		V^+ − 1.5	0		V^+ − 1.5	0		V^+ − 1.5	VDC
Supply Current	R_L = ∞ on All Comparators, T_A = 25°C		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mADC
	R_L = ∞ on All Amps, V^+ = 30 VDC		1	2.5		1	2.5			2.5			2.5		1	2.5	mADC
Voltage Gain	R_L ≥ 15 kΩ, T_A = 25°C, V^+ = 15 VDC (To Support Large V_O Swing)	50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 VDC V_{RL} = 5 VDC, R_L = 5.1 kΩ, T_A = 25°C		300			300			300			300			300		ns
Response Time	V_{RL} = 5 VDC, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3			1.3			1.3			1.5		µs
Output Sink Current	V_{IN^-} ≥ 1 VDC, V_{IN^+} = 0, V_O ≤ 1.5 VDC, T_A = 25°C	6.0	16		6.0	16		6.0	16		6.0	16		6	16		mADC
Saturation Voltage	V_{IN^-} ≥ 1 VDC, V_{IN^+} = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400		250	400		250	400		250	400			400	mVDC
Output Leakage Current	V_{IN^-} = 0, V_{IN^+} ≥ 1 VDC, V_O = 5 VDC, T_A = 25°C		0.1			0.1			0.1			0.1			0.1		nADC

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM193A			LM2903			LM293A, LM393A			LM293, LM393			LM193			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 9)			4.0		9	15		4.0			9			9		mVDC
Input Offset Current	$I_{IN+} - I_{IN-}$		±100			50	200		±150			±150			±100		nADC
Input Bias Current	I_{IN+} or I_{IN-} with Output in Linear Range		300	400		200	500		400			400			300	400	nADC
Input Common-Mode Voltage Range		0	$V^+-2.0$		0	$V^+-2.0$		0	$V^+-2.0$		0	$V^+-2.0$		0	$V^+-2.0$		VDC
Saturation Voltage	$V_{IN-} \geq 1$ VDC, $V_{IN+} = 0$, $I_{SINK} \leq 4$ mA.		700			400	700		700			700			700		mVDC
Output Leakage Current	$V_{IN-} = 0$, $V_{IN+} \geq 1$ VDC, $V_O = 30$ VDC.		1.0			1.0			1.0			1.0			1.0		μADC
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 VDC for V^-, (if Used). (Note 8)		36			28			36			36			36		VDC

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A/LM2903 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: The input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 VDC.

Note 4: These specifications apply for $V^+ = 5$ VDC and −55°C ≤ TA ≤ +125°C, unless otherwise stated. With the LM293/LM293A all temperature specifications are limited to −25°C ≤ TA ≤ +85°C and the LM393/LM393A temperature specifications are limited to 0°C ≤ TA ≤ +70°C. The LM2903 is limited to −40°C ≤ TA ≤ +85°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5$V, but either or both inputs can go to 30 VDC without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 VDC (or 0.3 VDC below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O = 1.4$ VDC, RS = 0Ω with V^+ from 5 VDC to 30 VDC; and over the full input common-mode range (0 VDC to $V^+ - 1.5$ VDC).

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

Typical Performance Characteristics LM2903

Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

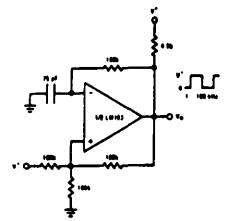
The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

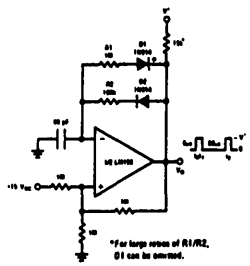
The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

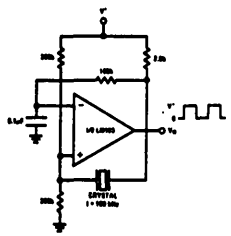
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



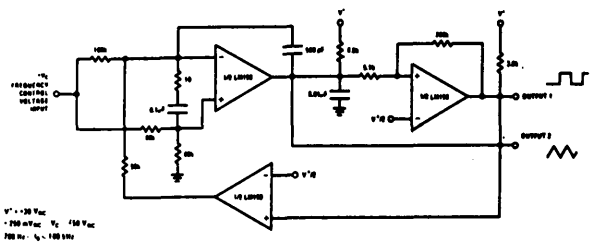
Squarewave Oscillator



Pulse Generator

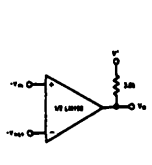


Crystal Controlled Oscillator

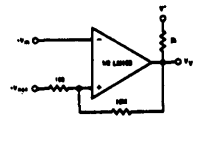


Two-Decade High-Frequency VCO

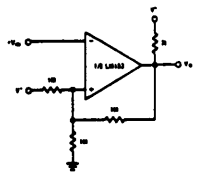
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



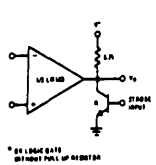
Basic Comparator



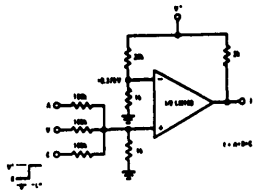
Non-Inverting Comparator with Hysteresis



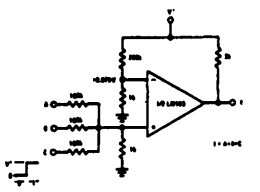
Inverting Comparator with Hysteresis



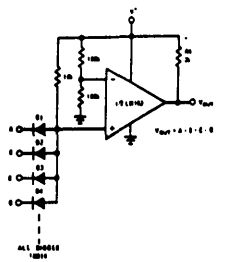
Output Strobing



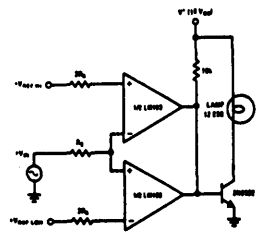
AND Gate



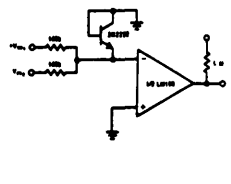
OR Gate



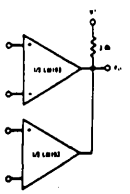
Large Fan-in AND Gate



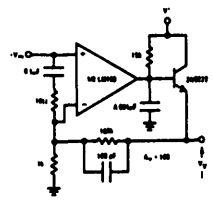
Limit Comparator



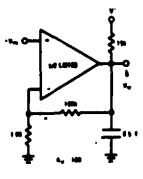
Comparing Input Voltages of Opposite Polarity



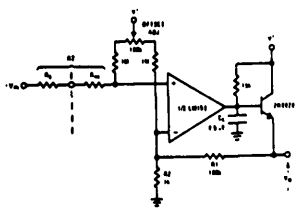
ORing the Outputs



Improved Op Amp

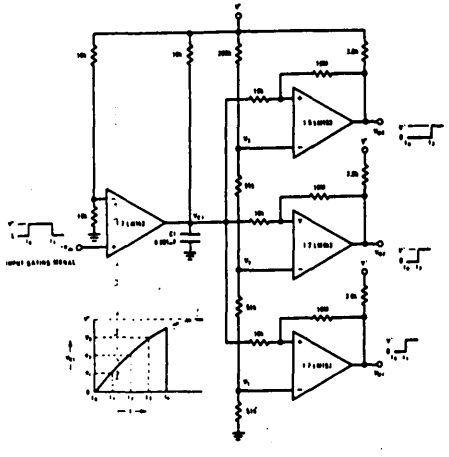


Low Frequency Op Amp

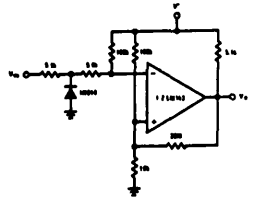


Low Frequency Op Amp with Offset Adjust

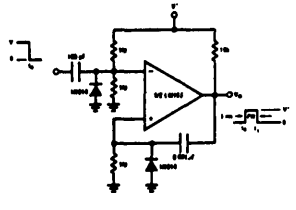
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



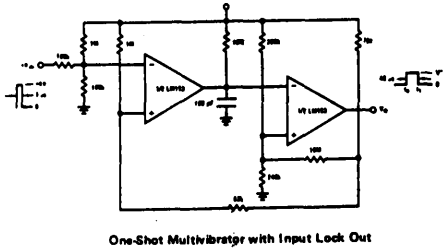
Time Delay Generator



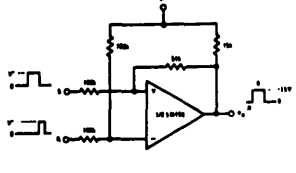
Zero Crossing Detector (Single Power Supply)



One-Shot Multivibrator

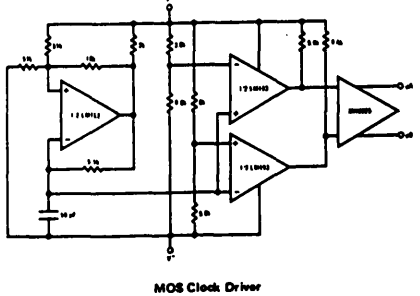


One-Shot Multivibratgr with Input Lock Out

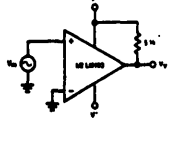


Bi-Stable Multivibrator

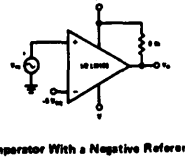
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)



MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference

ANALOG DEVICES

Pin Programmable Precision Voltage Reference

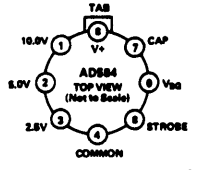
AD584*

FEATURES

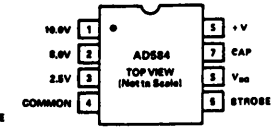
- Four Programmable Output Voltages: 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient: 5ppm/°C max, 0 to +70°C (AD584L) 15ppm/°C max, −55°C to +125°C (AD584T)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability

AD584 PIN CONFIGURATIONS

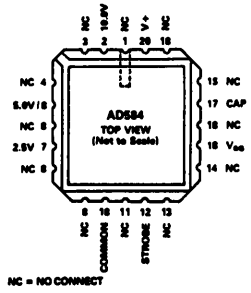
8-Pin TO-99



8-Pin DIP



20-Pin LCC



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C and packaged in 8-pin plastic packages; the AD584S and T are specified for the -55°C to +125°C range. All grades are packaged in a hermetically sealed eight-terminal TO-99 metal can and 20-pin LCC for surface mount applications.

*Covered by U.S. Patent No. 3,887,863; RE 30,586

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).

SPECIFICATIONS (@ V_{IN} = 15V and 25°C)

Model	AD584J Min	AD584J Typ	AD584J Max	AD584K Min	AD584K Typ	AD584K Max	AD584L Min	AD584L Typ	AD584L Max	Units
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal Outputs of:										
10.000V			±30			±10			±5	mV
7.500V			±20			±8			±4	mV
5.000V			±15			±6			±3	mV
2.500V			±7.5			±3.5			±2.5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]										
10.000, 7.500, 5.000V Outputs			30			15			5	ppm/°C
2.500V Output			30			15			10	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5			1.5		μA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		μs
NOISE (0.1 to 10Hz)		50			50			50		μV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
15V≤V_{IN}≤30V			0.002			0.002			0.002	%/V
(V_{OUT} + 2.5V)≤V_{IN}≤15V			0.005			0.005			0.005	%/V
LOAD REGULATION										
0≤I_{OUT}≤5mA, All Outputs		20	50		20	50		20	50	ppm/mA
OUTPUT CURRENT										
V_{IN}=V_{OUT} + 2.5V										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			mA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTIONS[3]										
TO-99 (H-08A)		AD584JH			AD584KH			AD584LH		
Plastic (N-8)		AD584JN			AD584KN			AD584LN		
LCC (E-20A)		AD584JE			AD584KE			AD584LE		

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]See Section 14 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Ground	40V
Power Dissipation @ +25°C	600mW
Operating Junction Temperature Range	−55°C to +125°C
Lead Temperature (Soldering 10sec)	+300°C
Thermal Resistance	
Junction-to-Ambient (H-08A)	150°C/W
(E-20A)	120°C/W

Model	AD584S Min	AD584S Typ	AD584S Max	AD584T Min	AD584T Typ	AD584T Max	Units
OUTPUT VOLTAGE TOLERANCE							
Maximum Error[1] for Nominal Outputs of:							
10.000V			±30			±10	mV
7.500V			±20			±8	mV
5.000V			±15			±6	mV
2.500V			±7.5			±3.5	mV
OUTPUT VOLTAGE CHANGE							
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]							
10.000, 7.500, 5.000V Outputs			30			15	ppm/°C
2.500V Output			30			20	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200		µs
NOISE (0.1 to 10Hz)		50			50		µV p-p
LONG-TERM STABILITY		25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30		mA
LINE REGULATION (No Load)							
$15V \le V_{IN} \le 30V$			0.002			0.002	%/V
$(V_{OUT} + 2.5V) \le V_{IN} \le 15V$			0.005			0.005	%/V
LOAD REGULATION $0 \le I_{OUT} \le 5mA$, All Outputs		20	50		20	50	ppm/mA
OUTPUT CURRENT $V_{IN} \ge V_{OUT} + 2.5V$							
Source @ +25°C	10			10			mA
Source T_{min} to T_{max}	5			5			mA
Sink T_{min} to T_{max}	200			200			µA
Sink −55°C to +85°C	5			5			mA
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	°C
PACKAGE OPTIONS[3]							
TO-99 (H-08A)		AD584SH			AD584TH		
LCC (E-20A)		AD584SE			AD584TE		

NOTES
[1] At Pin 1.
[2] Calculated as average over the operating temperature range.
[3] See Section 14 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Applying the AD584

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

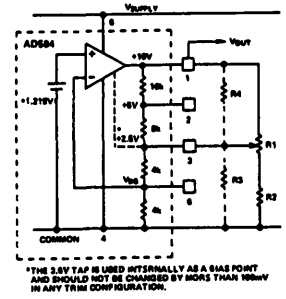


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

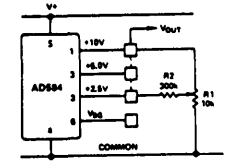


Figure 2. Output Trimming

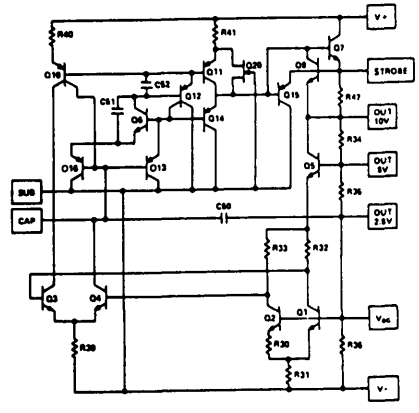


Figure 3. Schematic Diagram

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 4) specified for a particular grade (i.e., S snd T grades); three-point measurement guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

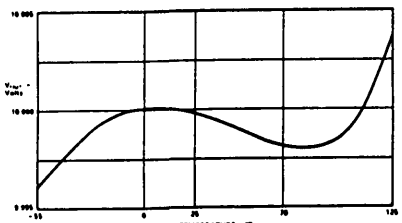


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

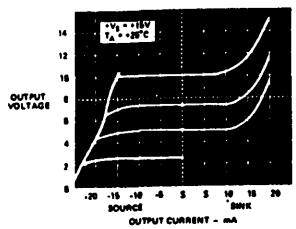


Figure 5. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD584. Figure 6a is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

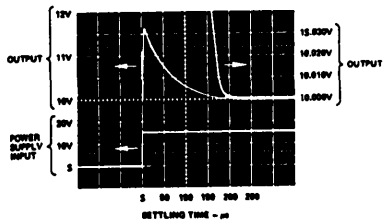


Figure 6. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 8. However, this will tend to increase the turn-on settling time of the device so ample warm-up time should be allowed.

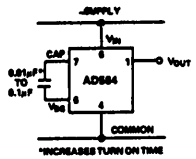


Figure 7. Additional Noise Filtering with an External Capacitor

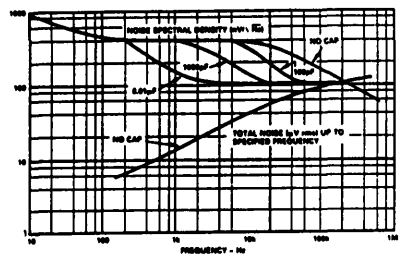


Figure 8. Spectral Noise Density and Total rms Noise vs. Frequency

Applications of the AD584

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 9 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 9.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

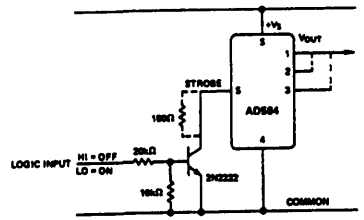


Figure 9. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 10 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

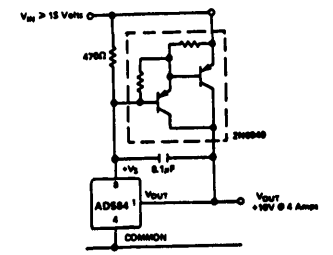


Figure 10. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 11. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

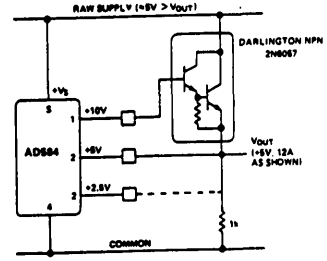


Figure 11. NPN Output Current Booster

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 12). Of course, the minimum voltage required to drive the connection is 5 volts.

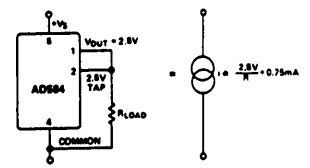


Figure 12. A Two-Component Precision Current Limiter

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the

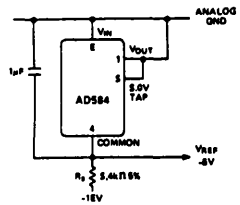


Figure 13. Two-Terminal -5 Volt Reference

device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 14, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

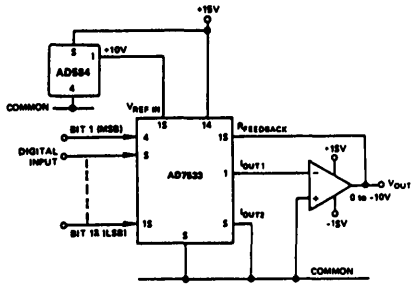


Figure 14. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 15). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k

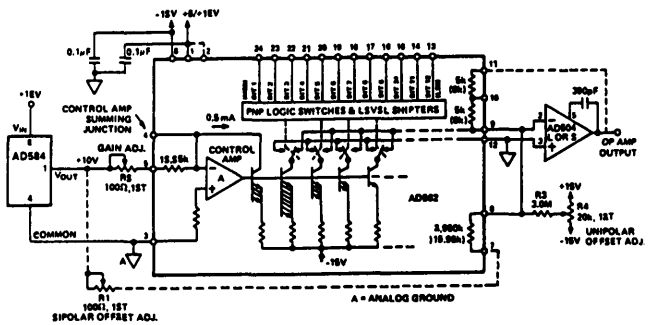
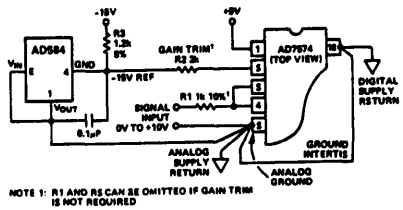


Figure 15. Precision 12-Bit D/A Converter

span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 17 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 16. AD584 as Negative 10 Volt Reference for CMOS ADC

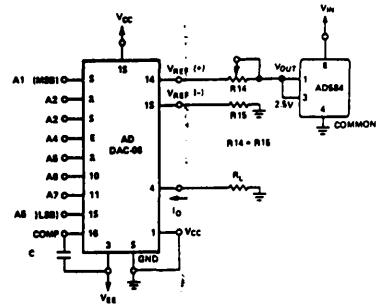
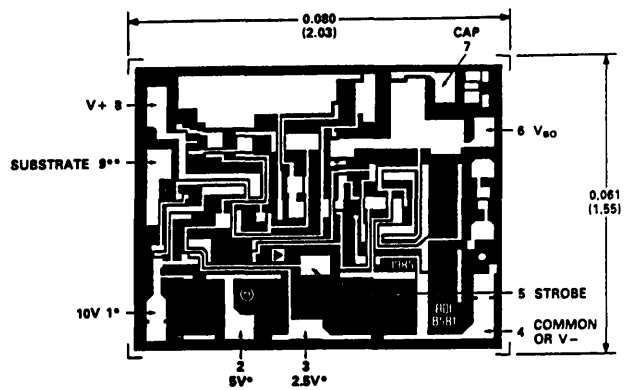


Figure 17. Current Output 8-Bit D/A

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).

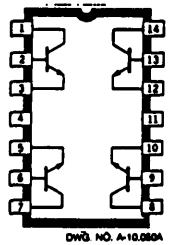


PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8-PIN METAL PACKAGE.
*INTERCONNECTIONS REQUIRED; SEE PIN DESIGNATIONS FOR INFORMATIONS.
**NOT BROUGHT OUT IN PACKAGED DEVICE.

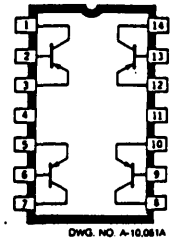
SERIES TPQ
QUAD TRANSISTOR ARRAYS

SPRAGUE SERIES TPQ quad transistor arrays are general-purpose silicon transistor arrays consisting of four independent devices. Shown are 12 NPN types, 12 PNP types, and nine NPN/PNP complementary pairs.

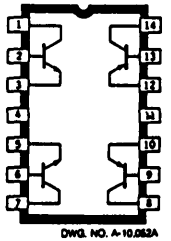
All of these devices are furnished in a 14-pin dual in-line plastic package. The molded package is identical to that used in most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.



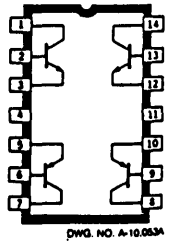
TPQ2221 TPQ3725A
TPQ2222 TPQ3904
TPQ2483 TPQ5550
TPQ2484 TPQ5551
TPQ3724 TPQA05
TPQ3725 TPQA06



TPQ2906 TPQ4258
TPQ2907 TPQ4354
TPQ2907A TPQ5400
TPQ3798 TPQ5401
TPQ3799 TPQA55
TPQ3906 TPQA56



TPQ6001
TPQ6002
TPQ6100
TPQ6100A



TPQ6501
TPQ6502
TPQ6600
TPQ6600A
TPQ6700

ABSOLUTE MAXIUMUM RATINGS

Power Dissipation, P_D (Each Transistor) ..... 500 mW
(Total Package) ..... 2.0 W*
Operating Temperature Range, T_A ..... −55°C to +150°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at the rate of 16 mW/°C above T_A = +25°C

Additional information on
TPP and TPQ Transistor arrays is available from:

Sprague Electric Company
Discrete Semiconductor Operation
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Part Number (See Note)	Min. BV_{CBO} (V)	Min. BV_{CEO} (V)	Min. BV_{EBO} (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	D-C Current Gain Min. h_{FE}	Conditions I_C (mA)	Conditions V_{CE} (V)	Saturation Voltage Max. V_{CE} (V)	Saturation Voltage Max. V_{BE} (V)	@ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	Max. C_{ob} (pF)	Similar Discrete Devices
Two NPN/Two PNP Devices															
TPQ6001	60	30	5.0	30	50	25	1.0	10	0.40	1.30	150	200	50	8.0	2N2221 and 2N2906
						35	10	10	1.40	2.00	300				
						40	150	10							
						20	300	10							
TPQ6002 (Note 1)	60	30	5.0	30	50	50	1.0	10	0.40	1.30	150	200	50	8.0	2N2222 and 2N2907
						75	10	10	1.40	2.00	300				
						100	150	10							
						30	300	10							
TPQ6100	60	40	5.0	10	50	50	0.1	5.0	0.25	0.80	1.0	100	0.5	4.0	2N2483 and 2N3798
						75	0.5	5.0							
						75	1.0	5.0							
						60	10	5.0							
TPQ6100A	60	45	5.0	10	50	100	0.1	5.0	0.25	0.80	1.0	100	0.5	4.0	2N2484 and 2N3799
						150	0.5	5.0							
						150	1.0	5.0							
						60	10	5.0							
TPQ6501	60	30	5.0	30	50	25	1.0	10	0.40	1.30	150	200	50	8.0	2N2221 and 2N2906
						35	10	10	1.40	2.00	300				
						40	150	10							
						20	300	10							
TPQ6502	60	30	5.0	30	50	50	1.0	10	0.40	1.30	150	200	50	8.0	2N2222 and 2N2907
						75	10	10	1.40	2.00	300				
						100	150	10							
						30	300	10							
TPQ6600	60	40	5.0	10	50	50	0.1	5.0	0.25	0.80	1.0	100	0.5	4.0	2N2483 and 2N3798
						75	0.5	5.0							
						75	1.0	5.0							
						60	10	5.0							
TPQ6600A	60	45	5.0	10	50	100	0.1	5.0	0.25	0.80	1.0	100	0.5	4.0	2N2484 and 2N3799
						150	0.5	5.0							
						150	1.0	5.0							
						60	10	5.0							
TPQ6700	40	40	5.0	50	30	30	0.1	1.0	0.25	0.90	10	200	10	4.5	2N3904 and 2N3906
						50	1.0	1.0							
						70	10	1.0							

NOTE:
NPN/PNP complementary pairs. Polarity shown is for NPN devices.

TYPES SN55140, SN55141, SN55142, SN55143, SN75140, SN75141, SN75142, SN75143 DUAL LINE RECEIVERS

BULLETIN NO. DL-S 7712456, JANUARY 1977—REVISED AUGUST 1977

features common to all eight types

- Single 5-V Supply
- ±100 mV Sensitivity
- For Applications As:
  Single-Ended Line Receiver
  Gated Oscillator
  Level Comparator

features of '140 and '141

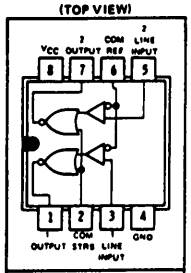
- Common Reference Pin
- Common Strobe
- '141 Has Diode-Protected Input Stage for Power-Off Condition

- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications

features of '142 and '143

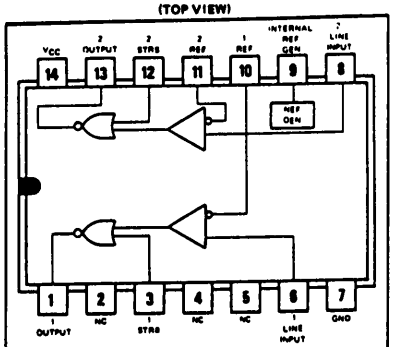
- Individual Reference Pins
- Individual Strobes
- Internal 2.5-Volt Reference Available
- '143 Has Diode-Protected Input Stage for Power-Off Condition

SN55140, SN55141 . . .
JG DUAL-IN-LINE PACKAGE
SN75140, SN75141 . . .
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
see function table

SN55142, SN55143 . . . J DUAL-IN-LINE PACKAGE
SN75142, SN75143 . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

Pin 2 must be left open on parts date-coded 7736 or lower.

description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 volts to 3.5 volts, making it possible to optimize noise immunity for a given system design. A 2.5-volt internal reference is available for use on the '142 and '143. Due to its low input current (less than 100 microamperes), it is ideally suited for party-line (bus-organized) systems.

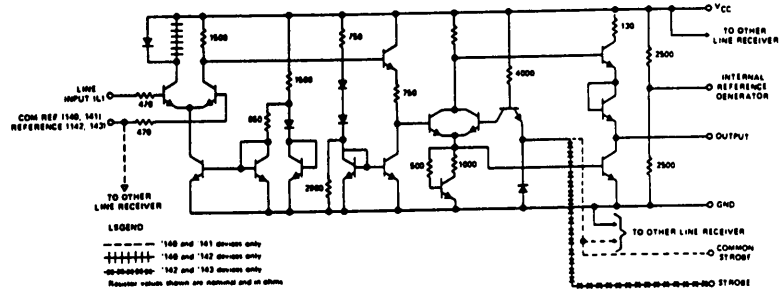
The '140 has a common reference voltage pin and a common strobe. The '141 is the same as the '140 except that the input stage is diode protected. Each receiver of the '142 has an individual reference voltage pin and an individual strobe. The '143 is the same as the '142 except that the input stage is diode protected. The internal reference voltage of the '142 and '143 can be externally adjusted with a single resistor from 1.5 volts to 3.5 volts.

FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
$\leq V_{ref} - 100$ mV	L	H
$\geq V_{ref} + 100$ mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Reference input voltage, V_{ref}	5.5 V
Line input voltage with respect to ground	−2 V to 5.5 V
Line input voltage with respect to V_{ref}	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	600 mW
Operating free-air temperature range: SN55' Circuits	−55°C to 125°C
SN75' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J or JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. Unless otherwise specified, voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J and JG packages, these chips are glass-mounted.

recommended operating conditions

	SN55' CIRCUITS			SN75' CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Reference input voltage, V_{ref}	1.5		3.5	1.5		3.5	V
Input voltage, line or strobe, V_I	0		5.5	0		5.5	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IH(L)}$	High-level line input voltage			V_{ref} + 100			mV
$V_{IL(L)}$	Low-level line input voltage					V_{ref} − 100	mV
$V_{IH(S)}$	High-level strobe input voltage			2			V
$V_{IL(S)}$	Low-level strobe input voltage					0.8	V
V_{OH}	High-level output voltage		$V_{IL(L)}$ = V_{ref} − 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)}$ = V_{ref} + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA			0.4	V
			$V_{IL(L)}$ = V_{ref} − 100 mV, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA			0.4	
$V_{IK(S)}$	Strobe input clamp voltage		$I_{I(S)}$ = −12 mA			−1.5	V
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V			1	mA
		Com strb				2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V			40	µA
		Com strb				80	
		Line input	$V_{I(L)}$ = V_{CC}, V_{ref} = 1.5 V		35	100	
		Reference	$V_{I(L)}$ = 0 V, V_{ref} = 3.5 V		35	100	
		Com ref			70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V			−1.6	mA
		Com strb				−3.2	
		Line input	$V_{I(L)}$ = 0 V, V_{ref} = 1.5 V			−10	µA
		Reference	$V_{I(L)}$ = 1.5 V, V_{ref} = 0 V			−10	
		Com ref				−20	
V_{gen}	Internal reference generator voltage	'142, '143	V_{CC} = 5 V, I_{gen} = 0	2.3	2.5	2.7	V
			V_{CC} = 5 V, I_{gen} = 70 µA		2.4		
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V	−18		−55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} − 100 mV		18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} + 100 mV		20	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high-level output from line input	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low-level output from line input			22	30	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			12	22	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			8	15	

TYPES SN55140, SN55141, SN55142, SN55143,
SN75140, SN75141, SN75142, SN75143
DUAL LINE RECEIVERS

PARAMETER MEASUREMENT INFORMATION

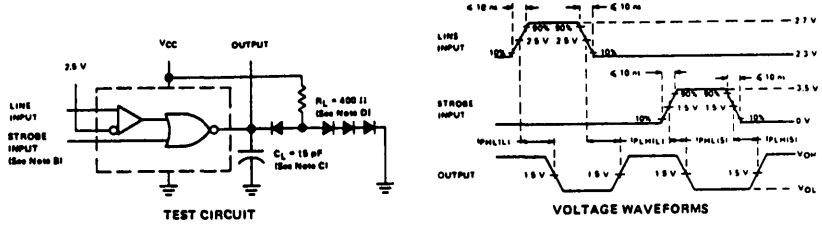


FIGURE 1

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω.
B. Unused strobe is to be open or high.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

TYPICAL CHARACTERISTICS

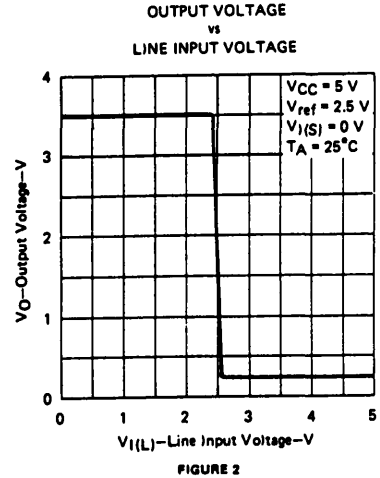
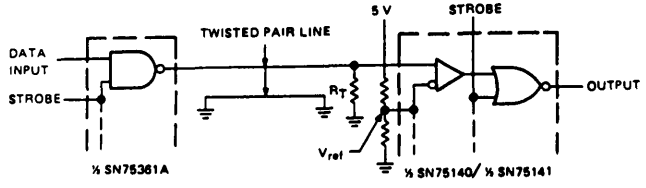


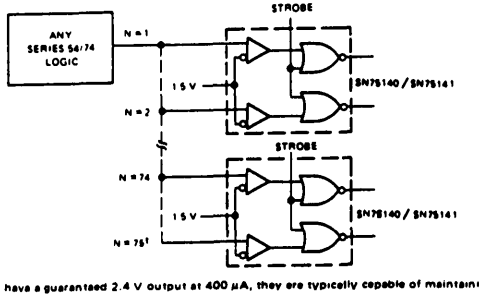
FIGURE 2

TYPICAL APPLICATION DATA

line receiver

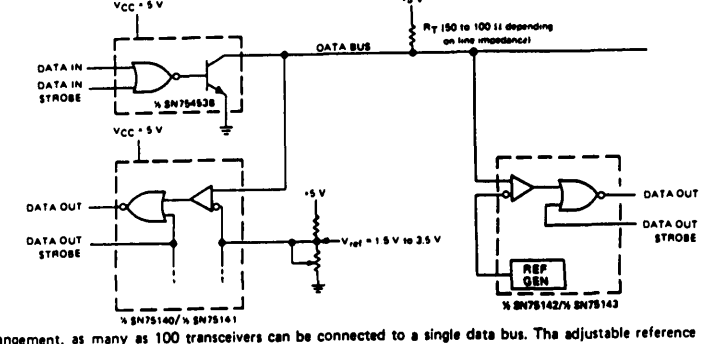


high fan-out from standard TTL gate



† Although most Series 54/74 circuits have a guaranteed 2.4 V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

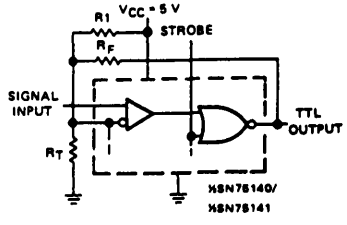
dual bus transceiver



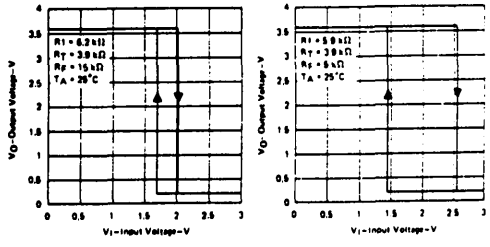
Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package, and only one power supply is required (+5 V). Data In and Data Out terminals are TTL compatible.

TYPICAL APPLICATION DATA

schmitt trigger

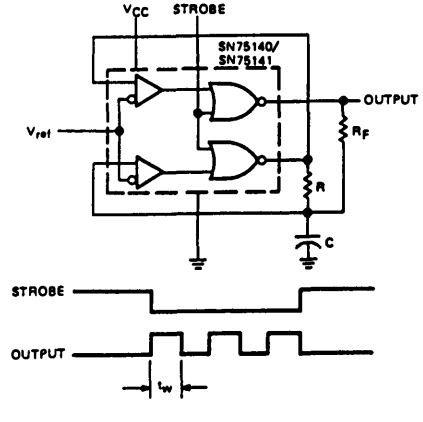


EXAMPLES OF TRANSFER CHARACTERISTICS

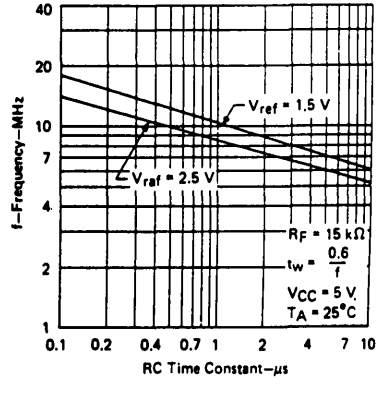


Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R1, R_F and R_T may be adjusted for the desired hysteresis and trigger levels.

gated oscillator

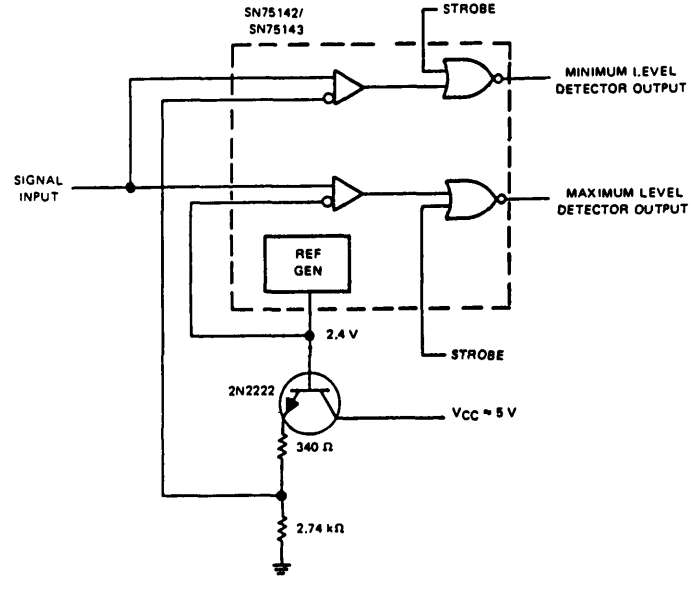


OSCILLATOR FREQUENCY
vs
RC TIME CONSTANT



TYPICAL APPLICATION DATA

level detector



ANALOG DEVICES

High Precision 10V IC Reference

AD581*

FEATURES

Laser-Trimmed to High Accuracy:
- 10.000 Volts ±5mV (L and U)

Trimmed Temperature Coefficient:
- 5ppm/°C max, 0 to +70°C (L)
- 10ppm/°C max, -55°C to +125°C (U)

Excellent Long-Term Stability:
- 25ppm/1000 hrs. (Noncumulative)

Negative 10 Volt Reference Capability
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
3-Terminal TO-5 Package

AD581 FUNCTIONAL BLOCK DIAGRAM

TO-5
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

*Covered by Patent Nos. 3,887,863; RE 30,586

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J Min	AD581J Typ	AD581J Max	AD581K Min	AD581K Typ	AD581K Max	AD581L Min	AD581L Typ	AD581L Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C			**±13.5**			**±6.75**			**±2.25**	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			**30**			**15**			**5**	ppm/°C
LINE REGULATION 15V ≤ V_{IN} ≤ 30V		**3.0** (0.002)			**3.0** (0.002)			**3.0** (0.002)		mV %/V
13V ≤ V_{IN} ≤ 15V		**1.0** (0.005)			**1.0** (0.005)			**1.0** (0.005)		mV %/V
LOAD REGULATION 0 ≤ I_{OUT} ≤ 5mA		200	500		200	500		200	500	μV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.5	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		μs
NOISE (0.1 to 10Hz)		50			50			50		μV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source at +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			μA
Sink -55°C to +85°C	-			-			-			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	-65		+150	-65		+150	-65		+150	°C
PACKAGE OPTION[2] TO-5 (H-03B)		AD581JH			AD581KH			AD581LH		

Model	AD581S Min	AD581S Typ	AD581S Max	AD581T Min	AD581T Typ	AD581T Max	AD581U Min	AD581U Typ	AD581U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C			**±30**			**±15**			**±15**	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			**30**			**15**			**10**	ppm/°C
LINE REGULATION 15V ≤ V_{IN} ≤ 30V			**3.0** (0.002)			**3.0** (0.002			**3.5** (0.002	mV %/V
13V ≤ V_{IN} ≤ 15V			**1.0** (0.005)			**1.0** (0.005)			**1.5** (0.005	mV %/V
LOAD REGULATION 0 ≤ I_{OUT} ≤ 5mA		200	500		200	500		200	500	μV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.5	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		μs
NOISE (0.1 to 10Hz)		50			50			50		μV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source at +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			μA
Sink -55°C to +55°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	-55		+125	-55		+125	-55		+125	°C
Operating	-65		+150	-65		+150	-65		+150	°C
PACKAGE OPTION[2] TO-5 (H-03B)		AD581SH			AD581TH			AD581UH		

NOTES
[1]See Figure 7.
[2]See Section 13 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAX RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . . -55°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient . . . . . 150°C/W

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

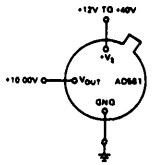


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a system calibrated to a main system reference). System calibration may also require a reference slightly different from 10.000 volts. In either case, the optional trim circuit shown in Figure 2 will offset the output by up to ±30 millivolts (with the 22Ω resistor, if needed, with minimal effect on other device characteristics.

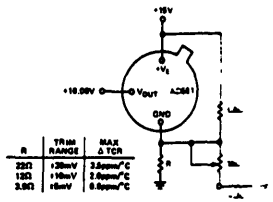


Figure 2. Optional Fine Trim Connection

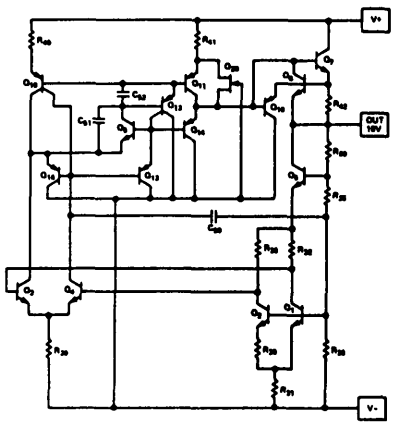


Figure 3. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard Zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

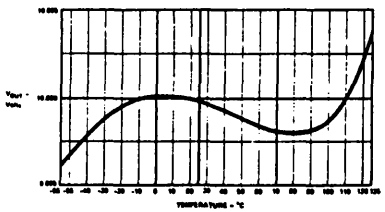


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

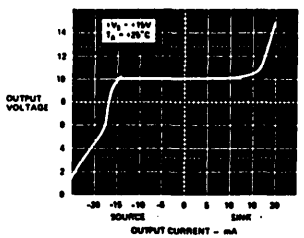


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

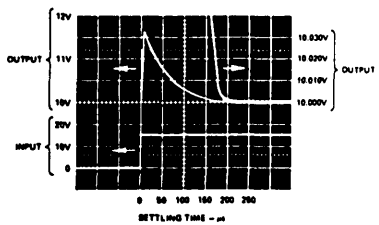


Figure 6. Output Settling Characteristic

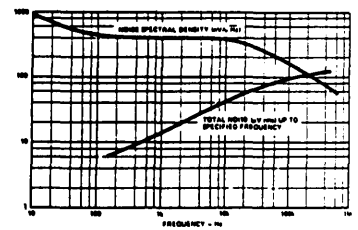


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

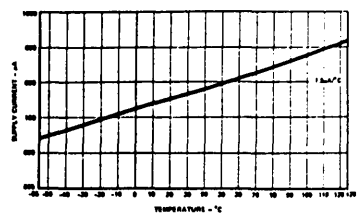


Figure 8. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

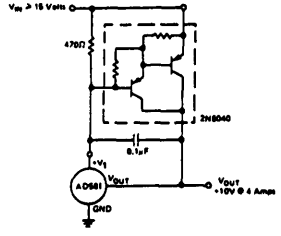


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that the other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

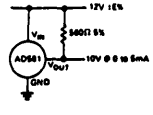


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

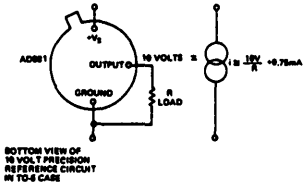


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "Zener" mode to provide a precision -10.00 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

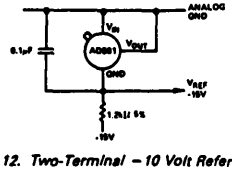


Figure 12. Two-Terminal – 10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7533 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 14, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to -10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its -10 volt "Zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\,IN}$ of the CMOS DAC). The AD581 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

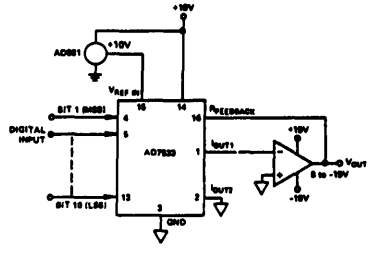


Figure 13. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

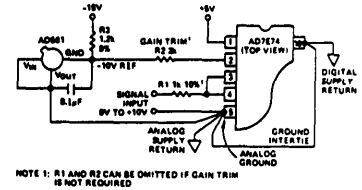


Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

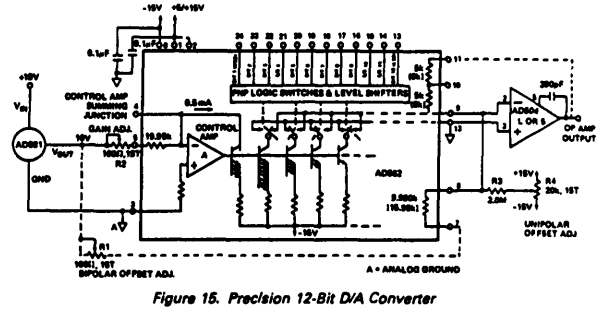


Figure 15. Precision 12-Bit D/A Converter

National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

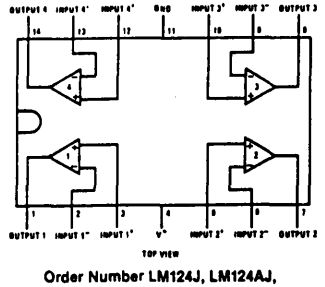
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) (temperature compensated) 1 MHz
- Wide power supply range:
  - Single supply 3 V_{DC} to 30 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) 45 nA_{DC}
- Low input offset voltage 2 mV_{DC}
- and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package

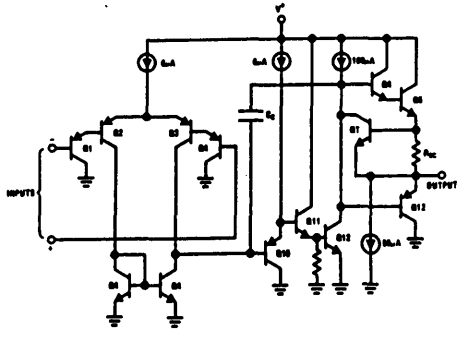


TOP VIEW

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N
See NS Package N14A

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}	Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA
Differential Input Voltage	32 V_{DC}	26 V_{DC}	Operating Temperature Range	−40°C to +85°C
Input Voltage	−0.3 V_{DC} to +26 V_{DC}	−0.3 V_{DC} to +26 V_{DC}	LM324/LM324A	0°C to +70°C
Power Dissipation (Note 1)			LM224/LM224A	−25°C to +85°C
Molded DIP	570 mW	570 mW	LM124/LM124A	−55°C to +125°C
Cavity DIP	900 mW		Storage Temperature Range	−65°C to +150°C
Flat Pack	800 mW		Lead Temperature (Soldering, 10 seconds)	300°C
Output Short-Circuit to GND (One Amplifier) (Note 2)	Continuous	Continuous		
$V^+ \leq 15$ V_{DC} and $T_A = 25°C$				

Electrical Characteristics ($V^+ = +5.0$ V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV$_{DC}$
Input Bias Current (Note 6)	$I_{IN}(+)$ or $I_{IN}(-)$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA$_{DC}$
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA$_{DC}$
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30$ V_{DC}, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V$_{DC}$
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA$_{DC}$
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA$_{DC}$
	Over Full Temperature Range																			
Large Signal Voltage Gain	$V^+ = 15$ V_{DC} (For Large V_O Swing) $R_L \geq 2$ kΩ, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2$ kΩ, $T_A = 25°C$ (LM2902 $R_L \geq 10$ kΩ)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V$_{DC}$
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current																				
Source	$V_{IN}^+ = 1$ V_{DC}, $V_{IN}^- = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA$_{DC}$
Sink	$V_{IN}^- = 1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA$_{DC}$
	$V_{IN}^- = 1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $T_A = 25°C$, $V_O = 200$ mV$_{DC}$	12	50		12	50		12	50		12	50		12	50					μA$_{DC}$
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA$_{DC}$

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7			$\mu V/^\circ C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10			$pA_{DC}/^\circ C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

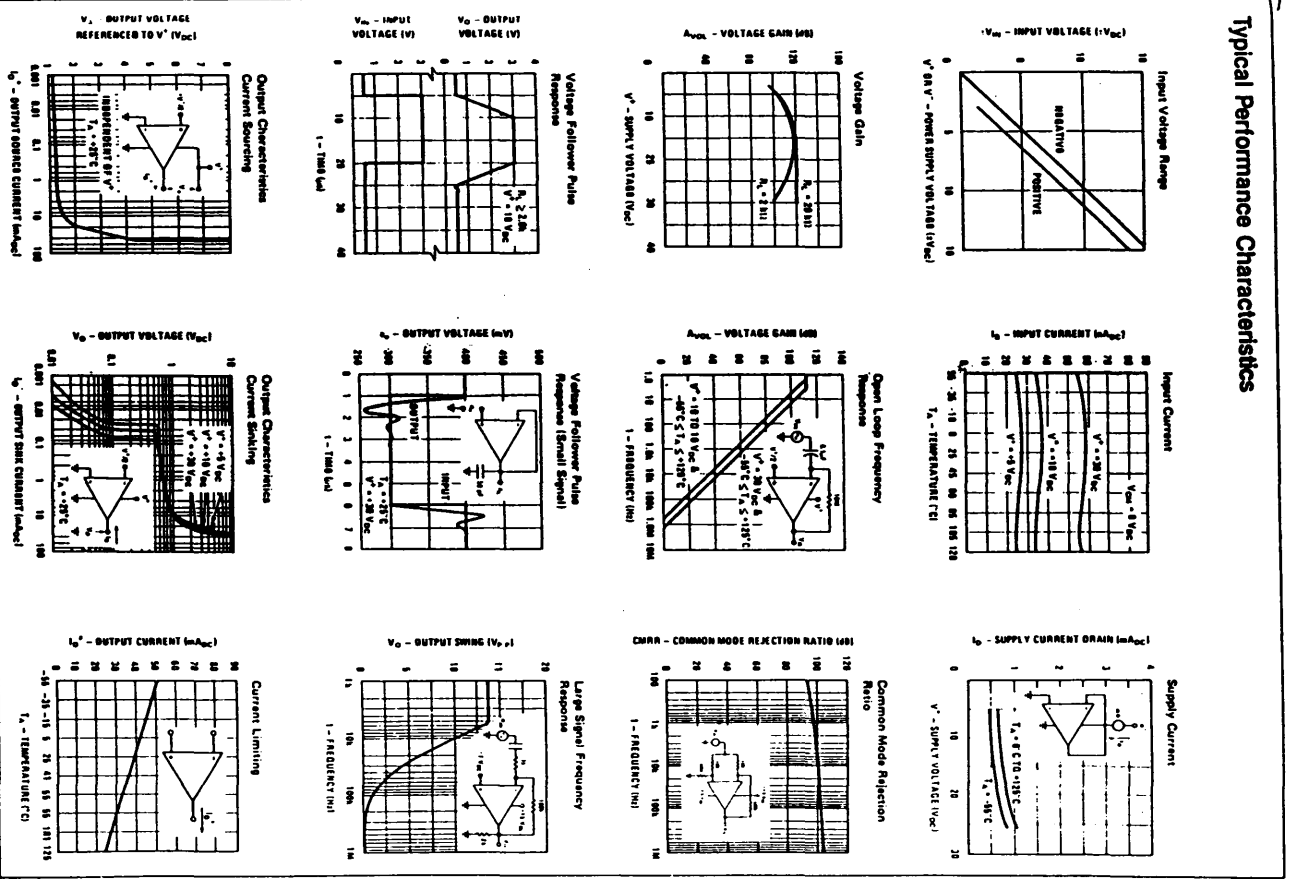
Note 5: $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

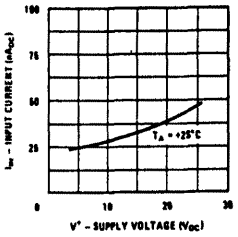
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Typical Performance Characteristics

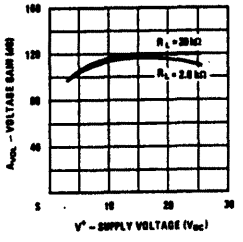


Typical Performance Characteristics (LM2902 only)

Input Current



Voltage Gain



Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of powar supply voltage with little change in performance charactaristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package hava been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertantly installed backwards in a test socket as an unlimited current surge through tha resulting forward diode within the IC could causa fusing of the internal conductors and result in e destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes ara not needed, no large input currents result from large differential input voltages. Tha differential input voltage may be largar than V$^+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers hava a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currants. Therefore both NPN and PNP external current boost transistors can be used to extand the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, whera the load is capacitively coupled to the output of the amplifiar, a resistor should be used, from the output of tha ampliflar to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitiva loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifiar.

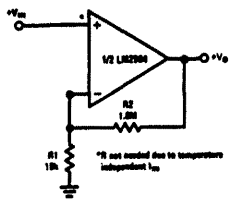
The bias network of the LM124 establishas a drain current which is independent of the magnitude of tha power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to tha positive power supply should be of short time duration. Units can be destroyed, not as e result of the short circuit current causing metal fusing, but rather dua to tha large increasa in IC chip dissipation which will cause evantual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase tha total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with tha output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

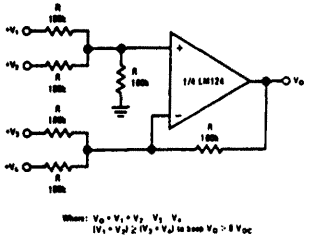
The circuits presented in the section on typical applications emphasiza operation on only a singla power supply voltage. If complamentary power supplies are availabla, all of the standard op amp circuits can be used. In general, introducing e pseudo-ground (a bias voltage reference of V$^+$/2) will allow operation abova and below this value in singla power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not raquired and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications (V$^+$ = 5.0 V$_{DC}$)

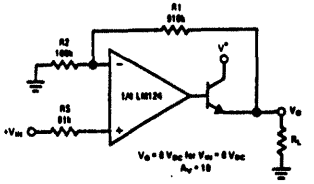
Non-Inverting DC Gain (0V Input = 0V Output)



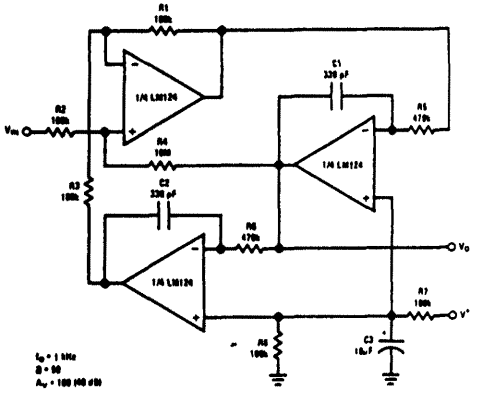
DC Summing Amplifier
(V$_{IN}$'S ≥ 0 V$_{DC}$ AND V$_O$ ≥ 0 V$_{DC}$)



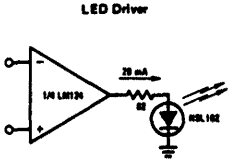
Power Amplifier



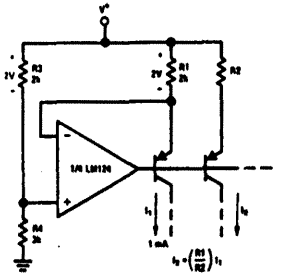
"BI-QUAD" RC Active Bandpass Filter



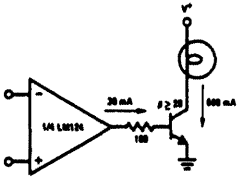
LED Driver



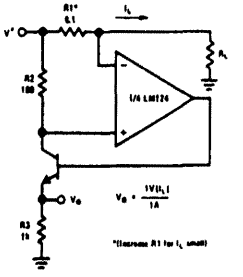
Fixed Current Sources



Lamp Driver

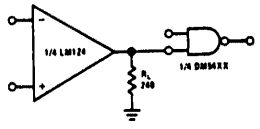


Current Monitor

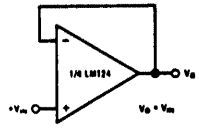


Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

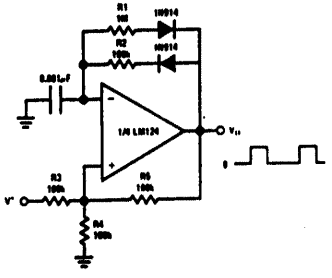
Driving TTL



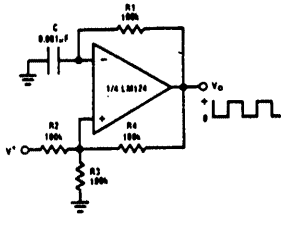
Voltage Follower



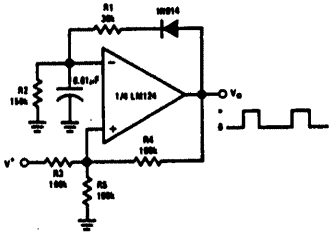
Pulse Generator



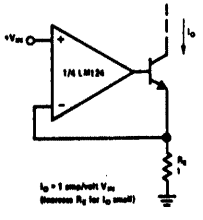
Squarewave Oscillator



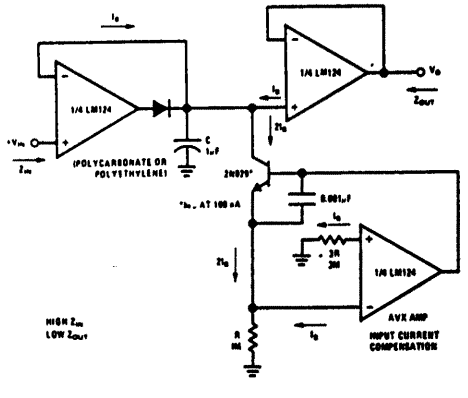
Pulse Generator



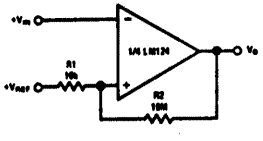
High Compliance Current Sink



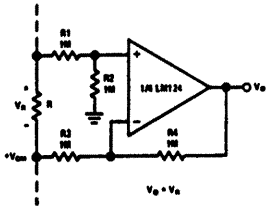
Low Drift Peak Detector



Comparator with Hysteresis



Ground Referencing A Differential Input Signal



Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

Voltage Controlled Oscillator Circuit

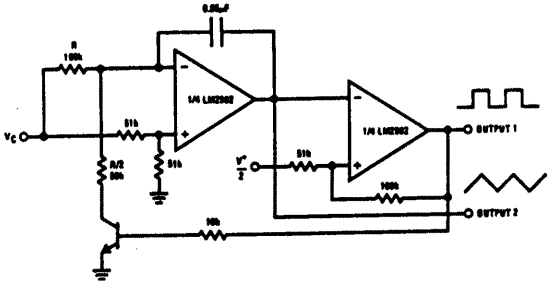
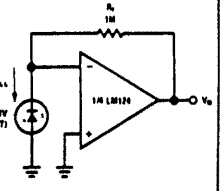
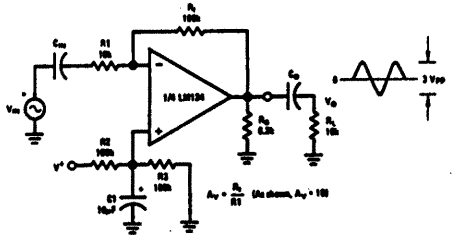


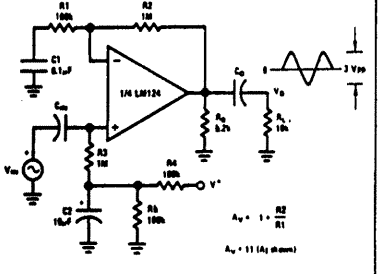
Photo Voltaic-Cell Amplifier



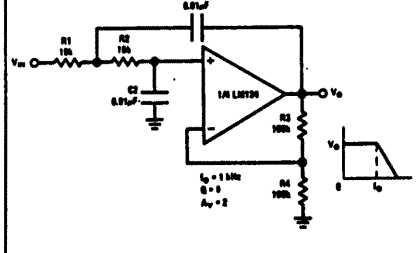
AC Coupled Inverting Amplifier



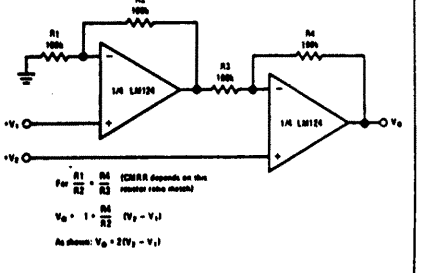
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter

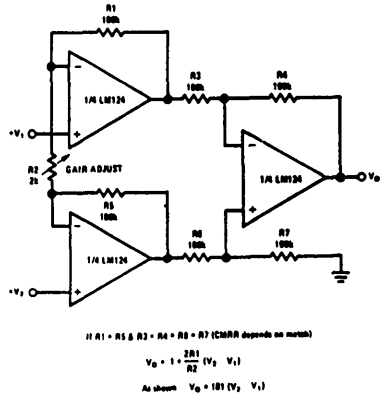


High Input Z, DC Differential Amplifier



Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

High Input Z Adjustable-Gain DC Instrumentation Amplifier

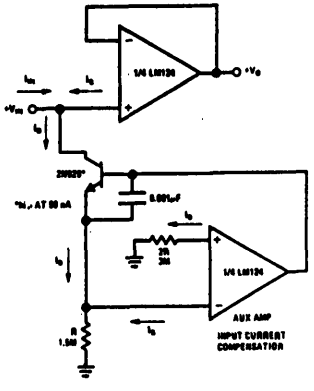


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

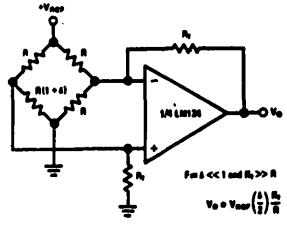
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



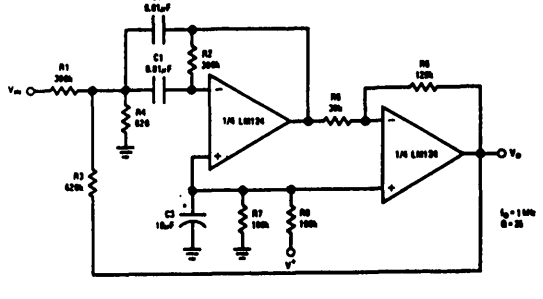
Bridge Current Amplifier



For $\delta << 1$ and $R_L >> R$

$$V_O = V_{REF}\left(\frac{\delta}{2}\right)\frac{R_2}{R}$$

Bandpass Active Filter



HARRIS

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

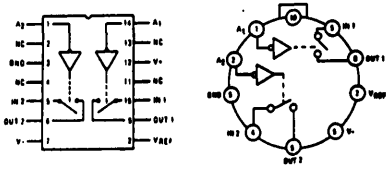
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (240ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

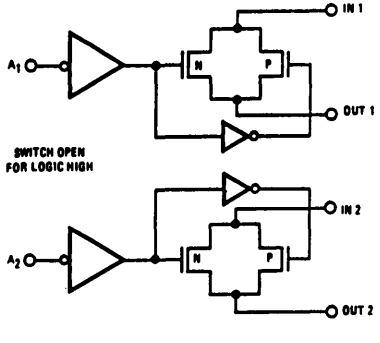
PINOUT

TOP VIEWS



CASE TIED TO V-

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	+V_{Supply} +4V	HI-200-2	-55°C to +125°C
	-V_{Supply} -4V	HI-200-4	-25°C to +85°C
Analog Input Voltage (One Switch)	+V_{Supply} +2.0V	HI-200-5	0°C to +75°C
	-V_{Supply} -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-200-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-200-5** 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.6			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		80			80		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C		15			15		mW
	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

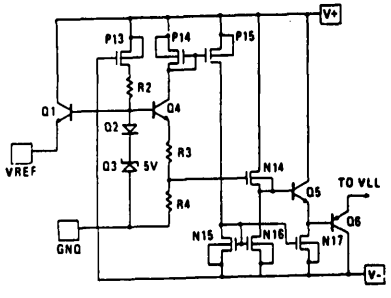
NOTES: 1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs are MOS gates - Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = 0V for Both Switches
6. Refer to leakage current measurement diagram on page 3-8

** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +80°C.

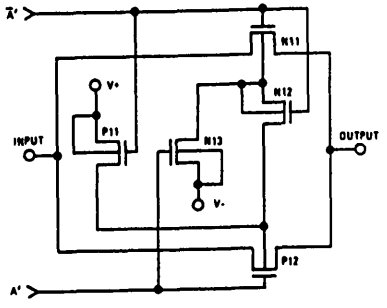
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT

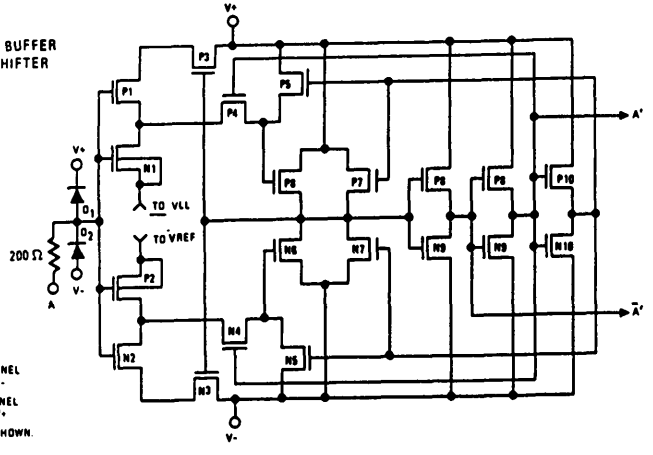
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V-

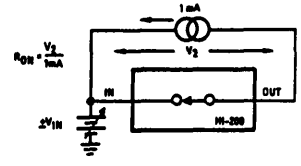
ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN.

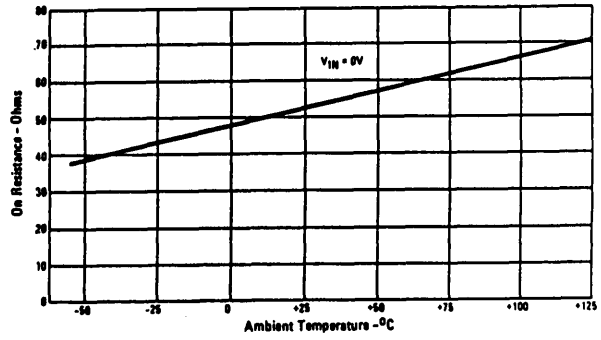
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED T_A = 25°C, V_{SUPPLY} = ± 15V, V_{AH} = 2.4V V_{AL} = 0.8V AND V_{REF} = OPEN).

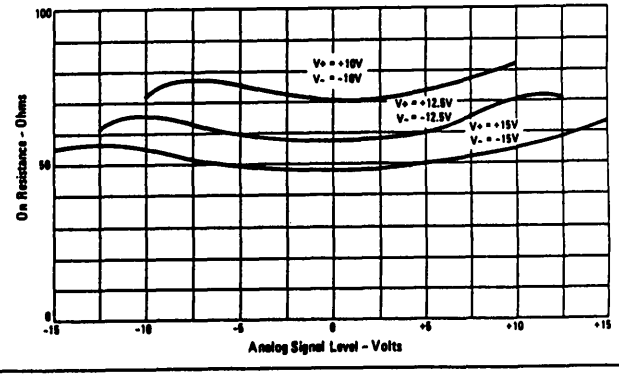
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



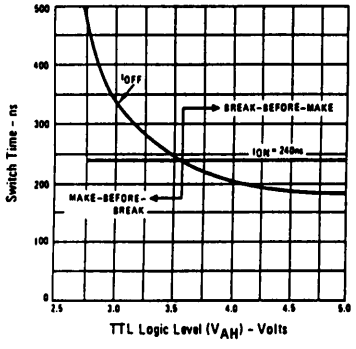
ON RESISTANCE vs. TEMPERATURE



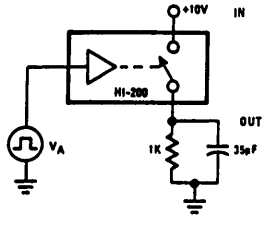
(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



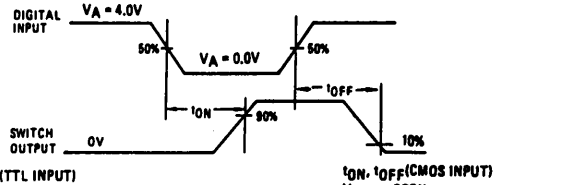
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



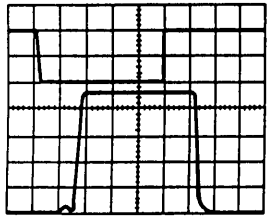
ON/OFF SWITCH TIME vs.
LOGIC LEVEL



SWITCHING WAVEFORMS

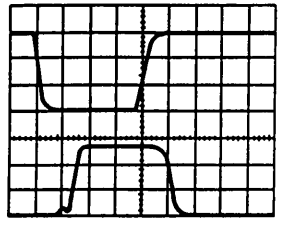


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



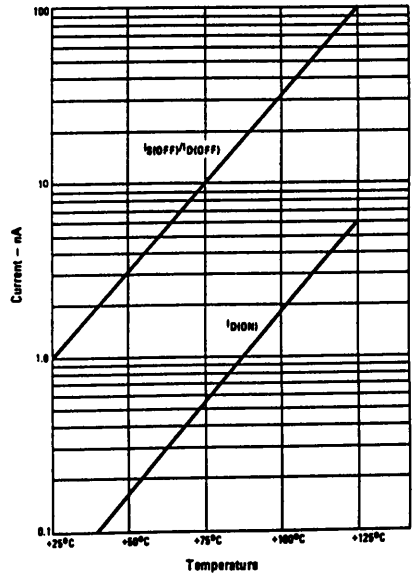
Top: TTL Input Vertical: 2V/Div.
Bottom: Output Horizontal: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V

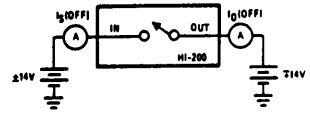


Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 200ns/Div.

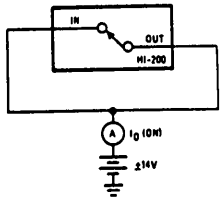
SWITCH LEAKAGE CURRENT vs.
TEMPERATURE (HI-200)



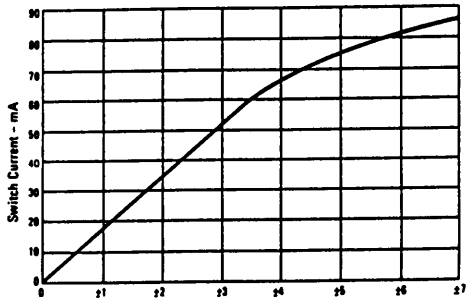
OFF LEAKAGE CURRENT
vs. TEMPERATURE



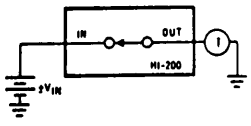
ON LEAKAGE CURRENT
vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE



SWITCH CURRENT
vs. VOLTAGE



6.0 APPENDIX

List of Relevant NRAO Technical Reports, Memos and Reference Data

VLBA Technical Report No. 12, VLBA Standard Interface Board Manual, W. Koski and D. Weber, July 1991

VLBA Technical Report No. 1, Low Noise, 8.4 GHz, Cryogenic GASFET Front-End S. Weinreb, H. Dill, R. Harris August 1984

VLBA Technical Report No. 2, 1.5 GHz Cryogenic Front-End, R. Norrod, September 1986

VLBA Technical Report No. 3, 4.8 GHz Cryogenic Front-End, R. Norrod, December 1986

VLBA Technical Report No. 10, Model F104, 2.3 Ghz Cryogenic Front-End R. Norrod, M. Masterman, June 3, 1991

Discussion of the Front-End Monitor and Control System, VLBA Electronics Memo 41, Dick Thompson, April 1985

Vertex Room Interfacing, VLBA Electronics Memo 42, R. Norrod, April 1985

Front-End Monitor and Control, VLBA Electronics Memo 43, S. Weinreb, April 1985

Meeting on Front-End Interface, VLBA Electronics Memo 44, Dick Thompson, May 1985

Specifications:

A55001N002-A Monitor and Control Standard Interface
A55001N001 Monitor and Control Bus at VLBA Stations
EIA RS-485 Standard

Listing of F117 Test Program, F117_2T.BAS

F117 TEST PROGRAM F117_2.BAS
VERSION 1/2/93
Written by Larry May

The program listed below is the F117 module test program used to test the VLBA F117 module in the AOC Front-End Laboratory. It is used in an IBM-compatible AT class PC using the C53510A007 Loop Back Test Fixture. The program was written in Microsoft BASIC.

```
'*****************************************************************************************************
Program F117_2.BAS,  Version 1/2/93
DEFINT A-Z
'$INCLUDE: 'COMMDECL.BAS'
DECLARE SUB CHECKUM ()
DECLARE SUB DELAY2 ()
DECLARE SUB SERCON ()
DECLARE SUB DELAY1 ()
DECLARE SUB CHKPRNT1 ()
DECLARE SUB RDMON1 ()
DECLARE SUB HEAD1 ()
DECLARE SUB SETUP1 ()
DIM PORTCONFIG AS ModemType
DIM MONCHAR$(16, 3)
DIM DIGCHAR$(&H24, 3, 16)
DIM ANLGCHAR$(&H1F, 3, 16)
DIM ANVAL(&H1F, 16)
COMMON MONCHAR$()
COMMON FLAGER1
COMMON PERERROR
COMMON DLY1
CALL OpenCom("COM1: 57600,E,8,1,RB512")
IF ERR THEN
  PRINT "ERROR OPENING THE COM PORT"
  END
END IF
DLY1 = 800
SUMCHECK = 0   'total test sumation flag
GONO = 0
CMD = 5      'preset cryo to off for monit mode
'*************************************************************************
'                          F117 TEST PROGRAM
CLS
HEAD1       ' creates main header
SETUP1      ' displays setup requests
'*************************************************************************
'               select 117 or FE test
CLS
'PALETTE 0, 1
COLOR 3
PRINT ""
PRINT ""
PRINT ""
PRINT "   ********************************************************************"
PRINT "   *                                                    L.MAY 04-92 **"
PRINT "   *                                                                **"
PRINT "   *   SELECT             FOR                                       **"
PRINT "   *  ---------------------------------------------------------     **"
PRINT "   *                                                                **"
PRINT "   *     1           F117  MAN LOOP TEST                            **"
PRINT "   *                                                                **"
PRINT "   *     2           F117  AUTO LOOP TEST                           **"
PRINT "   *                                                                **"
PRINT "   *     3           Front End MONIT                                **"
PRINT "   *                                                                **"
```

```
PRINT "   *  ------------------------------------------------------   *"
PRINT "   *     Q           QUIT PROGRAM                               *"
PRINT "   ************************************************************"
PRINT "         ";
INPUT T$
IF T$ = "1" THEN FLAGER3 = 1    ' f117 man loop test
IF T$ = "2" THEN FLAGER3 = 2    ' f117 auto loop test
IF T$ = "3" THEN FLAGER3 = 3    ' FE monit
IF T$ = "Q" THEN END
'*************************************************************************
'             F117  LOOP TEST
COLOR 6
IF FLAGER3 = 1 OR FLAGER3 = 2 THEN
PRINT ""
PRINT "BE SURE TO CONNECT FRONT LOOP BACK TEST JUMPER ON F117"
PRINT ""
INPUT "PRESS ENTER TO CONTINUE"; T$
END IF
IF FLAGER3 = 3 THEN
PRINT ""
PRINT "BE SURE TO CONNECT FE CABLES TO F117"
PRINT ""
INPUT "PRESS ENTER TO CONTINUE"; T$
END IF
'*************************************************************
'       precheck SIB mon words in upper initial address
COLOR 13
PRINT "PRECHECK MON WORDS"
PRINT ""
FOR N = 0 TO 15
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H7F))
   IF N = 0 THEN CALL ComPrint(CHR$(&HF0))
   IF N = 1 THEN CALL ComPrint(CHR$(&HF1))
   IF N = 2 THEN CALL ComPrint(CHR$(&HF2))
   IF N = 3 THEN CALL ComPrint(CHR$(&HF3))
   IF N = 4 THEN CALL ComPrint(CHR$(&HF4))
   IF N = 5 THEN CALL ComPrint(CHR$(&HF5))
   IF N = 6 THEN CALL ComPrint(CHR$(&HF6))
   IF N = 7 THEN CALL ComPrint(CHR$(&HF7))
   IF N = 8 THEN CALL ComPrint(CHR$(&HF8))
   IF N = 9 THEN CALL ComPrint(CHR$(&HF9))
   IF N = 10 THEN CALL ComPrint(CHR$(&HFA))
   IF N = 11 THEN CALL ComPrint(CHR$(&HFB))
   IF N = 12 THEN CALL ComPrint(CHR$(&HFC))
   IF N = 13 THEN CALL ComPrint(CHR$(&HFD))
   IF N = 14 THEN CALL ComPrint(CHR$(&HFE))
   IF N = 15 THEN CALL ComPrint(CHR$(&HFF))
 N2 = 15 - N
CALL ComPrint(CHR$(&H0))
CALL ComPrint(CHR$(&H0))
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
```

```
  COLOR 3
  PRINT "ADR #BE-"; N2; " ="; COMSTRING$;
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  MONCHAR$(N, COUNT%) = ONECHAR$
  PRINT "  CHAR"; COUNT%; "="; ASC(ONECHAR$);
  NEXT COUNT%
  PRINT ""
END IF
NEXT N
'*********************************************************************
       IF ASC(MONCHAR$(12, 1)) <> 6 THEN FLAGER1 = 1
       IF ASC(MONCHAR$(12, 1)) = 6 THEN
           FLAGER1 = 0
           IDCHAR = ASC(MONCHAR$(12, 3))
       END IF
COLOR 2
IF FLAGER1 = 0 THEN PRINT "ID ACK OK FIRST PASS";
'*********************************************************************
' retry ID ACK if bad first try
IF FLAGER1 = 1 THEN
  FOR N = 1 TO 99
DELAY1
    PORTCONFIG.Baud = 57600
    PORTCONFIG.Parity = "E"
    PORTCONFIG.DBits = 8
    PORTCONFIG.SBits = 1
    CALL SetCom(PORTCONFIG)
DELAY1
    CALL ComPrint(CHR$(&H16))
    PORTCONFIG.Baud = 57600
    PORTCONFIG.Parity = "O"
    PORTCONFIG.DBits = 8
    PORTCONFIG.SBits = 1
DELAY1
    CALL SetCom(PORTCONFIG)
DELAY1
    CALL ComPrint(CHR$(&H7F))
DELAY1
    CALL ComPrint(CHR$(&HFC))
DELAY1
    CALL ComPrint(CHR$(&H0))
DELAY1
    CALL ComPrint(CHR$(&H0))
DELAY1
    IF NOT (ComEof%) THEN
       COMSTRING$ = ComInput$(ComLoc%)
DELAY1
       IF ASC(MONCHAR$(12, 1)) <> 6 THEN PERERROR = PERERROR + 1
       IF ASC(MONCHAR$(12, 1)) = 6 THEN
           FLAGER2 = 1    ' found at least one good ID
           IDCHAR = ASC(MONCHAR$(12, 3))
       END IF
    END IF
  NEXT N
  COLOR 4
  PRINT ""
  PRINT "PERCENT ID NAK OUT OF 100 TRIES ="; PERERROR
END
END IF
IF ASC(MONCHAR$(12, 3)) > 127 THEN IDP = 1 ELSE IDP = 0
```

```
IDN = ASC(MONCHAR$(12, 3))
IF IDP = 1 THEN IDN = IDN - 128
IF IDN = 0 THEN
  BAND$ = "75 mHz"
  Par = 1
  BLKSTHI = &H1
  BLKSTLO = &H0
  BELO = &H40
END IF
IF IDN = 1 THEN
  BAND$ = "90/50 cm"
  Par = 0
  BLKSTHI = &H1
  BLKSTLO = &H80
  BELO = &HC0
END IF
IF IDN = 2 THEN
  BAND$ = "20 cm"
  Par = 0
  BLKSTHI = &H2
  BLKSTLO = &H0
  BELO = &H40
END IF
IF IDN = 3 THEN
  BAND$ = "13 cm"
  Par = 1
  BLKSTHI = &H2
  BLKSTLO = &H80
  BELO = &HC0
END IF
IF IDN = 4 THEN
  BAND$ = "6 cm"
  Par = 0
  BLKSTHI = &H3
  BLKSTLO = &H0
  BELO = &H40
  END IF
IF IDN = 5 THEN
  BAND$ = "4 cm"
  Par = 1
  BLKSTHI = &H3
  BLKSTLO = &H80
  BELO = &HC0
END IF
IF IDN = 6 THEN
  BAND$ = "3 cm"
  Par = 1
  BLKSTHI = &H4
  BLKSTLO = &H0
  BELO = &H40
END IF
IF IDN = 7 THEN
  BAND$ = "2 cm"
  Par = 0
  BLKSTHI = &H4
  BLKSTLO = &H80
  BELO = &HC0
END IF
IF IDN = 8 THEN
  BAND$ = "1.3 cm"
  Par = 0
  BLKSTHI = &H5
  BLKSTLO = &H0
  BELO = &H40
END IF
```

```
IF IDN = 9 THEN
  BAND$ = "7 mm"
  Par = 1
  BLKSTHI = &H5
  BLKSTLO = &H80
  BELO = &HC0
END IF
IF IDN = 10 THEN
  BAND$ = "4 mm"
  Par = 1
  BLKSTHI = &H6
  BLKSTLO = &H0
  BELO = &H40
END IF
IF IDN > 10 THEN BAND$ = "NO BAND"
IF Par <> IDP THEN
   COLOR 4
   PRINT "    ID = EVEN PARITY - BAD"
END IF
IF Par = IDP THEN
   COLOR 13
   PRINT "    ID = ODD PARITY - OK"
END IF
COLOR 2
PRINT "ID PARITY = ";
COLOR 13
PRINT IDP;
COLOR 2
PRINT "    ID VALUE = ";
COLOR 13
PRINT IDN;
COLOR 2
PRINT "   BAND MUST BE = ";
COLOR 13
PRINT BAND$
IF IDN > 10 THEN END
'*************************************************************
'          check all 16 char ack
FLAGER1 = 0
FOR N3 = 0 TO 15
IF ASC(MONCHAR$(N3, 1)) <> 6 THEN FLAGER1 = 1
NEXT N3
IF FLAGER1 = 1 THEN
   COLOR 4
   PRINT "NO ACK ONE OR MORE INITIAL MON WORDS"
   END
END IF
IF FLAGER1 = 0 THEN
   COLOR 2
   PRINT "ALL ACK OK FIRST PASS"
END IF
'*****************************************************************
'                 check for zeros
FLAGER1 = 0
FOR N3 = 0 TO 13
   FOR N4 = 2 TO 3
      IF ASC(MONCHAR$(N3, N4)) <> 0 AND N3 <> 5 AND N3 <> 12 THEN FLAGER1 = 1
   NEXT N4
NEXT N3
IF FLAGER1 = 1 THEN
  COLOR 4
  PRINT "ONE OR MORE MON WORDS NOT ZERO THAT SHOULD BE"
  END
END IF
IF FLAGER1 = 0 THEN
```

```
   COLOR 2
   PRINT "ALL MON WORDS THAT SHOULD BE ZERO - ARE ZERO"
END IF
'*************************************************************
'        interface type and revision code
COLOR 2
PRINT "Interface Type =";
COLOR 13
PRINT ASC(MONCHAR$(5, 2))
COLOR 2
PRINT "Interface revision code =";
COLOR 13
PRINT ASC(MONCHAR$(5, 3))
'*************************************************************
'                checks all 16 mon words 100 times
FLAGER1 = 0
FOR N5 = 1 TO 100
FOR N = 0 TO 15
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
DELAY1
 CALL SetCom(PORTCONFIG)
DELAY1
 CALL ComPrint(CHR$(&H7F))
DELAY1
   IF N = 0 THEN CALL ComPrint(CHR$(&HF0))
   IF N = 1 THEN CALL ComPrint(CHR$(&HF1))
   IF N = 2 THEN CALL ComPrint(CHR$(&HF2))
   IF N = 3 THEN CALL ComPrint(CHR$(&HF3))
   IF N = 4 THEN CALL ComPrint(CHR$(&HF4))
   IF N = 5 THEN CALL ComPrint(CHR$(&HF5))
   IF N = 6 THEN CALL ComPrint(CHR$(&HF6))
   IF N = 7 THEN CALL ComPrint(CHR$(&HF7))
   IF N = 8 THEN CALL ComPrint(CHR$(&HF8))
   IF N = 9 THEN CALL ComPrint(CHR$(&HF9))
   IF N = 10 THEN CALL ComPrint(CHR$(&HFA))
   IF N = 11 THEN CALL ComPrint(CHR$(&HFB))
   IF N = 12 THEN CALL ComPrint(CHR$(&HFC))
   IF N = 13 THEN CALL ComPrint(CHR$(&HFD))
   IF N = 14 THEN CALL ComPrint(CHR$(&HFE))
   IF N = 15 THEN CALL ComPrint(CHR$(&HFF))
 N2 = 15 - N
DELAY1
CALL ComPrint(CHR$(&H0))
DELAY1
CALL ComPrint(CHR$(&H0))
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
DELAY1
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
```

```
    END IF
  MONCHAR$(N, COUNT%) = ONECHAR$
  NEXT COUNT%
END IF
NEXT N
'*********************************************************************
CHKPRNT1     ' checks values of monitor words & prints error message
'*************************************************
'          check all 16 char ack
FLAGER1 = 0
FOR N3 = 0 TO 15
  IF ASC(MONCHAR$(N3, 1)) <> 6 THEN FLAGER1 = 1
NEXT N3
IF FLAGER1 = 1 THEN
   COLOR 4
   PRINT "NO ACK ONE OR MORE SUBSEQUENT MON WORDS"
   END
END IF
'*********************************************************************
'                 check for zeros
FLAGER1 = 0
FOR N3 = 0 TO 13
   FOR N4 = 2 TO 3
      IF ASC(MONCHAR$(N3, N4)) <> 0 AND N3 <> 5 AND N3 <> 12 THEN FLAGER1 = 1
   NEXT N4
NEXT N3
IF FLAGER1 = 1 THEN
  COLOR 4
  PRINT "ONE OR MORE MON WORDS NOT ZERO THAT SHOULD BE"
  END
END IF
LOCATE 24, 1
PRINT "CHECKING ALL FIRST 16 SIB MON WORDS 100 TIMES - CHECK #"; N5;
NEXT N5
LOCATE 24, 1
PRINT "                                                                    ";
LOCATE 24, 1
COLOR 14
IF FLAGER3 = 1 THEN INPUT "SIB FIRST 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE"; T$
IF FLAGER3 = 2 OR FLAGER3 = 3 THEN PRINT "SIB FIRST 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE"; T$
'*********************************************************************
'*********************************************************************
'                relocate response address of sib
'*********************************
'       clear array
FOR N = 0 TO 15
  FOR COUNT% = 1 TO 3
     MONCHAR$(N, COUNT%) = "1"
  NEXT COUNT%
NEXT N
'*********************************************
'        begin repeat of initial sib test
CLS
PRINT "IDN ="; IDN
 IF IDN = 0 THEN
    CADR1LO = &H0
    CADR2LO = &H1
 END IF
 IF IDN = 1 THEN
    CADR1LO = &H2
    CADR2LO = &H3
 END IF
 IF IDN = 2 THEN
    CADR1LO = &H4
    CADR2LO = &H5
```

```
 END IF
 IF IDN = 3 THEN
    CADR1LO = &H6
    CADR2LO = &H7
 END IF
 IF IDN = 4 THEN
    CADR1LO = &H8
    CADR2LO = &H9
 END IF
 IF IDN = 5 THEN
    CADR1LO = &HA
    CADR2LO = &HB
 END IF
 IF IDN = 6 THEN
    CADR1LO = &HC
    CADR2LO = &HD
 END IF
 IF IDN = 7 THEN
    CADR1LO = &HE
    CADR2LO = &HF
 END IF
 IF IDN = 8 THEN
    CADR1LO = &H10
    CADR2LO = &H11
 END IF
 IF IDN = 9 THEN
    CADR1LO = &H12
    CADR2LO = &H13
 END IF
 IF IDN = 10 THEN
    CADR1LO = &H14
    CADR2LO = &H15
 END IF
PRINT "IDN ="; IDN; "    CADR1LO ="; CADR1LO; "   CADR2LO ="; CADR2LO
'*****************************************************
'                   send new block size
PRINT ""
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 CALL ComPrint(CHR$(&H80))    ' msb of adr to load data
DELAY1
 CALL ComPrint(CHR$(CADR1LO))    ' lsb of adr to load data
DELAY1
 CALL ComPrint(CHR$(&H0))      ' msb block size
DELAY1
 CALL ComPrint(CHR$(&H40))      ' lsb block size
DELAY1
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
  DELAY1
  COLOR 3
  PRINT " BLOCK SIZE COMMAND RESPONSE ="; COMSTRING$;
```

```
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  PRINT "  CHAR"; COUNT%; " ="; ASC(ONECHAR$);
  NEXT COUNT%
  PRINT ""
END IF
PRINT "JUST SENT BLOCK SIZE COMMAND"
'*************************************************
'                    send new block start adr
PRINT ""
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
DELAY1
 CALL ComPrint(CHR$(&H80))   ' msb adr to load data
DELAY1
DELAY1
 CALL ComPrint(CHR$(CADR2LO))   ' lsb adr to load data
DELAY1
DELAY1
PRINT "BLKSTHI="; BLKSTHI
 CALL ComPrint(CHR$(BLKSTHI))    ' msb block start adr hi
DELAY1
DELAY1
PRINT "BLKSTLO+"; BLKSTLO
 CALL ComPrint(CHR$(BLKSTLO))   ' lsb block start adr lo
DELAY1
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
  DELAY1
  COLOR 3
  PRINT "BLOCK START ADR COMMAND RESPONSE ="; COMSTRING$;
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  PRINT "  CHAR"; COUNT%; " ="; ASC(ONECHAR$);
  NEXT COUNT%
  PRINT ""
END IF
'*********************************************************************
'            repeat initial mon word checks at relocated address
PERERROR = 0   'CLEAR ERROR COUNTER
DELAY1
FOR N2 = 0 TO 15
  FOR N3 = 0 TO 3
```

```
  MONCHAR$(N2, N3) = "0"
  NEXT N3
NEXT N2
PRINT ""
PRINT " STARTING RECHECK OF RELOCATED MON WORDS"
PRINT ""
DELAY1
   IF BELO = &H40 THEN X = 1
   IF BELO = &HC0 THEN X = 2
FOR N = 0 TO 15
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 CALL ComPrint(CHR$(BLKSTHI))    ' msb block start adr hi
DELAY1
   IF N = 0 AND X = 1 THEN CALL ComPrint(CHR$(&H30))
   IF N = 0 AND X = 2 THEN CALL ComPrint(CHR$(&HB0))
   IF N = 1 AND X = 1 THEN CALL ComPrint(CHR$(&H31))
   IF N = 1 AND X = 2 THEN CALL ComPrint(CHR$(&HB1))
   IF N = 2 AND X = 1 THEN CALL ComPrint(CHR$(&H32))
   IF N = 2 AND X = 2 THEN CALL ComPrint(CHR$(&HB2))
   IF N = 3 AND X = 1 THEN CALL ComPrint(CHR$(&H33))
   IF N = 3 AND X = 2 THEN CALL ComPrint(CHR$(&HB3))
   IF N = 4 AND X = 1 THEN CALL ComPrint(CHR$(&H34))
   IF N = 4 AND X = 2 THEN CALL ComPrint(CHR$(&HB4))
   IF N = 5 AND X = 1 THEN CALL ComPrint(CHR$(&H35))
   IF N = 5 AND X = 2 THEN CALL ComPrint(CHR$(&HB5))
   IF N = 6 AND X = 1 THEN CALL ComPrint(CHR$(&H36))
   IF N = 6 AND X = 2 THEN CALL ComPrint(CHR$(&HB6))
   IF N = 7 AND X = 1 THEN CALL ComPrint(CHR$(&H37))
   IF N = 7 AND X = 2 THEN CALL ComPrint(CHR$(&HB7))
   IF N = 8 AND X = 1 THEN CALL ComPrint(CHR$(&H38))
   IF N = 8 AND X = 2 THEN CALL ComPrint(CHR$(&HB8))
   IF N = 9 AND X = 1 THEN CALL ComPrint(CHR$(&H39))
   IF N = 9 AND X = 2 THEN CALL ComPrint(CHR$(&HB9))
   IF N = 10 AND X = 1 THEN CALL ComPrint(CHR$(&H3A))
   IF N = 10 AND X = 2 THEN CALL ComPrint(CHR$(&HBA))
   IF N = 11 AND X = 1 THEN CALL ComPrint(CHR$(&H3B))
   IF N = 11 AND X = 2 THEN CALL ComPrint(CHR$(&HBB))
   IF N = 12 AND X = 1 THEN CALL ComPrint(CHR$(&H3C))
   IF N = 12 AND X = 2 THEN CALL ComPrint(CHR$(&HBC))
   IF N = 13 AND X = 1 THEN CALL ComPrint(CHR$(&H3D))
   IF N = 13 AND X = 2 THEN CALL ComPrint(CHR$(&HBD))
   IF N = 14 AND X = 1 THEN CALL ComPrint(CHR$(&H3E))
   IF N = 14 AND X = 2 THEN CALL ComPrint(CHR$(&HBE))
   IF N = 15 AND X = 1 THEN CALL ComPrint(CHR$(&H3F))
   IF N = 15 AND X = 2 THEN CALL ComPrint(CHR$(&HBF))
 N2 = 15 - N
DELAY1
CALL ComPrint(CHR$(&H0))
DELAY1
CALL ComPrint(CHR$(&H0))
DELAY1
IF NOT (ComEof%) THEN
```

```
  COMSTRING$ = ComInput$(ComLoc%)
  COLOR 3
  PRINT "ADR #BE-"; N2; " ="; COMSTRING$;
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  MONCHAR$(N, COUNT%) = ONECHAR$
  PRINT "  CHAR"; COUNT%; "="; ASC(ONECHAR$);
  NEXT COUNT%
  PRINT ""
END IF
NEXT N
'*********************************************************************
       IF ASC(MONCHAR$(12, 1)) <> 6 THEN FLAGER1 = 1
       IF ASC(MONCHAR$(12, 1)) = 6 THEN
           FLAGER1 = 0
           IDCHAR = ASC(MONCHAR$(12, 3))
       END IF
COLOR 2
IF FLAGER1 = 0 THEN PRINT "relocated ID ACK OK FIRST PASS";
'*********************************************************************
' retry ID ACK if bad first try
IF FLAGER1 = 1 THEN
  FOR N3 = 1 TO 99
LOCATE 20, 20
PRINT N3;
MONCHAR$(12, 3) = "0"
FOR N = 12 TO 12
DELAY1
DELAY1
    PORTCONFIG.Baud = 57600
    PORTCONFIG.Parity = "E"
    PORTCONFIG.DBits = 8
    PORTCONFIG.SBits = 1
    CALL SetCom(PORTCONFIG)
DELAY1
    CALL ComPrint(CHR$(&H16))
DELAY1
    PORTCONFIG.Baud = 57600
    PORTCONFIG.Parity = "O"
    PORTCONFIG.DBits = 8
    PORTCONFIG.SBits = 1
    CALL SetCom(PORTCONFIG)
DELAY1
CALL ComPrint(CHR$(BLKSTHI))
DELAY1
   IF N = 0 AND X = 1 THEN CALL ComPrint(CHR$(&H30)): PRINT "LO ADR = &H30 OK"; N3
   IF N = 0 AND X = 2 THEN CALL ComPrint(CHR$(&HB0))
   IF N = 1 AND X = 1 THEN CALL ComPrint(CHR$(&H31))
   IF N = 1 AND X = 2 THEN CALL ComPrint(CHR$(&HB1))
   IF N = 2 AND X = 1 THEN CALL ComPrint(CHR$(&H32))
   IF N = 2 AND X = 2 THEN CALL ComPrint(CHR$(&HB2))
   IF N = 3 AND X = 1 THEN CALL ComPrint(CHR$(&H33))
   IF N = 3 AND X = 2 THEN CALL ComPrint(CHR$(&HB3))
   IF N = 4 AND X = 1 THEN CALL ComPrint(CHR$(&H34))
   IF N = 4 AND X = 2 THEN CALL ComPrint(CHR$(&HB4))
   IF N = 5 AND X = 1 THEN CALL ComPrint(CHR$(&H35))
   IF N = 5 AND X = 2 THEN CALL ComPrint(CHR$(&HB5))
   IF N = 6 AND X = 1 THEN CALL ComPrint(CHR$(&H36))
   IF N = 6 AND X = 2 THEN CALL ComPrint(CHR$(&HB6))
   IF N = 7 AND X = 1 THEN CALL ComPrint(CHR$(&H37))
   IF N = 7 AND X = 2 THEN CALL ComPrint(CHR$(&HB7))
```

```
   IF N = 8 AND X = 1 THEN CALL ComPrint(CHR$(&H38))
   IF N = 8 AND X = 2 THEN CALL ComPrint(CHR$(&HB8))
   IF N = 9 AND X = 1 THEN CALL ComPrint(CHR$(&H39))
   IF N = 9 AND X = 2 THEN CALL ComPrint(CHR$(&HB9))
   IF N = 10 AND X = 1 THEN CALL ComPrint(CHR$(&H3A))
   IF N = 10 AND X = 2 THEN CALL ComPrint(CHR$(&HBA))
   IF N = 11 AND X = 1 THEN CALL ComPrint(CHR$(&H3B))
   IF N = 11 AND X = 2 THEN CALL ComPrint(CHR$(&HBB))
   IF N = 12 AND X = 1 THEN CALL ComPrint(CHR$(&H3C))
   IF N = 12 AND X = 2 THEN CALL ComPrint(CHR$(&HBC))
   IF N = 13 AND X = 1 THEN CALL ComPrint(CHR$(&H3D))
   IF N = 13 AND X = 2 THEN CALL ComPrint(CHR$(&HBD))
   IF N = 14 AND X = 1 THEN CALL ComPrint(CHR$(&H3E))
   IF N = 14 AND X = 2 THEN CALL ComPrint(CHR$(&HBE))
   IF N = 15 AND X = 1 THEN CALL ComPrint(CHR$(&H3F))
   IF N = 15 AND X = 2 THEN CALL ComPrint(CHR$(&HBF))
DELAY1
    CALL ComPrint(CHR$(&H0))
DELAY1
    CALL ComPrint(CHR$(&H0))
DELAY1
    IF NOT (ComEof%) THEN
       COMSTRING$ = ComInput$(ComLoc%)
DELAY1
       IF ASC(MONCHAR$(12, 1)) <> 6 THEN PERERROR = PERERROR + 1
       IF ASC(MONCHAR$(12, 1)) = 6 THEN
           FLAGER2 = 1    ' found at least one good ID
           IDCHAR = ASC(MONCHAR$(13, 3))
       END IF
    END IF
  NEXT N
NEXT N3
  COLOR 4
  PRINT ""
  PRINT "relocated PERCENT ID NAK OUT OF 100 TRIES ="; PERERROR
END
END IF
IF ASC(MONCHAR$(12, 3)) > 127 THEN IDP = 1 ELSE IDP = 0
IDN = ASC(MONCHAR$(12, 3))
IF IDP = 1 THEN IDN = IDN - 128
IF IDN = 0 THEN BAND$ = "75 mHz": Par = 1    ' CBLKSTHI = &H81: MBLKSTHI = &H1: BLKSTLO = &H0
IF IDN = 1 THEN BAND$ = "90/50 cm": Par = 0   ' CBLKSTHI = &H81: MBLKSTHI = &H1: BLKSTLO = &H80
IF IDN = 2 THEN BAND$ = "20 cm": Par = 0     ' CBLKSTHI = &H82: MBLKSTHI = &H2: BLKSTLO = &H0
IF IDN = 3 THEN BAND$ = "13 cm": Par = 1     ' CBLKSTHI = &H82: MBLKSTHI = &H2: BLKSTLO = &H80
IF IDN = 4 THEN BAND$ = "6 cm": Par = 0      ' CBLKSTHI = &H83: MBLKSTHI = &H3: BLKSTLO = &H0
IF IDN = 5 THEN BAND$ = "4 cm": Par = 1      ' CBLKSTHI = &H83: MBLKSTHI = &H3: BLKSTLO = &H80
IF IDN = 6 THEN BAND$ = "3 cm": Par = 1      ' CBLKSTHI = &H84: MBLKSTHI = &H4: BLKSTLO = &H0
IF IDN = 7 THEN BAND$ = "2 cm": Par = 0      ' CBLKSTHI = &H84: MBLKSTHI = &H4: BLKSTLO = &H80
IF IDN = 8 THEN BAND$ = "1.3 cm": Par = 0    ' CBLKSTHI = &H85: MBLKSTHI = &H5: BLKSTLO = &H0
IF IDN = 9 THEN BAND$ = "7 mm": Par = 1      ' CBLKSTHI = &H85: MBLKSTHI = &H5: BLKSTLO = &H80
IF IDN = 10 THEN BAND$ = "4 mm": Par = 1     ' CBLKSTHI = &H86: MBLKSTHI = &H6: BLKSTLO = &H0
IF IDN > 10 THEN BAND$ = "NO BAND"
IF Par <> IDP THEN
   COLOR 4
   PRINT "    ID = EVEN PARITY - BAD"
END IF
IF Par = IDP THEN
   COLOR 13
   PRINT "    ID = ODD PARITY - OK"
END IF
COLOR 2
PRINT "ID PARITY = ";
COLOR 13
PRINT IDP;
COLOR 2
```

```
PRINT "    ID VALUE = ";
COLOR 13
PRINT IDN;
COLOR 2
PRINT "   BAND MUST BE = ";
COLOR 13
PRINT BAND$
IF IDN > 10 THEN END
'*************************************************************
'          check all 16 char ack
FLAGER1 = 0
FOR N3 = 0 TO 15
IF ASC(MONCHAR$(N3, 1)) <> 6 THEN FLAGER1 = 1
NEXT N3
IF FLAGER1 = 1 THEN
   COLOR 4
   PRINT "NO ACK ONE OR MORE relocated INITIAL MON WORDS"
   END
END IF
IF FLAGER1 = 0 THEN
   COLOR 2
   PRINT "ALL relocated ACK OK FIRST PASS"
END IF
'*****************************************************************
'                  check for zeros
FLAGER1 = 0
FOR N3 = 3 TO 11
   FOR N4 = 2 TO 3
      IF ASC(MONCHAR$(N3, N4)) <> 0 AND N3 <> 5 AND N3 <> 6 AND N3 <> 7 THEN FLAGER1 = 1
   NEXT N4
NEXT N3
IF FLAGER1 = 1 THEN
  COLOR 4
  PRINT "ONE OR MORE relocated MON WORDS NOT ZERO THAT SHOULD BE"
  END
END IF
IF FLAGER1 = 0 THEN
   COLOR 2
   PRINT "ALL relocated MON WORDS THAT SHOULD BE ZERO - ARE ZERO"
END IF
'*****************************************************************
'        interface type and revision code
COLOR 2
PRINT "relocated Interface Type =";
COLOR 13
PRINT ASC(MONCHAR$(5, 2))
COLOR 2
PRINT "relocated Interface revision code =";
COLOR 13
PRINT ASC(MONCHAR$(5, 3))
'*****************************************************************
'                checks all 16 mon words 100 times
FLAGER1 = 0
FOR N5 = 1 TO 100
FOR N = 0 TO 15
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
```

```
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 CALL ComPrint(CHR$(&H1))
DELAY1
   IF N = 0 THEN CALL ComPrint(CHR$(&H30))
   IF N = 1 THEN CALL ComPrint(CHR$(&H31))
   IF N = 2 THEN CALL ComPrint(CHR$(&H32))
   IF N = 3 THEN CALL ComPrint(CHR$(&H33))
   IF N = 4 THEN CALL ComPrint(CHR$(&H34))
   IF N = 5 THEN CALL ComPrint(CHR$(&H35))
   IF N = 6 THEN CALL ComPrint(CHR$(&H36))
   IF N = 7 THEN CALL ComPrint(CHR$(&H37))
   IF N = 8 THEN CALL ComPrint(CHR$(&H38))
   IF N = 9 THEN CALL ComPrint(CHR$(&H39))
   IF N = 10 THEN CALL ComPrint(CHR$(&H3A))
   IF N = 11 THEN CALL ComPrint(CHR$(&H3B))
   IF N = 12 THEN CALL ComPrint(CHR$(&H3C))
   IF N = 13 THEN CALL ComPrint(CHR$(&H3D))
   IF N = 14 THEN CALL ComPrint(CHR$(&H3E))
   IF N = 15 THEN CALL ComPrint(CHR$(&H3F))
 N2 = 15 - N
DELAY1
CALL ComPrint(CHR$(&H0))
DELAY1
CALL ComPrint(CHR$(&H0))
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
  DELAY1
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  MONCHAR$(N, COUNT%) = ONECHAR$
  NEXT COUNT%
END IF
NEXT N
'*********************************************************************
CHKPRNT1     ' checks values of monitor words & prints error message
'*********************************************************************
'************************************************************
'          check all 16 char ack
FLAGER1 = 0
FOR N3 = 0 TO 15
  IF ASC(MONCHAR$(N3, 1)) <> 6 THEN FLAGER1 = 1
NEXT N3
IF FLAGER1 = 1 THEN
   COLOR 4
   PRINT "NO ACK ONE OR MORE SUBSEQUENT relocated MON WORDS"
   END
END IF
'*********************************************************************
'                check for zeros
FLAGER1 = 0
FOR N3 = 3 TO 11
   FOR N4 = 2 TO 3
      IF ASC(MONCHAR$(N3, N4)) <> 0 AND N3 <> 5 AND N3 <> 6 AND N3 <> 7 THEN FLAGER1 = 1
   NEXT N4
NEXT N3
IF FLAGER1 = 1 THEN
  COLOR 4
```

```
  PRINT "ONE OR MORE relocated MON WORDS NOT ZERO THAT SHOULD BE"
  END
END IF
LOCATE 24, 1
PRINT "CHECKING ALL relocated 16 SIB MON WORDS 100 TIMES - CHECK #"; N5;
NEXT N5
LOCATE 24, 1
PRINT "                                                                    ";
LOCATE 24, 1
COLOR 14
IF FLAGER3 = 1 THEN INPUT "SIB relocated 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE"; T$
IF FLAGER3 = 2 OR FLAGER3 = 3 THEN PRINT "SIB relocated 16 MON WORDS LOOK OK - PRESS ENTER TO CONTINUE"; T$
'=============================================================================
'      $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
'*****************************************************************************
'             send out digital control lines
FOR N6 = 1 TO 12   ' types of STATE & CAL control conditions
CLS
IF FLAGER3 = 3 THEN N6 = 1  'initialize state for fe monit
FELOOP:   'fe loop restart point for refresh display
DO
IF FLAGER3 = 3 THEN
  T$ = INKEY$
  IF T$ = "N" OR T$ = "n" THEN
    LOCATE 23, 20
    INPUT "PRESS ENTER TO CONTINUE"; T$
    N6 = N6 + 1                      'increment cal condition for fe monit
    IF N6 > 3 THEN N6 = 1
  END IF
END IF
IF FLAGER3 <> 3 THEN
  IF N6 = 1 THEN XCH = &H3: CALCON = &H0  'CAL OFF & MOD OFF
  IF N6 = 2 THEN XCH = &H1: CALCON = &H1  'LO CAL MOD & MOD ON
  IF N6 = 3 THEN XCH = &H6: CALCON = &H1  'LO CAL MOD & MOD OFF
  IF N6 = 4 THEN XCH = &H4: CALCON = &H2  'LO CAL CONT & MOD ON
  IF N6 = 5 THEN XCH = &H3: CALCON = &H0  'CAL OFF & MOD OFF
  IF N6 = 6 THEN XCH = &H1: CALCON = &H4  'HI CAL MOD & MOD ON
  IF N6 = 7 THEN XCH = &H6: CALCON = &H4  'HI CAL MOD & MOD OFF
  IF N6 = 8 THEN XCH = &H4: CALCON = &H8  'HI CAL CONT & MOD OFF
  IF N6 = 9 THEN XCH = &H7: CALCON = &H0  'CAL OFF & MOD OFF
  IF N6 = 10 THEN XCH = &H5: CALCON = &H0  'CAL OFF & MOD OFF
  IF N6 = 11 THEN XCH = &H2: CALCON = &H2  'LO CAL CONT & MOD OFF
  IF N6 = 12 THEN XCH = &H0: CALCON = &H4  'HI CAL MOD & MOD OFF
END IF
IF FLAGER3 = 3 THEN
  IF N6 = 1 THEN XCH = &H7: CALCON = &H0  'COOL & CAL OFF & MOD OFF
  IF N6 = 2 THEN XCH = &H7: CALCON = &H2  'COOL & LO CAL MOD ON
  IF N6 = 3 THEN XCH = &H7: CALCON = &H8  'COOL & HI CAL MOD ON
END IF
DELAY1
FOR DIGOUT = &H20 TO &H22   'dig out control adresses
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
```

```
DELAY1
 BNDADRHI = &H80 + BLKSTHI    ' start adr + offset hi
 CALL ComPrint(CHR$(BNDADRHI))  ' send adr hi
DELAY1
 BNDADRLO = DIGOUT + BLKSTLO    ' start adr + offset lo
 CALL ComPrint(CHR$(BNDADRLO))      ' send adr lo
DELAY1
IF DIGOUT = &H20 OR DIGOUT = &H21 THEN CALL ComPrint(CHR$(XCH))    ' msb data out   INCLDING &H21? **********
IF DIGOUT = &H22 THEN CALL ComPrint(CHR$(CALCON))     ' msb data out
DELAY1
IF DIGOUT = &H20 OR DIGOUT = &H21 THEN CALL ComPrint(CHR$(XCH))    ' lsb data out   INCLUDING &H21? **********
IF DIGOUT = &H22 THEN CALL ComPrint(CHR$(CALCON))     ' msb data out
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
  DELAY1
  COLOR 3
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  NEXT COUNT%
END IF
NEXT DIGOUT
'*************************************************************************
'             read all digital lines
FOR DIGREAD = &H20 TO &H24
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 BNDADRHI = &H0 + BLKSTHI    ' start adr + offset hi
 CALL ComPrint(CHR$(BNDADRHI))  ' send adr hi
DELAY1
 BNDADRLO = DIGREAD + BLKSTLO    ' start adr + offset lo
 CALL ComPrint(CHR$(BNDADRLO))      ' send adr lo
DELAY1
 CALL ComPrint(CHR$(&H0))     ' msb filler
DELAY1
 CALL ComPrint(CHR$(&H0))     ' msb filler
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
DELAY1
  COLOR 3
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  DIGCHAR$(DIGREAD, COUNT%, N6) = ONECHAR$:
```

```
  NEXT COUNT%
END IF
DELAY1
NEXT DIGREAD
DELAY1
DELAY1
DELAY1
DELAY1
'*************************************************************************
'             read all analog lines
FOR ANLGRD = &H4 TO &H1F
  FOR CNT% = 1 TO 3
    FOR G6 = 1 TO 16
        ANLGCHAR$(ANLGRD, CNT%, G6) = "0"
    NEXT G6
  NEXT CNT%
NEXT ANLGRD
FOR ANLGRD = &H4 TO &H1F
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "E"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
 CALL ComPrint(CHR$(&H16))
DELAY1
 PORTCONFIG.Baud = 57600
 PORTCONFIG.Parity = "O"
 PORTCONFIG.DBits = 8
 PORTCONFIG.SBits = 1
 CALL SetCom(PORTCONFIG)
DELAY1
 BNDADRHI = &H0 + BLKSTHI    ' start adr + offset hi
 CALL ComPrint(CHR$(BNDADRHI))  ' send adr hi
DELAY1
 BNDADRLO = ANLGRD + BLKSTLO    ' start adr + offset lo
 CALL ComPrint(CHR$(BNDADRLO))      ' send adr lo
DELAY1
 CALL ComPrint(CHR$(&H0))    ' msb filler
DELAY1
 CALL ComPrint(CHR$(&H0))    ' lsb filler
DELAY1
IF NOT (ComEof%) THEN
  COMSTRING$ = ComInput$(ComLoc%)
DELAY1
  COLOR 3
  NUMSPACES% = 0
  FOR COUNT% = 1 TO LEN(COMSTRING$)
  ONECHAR$ = MID$(COMSTRING$, COUNT%, 1)
    IF ONECHAR$ = "" THEN
      NUMSPACES% = NUMSPACES + 1
    END IF
  ANLGCHAR$(ANLGRD, COUNT%, N6) = ONECHAR$
  NEXT COUNT%
END IF
DELAY1
NEXT ANLGRD
'*************************************************************************
'             check status of all returned data
'*************************************************************************
'             print all data
SCREEN 9
LINE (5, 5)-(295, 176), 14, B      'draw box
LINE (7, 7)-(293, 174), 14, B      'draw box
LINE (305, 5)-(600, 176), 14, B    'draw box
```

```
LINE (307, 7)-(598, 174), 14, B    'draw box
COLOR 15
LOCATE 1, 3
PRINT " FE ELEC ";
LOCATE 1, 25
PRINT " "; BAND$; " ";
LOCATE 1, 41
PRINT " FE CRYO ";
LOCATE 1, 63
PRINT " "; BAND$; " ";
CALMODE = ASC(DIGCHAR$(&H22, 3, N6))
  IF CALMODE = 0 THEN CAL$ = "CAL OFF"
  IF CALMODE = 1 THEN CAL$ = "LO CAL SW"
  IF CALMODE = 2 THEN CAL$ = "LO CAL CONT"
  IF CALMODE = 4 THEN CAL$ = "HI CAL SW"
  IF CALMODE = 8 THEN CAL$ = "HI CAL CONT"
  THISCHK = 0
  IF N6 = 1 AND CALMODE <> 0 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 2 AND CALMODE <> 1 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 3 AND CALMODE <> 1 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 4 AND CALMODE <> 2 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 5 AND CALMODE <> 0 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 6 AND CALMODE <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 7 AND CALMODE <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 8 AND CALMODE <> 8 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 9 AND CALMODE <> 0 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 10 AND CALMODE <> 0 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 11 AND CALMODE <> 2 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 12 AND CALMODE <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
LOCATE 3, 6
COLOR 2
PRINT "CAL MODE";
LOCATE 3, 17
PRINT "          ";
LOCATE 3, 17
COLOR 13
IF THISCHK = 1 AND FLAGER3 <> 3 THEN COLOR 4: FLAGER3 = 1
PRINT CAL$;
IF FLAGER3 = 1 OR FLAGER3 = 2 THEN CMD = ASC(DIGCHAR$(&H20, 3, N6))
  IF CMD = 0 THEN CMD$ = "START"
  IF CMD = 2 THEN CMD$ = "HEAT"
  IF CMD = 4 THEN CMD$ = "STRESS"
  IF CMD = 5 THEN CMD$ = "OFF"
  IF CMD = 6 THEN CMD$ = "PUMP"
  IF CMD = 7 THEN CMD$ = "COOL"
  IF CMD = 1 OR CMD = 3 THEN CMD$ = "INVALID"
  THISCHK = 0
  IF N6 = 1 AND CMD <> 3 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 2 AND CMD <> 1 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 3 AND CMD <> 6 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 4 AND CMD <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 5 AND CMD <> 3 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 6 AND CMD <> 1 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 7 AND CMD <> 6 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 8 AND CMD <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 9 AND CMD <> 7 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 10 AND CMD <> 5 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 11 AND CMD <> 2 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 12 AND CMD <> 0 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
LOCATE 3, 41
COLOR 2
PRINT "CMD"
LOCATE 3, 45
COLOR 13
IF THISCHK = 1 AND FLAGER3 <> 3 THEN COLOR 4: FLAGER3 = 1
```

```
PRINT CMD$;
SBIT3 = 0
SBIT4 = 0
SBIT5 = 0
State = ASC(DIGCHAR$(&H21, 3, N6))
IF State >= 128 THEN State = State - 128
IF State >= 64 THEN State = State - 64
IF State >= 32 THEN
  State = State - 32
  SBIT5 = 1
END IF
IF State >= 16 THEN
  State = State - 16
  SBIT4 = 1
END IF
IF State >= 8 THEN
  State = State - 8
  SBIT3 = 1
END IF
  IF State = 0 THEN STATEP$ = "START"
  IF State = 2 THEN STATEP$ = "HEAT"
  IF State = 4 THEN STATEP$ = "STRESS"
  IF State = 5 THEN STATEP$ = "OFF"
  IF State = 6 THEN STATEP$ = "PUMP"
  IF State = 7 THEN STATEP$ = "COOL"
  IF State = 1 OR State = 3 THEN STATEP$ = "INVALID"
  THISCHK = 0
  IF N6 = 1 AND State <> 3 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 2 AND State <> 1 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 3 AND State <> 6 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 4 AND State <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 5 AND State <> 3 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 6 AND State <> 1 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 7 AND State <> 6 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 8 AND State <> 4 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 9 AND State <> 7 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 10 AND State <> 5 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 11 AND State <> 2 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 12 AND State <> 0 THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
COLOR 2
LOCATE 3, 60
PRINT "STATE";
COLOR 13
IF THISCHK = 1 AND FLAGER3 <> 3 THEN COLOR 4: FLAGER3 = 1
LOCATE 3, 67
PRINT STATEP$;
COLOR 2
LOCATE 14, 28
PRINT "COMPUT/MAN = ";
COLOR 13
IF SBIT3 = 1 THEN PRINT "COMPUT";
IF SBIT3 = 0 THEN PRINT "MANUAL";
COLOR 2
LOCATE 5, 41
PRINT "PUMP REQ";
COLOR 13
LOCATE 5, 50
IF SBIT4 = 1 THEN PRINT "ON";
IF SBIT4 = 0 THEN PRINT "OFF";
COLOR 2
LOCATE 7, 41
PRINT "VALVE";
COLOR 13
LOCATE 7, 47
IF SBIT5 = 1 THEN PRINT "OPEN";
```

```
IF SBIT5 = 0 THEN PRINT "CLOSED";
COLOR 2
LOCATE 5, 3
PRINT "CAL I";
PRINT "        ";
LOCATE 5, 8
COLOR 13
IF N6 < 4.5 OR N6 = 11 THEN
NUM1& = ASC(ANLGCHAR$(&H4, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H4, 3, N6)) AND &HF0
END IF
IF N6 > 4.5 AND N6 <> 11 THEN
NUM1& = ASC(ANLGCHAR$(&H5, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H5, 3, N6)) AND &HF0
END IF
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF N6 < 4.5 OR N6 = 11 THEN ANVAL(&H4, N6) = ANVAL
IF N6 > 4.5 AND N6 <> 11 THEN ANVAL(&H5, N6) = ANVAL
THISCHK = 0
  IF N6 = 1 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 2 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 3 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 4 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 5 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 6 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 7 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 8 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 9 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 10 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 11 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 12 AND (ANVAL < -500 OR ANVAL > 500) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  COLOR 13
  IF THISCHK = 1 AND FLAGER3 <> 3 THEN COLOR 4: FLAGER3 = 1
  PRINT INT(ANVAL);
COLOR 2
LOCATE 5, 15
PRINT "V";
LOCATE 5, 16
PRINT "        ";
LOCATE 5, 16
COLOR 13
IF N6 < 4.5 OR N6 = 11 THEN
NUM1& = ASC(ANLGCHAR$(&H6, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H6, 3, N6)) AND &HF0
END IF
IF N6 > 4.5 AND N6 <> 11 THEN
NUM1& = ASC(ANLGCHAR$(&H7, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H7, 3, N6)) AND &HF0
END IF
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
IF FLAGER3 = 3 THEN ANVAL = 4000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 4000 * ANVAL& / 32768
IF N6 < 4.5 OR N6 = 11 THEN ANVAL(&H6, N6) = ANVAL
IF N6 > 4.5 AND N6 <> 11 THEN ANVAL(&H7, N6) = ANVAL
THISCHK = 0
  IF N6 = 1 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 2 AND (ANVAL < 2700 OR ANVAL > 2850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
```

```
  IF N6 = 3 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 4 AND (ANVAL < 2700 OR ANVAL > 2850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 5 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 6 AND (ANVAL < 2700 OR ANVAL > 2850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 7 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 8 AND (ANVAL < 2700 OR ANVAL > 2850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 9 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 10 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 11 AND (ANVAL < 2700 OR ANVAL > 2850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 12 AND (ANVAL < 2700 OR ANVAL > 2850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  COLOR 13
  IF THISCHK = 1 AND FLAGER3 <> 3 THEN COLOR 4: FLAGER3 = 1
  PRINT ANVAL / 100;
COLOR 2
LOCATE 5, 25
PRINT "LED";
LOCATE 5, 31
COLOR 13
NUM1& = ASC(ANLGCHAR$(&HA, 2, N6))
NUM2& = ASC(ANLGCHAR$(&HA, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&HA, N6) = ANVAL
CHECKUM
COLOR 13
PRINT ANVAL / 100;
LOCATE 6, 25
COLOR 2
PRINT "SENS";
LOCATE 6, 31
COLOR 13
NUM1& = ASC(ANLGCHAR$(&HB, 2, N6))
NUM2& = ASC(ANLGCHAR$(&HB, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&HB, N6) = ANVAL
CHECKUM
COLOR 13
PRINT ANVAL / 100;
LOCATE 5, 60
COLOR 2
PRINT "AC I";
LOCATE 5, 65
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H9, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H9, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H9, N6) = ANVAL
CHECKUM
COLOR 13
PRINT ANVAL / 100;
LOCATE 7, 7
COLOR 2
```

```
PRINT "7.5v";
LOCATE 7, 12
COLOR 13
NUM1& = ASC(ANLGCHAR$(&HC, 2, N6))
NUM2& = ASC(ANLGCHAR$(&HC, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&HC, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
  COLOR 13
  PRINT ANVAL / 1000;
END IF
LOCATE 7, 23
COLOR 2
PRINT "GND";
LOCATE 7, 27
COLOR 13
NUM1& = ASC(ANLGCHAR$(&HD, 2, N6))
NUM2& = ASC(ANLGCHAR$(&HD, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&HD, N6) = ANVAL
THISCHK = 0
  IF N6 = 1 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 2 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 3 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 4 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 5 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 6 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 7 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 8 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 9 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 10 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 11 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
  IF N6 = 12 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
COLOR 13
IF THISCHK = 1 AND FLAGER3 <> 3 THEN COLOR 4: FLAGER3 = 1
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL / 1000;
END IF
LOCATE 7, 60
COLOR 2
PRINT "15K"
LOCATE 7, 64
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H14, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H14, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
```

```
ANVAL(&H14, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL;
END IF
LOCATE 9, 3
COLOR 2
PRINT "LF FET #1";
LOCATE 9, 13
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H10, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H10, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H10, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL / 100;
END IF
LOCATE 9, 22
COLOR 2
PRINT "RT FET #1"
LOCATE 9, 32
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H11, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H11, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H11, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL / 100;
END IF
LOCATE 9, 41
COLOR 2
PRINT "PUMP VAC";
LOCATE 9, 50
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H8, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H8, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H8, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
```

```
   PRINT ANVAL;
END IF
LOCATE 9, 60
COLOR 2
PRINT "50K";
LOCATE 9, 64
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H15, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H15, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H15, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL;
END IF
LOCATE 11, 3
COLOR 2
PRINT "LF FET #2";
LOCATE 11, 13
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H12, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H12, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H12, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL / 100;
END IF
LOCATE 11, 22
COLOR 2
PRINT "RT FET #2";
LOCATE 11, 32
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H13, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H13, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H13, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL / 100;
END IF
LOCATE 11, 41
COLOR 2
PRINT "DEWER VAC";
```

```
LOCATE 11, 51
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H17, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H17, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H17, N6) = ANVAL
CHECKUM
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
IF FLAGER3 = 3 THEN
   COLOR 13
   PRINT ANVAL;
END IF
LOCATE 11, 60
COLOR 2
PRINT "300K";
LOCATE 11, 65
COLOR 13
NUM1& = ASC(ANLGCHAR$(&H16, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H16, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&'- &H8000
IF FLAGER3 = 3 THEN ANVAL = 1000 * ANVAL& / 32768
IF FLAGER3 < 3 THEN ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H16, N6) = ANVAL
CHECKUM
IF FLAGER3 = 3 THEN
  COLOR 13
  PRINT ANVAL;
END IF
IF FLAGER3 < 3 THEN PRINT ANVAL / 100;
FULID$ = HEX$(ASC(DIGCHAR$(&H23, 2, 1))) + HEX$(ASC(DIGCHAR$(&H23, 3, 1)))
FREQ$ = RIGHT$(FULID$, 1)
MMOD1$ = MID$(FULID$, 3, 1)
MMOD = ASC(MMOD1$)
IF MMOD >= 48 AND MMOD <= 57 THEN MMOD = MMOD - 48
IF MMOD >= 65 AND MMOD <= 70 THEN MMOD = MMOD - 55
IF MMOD >= 8 THEN MMOD = MMOD - 8
IF MMOD >= 4 THEN MMOD = MMOD - 4
HISN$ = MID$(FULID$, 1, 1)
HISN = ASC(HISN$)
IF HISN >= 48 AND HISN <= 57 THEN HISN = HISN - 48
IF HISN >= 65 AND HISN <= 70 THEN HISN = HISN - 55
SNSUM = 0
IF HISN >= 8 THEN HISN = HISN - 8
IF HISN >= 4 THEN HISN = HISN - 4
IF HISN >= 2 THEN HISN = HISN - 2: SNSUM = SNSUM + 32
IF HISN >= 1 THEN HISN = HISN - 1: SNSUM = SNSUM + 16
LOSN$ = MID$(FULID$, 2, 1)
LOSN = ASC(LOSN$)
IF LOSN >= 48 AND LOSN <= 57 THEN LOSN = LOSN - 48
IF LOSN >= 65 AND LOSN <= 70 THEN LOSN = LOSN - 55
IF LOSN >= 8 THEN LOSN = LOSN - 8: SNSUM = SNSUM + 8
IF LOSN >= 4 THEN LOSN = LOSN - 4: SNSUM = SNSUM + 4
IF LOSN >= 2 THEN LOSN = LOSN - 2: SNSUM = SNSUM + 2
IF LOSN >= 1 THEN LOSN = LOSN - 1: SNSUM = SNSUM + 1
'+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
'+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
NUM1& = ASC(ANLGCHAR$(&H18, 2, N6))
```

```
NUM2& = ASC(ANLGCHAR$(&H18, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H18, N6) = ANVAL
CHAN(1) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H19, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H19, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H19, N6) = ANVAL
CHAN(2) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H1A, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H1A, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H1A, N6) = ANVAL
CHAN(3) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H1B, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H1B, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H1B, N6) = ANVAL
CHAN(4) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H1C, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H1C, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H1C, N6) = ANVAL
CHAN(5) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H1D, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H1D, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H1D, N6) = ANVAL
CHAN(6) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H1E, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H1E, 3, N6)) AND &HF0
SNUM = 0
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H1E, N6) = ANVAL
CHAN(7) = ANVAL
NUM1& = ASC(ANLGCHAR$(&H1F, 2, N6))
NUM2& = ASC(ANLGCHAR$(&H1F, 3, N6)) AND &HF0
SNUM = 0
```

```
IF NUM1& >= 128 THEN NUM1& = NUM1& - 128: SNUM = 1
ANVAL& = 256 * NUM1& + NUM2&
IF SNUM = 1 THEN ANVAL& = 32768 - ANVAL&
ANVAL = 1000 * ANVAL& / 32768
ANVAL(&H1F, N6) = ANVAL
CHAN(8) = ANVAL
FOR N = 1 TO 8
  ANVAL = CHAN(N)
  CHECKUM
    IF THISCHK > 0 THEN
      COLOR 4
      PRINT "BAD AUX ANLALOG"
    END IF
    IF THISCHK = 0 THEN COLOR 13
NEXT N
'*********************************************************************
'                            test faces
IF FLAGER3 = 1 OR FLAGER3 = 2 THEN
LOCATE 15, 1
IF SUMCHECK < .5 THEN
  COLOR 2
  PRINT "                                    ADR"
  COLOR 3
  PRINT "    *";
  COLOR 2
  PRINT "                              20 & 22";
  COLOR 3
  PRINT "                               *"
  PRINT "     * *";
  COLOR 2
  PRINT "                          READ-BACK";
  COLOR 3
  PRINT "                           * *"
  PRINT "      *   *";
  COLOR 2
  PRINT "                   DIGITAL COMMANDS";
  COLOR 3
  PRINT "                   *   *"
  PRINT "       *      *";
  COLOR 13
  PRINT "                      OK";
  COLOR 3
  PRINT "                      *      *"
  LOCATE 21, 1
END IF
IF SUMCHECK > .5 THEN
  COLOR 2
  PRINT "                                    ADR"
  COLOR 4
  PRINT "";
  COLOR 2
  PRINT "                                 20 & 22";
  COLOR 4
  PRINT ""
  PRINT "";
  COLOR 2
  PRINT "                                READ-BACK";
  COLOR 4
  PRINT ""
  PRINT "";
  COLOR 2
  PRINT "                              DIGITAL COMMANDS";
  COLOR 4
  PRINT ""
  PRINT "";
```

```
  COLOR 13
  PRINT "                                        OK";
  COLOR 4
  LOCATE 21, 1
END IF
END IF
'*****************************************************************
IF ((FLAGER3 = 1 OR FLAGER3 = 2) AND SUMCHECK < .5) OR FLAGER3 = 3 THEN
LOCATE 20, 11
COLOR 3
PRINT "           * * * * * * * * * * * *"
PRINT "         *";
COLOR 2
PRINT "   F117 SN = ";
COLOR 13
PRINT ASC(DIGCHAR$(&H24, 3, 1));
COLOR 2
PRINT "   ID = ";
COLOR 13
PRINT IDN;
COLOR 2
PRINT "       BAND = ";
COLOR 13
PRINT BAND$;
COLOR 3
PRINT "     *"
PRINT "            *";
COLOR 2
PRINT "   FE SN = ";
COLOR 13
PRINT SNSUM;
COLOR 2
PRINT "  FE FREQ = ";
COLOR 13
PRINT FREQ$;
COLOR 2
PRINT "     MOD = ";
COLOR 13
PRINT MMOD;
COLOR 3
PRINT "     *"
PRINT "                *";
COLOR 14
IF FLAGER3 <> 3 THEN
PRINT "          PRESS ENTER TO CONTINUE";
END IF
IF FLAGER3 = 3 THEN
PRINT "                                  ";
END IF
COLOR 3
PRINT "        *"
PRINT "                      * * * * * * * * * * * *";
END IF
IF (FLAGER3 = 1 OR FLAGER3 = 2) AND SUMCHECK > .5 THEN
LOCATE 20, 1
COLOR 4
PRINT "                * * * * * * * * * * * * * * * * * *"
PRINT "            *";
COLOR 2
PRINT "    F117 SN = ";
COLOR 13
PRINT ASC(DIGCHAR$(&H24, 3, 1));
COLOR 2
PRINT "   ID = ";
COLOR 13
```

```
PRINT IDN;
COLOR 2
PRINT "      BAND = ";
COLOR 13
PRINT BAND$;
COLOR 4
PRINT "  *"
PRINT "       *";
COLOR 2
PRINT "          FE SN = ";
COLOR 13
PRINT SNSUM;
COLOR 2
PRINT "  FE FREQ = ";
COLOR 13
PRINT FREQ$;
COLOR 2
PRINT "     MOD = ";
COLOR 13
PRINT MMOD;
COLOR 4
PRINT "           *"
PRINT "    *";
COLOR 14
IF FLAGER3 <> 3 THEN
PRINT "                        PRESS ENTER TO CONTINUE";
END IF
IF FLAGER3 = 3 THEN
PRINT "                                              ";
END IF
COLOR 4
PRINT "                    *"
PRINT "   **  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  **";
END IF
LOCATE 23, 26
  PRINT "                              ";
COLOR 14
IF FLAGER3 = 1 THEN
  LOCATE 23, 26
  INPUT "PRESS ENTER TO CONTINUE"; T$
END IF
IF FLAGER3 = 3 THEN
  LOCATE 23, 20
  PRINT "                                     ";
  LOCATE 23, 14
  PRINT "PRESS  ";
  COLOR 13
  PRINT "C";
  COLOR 3
  PRINT " FOR CRYO ";
  COLOR 13
  PRINT " N";
  COLOR 3
  PRINT " FOR NEXT CAL OR ";
  COLOR 13
  PRINT "Q";
  COLOR 3
  PRINT " TO QUIT";
  T3$ = INKEY$
  LOCATE 15, 20
  PRINT "7 FOR COOL"
  LOCATE 16, 20
  PRINT "4 FOR STRESS"
  LOCATE 17, 20
  PRINT "5 FOR OFF"
```

```
  LOCATE 15, 45
  PRINT "2 FOR HEAT"
  LOCATE 16, 45
  PRINT "6 FOR PUMP"
  LOCATE 17, 45
  PRINT "0 FOR STARTUP"
  LOCATE 18, 28
  COLOR 2
  IF T$ = "C" OR T$ = "c" THEN
    INPUT "ENTER CRYO CMD # ="; CMD
  END IF
END IF
IF FLAGER3 = 2 OR FLAGER3 = 3 THEN T$ = ""
IF FLAGER3 = 3 AND T3$ <> "Q" AND T3$ <> "q" THEN GOTO FELOOP
LOOP UNTIL T$ = ""
LOCATE 25, 28
PRINT "                              "
LOCATE 25, 28
'*****************************************************
'            backup display
IF FLAGER3 = 1 OR FLAGER3 = 3 THEN   'display for man test
CLS
FOR N9 = &H4 TO &H1F
COEF! = 1
DIV! = 100
IF FLAGER3 <> 2 AND N9 = &H4 THEN N9$ = "ma": X1 = 1: Y1 = 3
IF FLAGER3 <> 2 AND N9 = &H5 THEN N9$ = "ma": X1 = 1: Y1 = 4
IF FLAGER3 <> 2 AND N9 = &H6 THEN N9$ = "V": X1 = 1: Y1 = 5
IF FLAGER3 <> 2 AND N9 = &H7 THEN N9$ = "V": X1 = 1: Y1 = 6
IF FLAGER3 <> 2 AND N9 = &H8 THEN N9$ = "V": X1 = 1: Y1 = 7
IF FLAGER3 <> 2 AND N9 = &H9 THEN N9$ = "A": X1 = 1: Y1 = 8
IF FLAGER3 <> 2 AND N9 = &HA THEN N9$ = "V": X1 = 1: Y1 = 9
IF FLAGER3 <> 2 AND N9 = &HB THEN N9$ = "V": X1 = 1: Y1 = 10
IF FLAGER3 <> 2 AND N9 = &HC THEN N9$ = "V": X1 = 1: Y1 = 11
IF FLAGER3 <> 2 AND N9 = &HD THEN N9$ = "V": X1 = 1: Y1 = 12
IF FLAGER3 <> 2 AND N9 = &H10 THEN N9$ = "V": X1 = 25: Y1 = 3
IF FLAGER3 <> 2 AND N9 = &H11 THEN N9$ = "V": X1 = 25: Y1 = 4
IF FLAGER3 <> 2 AND N9 = &H12 THEN N9$ = "V": X1 = 25: Y1 = 5
IF FLAGER3 <> 2 AND N9 = &H13 THEN N9$ = "V": X1 = 25: Y1 = 6
IF FLAGER3 <> 2 AND N9 = &H14 THEN N9$ = "K": X1 = 25: Y1 = 7
IF FLAGER3 <> 2 AND N9 = &H15 THEN N9$ = "K": X1 = 25: Y1 = 8
IF FLAGER3 <> 2 AND N9 = &H16 THEN N9$ = "K": X1 = 25: Y1 = 9
IF FLAGER3 <> 2 AND N9 = &H17 THEN N9$ = "V": X1 = 25: Y1 = 10
IF FLAGER3 <> 2 AND N9 = &H18 THEN N9$ = "V": X1 = 50: Y1 = 4
IF FLAGER3 <> 2 AND N9 = &H19 THEN N9$ = "V": X1 = 50: Y1 = 5
IF FLAGER3 <> 2 AND N9 = &H1A THEN N9$ = "V": X1 = 50: Y1 = 6
IF FLAGER3 <> 2 AND N9 = &H1B THEN N9$ = "V": X1 = 50: Y1 = 7
IF FLAGER3 <> 2 AND N9 = &H1C THEN N9$ = "V": X1 = 50: Y1 = 8
IF FLAGER3 <> 2 AND N9 = &H1D THEN N9$ = "V": X1 = 50: Y1 = 9
IF FLAGER3 <> 2 AND N9 = &H1E THEN N9$ = "V": X1 = 50: Y1 = 10
COLOR 3
LOCATE 1, 1
PRINT "TEST STATE ";
COLOR 13
PRINT N6;
COLOR 2
PRINT "  ANALOG = ";
COLOR 13
IF N6 = 1 OR N6 = 2 OR N6 = 5 OR N6 = 6 OR N6 = 11 OR N6 = 12 THEN PRINT "8.2";
IF N6 = 3 OR N6 = 4 OR N6 = 7 OR N6 = 8 OR N6 = 9 OR N6 = 10 THEN PRINT "0";
COLOR 2
PRINT " v   MOD = ";
COLOR 13
IF N6 = 1 OR N6 = 2 OR N6 = 5 OR N6 = 6 OR N6 = 8 OR N6 = 11 OR N6 = 12 THEN PRINT "ON/0";
IF N6 = 3 OR N6 = 4 OR N6 = 7 OR N6 = 8 OR N6 = 9 OR N6 = 10 THEN PRINT "OFF/1";
```

```
COLOR 2
PRINT "   EVEN BITS = ";
COLOR 13
IF N6 = 1 OR N6 = 2 OR N6 = 5 OR N6 = 6 OR N6 = 9 OR N6 = 10 THEN PRINT "0";
IF N6 = 3 OR N6 = 4 OR N6 = 7 OR N6 = 8 OR N6 = 11 OR N6 = 12 THEN PRINT "1";
COLOR 2
PRINT "   ODD BITS = ";
COLOR 13
IF N6 = 1 OR N6 = 3 OR N6 = 5 OR N6 = 7 OR N6 = 9 OR N6 = 11 THEN PRINT "0";
IF N6 = 2 OR N6 = 4 OR N6 = 6 OR N6 = 8 OR N6 = 10 OR N6 = 12 THEN PRINT "1";
COLOR 2
LOCATE Y1, X1
IF N9 <> &HE AND N9 <> &HF THEN PRINT "ADR  "; HEX$(N9); "  ";
COLOR 13
IF N9 <> &HE AND N9 <> &HF THEN PRINT (COEF! * ANVAL(N9, N6)) / DIV!; N9$
COLOR 2
LOCATE 14, 1
PRINT "CMD   MONIT WORD &H20 =";
COLOR 13
CHAR1 = ASC(DIGCHAR$(&H20, 3, N6))
PRINT CHAR1;
IF CHAR1 < 128 THEN BITC8 = 0
IF CHAR1 >= 128 THEN
  BITC8 = 1
  CHAR1 = CHAR1 - 128
END IF
IF CHAR1 < 64 THEN BITC7 = 0
IF CHAR1 >= 64 THEN
  BITC7 = 1
  CHAR1 = CHAR1 - 64
END IF
IF CHAR1 < 32 THEN BITC6 = 0
IF CHAR1 >= 32 THEN
  BITC6 = 1
  CHAR1 = CHAR1 - 32
END IF
IF CHAR1 < 16 THEN BITC5 = 0
IF CHAR1 >= 16 THEN
  BITC5 = 1
  CHAR1 = CHAR1 - 16
END IF
IF CHAR1 < 8 THEN BITC4 = 0
IF CHAR1 >= 8 THEN
  BITC4 = 1
  CHAR1 = CHAR1 - 8
END IF
IF CHAR1 < 4 THEN BITC3 = 0
IF CHAR1 >= 4 THEN
  BITC3 = 1
  CHAR1 = CHAR1 - 4
END IF
IF CHAR1 < 2 THEN BITC2 = 0
IF CHAR1 >= 2 THEN
  BITC2 = 1
  CHAR1 = CHAR1 - 2
END IF
   BITC1 = CHAR1
LOCATE 14, 30

PRINT "   "; BITC8; BITC7; BITC6; BITC5; BITC4; BITC3; BITC2; BITC1
COLOR 2
PRINT "CAL   MONIT WORD &H21 =";
COLOR 13
CHAR1 = ASC(DIGCHAR$(&H21, 3, N6))
PRINT CHAR1;
```

```
IF CHAR1 < 128 THEN BITC8 = 0
IF CHAR1 >= 128 THEN
  BITC8 = 1
  CHAR1 = CHAR1 - 128
END IF
IF CHAR1 < 64 THEN BITC7 = 0
IF CHAR1 >= 64 THEN
  BITC7 = 1
  CHAR1 = CHAR1 - 64
END IF
IF CHAR1 < 32 THEN BITC6 = 0
IF CHAR1 >= 32 THEN
  BITC6 = 1
  CHAR1 = CHAR1 - 32
END IF
IF CHAR1 < 16 THEN BITC5 = 0
IF CHAR1 >= 16 THEN
  BITC5 = 1
  CHAR1 = CHAR1 - 16
END IF
IF CHAR1 < 8 THEN BITC4 = 0
IF CHAR1 >= 8 THEN
  BITC4 = 1
  CHAR1 = CHAR1 - 8
END IF
IF CHAR1 < 4 THEN BITC3 = 0
IF CHAR1 >= 4 THEN
  BITC3 = 1
  CHAR1 = CHAR1 - 4
END IF
IF CHAR1 < 2 THEN BITC2 = 0
IF CHAR1 >= 2 THEN
  BITC2 = 1
  CHAR1 = CHAR1 - 2
END IF
   BITC1 = CHAR1
LOCATE 15, 30
PRINT "   "; BITC8; BITC7; BITC6; BITC5; BITC4; BITC3; BITC2; BITC1
COLOR 2
PRINT "STATE MONIT WORD &H22 =";
COLOR 13
CHAR1 = ASC(DIGCHAR$(&H22, 3, N6))
PRINT CHAR1;
IF CHAR1 < 128 THEN BITC8 = 0
IF CHAR1 >= 128 THEN
  BITC8 = 1
  CHAR1 = CHAR1 - 128
END IF
IF CHAR1 < 64 THEN BITC7 = 0
IF CHAR1 >= 64 THEN
  BITC7 = 1
  CHAR1 = CHAR1 - 64
END IF
IF CHAR1 < 32 THEN BITC6 = 0
IF CHAR1 >= 32 THEN
  BITC6 = 1
  CHAR1 = CHAR1 - 32
END IF
IF CHAR1 < 16 THEN BITC5 = 0
IF CHAR1 >= 16 THEN
  BITC5 = 1
  CHAR1 = CHAR1 - 16
END IF
IF CHAR1 < 8 THEN BITC4 = 0
IF CHAR1 >= 8 THEN
```

```
  BITC4 = 1
  CHAR1 = CHAR1 - 8
END IF
IF CHAR1 < 4 THEN BITC3 = 0
IF CHAR1 >= 4 THEN
  BITC3 = 1
  CHAR1 = CHAR1 - 4
END IF
IF CHAR1 < 2 THEN BITC2 = 0
IF CHAR1 >= 2 THEN
  BITC2 = 1
  CHAR1 = CHAR1 - 2
END IF
   BITC1 = CHAR1
LOCATE 16, 30
PRINT "   "; BITC8; BITC7; BITC6; BITC5; BITC4; BITC3; BITC2; BITC1
COLOR 2
PRINT "ID1   MONIT WORD &H23 =";
COLOR 13
CHAR1 = ASC(DIGCHAR$(&H23, 2, N6))
PRINT CHAR1;
IF CHAR1 < 128 THEN BITC8 = 0
IF CHAR1 >= 128 THEN
  BITC8 = 1
  CHAR1 = CHAR1 - 128
END IF
IF CHAR1 < 64 THEN BITC7 = 0
IF CHAR1 >= 64 THEN
  BITC7 = 1
  CHAR1 = CHAR1 - 64
END IF
IF CHAR1 < 32 THEN BITC6 = 0
IF CHAR1 >= 32 THEN
  BITC6 = 1
  CHAR1 = CHAR1 - 32
END IF
IF CHAR1 < 16 THEN BITC5 = 0
IF CHAR1 >= 16 THEN
  BITC5 = 1
  CHAR1 = CHAR1 - 16
END IF
IF CHAR1 < 8 THEN BITC4 = 0
IF CHAR1 >= 8 THEN
  BITC4 = 1
  CHAR1 = CHAR1 - 8
END IF
IF CHAR1 < 4 THEN BITC3 = 0
IF CHAR1 >= 4 THEN
  BITC3 = 1
  CHAR1 = CHAR1 - 4
END IF
IF CHAR1 < 2 THEN BITC2 = 0
IF CHAR1 >= 2 THEN
  BITC2 = 1
  CHAR1 = CHAR1 - 2
END IF
   BITC1 = CHAR1
LOCATE 17, 30
PRINT "   "; BITC8; BITC7; BITC6; BITC5; BITC4; BITC3; BITC2; BITC1
COLOR 2
PRINT "ID2   MONIT WORD &H23 =";
COLOR 13
CHAR1 = ASC(DIGCHAR$(&H23, 3, N6))
PRINT CHAR1;
IF CHAR1 < 128 THEN BITC8 = 0
```

```
IF CHAR1 >= 128 THEN
  BITC8 = 1
  CHAR1 = CHAR1 - 128
END IF
IF CHAR1 < 64 THEN BITC7 = 0
IF CHAR1 >= 64 THEN
  BITC7 = 1
  CHAR1 = CHAR1 - 64
END IF
IF CHAR1 < 32 THEN BITC6 = 0
IF CHAR1 >= 32 THEN
  BITC6 = 1
  CHAR1 = CHAR1 - 32
END IF
IF CHAR1 < 16 THEN BITC5 = 0
IF CHAR1 >= 16 THEN
  BITC5 = 1
  CHAR1 = CHAR1 - 16
END IF
IF CHAR1 < 8 THEN BITC4 = 0
IF CHAR1 >= 8 THEN
  BITC4 = 1
  CHAR1 = CHAR1 - 8
END IF
IF CHAR1 < 4 THEN BITC3 = 0
IF CHAR1 >= 4 THEN
  BITC3 = 1
  CHAR1 = CHAR1 - 4
END IF
IF CHAR1 < 2 THEN BITC2 = 0
IF CHAR1 >= 2 THEN
  BITC2 = 1
  CHAR1 = CHAR1 - 2
END IF
   BITC1 = CHAR1
LOCATE 18, 30
PRINT "   "; BITC8; BITC7; BITC6; BITC5; BITC4; BITC3; BITC2; BITC1
COLOR 2
PRINT "FE    MONIT WORD &H24 =";
COLOR 13
CHAR1 = ASC(DIGCHAR$(&H24, 3, N6))
PRINT CHAR1;
IF CHAR1 < 128 THEN BITC8 = 0
IF CHAR1 >= 128 THEN
  BITC8 = 1
  CHAR1 = CHAR1 - 128
END IF
IF CHAR1 < 64 THEN BITC7 = 0
IF CHAR1 >= 64 THEN
  BITC7 = 1
  CHAR1 = CHAR1 - 64
END IF
IF CHAR1 < 32 THEN BITC6 = 0
IF CHAR1 >= 32 THEN
  BITC6 = 1
  CHAR1 = CHAR1 - 32
END IF
IF CHAR1 < 16 THEN BITC5 = 0
IF CHAR1 >= 16 THEN
  BITC5 = 1
  CHAR1 = CHAR1 - 16
END IF
IF CHAR1 < 8 THEN BITC4 = 0
IF CHAR1 >= 8 THEN
  BITC4 = 1
```

```
  CHAR1 = CHAR1 - 8
END IF
IF CHAR1 < 4 THEN BITC3 = 0
IF CHAR1 >= 4 THEN
  BITC3 = 1
  CHAR1 = CHAR1 - 4
END IF
IF CHAR1 < 2 THEN BITC2 = 0
IF CHAR1 >= 2 THEN
  BITC2 = 1
  CHAR1 = CHAR1 - 2
END IF
   BITC1 = CHAR1
LOCATE 19, 30
PRINT "   "; BITC8; BITC7; BITC6; BITC5; BITC4; BITC3; BITC2; BITC1
NEXT N9
END IF  ' end of back up display
COLOR 14
LOCATE 23, 1
IF FLAGER3 = 1 OR FLAGER3 = 3 THEN INPUT "PRESS ENTER TO CONTINUE"; T$
IF FLAGER3 = 3 THEN END
IF SUMCHECK > .5 THEN GONO = SUMCHECK
SUMCHECK = 0
NEXT N6
IF (FLAGER3 = 1 OR FLAGER3 = 2) AND GONO < .5 THEN
  CLS
  COLOR 2
  LOCATE 10, 30
  PRINT "F117";
  COLOR 14
  PRINT "  PASSED";
  COLOR 2
  PRINT "  TESTING"
  LOCATE 12, 34
  PRINT "F117 SN = ";
  COLOR 13
  PRINT ASC(DIGCHAR$(&H24, 3, 1))
  COLOR 3
  LOCATE 16, 37
  PRINT TIME$
  LOCATE 18, 36
  PRINT DATE$
  PLAY "O3 T255 E8 E3"
END IF
IF (FLAGER3 = 1 OR FLAGER3 = 2) AND GONO > .5 THEN
  CLS
  COLOR 2
  LOCATE 10, 30
  PRINT "F117 ";
  COLOR 4
  PRINT " FAILED";
  COLOR 2
  PRINT "  TESTING"
  LOCATE 12, 34
  PRINT "F117 SN = ";
  COLOR 13
  PRINT ASC(DIGCHAR$(&H24, 3, 1))
  COLOR 3
  LOCATE 16, 37
  PRINT TIME$
  LOCATE 18, 36
  PRINT DATE$
  PLAY "T70 O0 D-"
END IF
LOCATE 23, 31
```

```
INPUT "PRESS ENTER TO END"; X$
CALL CloseCom
END
SUB CHECKUM
  'checks if within window value
SHARED ANVAL
SHARED SUMCHECK
THISCHK = 0
IF N6 = 1 AND (ANVAL < 800 OR ANVAL > 850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 2 AND (ANVAL < 800 OR ANVAL > 850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 3 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 4 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 5 AND (ANVAL < 800 OR ANVAL > 850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 6 AND (ANVAL < 800 OR ANVAL > 850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 7 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 8 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 9 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 10 AND (ANVAL < -25 OR ANVAL > 25) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 11 AND (ANVAL < 800 OR ANVAL > 850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF N6 = 12 AND (ANVAL < 800 OR ANVAL > 850) THEN SUMCHECK = SUMCHECK + 1: THISCHK = 1
IF THISCHK = 0 THEN COLOR 13
IF THISCHK = 1 THEN COLOR 4
END SUB
SUB CHKPRNT1
' checks mon ID words ACK & prints error messages
SHARED MONCHAR$()
SHARED FLAGER1
SHARED PERERROR
'**** ID check
FLAGER1 = 0    ' error flag
MONCHR = ASC(MONCHAR$(12, 1))
IF MONCHR = 6 THEN FLAGER1 = 0
IF MONCHR <> 6 THEN FLAGER1 = 1
IF FLAGER1 = 1 THEN
  COLOR 4
  PRINT "ERROR - NO ID ACK ON FIRST TRY"
  PERERROR = 1
END IF
END SUB
SUB DELAY1
' creates timing delay
SHARED DLY1
FOR T = 1 TO DLY1
Z = 1
NEXT T
END SUB
SUB DELAY2
' analog read delay
FOR N10 = 1 TO 2
Z = LOG(37.65)
LOCATE 24, 20
PRINT N10
NEXT N10
END SUB
SUB HEAD1
' main header
COLOR 3
PRINT ""
PRINT "*************************************************************************"
PRINT "**                                VLBA                                 **"
PRINT "**                    F117 MODULE TEST PROGRAM                         **"
PRINT "**                             &                                       **"
PRINT "**                         FE MONITOR                                  **"
PRINT "**                            by                                       **"
PRINT "**                         LDM MAR 92                                  **"
```

```
PRINT "*                                                                    *"
PRINT "* needs: F117, F117 test box / pwr sply, F117 cables & RS232 cable *"
PRINT "**************************************************************************"
PRINT ""
PRINT ""
END SUB
SUB SETUP1
' setup requests
COLOR 14
PRINT "Connect F117 rear cables to Willy box"
PRINT ""
COLOR 9
INPUT "Press ENTER when ready"; T$
PRINT ""
PRINT ""
COLOR 14
PRINT "Connect RS232 cable between Willy box & PC"
PRINT ""
COLOR 9
INPUT "Press ENTER when ready"; T$
PRINT ""
PRINT ""
COLOR 14
PRINT "Connect F117 front jumpers"
PRINT ""
COLOR 9
INPUT "Press ENTER when ready"; T$
PRINT ""
COLOR 14
PRINT "Connect ac pwr to F117 & turn ON"
PRINT ""
COLOR 9
INPUT "Press ENTER when ready"; T$
PRINT ""
END SUB
```