VLBA Technical Report No. 36

VLBA Baseband Converter Module T122

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October 1988

VLBA BASEBAND CONVERTER - MODULE T122

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ACQ 85	Tests of the swithched power or "synchronous" detectors in the I.F. distr. and baseband conv.
ACQ 86	Adjustments which may be required in the check-out of baseband converters
ACQ 88	The effect of bias current fluctuations on the phase noise of the FET oscillator
ACQ 101	VLBA Baseband Converter Bandpass
ACQ 111	New bandwidth compensation Gain codes for Baseband converters

Specifications:

Input Frequency Range	480-1020 MHz
Gain (2 MHz Bandwidth)	64 +/- 1 dB (for AGC=max gain)
Gain for other Bandwidths	+/-3 dB/Octave Decrease/Increase
Level Control Max Attenuation	30 dB
Level Control Phase Shift	<0.5 deg
Image Rejection	>26 dB over Video range 10 KHz to

	16 MHz
Nominal Output Power	0 +/- 0.5 dB
L.O. Range	500-1000 MHz in 10 KHz Steps
Energy in 10 KHz Sidebands	<-40 dBc
L.O. Phase Noise	<2 deg r.m.s.
L.O. Leakage Into Video	<-50 dBm
Gain Compression	<0.05 dB (1%)
SNR	>25 dB
Noise Temperature	<100,000 deg K
Dynamic Range	>30 dB
Temperature Coefficient of Phase	<1 deg/deg C/GHz
L.O. Setting Time	<1 sec
L.O. Repeatability	<0.1 deg Upon Return to Same Frequency
L.O. Leakage into Input	<-60 dBm
Temperature Coefficient of Gain	<0.1 dB/deg C
Temperature Coefficient of Differential Phase	<0.1 deg/deg C
Temperature Coefficient of Baseband Delay	<0.1 ns/deg C at 8 MHz BW
Input Switch Isolation	>60 dB
Bandpass Response(see ACQ 101)	8-Pole Butterworth
3 dB Point	45% of Nominal Sample Rate i.e. 2 MHz Bandwidth 3 dB Point is at 1.8 MHz

Response:

1) >10 dB down at Bandedge (0.5 Sample Rate) X 1.08
2) <0.5 dB Ripple Across Lower 80% of Band
3) <1 dB Between Units Across Upper 20%
4) <5 deg Phase Ripple Between Units Across Lower 80%
5) <10 deg Between Units Across upper 20%
6) <0.1 deg/deg C Drift Over 80%
7) <0.1 dB/deg C Drift Over 80%

The above ensure closure errors are <0.1 deg.

Bandwidths 16,8,4,2,1,0.5,0.25,0.125,0.0625 MHz

Response specs are a factor of 2 less stringent at 16 MHz bandwidth.

8751 Firmware Specs:

1) Total power integration and synchronous detection with periods of an integral number of 80 Hz switching cycles.

2) Auto-leveling (AGC) mode to maintain constant output power.

General Description:

The baseband converter selects any one of four I.F. inputs in the frequency range 480-1020 MHz and translates the I.F. spectrum to baseband using a synthesized local oscillator. The frequency conversion is performed in a single step using a "quadrature phasing" image reject mixer to separate the upper and lower sidebands. The upper and lower sideband baseband bandwidths are individually selected from 62.5 KHz to 16 MHz by FET switch-controlled active filters. FET switches are also used to switch precision resistors in two separate gain controls for each sideband. The first digital gain control provides the 3 dB steps needed to compensate for factors of 2 change in baseband bandwidth. The second digital gain control allows finer gain changes for automatic gain control (AGC).

The local oscillator (which covers 500 to 1000 MHz in 10 KHz steps),bandwidths and bandwidth compensating attenuation are under control of the monitor and control bus (MCB) using the standard 8032 microprocessor and standard firmware. An additional 8751 microprocessor (similar to 8032 but with RAM and EPROM all on one chip) is used to measure the baseband total power levels and to control the AGC attenuators in the auto-level mode. The 8751 also provides radiometric processing such as averaging and synchronous detection. Its operating mode is controlled by the MCB and it reports the radiometric averages via the MCB.

Theory of Operation:

4-Way Input Switch:

A 4-way input switch with high isolation is formed from commercial diode switches. Unselected inputs have the isolation of two unselected switch paths thereby doubling the 40 dB isolation of an individual switch to 70 dB or better. Switch loss is made up with an output amplifier. The reverse isolation of the amplifier also aids in preventing local oscillator leakage into other baseband converters.

500-1000 MHz Synthesizer:

The synthesizer consists of an oscillator with octave tuning range, a buffer amplifier and digital divider/phase detector contained in three separately shielded sub-modules.

The low phase noise oscillator is buffered and then divided by the desired ratio using a programmable synchronous divider. A digital phase/frequency detector driven by a 10KHz reference frequency provides frequency lock during acquisition and phase lock upon acquisition of the correct frequency. The 10 KHz reference is derived from 5 MHz and

synchronized to the station sync (1 PPS). The oscillator phase will repeat when returned to the same frequency - as if it had never left the original frequency. In addition, the synchronization of the 10 KHz transition with a 5 MHz transition just following the station sync ensures that the L.O. phases repeat following a power loss.

The phase lock loop can be analysed as a "time" lock servo. In this manner we avoid having to use divide ratios and specific frequencies. The phase detector produces output pulses whose width is equal to the time difference between reference transition and divided oscillator transition. The detector sensitivity is given by:

detector sensitivity = 2 * DVECL * G1 * G2 * 10**4 volts/sec

where

DVECL = ECL logic level difference ~ 800 mV

G1 = charge pump gain = ratio of discharge/charge time const.
= 4 * 47,000/330 = 570

G2 = operational amplifier gain = 3

detector sens ~ 3X10**7 volts/sec or 30 mV/nanosec

The oscillator tunes from 500 MHz to 1 GHz with a 10 volt change in tuning voltage with a tuning sensitivity of 100 MHz per volt or 0.2 sec/sec/volt at the low end of the range. The loop filter transfer function is of the form

(1+st2)/st1 (1)

where

t1 = 47 millisec

t2 = 155 microsec

With the above values the loop natural frequency is 1700 Hz and the damping ratio is 0.8. Special tuning sensitivity compensation circuitry maintains this damping ratio over the entire frequency range.

Figure 1 shows the tuning curve and fractional tuning sensitivity of the voltage controlled oscillator. The figure also shows how the dynamic resistance of the compensation network matches the tuning sensitivity. Table 1 shows the oscillator parameters from which the theoretical phase noise curve has been derived on the assumption that all noise originates from outside a closed loop bandwidth of 1 KHz using the integral of (see VLBA Acquisition Memo #03)

S(W) = log10 [(K*T*W*W)/(Q*Q*P*dw*dw)] -3 dBc/Hz

to derive the r.m.s. phase noise.

Phase r.m.s. (radians) = [SQRT(KT/pb)](W/Q)

where

K = Boltzmenn's Constant
T = Noise Temperature of Oscillator
W = Center Frequency (Hz)
P = Oscillator Power
b = Closed Loop Bandwidth (Hz)
Q = Locked Oscillator Q

which is approximately 4/Q degrees r.m.s. at 1 GHz assuming 300 deg K and one milliwatt oscillator power. For Q = 40 the theoretical phase noise is 0.1 degrees or -109 dBc/Hz at 10KHz from carrier.

FREQ	L(nH)	C(pF)	Rs(ohm)	Rp(ohm)	Qu	Ql
500	6	17	0.3	1200	62	~60
1000	6	4	0.3	5000	130	~50

where

Rs = Series resistance of varactor diode (derived from Q ~1000 at 50 MHz)
Rp = Equivalent parallel resistance of tank circuit
Qu = Unloaded circuit Q
Ql = Loaded Q

Notes:
1] For microstrip loss of 0.15 dB/foot series resistance =0.2 ohm/inch.
2] RT/Doroid (Rogers 5880 is used for low loss and low dielectric constant to minimize stray capacitance)

TABLE 1 Voltage cotrolled oscillator parameters

SSB Mixer:

The image separation mixer uses the phasing method of single sideband reception. The L.O. oscillator is divided into two components with 90 degrees phase difference using a commercial passive quadrature hybrid. The baseband outputs of the mixers are amplified in separate all pass networks with 90 degree difference phase before being added to form the lower sideband and subtracted to form the upper sideband. An ultra high frequency operational amplifier is used for each pole/zero pair. The first all pass amplifier following the mixer has 5.8 dB gain to raise its noise floor above the following stages which have unity gain. Each mixer is operated at 100 ohm input impedance to allow their inputs to be connected together for 50 ohm input impedance. This arrangement

eliminates the need for an input power splitter and improves the noise figure since the operational amplifiers have improved noise figure at an impedance greater than 50 ohms. The overall gain of the submodule is 20 dB including the gain of the summing amplifiers which follow the all pass networks. The all pass transfer function is

$$(stp-1)/(stp+1) \qquad (2)$$ (See Figure 1)

where

tp = all pass time constant = RC

Active Filters:

The same ultra high frequency operational amplifier used in the SSB mixer is also used in the active filter circuit. An 8-pole Butterworth response filter is formed from four operational amplifiers - each providing two poles. Fixed close tolerance capacitors are used and the pole positions moved for each bandwidth by using FET switches to select appropriate precision resistor values via eight bits in common to all filter sections of one sideband. The active filter circuit configuration chosen was that which employs a voltage follower which in its simplest form has the transfer function

$$1/(SCIR*SC2R+2SCIR+1) \qquad (3)$$ (See Figure 1)

allowing the poles to be scaled by scaling R. In the actual circuit the following factors are taken into account:

a) Stay capacitance to ground due to circuit board, operational amplifier and FET switches

b) The FET switch "on" resistance

c) The operational amplifier input resistance - (important only at the narrow bandwidths which use a large value of R)

d) The phase shift through the operational amplifier - (important only for the widest bandwidth)

The pole frequency shifts caused by the above are generally compensated by adjusting the RC values while the Q loss is corrected by increasing the voltage follower gain slightly above unity. A combination of circuit theory and computer simulation was used to arrive at the corrections.

Gain Control:

Following the active filters there is a gain control formed by using an FET switch to select resistor values which determine the gain of an operational amplifier. The least gain of 0 dB occurs with all switches

open and the closing of each switch increases the gain by 3 dB - only one switch being closed at a time. Thus each all zeroes selects 0 dB for 16 MHz bandwidth and each bit selects the gain to compensate for narrower bandwidths. Following the bandwidth compensation gain control there is another gain control whose resistor values are arranged to provide an 8 bit voltage gain control with maximum gain (FFH) of 12 dB. This gain control employs two FET switched paths for each resistor to improve the isolation between selected paths and ensure a low phase shift change with gain setting. Resistor values are corrected for the FET switch resistance.

Square Law Detector:

The square law detector uses the best known square law diode - namely the back diode. The back diode evolved from the germanium tunnel diode and has a voltage/current curve similar to the tunnel diode - but without the negative resistance slope - the "back" current starts at zero volts and the forward current is small for moderate voltages. The small detected voltage from the back diode is amplified with a high quality low offset operational amplifier and converted to a digital output with a voltage to frequency converter. This method of square law detection originated at NRAO many years ago and is still the best known method for achieving wide dynamic range and a uniform response to wide input bandwidths.

Digital Interface:

A digital interface board on a wire wrap panel provides both the MCB interface and a local microporcessor for radiometric calculations and automatic gain control.

The MCB interface uses the standard interface firmware and almost the same circuit as the standard interface. Drawing 54120D048 shows the "latched" memory allocation for the interface. 64 bits are set by MCB commands, 16 bits by hardware in the baseband converter and 48 bits are set by the local (8751) microprocessor. The 8751 is paced by a 160 Hz interrupt which is derived from 5 MHz and synchronized to the station sync (1PPS). A flow chart for the 8751 firmware is shown in Figure 54120L051 and internal RAM storage allocations are shown in Table 54120D052.

Power Distribution:

A power distribution PC board is provided to supply +/-6 volts for the SSB mixer and +/-12 volts for the active filter/gain control boards. In addition the board provides open collector drivers for the FET switches which require 12 volt logic to achieve low on resistance.

Circuit Details:

4-Way Input Switch:

The circuit shown in 54120S006 utilizes Minicircuit's PSW-1211 diode switches. The switches are driven by standard CMOS logic with decoding of the 2-bit input and for driving the switches. The bias lines have to be well bypassed to eliminate cross-coupling through these lines.

500-1000 MHz Oscillator:

The oscillator circuit (54120S005) is a Hartley oscillator utilizing a FET. Biasing for the FET is derived by resistive drop from 15v with grounded gate and a constant 4 ma to the source via a 3.6 k ohm resistor to -15v. Tuning is provided via a MA 46577B GaAs hyperabrupt varactor diode. The OP-07 amplifier converts the differential output from the phase detector to single ended output. The loop filter is formed by several components. R10 (33 ohms) and C3 (4.7 UF) form t2 (of equation 1) while R09 (10 Kohms) and C3 together with R03 and C2 form t1 (of equation 1). The zero formed by R03 and C2 cancels the pole formed by R09 and C3 so the final result is the transfer function of equation. D1, R07, C05 and D2 form a network whose dynamic resistance decreases with tuning voltage in a way needed to reduce t1 and compensate for the reduction of tuning sensitivity with increasing voltage. The TLC372 dual comparator provides an indication of lock using a wired "AND" to determine whether the tuning voltage is greater than 1 volt and less than 12 volts. In addition the lock detector senses excessive noise in the loop. A lock condition is not signalled if the integrated phase error is out of limits or there is more than 70 millivolts noise in the loop at the output of the OP-07.

Buffer Amplifier:

The oscillator output is buffered to drive the SSB mixer, the synthesizer divider and the front panel monitor. The circuit (54120S014) uses Avantek GPD amplifiers and Minicircuit's power splitters and attenuators. A high reverse isolation is needed to prevent "pulling" the local oscillator. The ciruit diagram shows the nominal levels and gains.

Synthesizer Digital Divider (Circuit 54120S017):

This digital divider is a synchronous counter based upon the swallow count principle in which the input divider stage either divides by 10 or 11 for the first few cycles depending upon the least most significant digit. In order to be able to divide frquencies up to 1 GHz a GaAs variable modulus counter is used. This IC is compatible with ECL but requires two additional reference voltages (Vss and VICH - see data sheet) for the internal GaAs FET logic and the input diode clamp which are provided by resistive voltage dividers. The counter stages are loaded with digits which are the hex complement plus one (see MCB protocol) and the counter counts up to all ones before being preset again. The 12040 phase detector is followed by a diode charge pump circuit to stretch out the narrow phase error pulses and increase the

detector phase sensitivity. To minimize D.C. offsets the diodes are biased to the mean ECL logic output.

SSB Mixer (Circuit 54120S013):

The circuit is in some ways quite straightforward (compared with MKII and III SSB Mixer) because each all-pass stage is independent of the other stages. The circuit is however complicated by the need to compensate the ultra high frquency 5539 operational amplifiers to ensure stability. The method of compensation is one in which the feedback ratio is reduced at high frequencies to ensure adequate phase margin by means of the 100 ohm and 100 pF placed in series across the input. In addition a 12 pF capacitor from pin 12 provides a phase lead to further improve stability margin. Pin 12 is an intermediate point in the operational amplifier circuit which leads the output at high frquencies. All operational amplifier stages have RC power filtering from + and -6 volt supply. The all pass stages which are fed by the mixer outputs have 5.8 dB gain while the other stages have unity gain. The output sum and difference amplifiers have 20 dB gain followed by 6 dB output loss owing to 50 ohm series resistors required to provide 50 ohm output impedance. Critical components are close tolerance (1% for resistors and 5% for capacitors) and resistor values have been adjusted to allow the use of standard capacitor values.

Active Filters and Gain Controls:

The active filters, gain controls and output amplifier are built in sections and assembled into one long PC board. Drawing 54120S003 shows the overall circuit with details of the active filter sections, bandwidth compensating gain control and AGC being shown in 54120S012, 4 and 1. The active filter sections are arranged in order of increasing Q. Separate power and control lines are used for active filter sections, bandwidth compensation gain and AGC.

The active filter sections use a 5539 operational amplifier and 4 quad DMOS FET switches to switch in the resistor values appropriate for each bandwidth. The capacitance C1 has been reduced from the theoretical value by the measured circuit board capacitance plus the 5539 input capacitance. C2 has been corrected for the circuit board capacitance and the 5002 capacitance to ground. The 5002 capacitance to ground in the second set of switches has been reduced by supplying the substrate through 1 Mohm resistors. Resistance values have been reduced to compensate for the switch on resistance. The 47 ohm and 50 pF across the 5539 input CC form the compensation network to ensure stable operation of the 5539. RC increases the closed loop gain slightly above unit to compensate for Q loss due mainly to the stray capacitance to ground on the FET switch side of C2.

The gain control circuits also use 5539 amplifiers and 5002 switches. It was necessary to bypass the control lines going to the bandwidth compensation attenuators owing to the large gain which follows.

Square Law Detector (Circuit 54120S002):

The square law detector circuit uses a BD4 back diode followed by an OP-27EN operational amplifier and ADFC32 voltage to frequency converter. The low offset E version of the OP-27 was chosen and in addition a 30 microvolt positive offset is provided via R05, 06, 07 to ensure that there is always a digital frequency output.

Digital Interface:

The digital interface board is a wire wrap panel whose circuits are shown in 54120S100, 101, 102. The part of the circuit associated with the MCB was largely copies from the MCB standard interface. 128 bits of latched memory are contained in 74259s with 74251 selectors for addressing. The latched memory is allocated according to Table 54120D048. The MCB 8032 and 8751 local microprocessors run independently with separate clocks and can read and write into latched memory. The 8751s priority interrupt is driven via the 160 Hz signal derived from 5 MHz. The station sync (1PPS) synchronizes this 160 Hz via the logic in B41,B52, B53 and B51. Timing diagram is the same as in the 32 MHz synthesizer module (see Drawing 54210S001). MCB commands and requests also generate an interrupt to the 8751 to avoid conflict with access to the latched memory. For example the 8751 only reads the mode bits which are set by the MCB after receiving and interrupt and before acknowledging the request. The program flow is shown in 54120L051. The current version of this firmware acknowledges the MCB in less than 50 microseconds.

Power Distribution and Module Wiring:

The power and control signals to the sensitive analog active filter and gain control circuitry are routed via a power distribution PC board (Drawing 54120S003) which contains voltage regulators and open collector drivers.

Drawing 54120S041 shows the overall module wiring diagram. All cables have the same connectors and pin allocations on each end except the cable from the 20 pin module connector to AJ2 on the digital interface. The cable assembly is shown in Figure 54120D049.

Front Panel Monitor:

The front panel provides the following BNC outputs:

L.O. Monitor	-10 dBm nominal
USB Baseband	-10 dBm nominal
LSB Baseband	-10 dBm nominal

I/O Connections and Power Levels:

Pin #	Function
1	GND
2	+5V (2100 ma)
3	5 MHz + 13 dBm Nominal
4	I.F.A -30 dBm/500 MHz Nominal
5	1 PPS >1V <5V 50 ohms
6	MCB Monitor Output (-)
7	MCB Monitor Output (+)
8	NC
9	USB Baseband Output 0 dBm nominal
10	I.F.B
11	I.F.C
12	MCB Command Input (-)
13	MCB Command Input (+)
14	-15V (550 ma)
15	+15V (850 ma)
16	LSB Baseband Output 0 dBm Nominal
17	I.F.D
18 Inner	Bin Slot Address Bit 0
	(Pull Ups on Board, 0 = GND, 1 = Open
19 Outer	Bin Slot Address Bit 1
19 Inner	Bin Slot Address Bit 2
19 Outer	Bin Slot Address Bit 3
20 Inner	Bin Slot Address Bit 4
20 Outer	Bin Slot Address Bit Parity

Address and Bit Assignments:

	Rack #	BB01	BB08
Bit Slot Address	1	20H	27H
	2	30H	37H

Control and Monitor Bit - See Drawing 54120D048
Relative Address* - and MCB Protocol in Acquisition Memo #65

Absolute Address = Address Placed in Indirect Location + Relative Address

Indirect Location = (Slot Address)*2 + 1 - See MCB Specification

Test Procedures:

Submodules can be tested individually using a bench test set-up. Complete module tests require the use of the station computer or a local replacement for the MCB control. One such replacement is the TRS-80 Model 100 and a printer. With this set-up test signals can be injected into the I.F. and converted to baseband for viewing on a scope

or plotting bandpasses on the printer. Drawing 54120K054 shows a check-out/test setup. The following checkout procedures have been used for modules serial numbers 9 through 16 after carefully inspecting boards for shorts and solder bridges:

1] Calibrate the square law detector submodules using a source of 5MHz at -22 dBm and a frequency counter or high quality scope.

2] Test filter boards in a working module.

3] Before appling power to the assembled module perform the following resistive checks and compare results with working module:

All I/O pins to ground (voltages,signals and address pins)
+ and - 6v to ground (at feedthrus on SSB mixer)
+ and -12v to ground (probe at regulators)
Front panel monitors to ground
All filter board control lines (should all be 20 K to gnd.)

Resolve any discrepencies. For example shorts between control lines will reduce resistance to ground (10 k for a single short). Shorts or incorrect power wiring will usually result in significant changes in the resistance to ground.

4] Apply power and check internal voltages +6,-6,+12,-12.

5] Establish MCB communication and set L.O. to 650 MHz

6] Check L.O. with a counter or analyser

7] Sweep converter and observe bandpass on USB and LSB monitors at 16 MHz and 62.5 kHz bandwidths.

8] After resolving any problems evident in previous tests run the automatic test software.

9] Check printout for deficiencies and if image rejection needs improving return to sweeper set-up and adjust input wire lengths and/or r.f. hybrid.

10] Check input switch isolation by switching to an unconnected input and injecting a much stronger test signal.

Replacement Instructions:

The baseband converter is a fairly complex module. Try to localize the malfunction to a particular submodule and then exchange the submodule. Be sure that the hardware control bits are being correctly set via the MCB. These can be probed on the digital interface board at

the locations given in Drawing 54120D053. "Solderwick" should be used to remove defective components from PC boards.

Parts List:

Data Sheets:

12040
SD5002N
NE5539N
ADFC32
10G070
5082-2835
5082-2810
BD4
LMX-113
MA46577B-20
JH-140
ATC-100
LH033CG (See 5 MHz Distributor)
GPD-1002
GPD-1003
RT/Duroid
OP-27
OP-07
TLC372CP
PSW-1211
MGF-1402

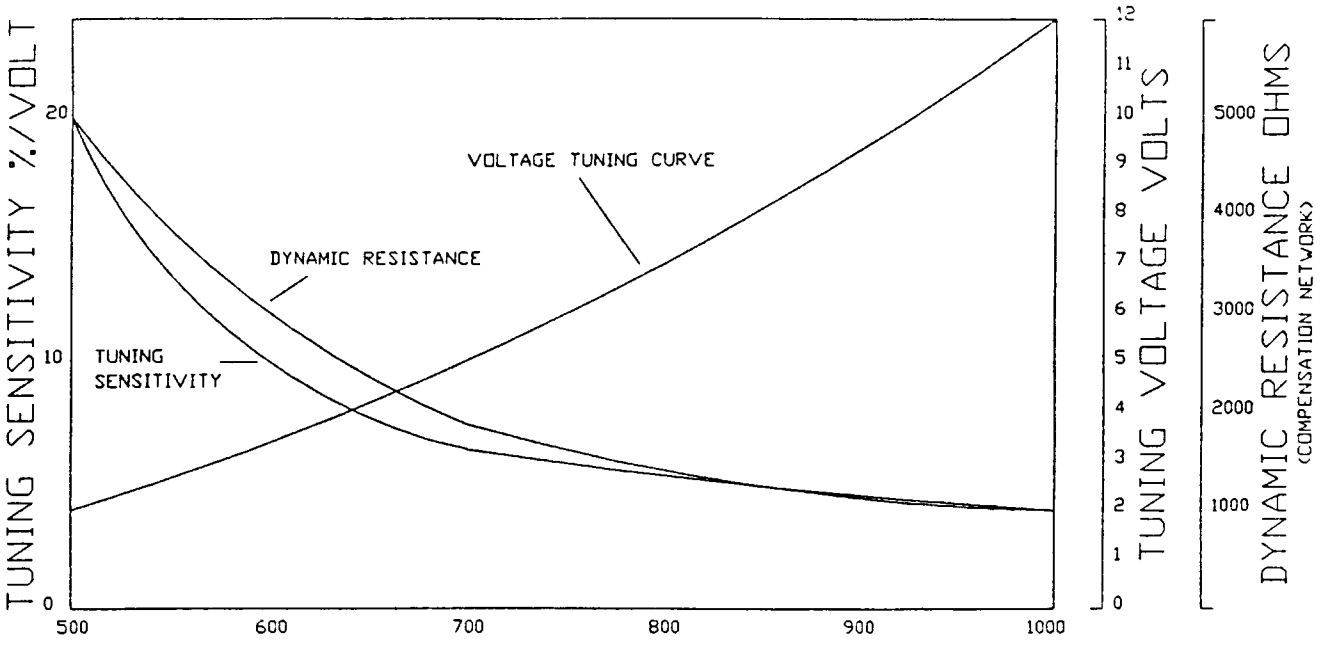
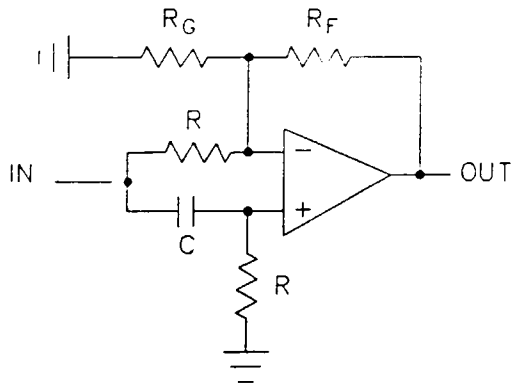


FIGURE 1 500-1000 MHZ VOLTAGE CONTROLLED OSCILLATOR

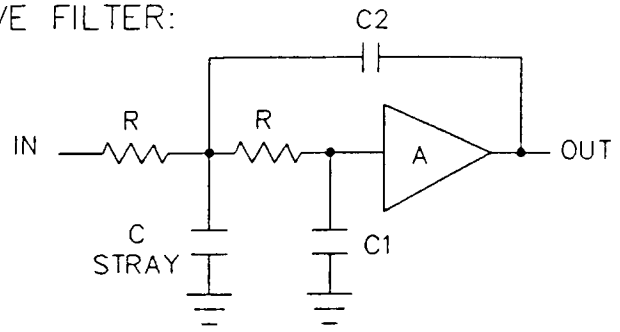
ALL PASS:



$$\text{TRANSFER FUNCTION} = \left(\frac{R_F}{R}\right)\left(\frac{RSC - 1}{RSC + 1}\right)$$

$$\text{WHEN} \qquad \frac{R}{R_G} + \frac{R}{R_F} = 1$$

ACTIVE FILTER:



$$\text{TRANSFER FUNCTION} = A/[1 + 2RSC_1 + S^2R^2C_1(C_2 + C\ \text{stray})]$$

$$\text{WHEN} \qquad A = 1 + (C\ \text{stray}/C_2)$$

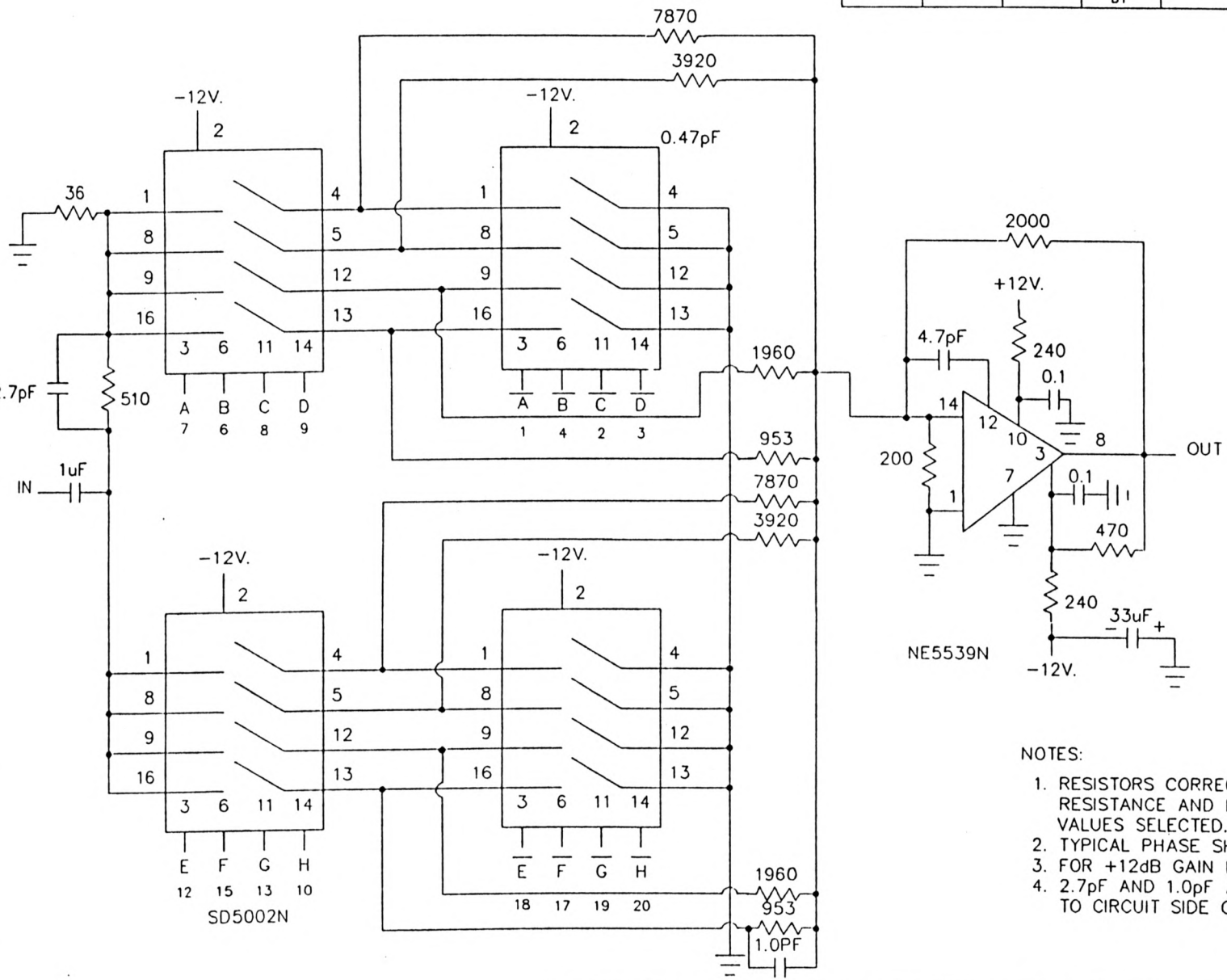
$$\text{FREQUENCY} = [1/(C_1(C_2 + C\ \text{stray}))]^{1/2}(1/R) \quad \text{rad/sec}$$

$$Q = ((C_2 + C\ \text{stray})/C_1)^{1/2}(1/2)$$

FIGURE 2 SIMPLIFIED CIRCUIT ANALYSIS FOR NE5539 CIRCUITS (USED IN VLBA BASEBAND CONVERTER)

NOTES:
1. SEE TEXT FOR COMPENSATION NETWORK FOR STABLE OPERATION.
2. SEE TEXT FOR DISCUSSION OF COMPUTER CIRCUIT SIMULATIONS.

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



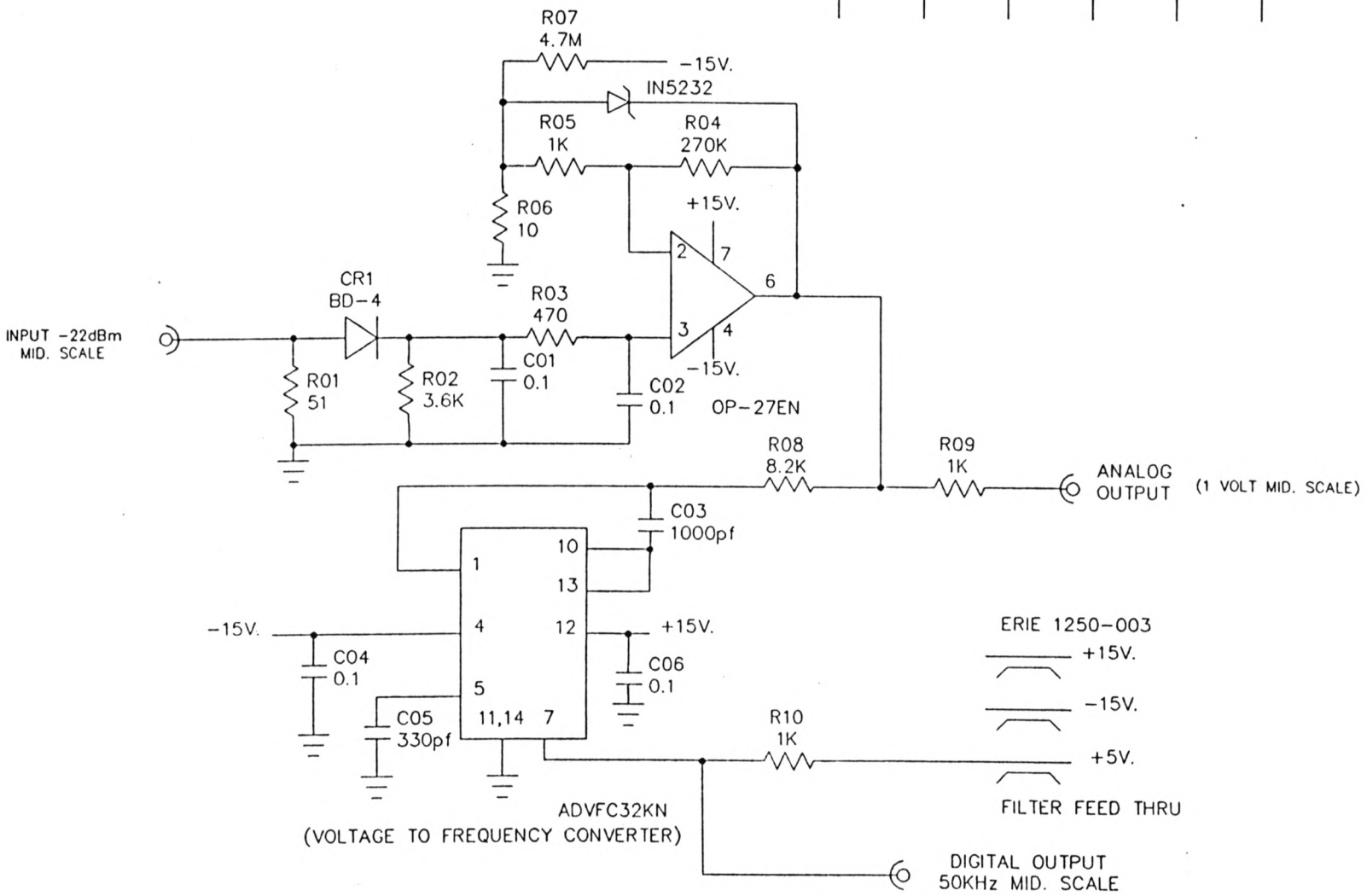
NOTES:

1. RESISTORS CORRECTED FOR 40 OHMS ON RESISTANCE AND NEAREST STANDARD VALUES SELECTED.
2. TYPICAL PHASE SHIFT 50ps/db
3. FOR +12dB GAIN LSB = .03dB
4. 2.7pF AND 1.0pF ARE SOLDERED TO CIRCUIT SIDE OF PC BOARD.

C - 54120S001

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 4/87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	4/87	DIGITAL ATTENUATOR FOR AGC VLBA BASEBAND CONVERTER
		CHECKED BY:		
LAST CHANGE MADE 10/21/88	SCALE NONE	APPROVAL PROJECT		AER\DIGATT / C / 54120S001 /
	CLASSIFICATION	ENGINEER		DWG SIZE / DWG NO / REV

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



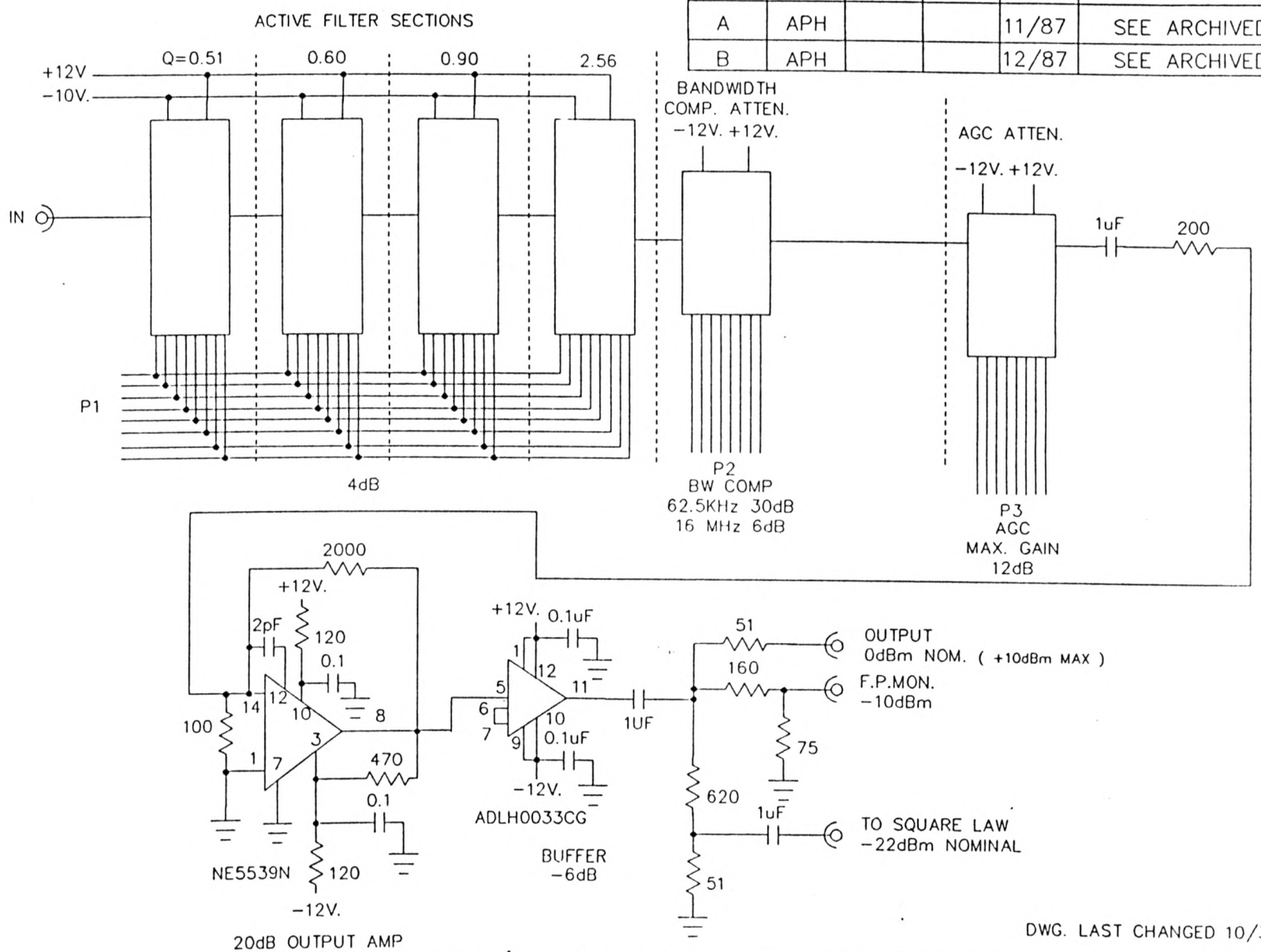
C - 54120S002

NOTES:

1. A 30uV D.C. OFFSET IS USED TO ENSURE THAT OUTPUT FREQUENCY > 0.
2. R04 IS ADJUSTED TO MAKE -22dBm = 1VOLT.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	7-87	SQUARE LAW DETECTOR
		CHECKED BY:		
	SCALE NONE	APPROVAL PROJECT		C / 54120S002
	CLASSIFICATION	ENGINEER:		AER\SQUARE / DWG SIZE / DWG NO / REV

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION
A	APH			11/87	SEE ARCHIVED DISKS
B	APH			12/87	SEE ARCHIVED DISKS



B

C - 54120S003

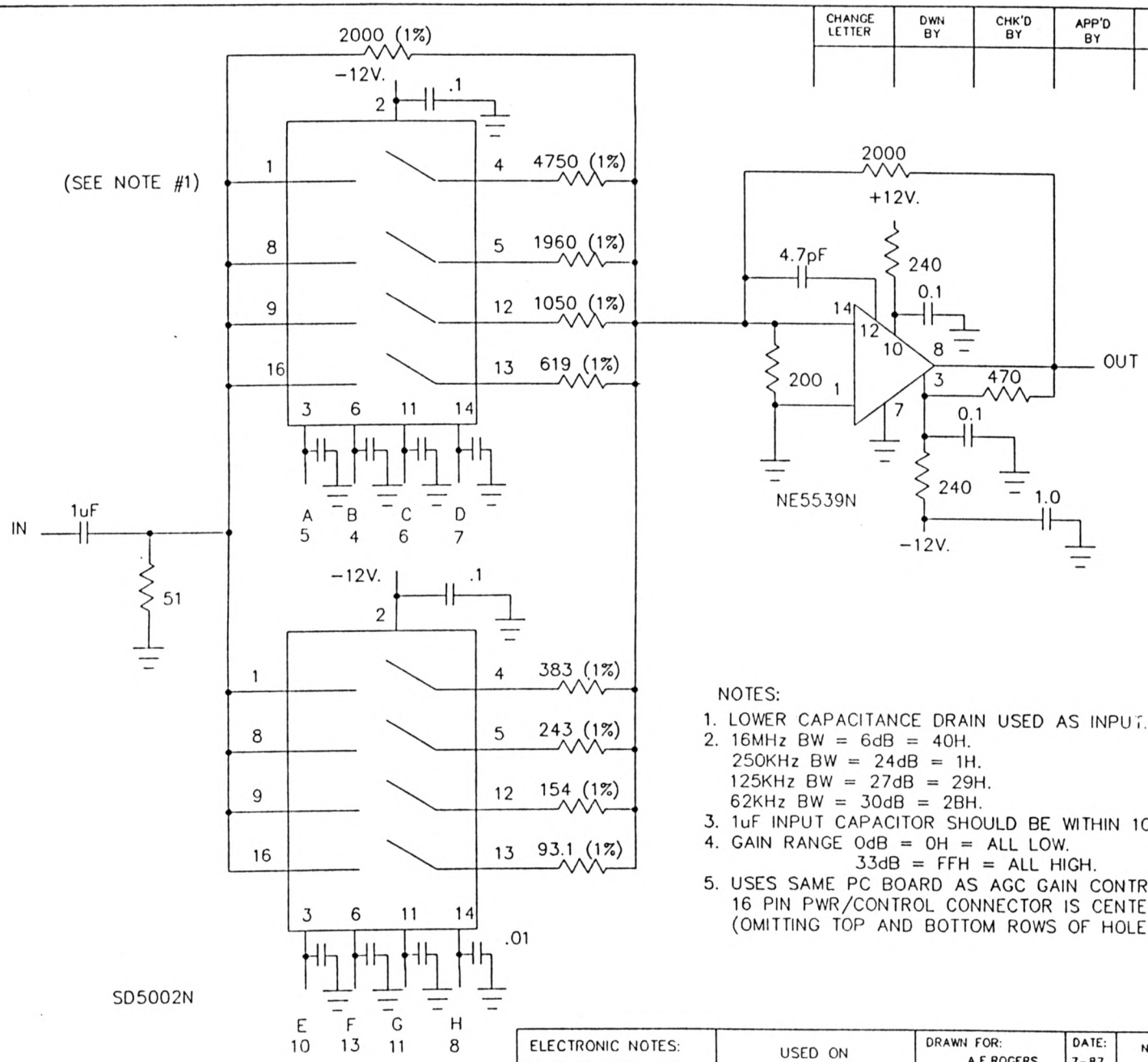
DWG. LAST CHANGED 10/31/88

NOTES:

1. DASHED LINES INDICATE SEPARATE PC BOARD SECTIONS.
2. SEE DRAWINGS 54120S012, 54120S001, AND 54120S004 FOR CIRCUITS OF ACTIVE FILTER, BANDWIDTH COMP., ATTEN. AND AGC.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 3/87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	3/87	BASEBAND FILT/AMP (BASEBAND FILTERS & BW GAIN & AGC)
		CHECKED BY:		
SCALE	PROJECT	APPROVAL		C / 54120S003 / B
CLASSIFICATION	ENGINEER			DWG NO REV

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



9 ——— +12V.

3 ——— -12V.

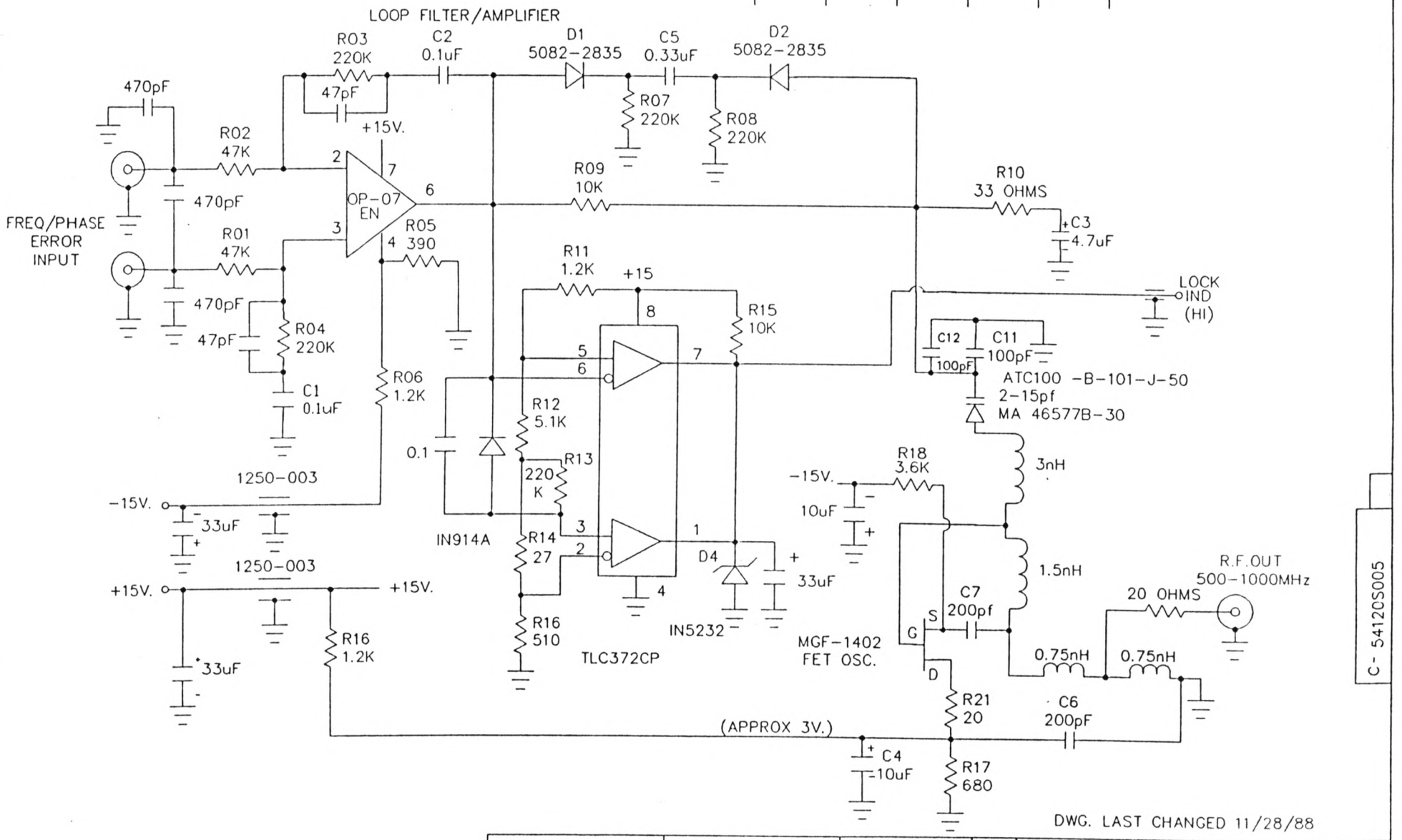
NOTES:

1. LOWER CAPACITANCE DRAIN USED AS INPUT.
2. 16MHz BW = 6dB = 40H.
   250KHz BW = 24dB = 1H.
   125KHz BW = 27dB = 29H.
   62KHz BW = 30dB = 2BH.
3. 1uF INPUT CAPACITOR SHOULD BE WITHIN 10%.
4. GAIN RANGE 0dB = 0H = ALL LOW.
   33dB = FFH = ALL HIGH.
5. USES SAME PC BOARD AS AGC GAIN CONTROL.
   16 PIN PWR/CONTROL CONNECTOR IS CENTERED
   (OMITTING TOP AND BOTTOM ROWS OF HOLES)

C- 54120S004

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	7-87	DIGITAL ATTENUATOR FOR BW COMPENSATION VLBA BASEBAND CONVERTER
		CHECKED BY:		
	SCALE NONE	APPROVAL PROJECT		C / 54120S004 /
	CLASSIFICATION	ENGINEER		AFR\BWCOMP / DWG SIZE / DWG NO / REV

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



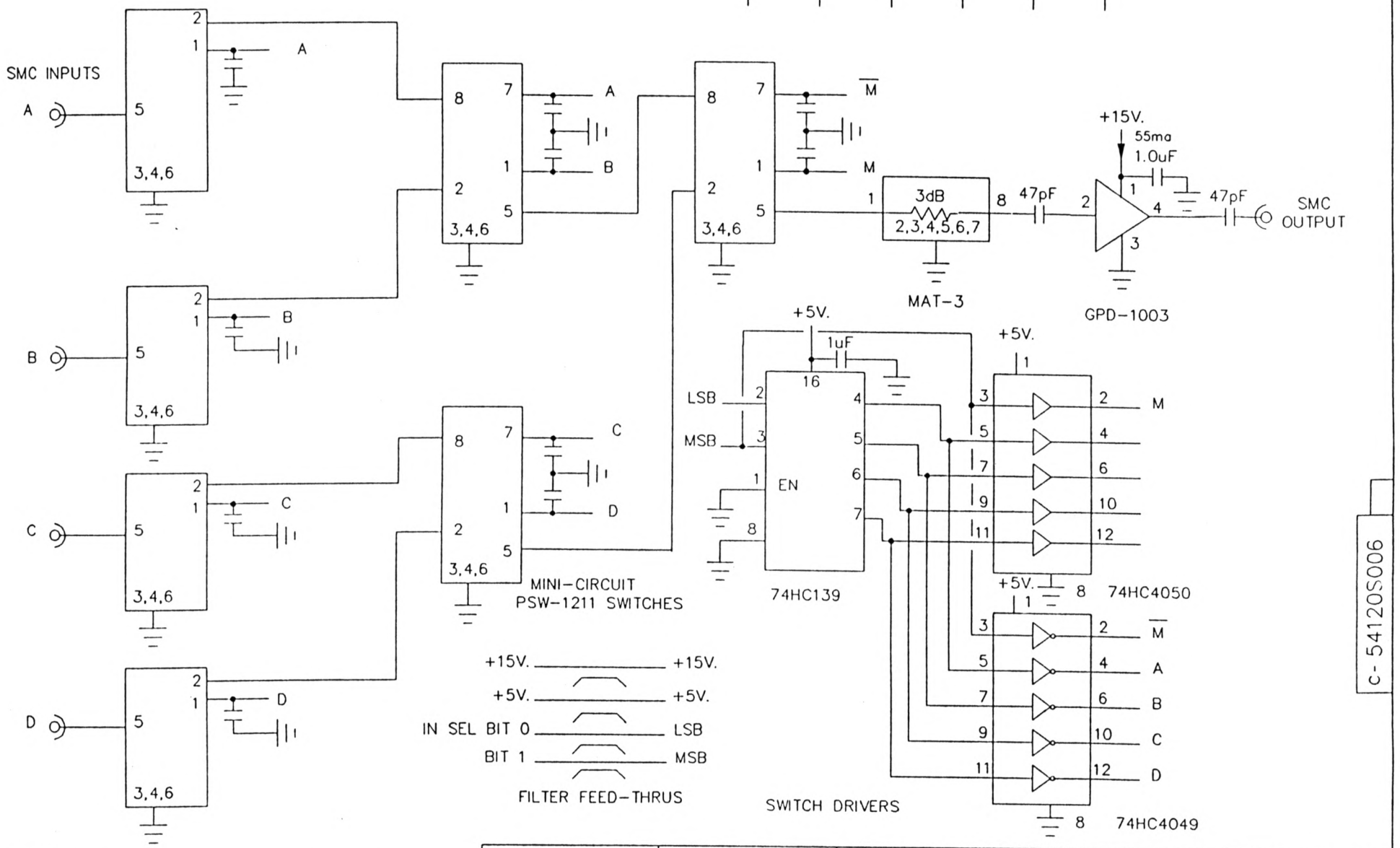
DWG. LAST CHANGED 11/28/88

NOTES:

1. IF NEEDED A TRIM RESISTOR OF 100K CAN BE ADDED BETWEEN PINS 1 OR 8 AND +15V (PIN 7) TO NULL 10KHz SIDEBANDS.
2. FERRITE CORE 4C4 IS PLACED BETWEEN MGF-1402 GATE AND SOURCE TO ELIMINATE THE TENDANCY FOR PARASITIC OSCILLATION AT 3GHz.
3. R16 MAY HAVE TO BE ADJUSTED FOR OPTIMUM FET BIAS.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 2/88	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.P.HEBERT	2/88	SYNTHESIZER OSCILLATOR (SUB-MODULE FOR BASEBAND CONVERTER) (WITH IMPROVED LOCK INDICATORS)
		CHECKED BY.		
	SCALE NONE	PROJECT		C / 54120S005
	CLASSIFICATION	ENGINEER		

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

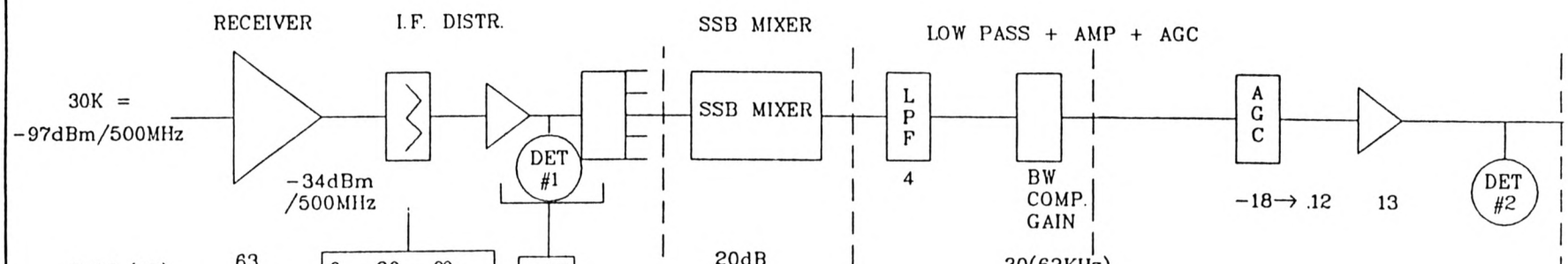


c- 541205006

NOTES:
1. ALL CAPACITORS ARE ATC100B201JMS50 EXCEPT AS NOTED.
2. ON SOME UNITS SOME FERROXCUBE 3E2A MATERIAL HAS BEEN PLACED NEAR INPUTS TO SUPPRESS RESONANCES.
3. COPPER FOIL IS USED TO FILL SPACE BETWEEN INPUT SWITCHES AND FRONT FACE OF BOX.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 4/87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	4/87	4-WAY SWITCH SUB MODULE FOR BASEBAND CONVERTER PC-BOARD 0dB GAIN, >70dB ISOLATION
		CHECKED BY:		
	SCALE NONE	APPROVAL PROJECT		C / 541205006
	CLASSIFICATION	ENGINEER		AER\SW3UBMOD / DWG SIZE / DWG NO / REV

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



NORMAL POWER LEVELS (30° K INPUT–0dB ATTEN SETTING)

(3,000 K –20dB ATTEN SETTING)	–30dBm/500MHz	–20dBm/50MHz	–15dBm	AGC = 2dB	0dBm
3,000 K LINE IN 62.5KHz CHANNEL [1]	–30dBm/500MHz	–20dBm	+5dBm	AGC= –18 dB	0dBm
1dB GAIN COMPRESSION LEVELS	6dBm	16dBm			+13dBm
INTERNAL NOISE LEVELS	–62dBm/500MHz (100,000K INCLUDING MIXER)				

DERIVED FROM ABOVE:

BASEBAND SNR BETTER THAN 32dB
WORST CASE SENSITIVITY INTERFERENCE WITHIN I.F. – BUT
OUTSIDE BASEBAND CHANNEL –71dBm AT FRONT – END INPUT.
DETECTOR #1 READS 1 VOLT AT –34dBm INPUT LEVEL FROM RECEIVER
DETECTOR #2 READS 1 VOLT AT 0dBm BASEBAND OUTPUT
(–10 dBm ON FRONT PANEL BNC MONITOR OUTPUT)

C—54120K007 A

NOTES

1. FOR STRONGER LINES THE BW COMP. GAIN CAN BE DECREASED TO AVOID RUNNING AGC BELOW –18dB

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0.5°
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE

CLASSIFICATION

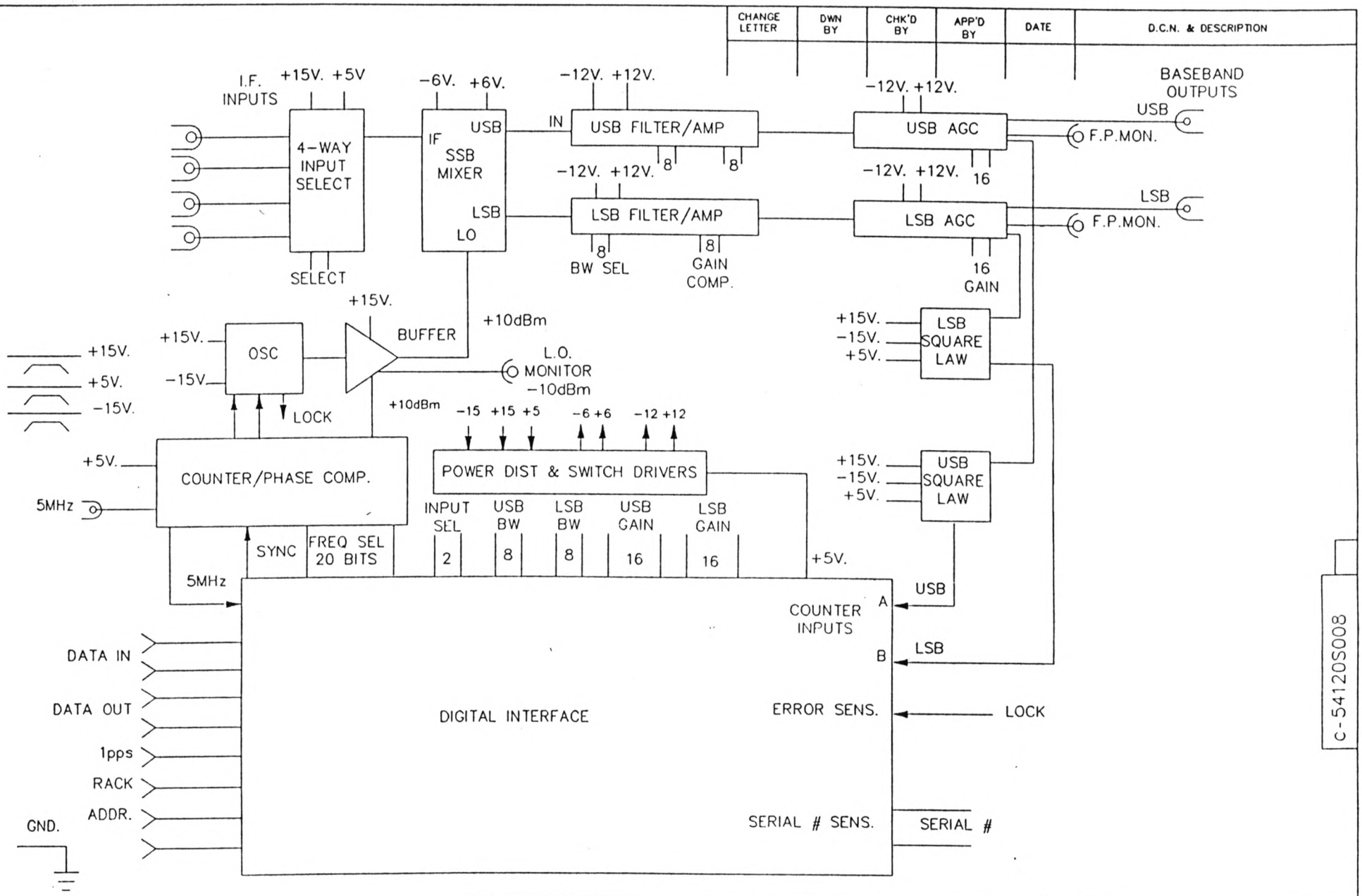
APPROVALS		
DRAWN FOR	A.E. ROGERS	DATE 1-87
DRAWN BY	A. PHILBROOK	1-87
CHECKED BY		
PROJECT ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
[redacted]		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

SIGNAL LEVELS IN VLBA RECEIVING SYSTEM

C	54120K007	A

APPV [redacted] DWG [redacted] DWN [redacted]



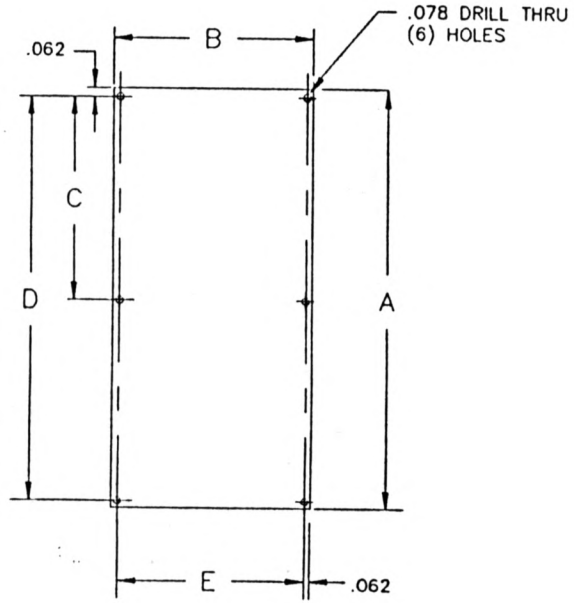
NOTES:

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS	
		DRAWN BY: A.PHILBROOK	7-87	BASEBAND CONVERTER 2 WIDE MODULE	
		CHECKED BY:			
	SCALE NONE	APPROVAL PROJECT		C	54120S008
	CLASSIFICATION	ENGINEER:		AER\BASCONV	DWG. SIZE / DWG. NO. / REV.

CHANGE LETTER	D'VN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

ITEMIZED TOP COVER DATA

	DIMENSIONS				
ITEM	A	B	C	D	E
1	1.75	1.50	.812	1.625	1.375
2	2.50	1.45	1.187	2.375	1.325
3	4.25	2.00	2.062	4.125	1.875
4	4.50	3.00	2.187	4.375	2.875



C-54120M009 A

NOTES

MATERIAL
.062 ALUM. 6061-T6

FINISH AND/OR HEAT TREATMENT
CLEAR ALODINE
(CONDUCTIVE FINISH)

SHOP NOTES: UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
FRACTIONAL ± 1/64
DECIMAL .XX ± .01
DECIMAL .XXX ± .005
ANGULAR ± 0°30'
3. SURFACE ROUGHNESS 63
PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY
WEIGHT
SCALE
CLASSIFICATION

APPROVALS

		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
[redacted]YSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

ITEMIZED TOP COVER PROTOTYPE
P.C.BOARD BOX
VLBA

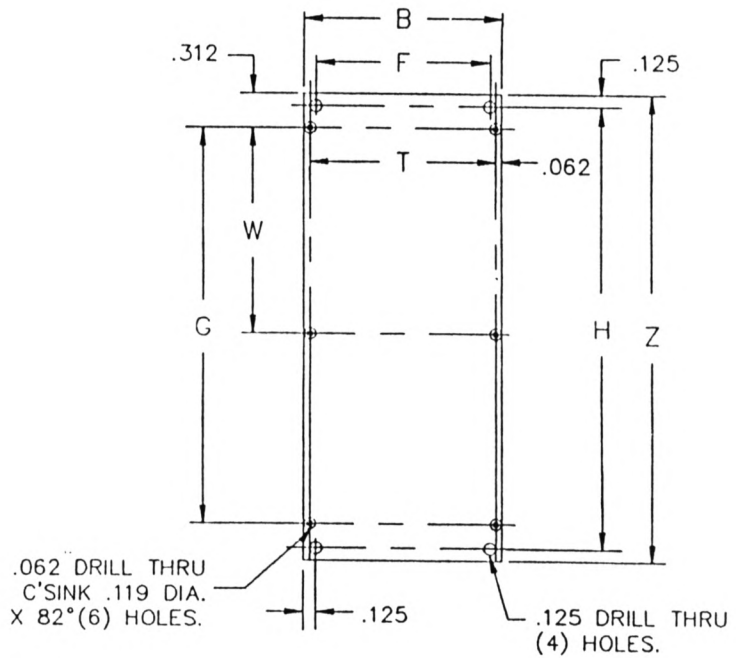
C 54120M009 A

AE[redacted] DW[redacted]

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

ITEMIZED BOTTOM COVER DATA

	DIMENSIONS						
ITEM	B	F	G	H	Z	W	T
1	1.50	1.250	1.625	2.000	2.25	.812	1.375
2	1.45	1.200	2.375	2.750	3.00	1.187	1.325
3	2.00	1.750	4.125	4.500	4.75	2.062	1.875
4	3.00	2.750	4.375	4.750	5.00	2.187	2.875



C-54120M010 A

NOTES

MATERIAL
.062 ALUM. 6061-T6

FINISH AND/OR HEAT TREATMENT
CLEAR ALODINE
(CONDUCTIVE FINISH)

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS 63 PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

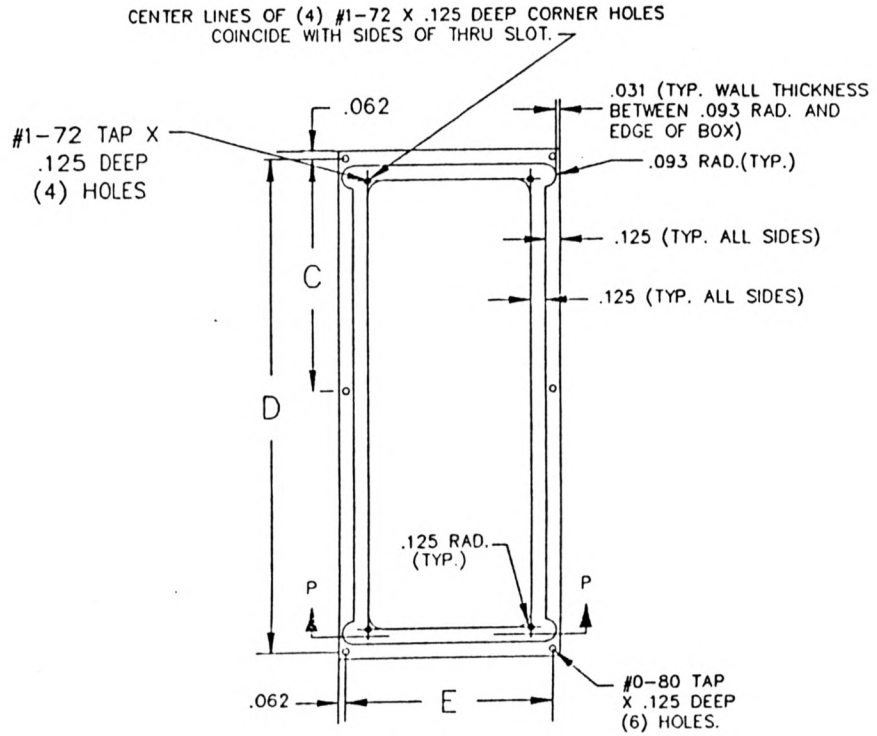
APPROVALS		
	DRAWN FOR A.E.ROGERS	DATE 7-87
	DRAWN BY A.PHILBROOK	7-87
	CHECKED BY	
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

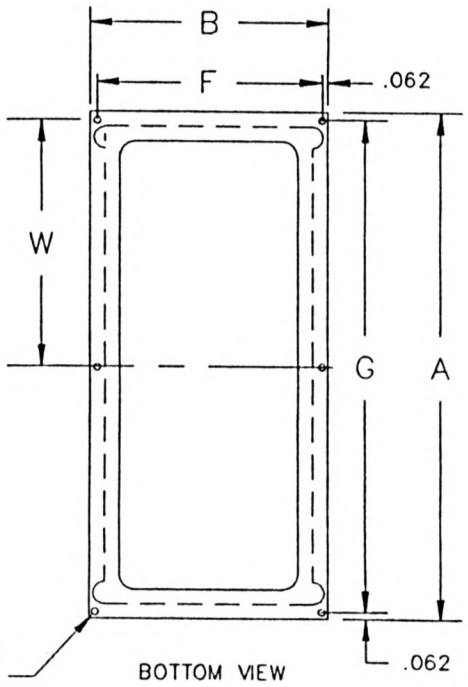
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

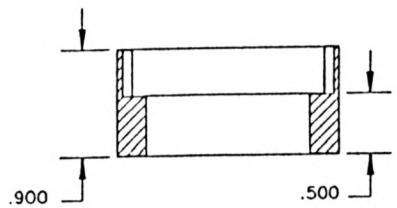
ITEMIZED BOTTOM COVER
PROTOTYPE P.C.BOARD BOX
VLBA

AER\ITEMBOT	C	54120M010	A
	DWG. SIZE	DWG. NO	REV.

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION
B	APH			8/87	CHANGED FROM #0-80 TO #1-72 HOLES







SECTION P-P

ITEMIZED BOX DATA

		DIMENSIONS								
ITEM	SUGGESTED PART#	A	B	C	D	E	F	G	W	P.C. BOARD SIZE
1	HAY17515	1.75	1.50	.812	1.625	1.375	1.375	1.625	.812	1.5 X 1.25
2	HAY25014	2.50	1.45	1.187	2.375	1.325	1.325	2.375	1.187	2.25 X 1.20
3	HAY42520	4.25	2.00	2.062	4.125	1.875	1.875	4.125	2.062	4.00 X 1.750
4	HAY45030	4.50	3.00	2.187	4.375	2.875	2.875	4.375	2.187	4.25 X 2.75

C-54120M011 B

NOTES

MATERIAL

ALUM. 6061-T6

FINISH AND/OR HEAT TREATMENT

CLEAR ALODINE (CONDUCTIVE FINISH)

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 (63)
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

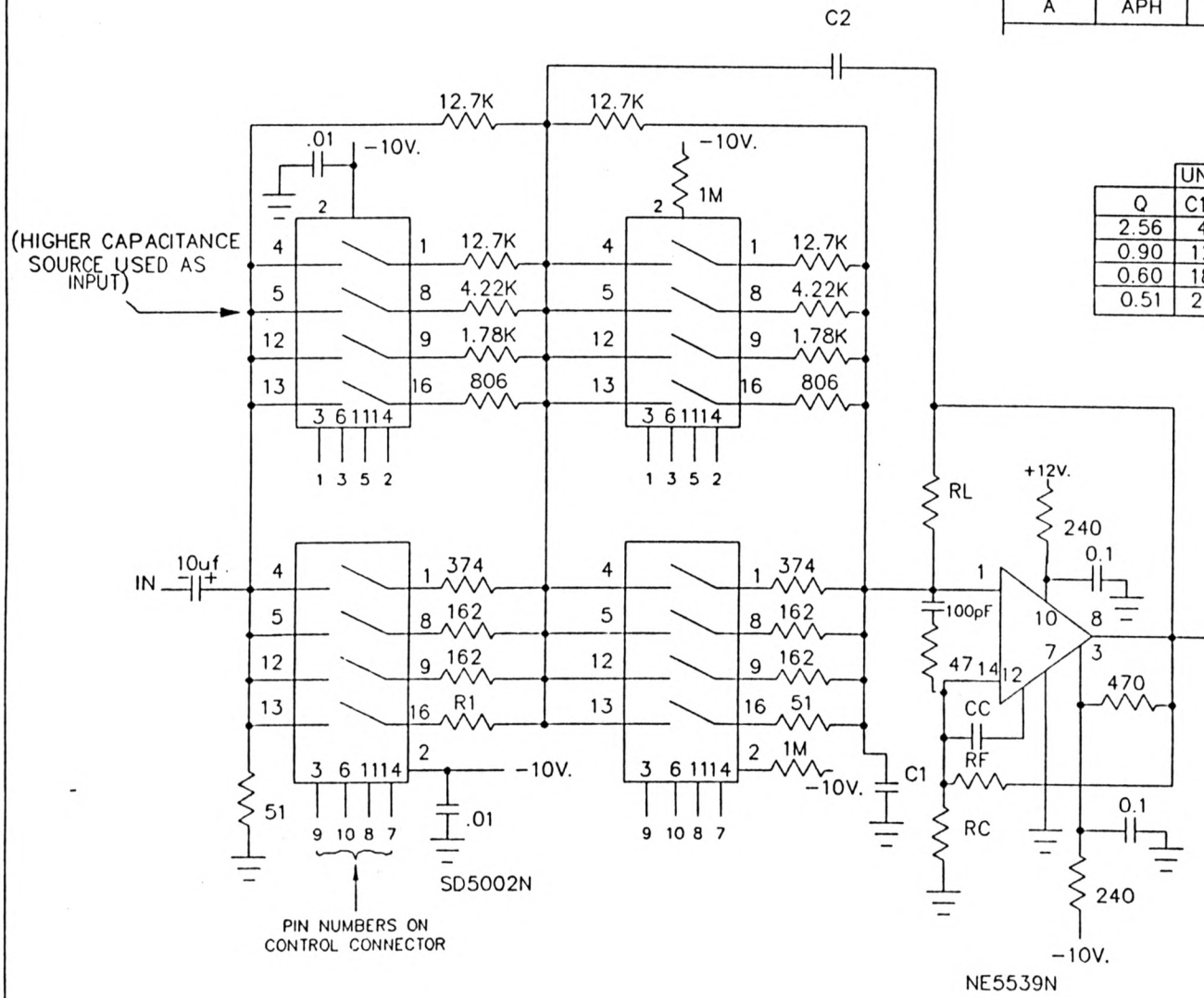
		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A PHILBROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

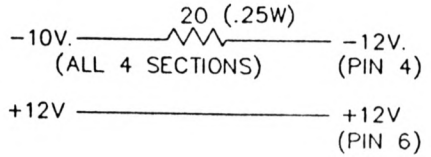
ITEMIZED PROTOTYPE P.C. BOARD BOX
VLBA

AEROSPACE MFGR	DWG. SIZE	DWG. NO.	REV.
	C	54120M011	B

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION
A	APH			12/87	REMOVED CAP FROM PIN 4 OF SD5002N



	UNCORRECTED		CORRECTED				
Q	C1pF	C2pF	C1pF	C2pF	RC	RF	CCpF
2.56	43	1133	22	1000	2.7K	220	150
0.90	123	398	100	390	2.7K	470	47
0.60	184	266	150	220	3.3K	470	47
0.51	217	225	200	180	3.3K	470	47



NOTES:

1. RESISTOR VALUES CORRECTED FOR 40 OHMS SWITCH ON RESISTANCE.
2. C1 CORRECTED FOR 20pF TO GROUND.
3. 62KHz BW ALL INPUTS LOW.
4. 16MHz BW ALL INPUTS HIGH.
5. 20 OHM RESISTORS (ON INPUT SECTION) DROP SUPPLY VOLTAGE FOR ALL FOUR SECTIONS.
6. "Q" CORRECTED FOR 40pF TO GROUND USING "RC".
7. RL IS NEEDED ON Q = 2.56 SECTION VALUE APPROX. 20K TO COMPENSATE FOR 5539 INPUT RESISTANCE.
8. CONTROL LINES ARE BYPASSED WITH 0.01uF TO GROUND ON INPUT SECTION.
9. R1 IS 51.1 OHMS EXCEPT ON Q=0.51 FOR WHICH IT HAS A VALUE OF 10 OHMS TO COMPENSATE FOR 50 OHM OUTPUT IMPEDENCE OF SSB MIXER.
10. ON Q=2.56 SECTION 51 OHM RESISTORS HAVE 180pF CAPACITORS IN PARALLEL.
11. 10uf INPUT CAPACTIOR IS ONLY ON Q=2.56 SECTION OTHER SECTIONS HAVE JUMPER.

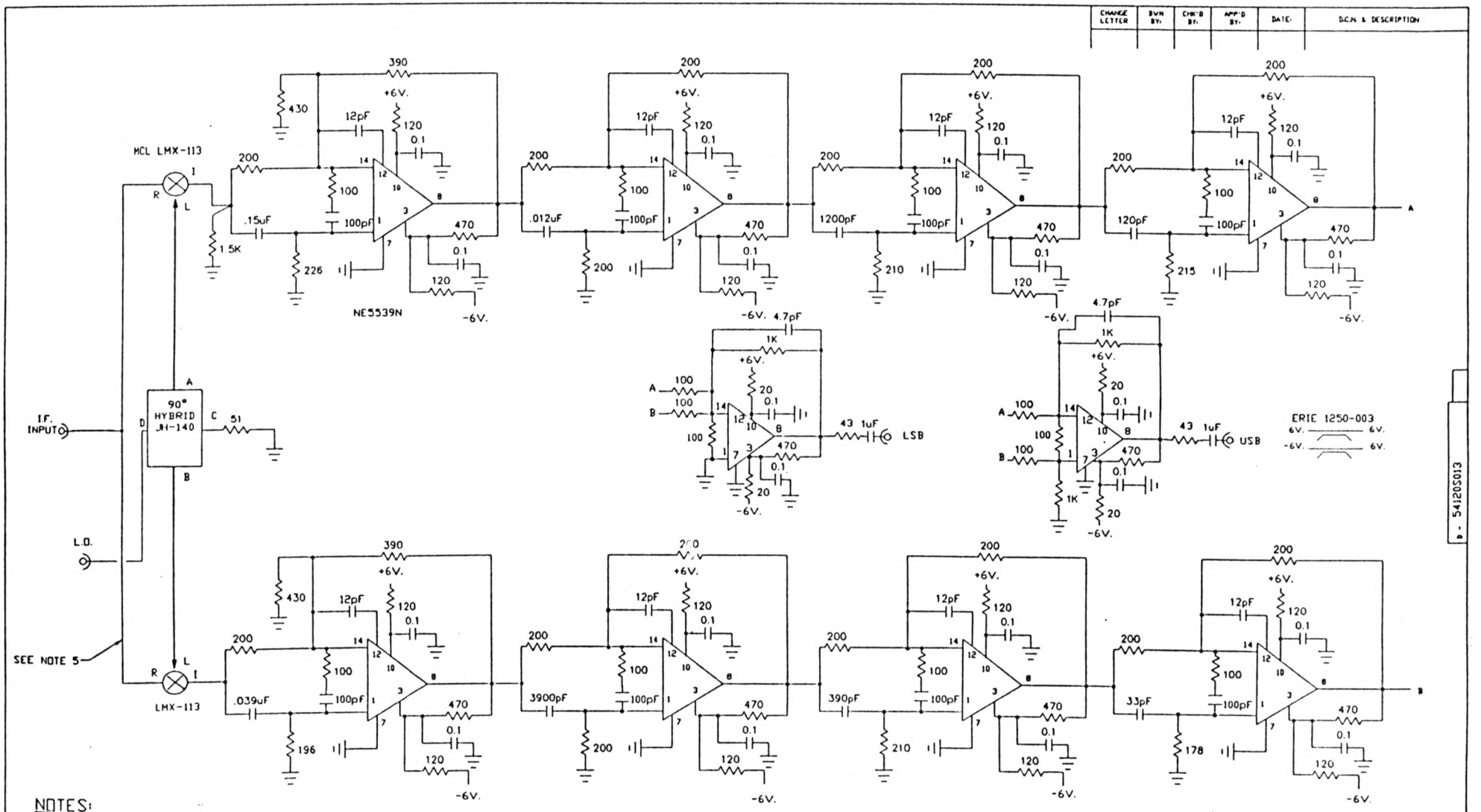
DWG. LAST CHANGED 10/31/88

C- 54120S012 A

NOTES:

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	7-87	
		CHECKED BY:		BASEBAND CONVERTER ACTIVE FILTER SECTION
	SCALE NONE	APPROVAL PROJECT		
	CLASSIFICATION	ENGINEER:		

AERSACTFILT	C	54120S012	A
	DWG SIZE	DWG NO	REV



NOTES:

1. GAIN APPROX. 20dB
2. N.F. APPROX. 26dB
3. SUPPLY CURRENT APPROX. 200ma.
4. IN SOME UNITS A RESISTOR (APPROX. 200 OHMS) IS PLACED BETWEEN PORTS C AND D TO TRIM PHASE FOR BETTER IMAGE REJECTION
5. INPUT LINE LENGTHS CAN BE TRIMMED FOR BEST IMAGE REJECTION.

DWG. LAST CHANGED 11/14/88

CHANGE LETTER	BY/N BY:	CHK'D BY:	APP'D BY:	DATE:	DESCRIPTION

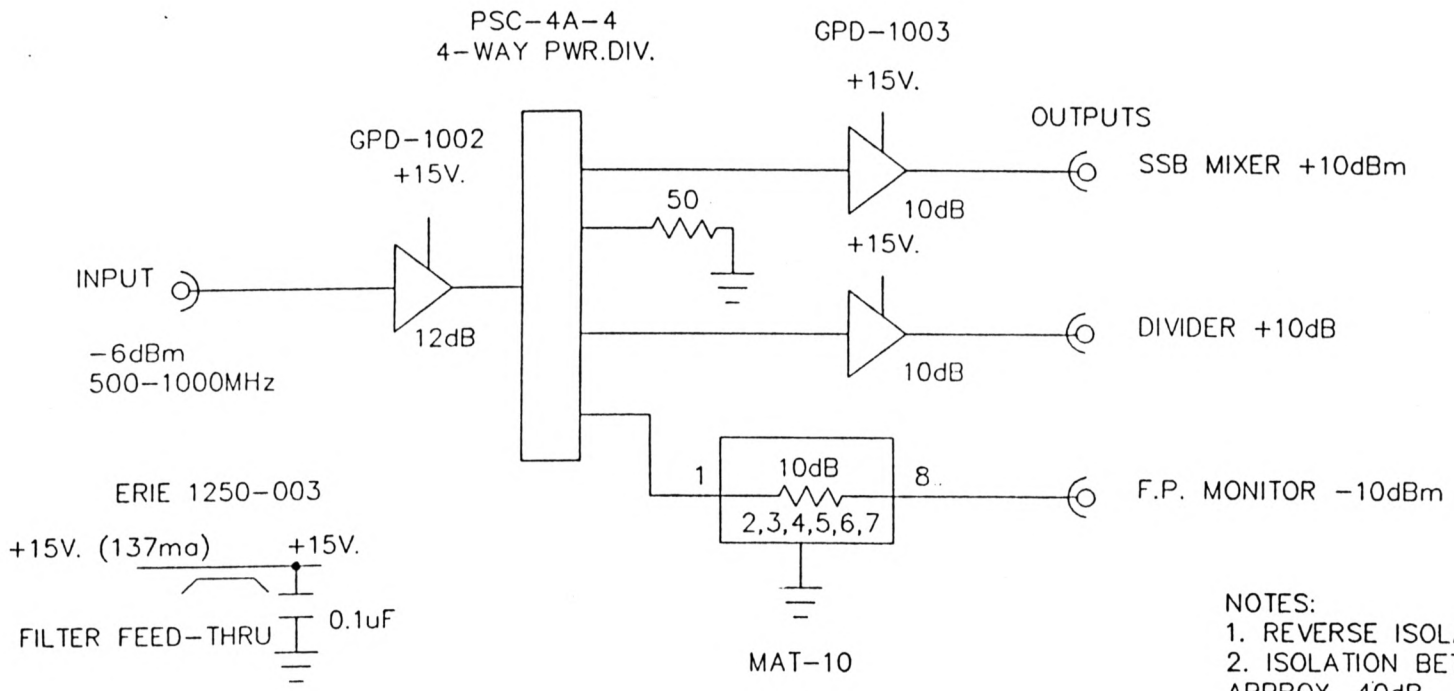
ELECTRONICS NOTES: UNLESS OTHERWISE NOTED: RESISTORS: INDUCTORS: CAPACITORS:	USED ON	DRAWN FOR: A.E. ROGERS	DATE 2-87
		DRAWN BY: A. PHILBROOK	2-87
	SCALE:	CHECKED BY:	
		ENGINEER:	

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD MASSACHUSETTS

SSB MIXER
SUBMODULE FOR BASEBAND CONVERTER

D - 54120S013

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



NOTES:
1. REVERSE ISOLATION APPROX. 65dB.
2. ISOLATION BETWEEN OUTPUTS APPROX. 40dB

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

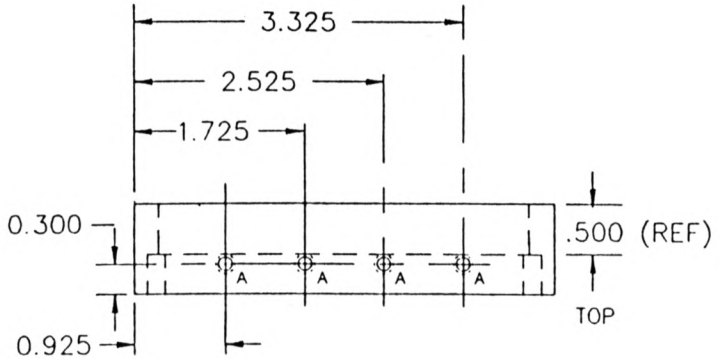
DRAWN FOR	A.E.ROGERS	DATE 11-85
DRAWN BY	A.PHILBROOK	11-85
CHECKED BY		

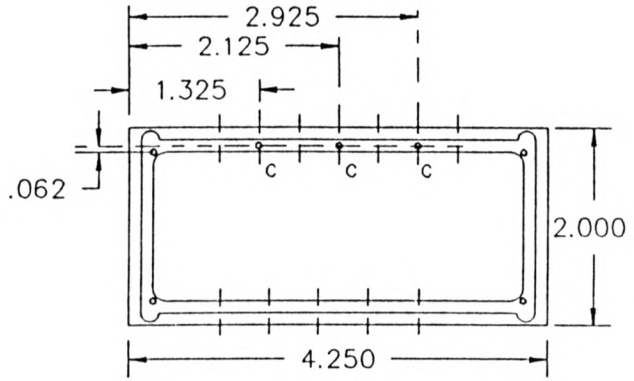
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

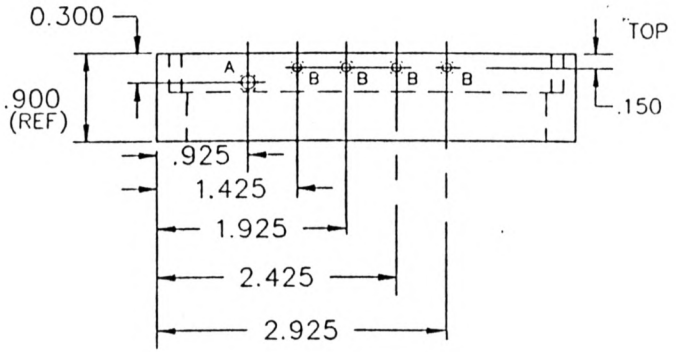
OSCILLATOR BUFFER SUBMODULE FOR BASEBAND CONVERTER P.C.BOARD

AER\OSCBUFF	B	54120S014	
	DWG. SIZE	DWG. NO.	REV.

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION
A	APH			8/87	ADDED (3) "C" HOLES







1. #10-32 TAP THRU (5) "A" HOLES.
2. #8-32 TAP THRU (4) "B" HOLES.
3. #1-72 TAP X .125 DEEP (3) "C" HOLES.

C—54120M015 A

NOTES

MATERIAL

REFER TO ITEMIZED PROTOTYPE P.C. BOARD VLBA, ITEM 3

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		

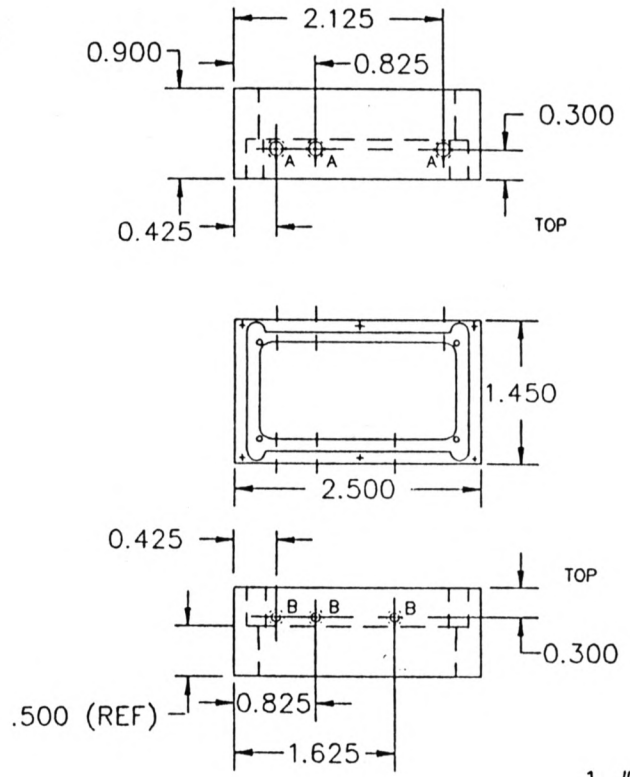
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

BOX DRILLING PLAN
FOR 4-WAY SWITCH

C 54120M015 A

AERV[redacted] DWG. S[redacted] DWG [redacted]

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. #10-32 TAP THRU (3) "A" HOLES
2. #8-32 TAP THRU (3) "B" HOLES

C-54120M016

NOTES

MATERIAL

REFER TO ITEMIZED PROTOTYPE P.C. BOARD VLBA, ITEM 2

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0.30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

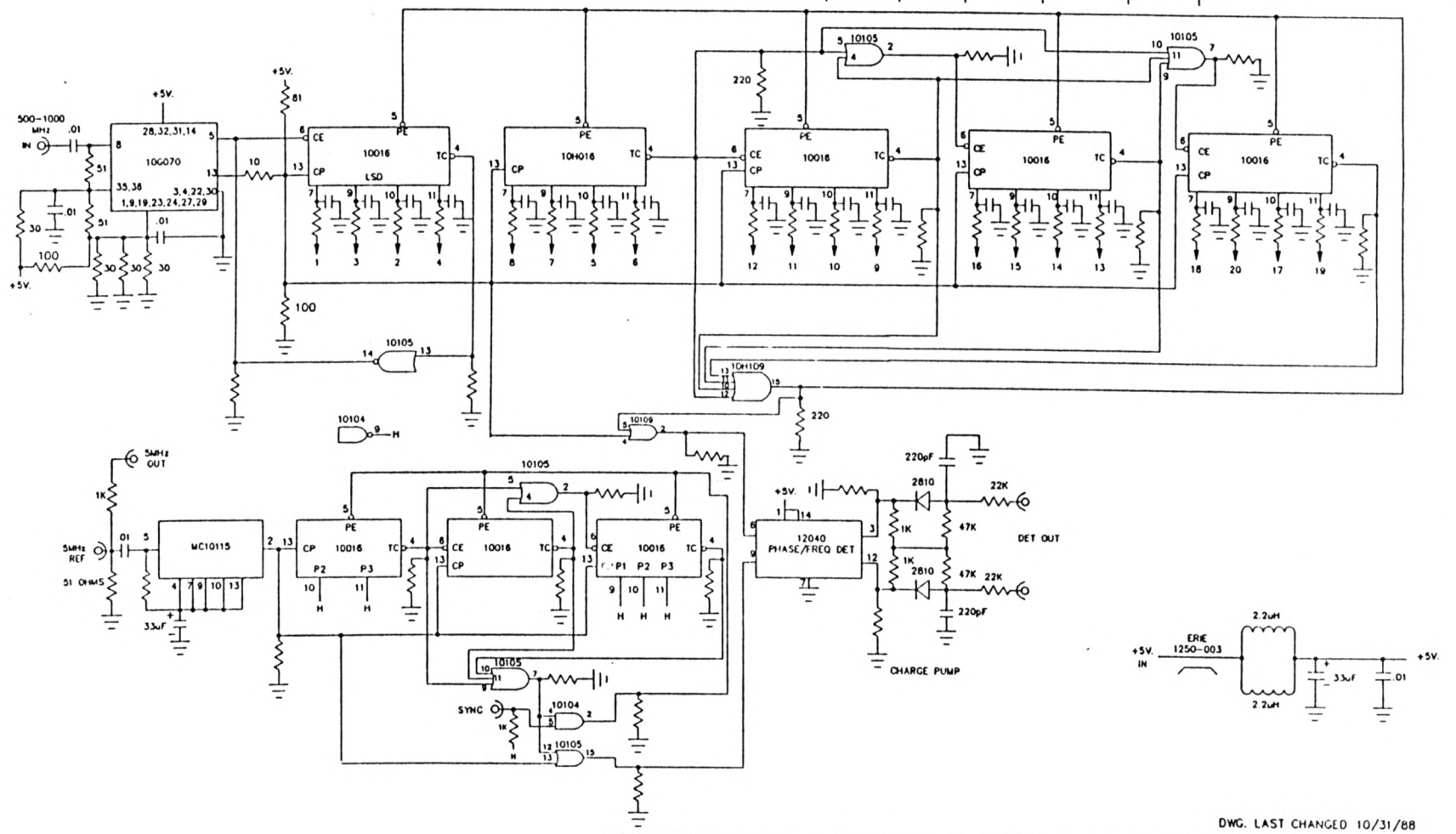
		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

BOX DRILLING PLAN FOR OSCILLATOR SUBMODULE

	C	54120M016

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	D.C.N. & DESCRIPTION



D - 541200017

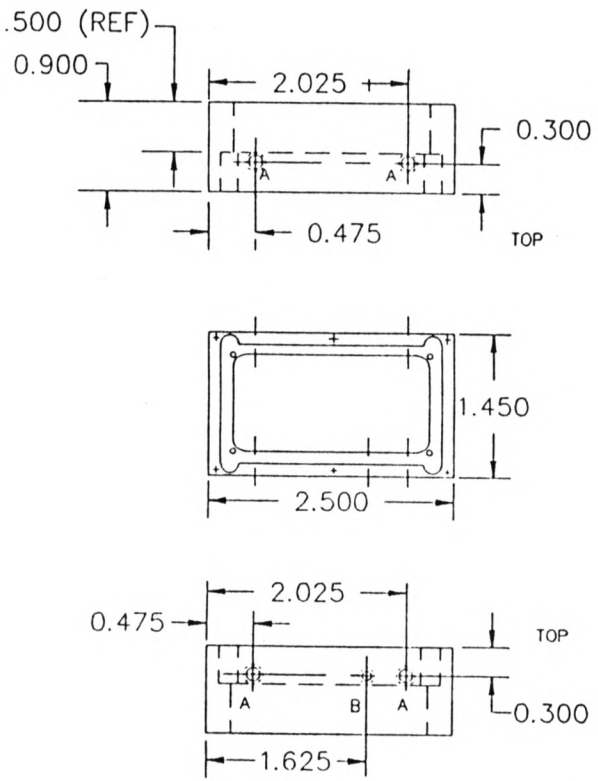
DWG. LAST CHANGED 10/31/88

NOTES:

1. ALL TERMINATION RESISTORS ARE 330 OHMS UNLESS OTHERWISE NOTED.
2. ALL RESISTORS IN SERIES WITH ECL FREQUENCY INPUTS ARE 1.5K.
3. ALL CAPACITORS ARE .01uF UNLESS OTHERWISE NOTED.
4. ADDITIONAL CAPACITORS ACROSS +5V. ARE DISTRIBUTED AROUND BOARD.
5. IT IS RECOMMENDED THAT ALL IC'S BE MOTOROLA 10KH SERIES.
6. 2 OF THE TERMINATIONS ARE ON CIRCUIT SIDE OF BOARD.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED	USED ON:	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
RESISTORS:		DRAWN BY: A.PHILBROOK	7-87	
CAPICTORS:		APPROVALS: CHECKED BY:		SYNTHESIZER COUNTER/DIVIDER SUBMODULE FOR BASEBAND CONVERTER
INDUCTORS:		PROJECT:		
	SCALE NONE	ENGINEER:		
	CLASSIFICATION	MAT'L & FINISH:		D 541205017

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. #10-32 TAPPED THRU (4) "A" HOLES
2. #8-32 TAPPED THRU (1) "B" HOLE

C — 54120M018

NOTES

MATERIAL

REFER TO ITEMIZED PROTOTYPE P.C. BOARD VLBA, ITEM 2

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0.30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

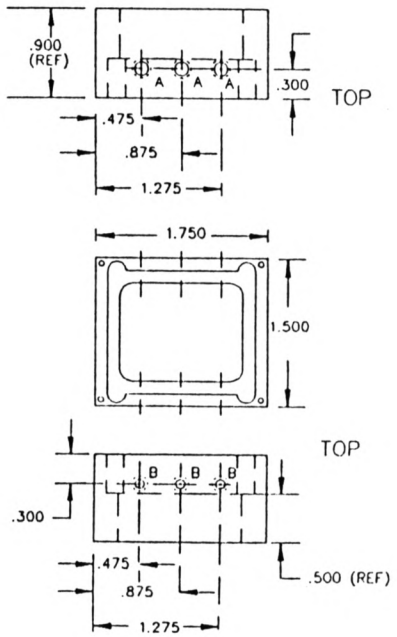
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

BOX DRILLING PLAN FOR
OSCILLATOR BUFFER

AER\DWGDRILL	DWG SIZE	DWG NO	REV.
	C	54120M018	

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. #10-32 TAPPED THRU (3) "A" HOLES
2. #8-32 TAPPED THRU (3) "B" HOLES

C — 54120M019

NOTES

MATERIAL

REFER TO ITEMIZED PROTOTYPE
P.C. BOARD VLBA
BOX HAY17515

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL XX ± .01
   DECIMAL XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 ✓
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

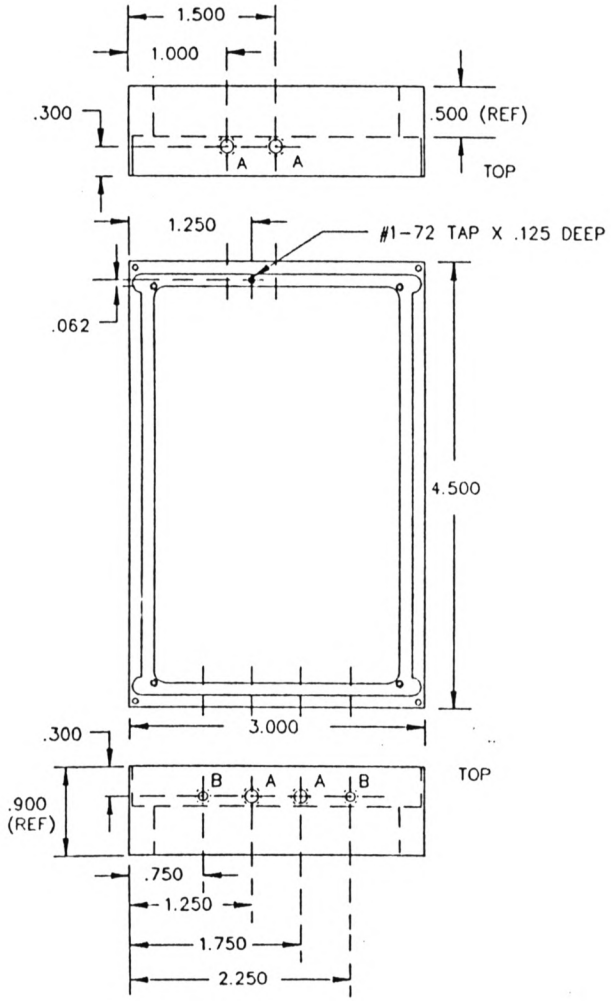
APPROVALS		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
SQUARE LAW DETECTOR

C — 54[redacted]0

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION
A	APH			8/87	#1-72 TAP X .125 DEEP



1 #10-32 TAPPED THRU (4) "A" HOLES.
2. #8-32 TAPPED THRU (2) "B" HOLES.

C-54120M020 A

NOTES

MATERIAL

REFER TO ITEMIZED PROTOTYPE
P.C. BOARD VLBA
BOX HAY45030

FINISH AND/OR HEAT TREATMENT

SHOP NOTES. UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

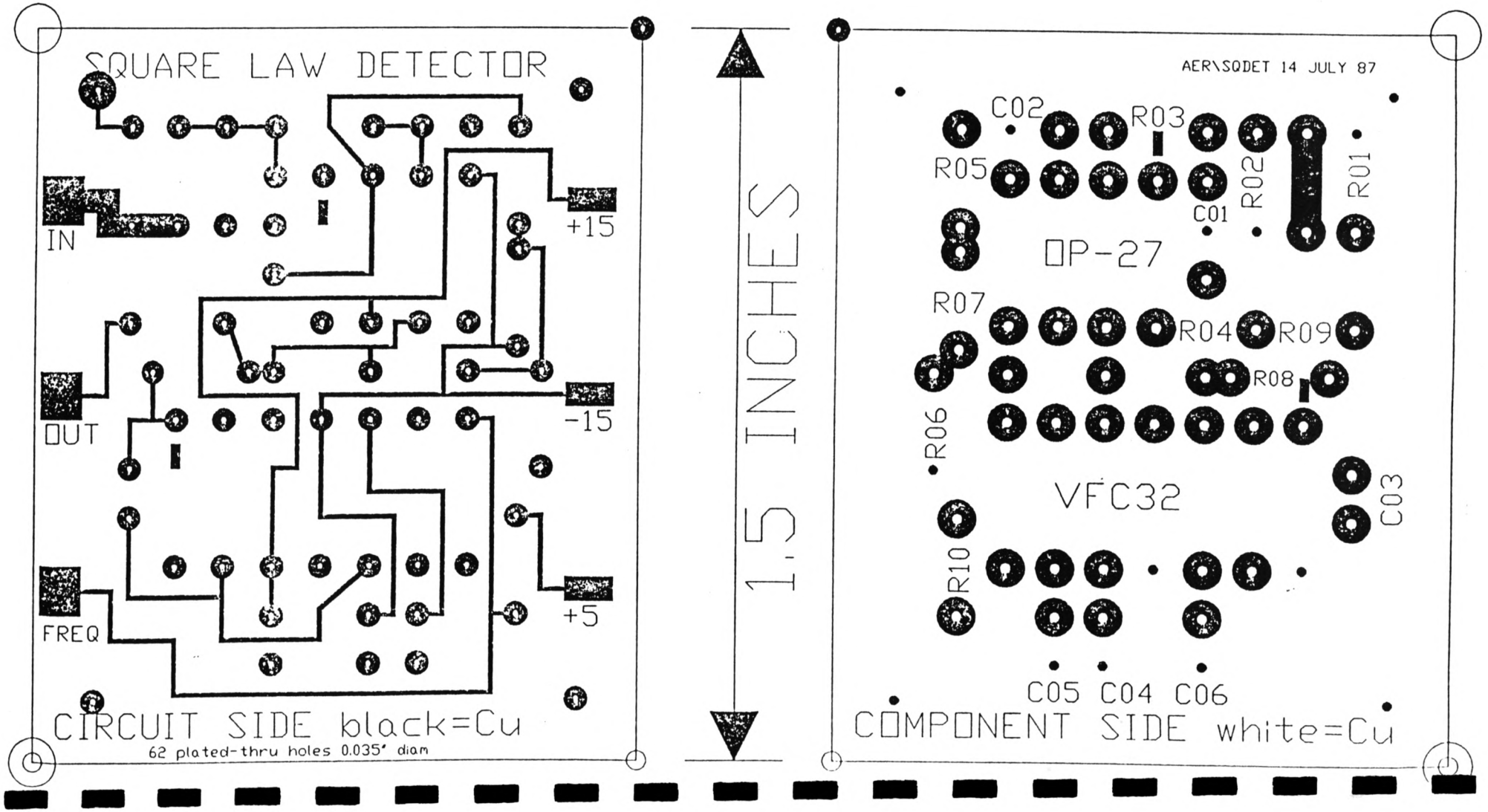
APPROVALS		DRAWN FOR A.E.ROGERS	DATE 7-87
		DRAWN BY A.PHILBROOK	7-87
		CHECKED BY	
	PROJECT		
	ENGINEER		
	MATL. & PROCESS		
	STRUCTURES		
	THERMAL		

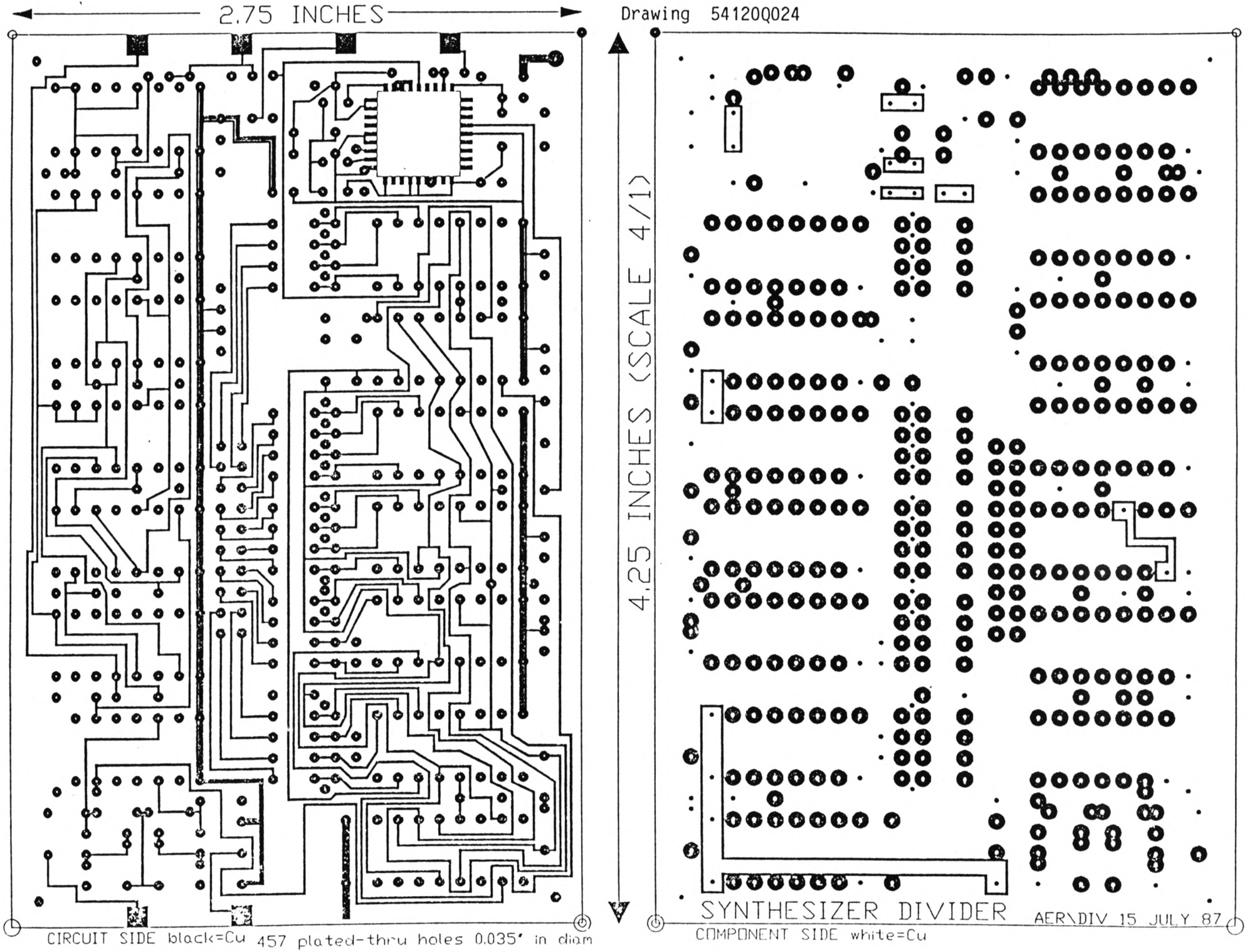
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

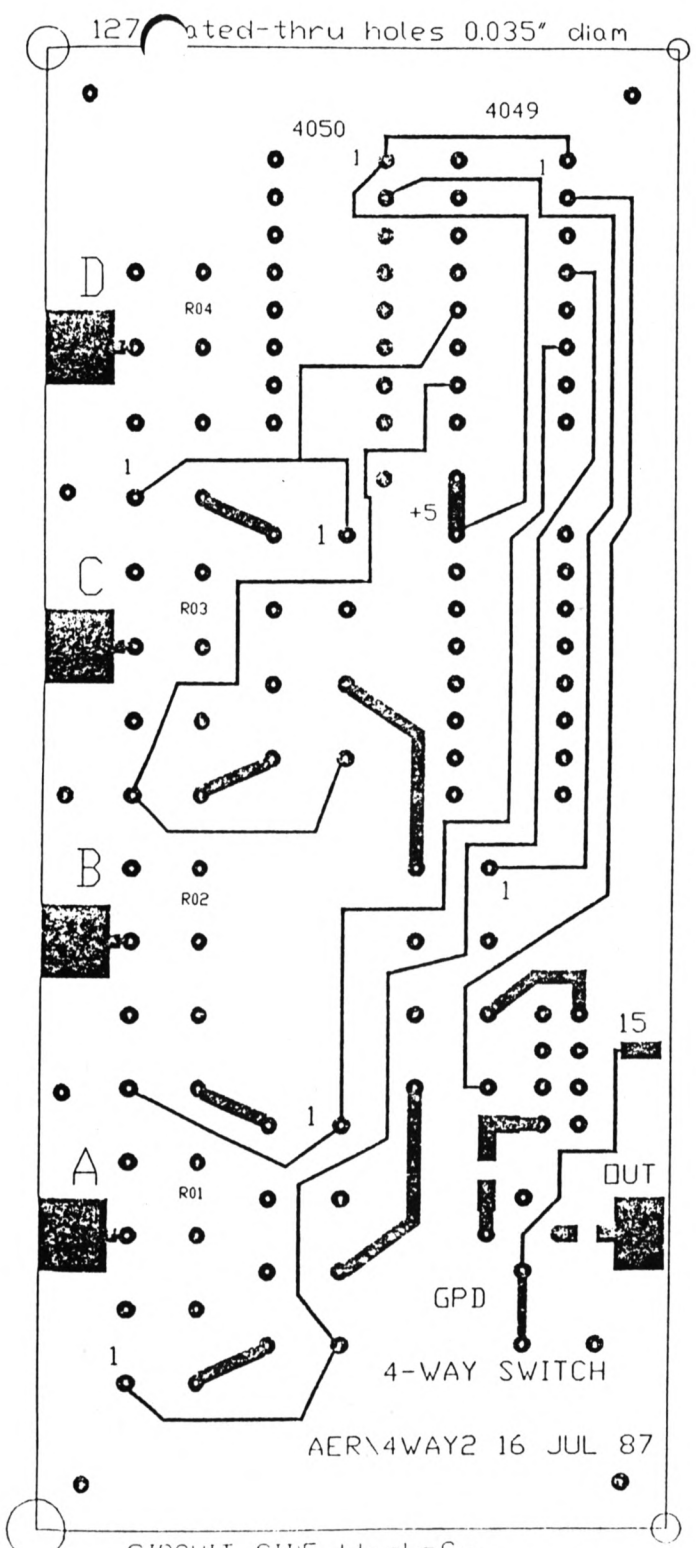
DRILLING PLAN FOR
SSB MIXER

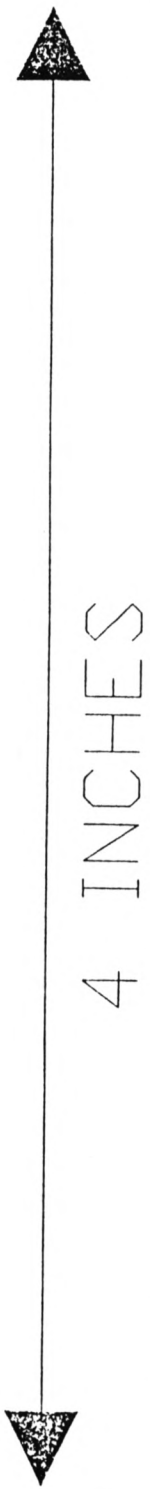
C

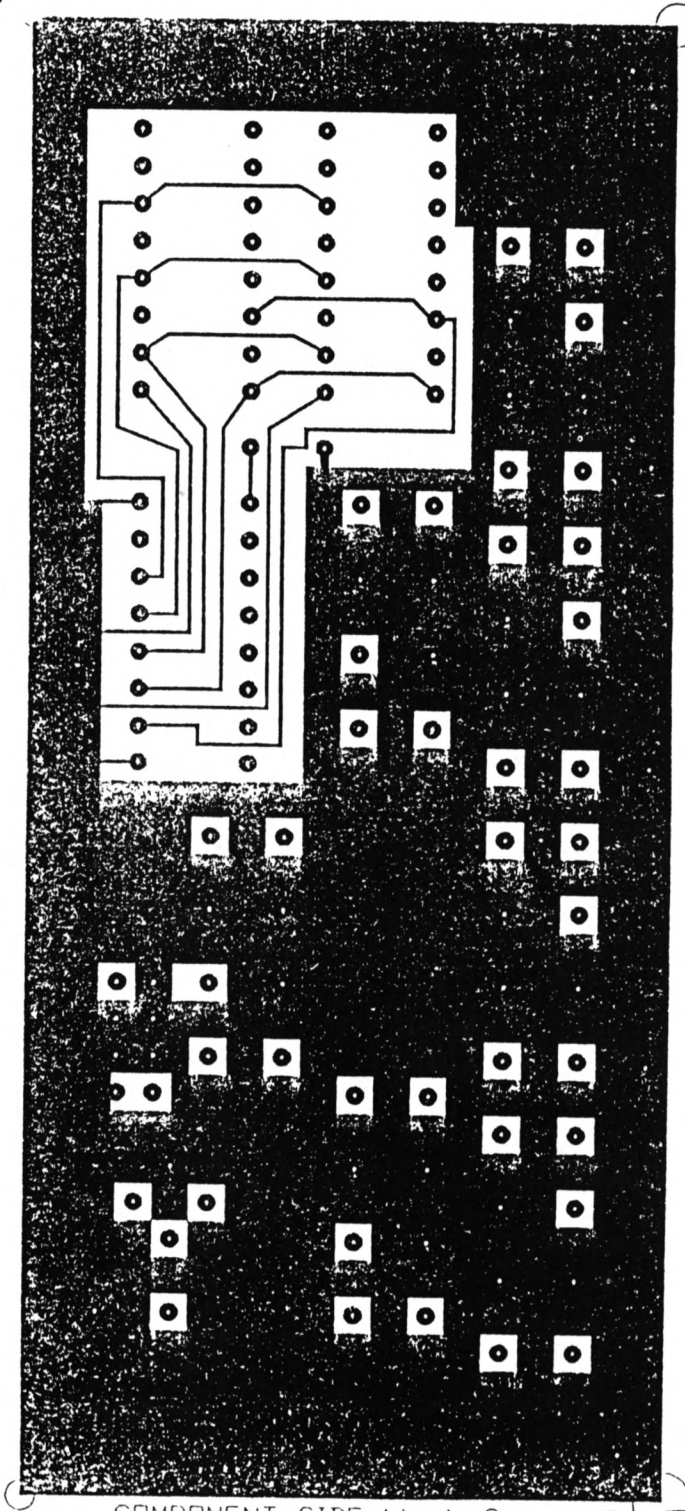
Drawing 541200Q023




2.75 INCHES
Drawing 541200024
4.25 INCHES (SCALE 4/1)
SYNTHESIZER DIVIDER
AER\DIV 15 JULY 87
CIRCUIT SIDE black=Cu 457 plated-thru holes 0.035" in diam
COMPONENT SIDE white=Cu

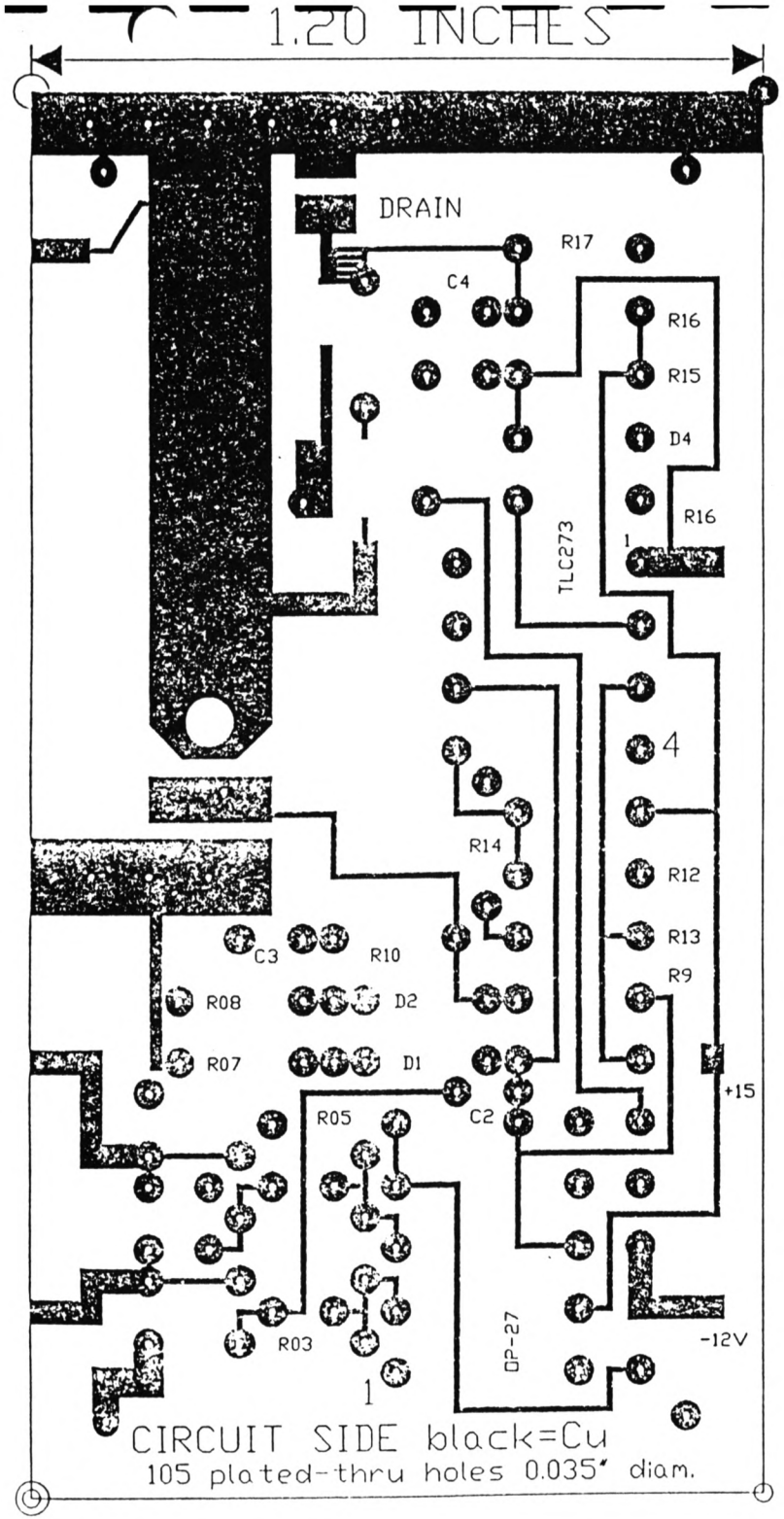


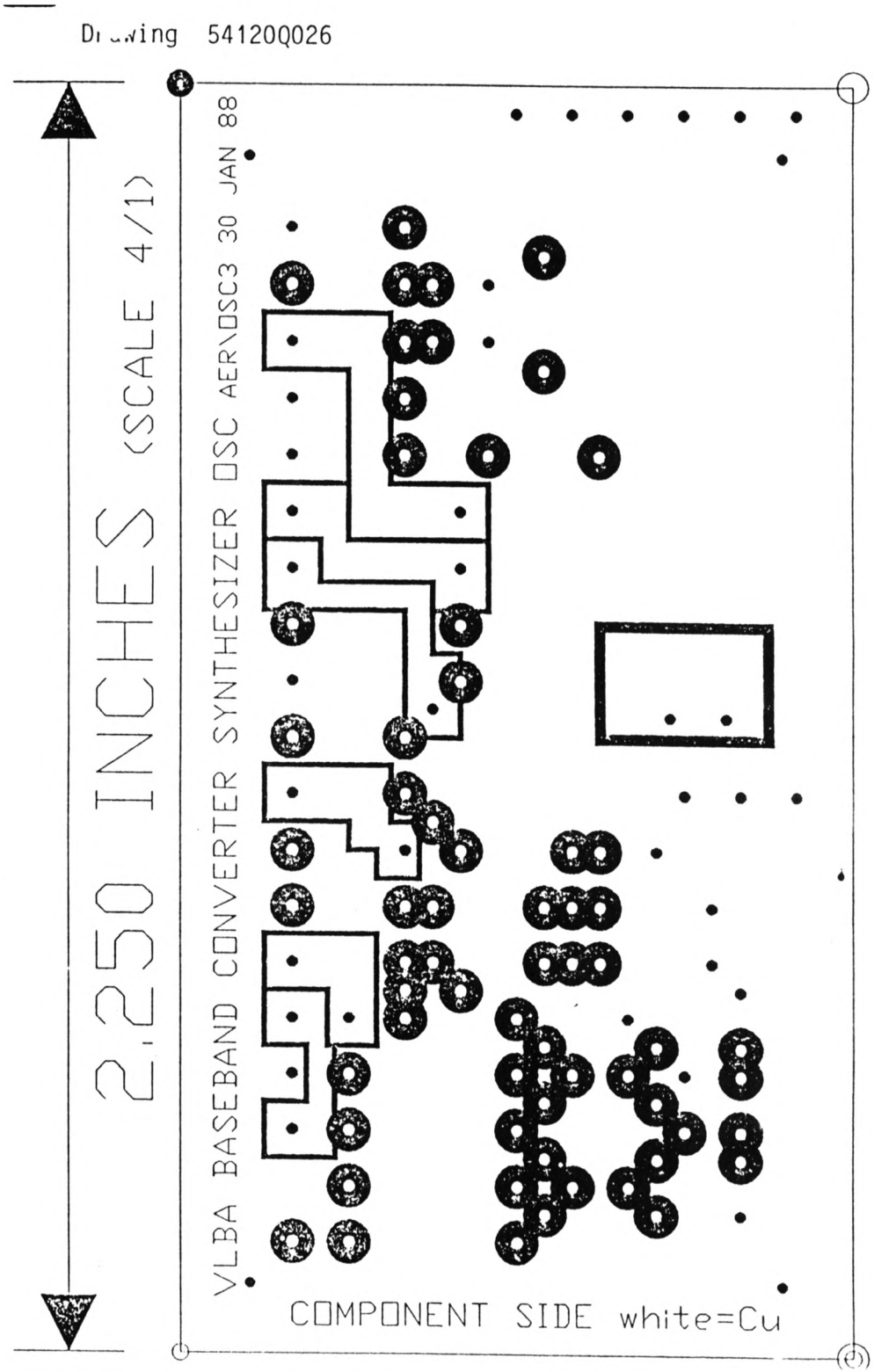


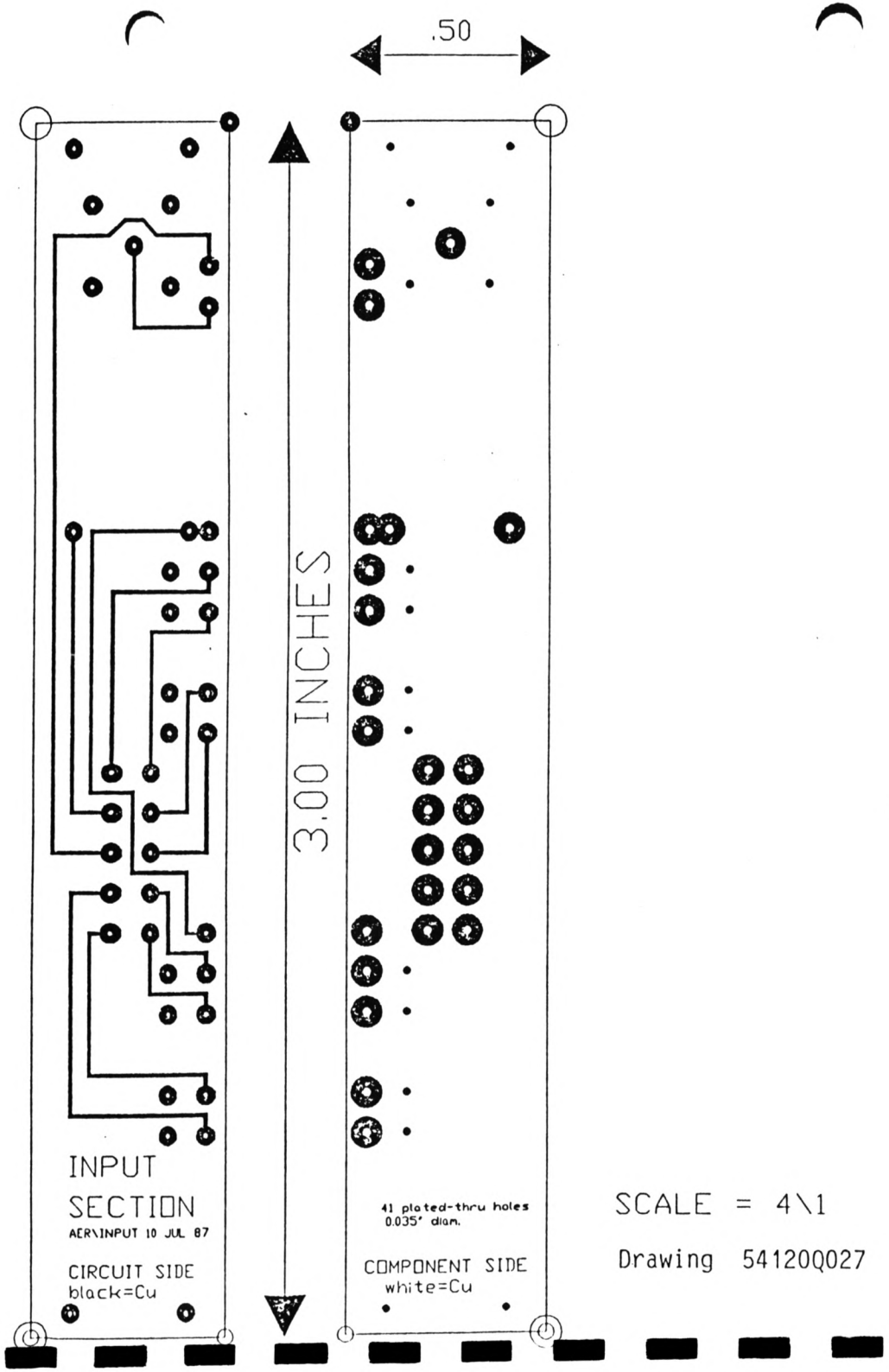


Drawing 54120Q025

Drawing 54120Q026



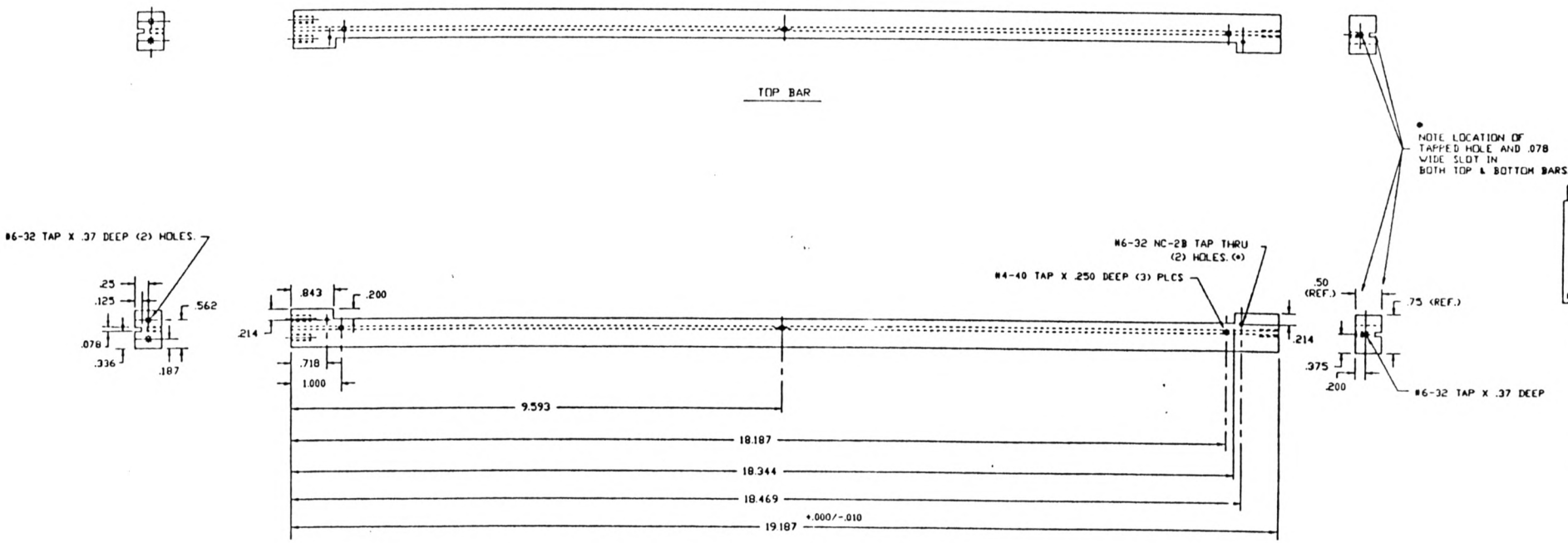




SCALE = 4\1

Drawing 54120Q027

CHANGE LETTER	BY	CHK'D BY	APP'D BY	DATE	DESCRIPTION
A	APH			11-87	CHANGED HOLE SIZE FROM 6-32 TO 4-40



D-54120M028 A

NOTES:

MATERIAL:
.75 X .50 ALUM. 6061-T6 BAR

FINISH AND/OR HEAT TREATMENT:
ALODINE

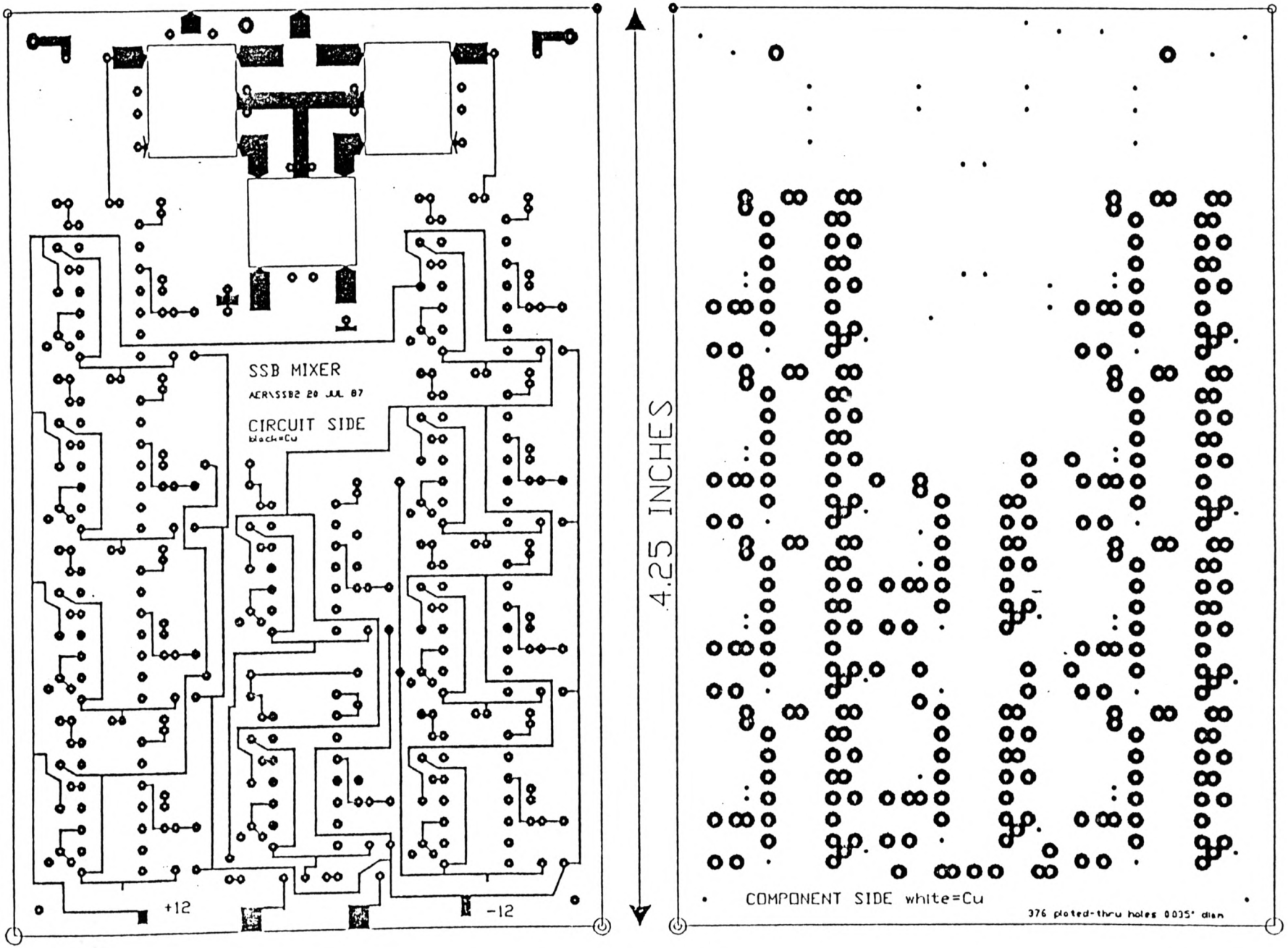
DRAWN BY	A.E.ROGERS	7-87
TRACED BY	A.PHILBRICK	7-87
DESIGNED BY		
PROJECT		
STRESS		
WELDMENTS		
STRUCTURE		
THERMAL		
HEAT TREATMENT	FULL	
QUALIFICATION		

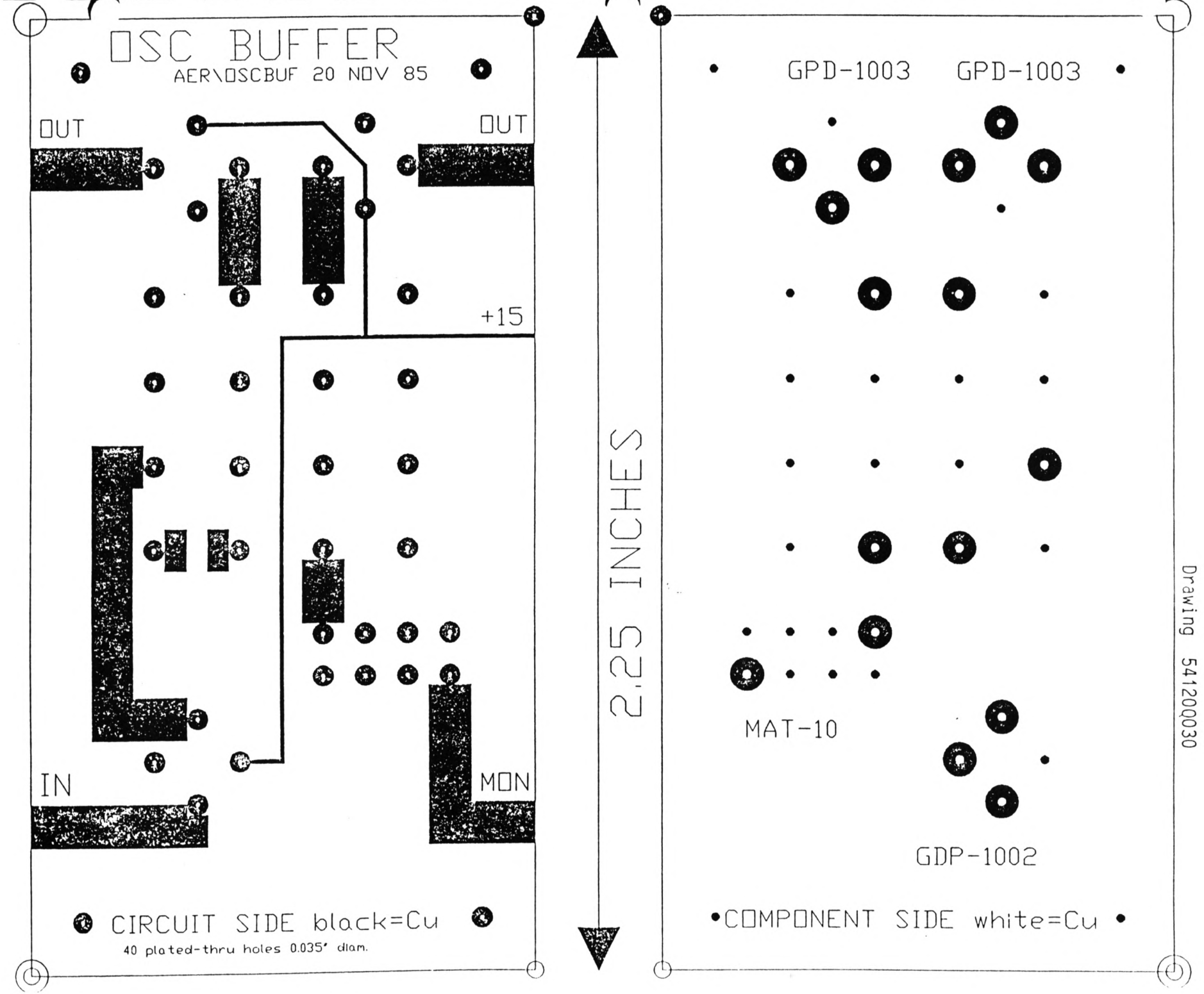
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

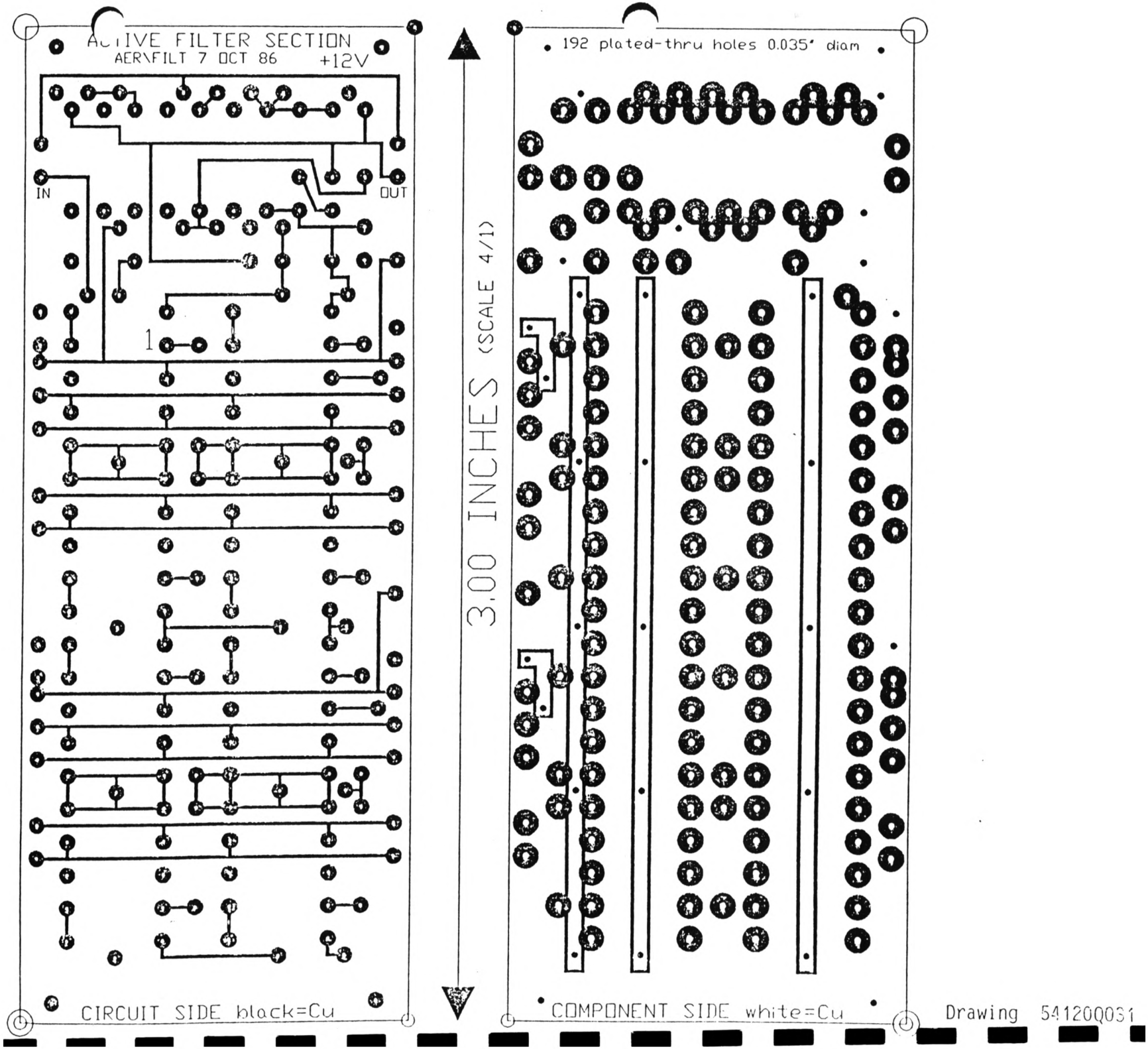
SUPPORT BAR MODIFICATIONS FOR BASEBAND CONVERTER MODULE

AER\SUPBAR	D	54120M028	A

Drawing 54120Q029




OSC BUFFER
AER\OSCBUF 20 NOV 85
OUT
OUT
+15
IN
MON
CIRCUIT SIDE black=Cu
40 plated-thru holes 0.035" diam.
2.25 INCHES
GPD-1003
GPD-1003
MAT-10
GDP-1002
•COMPONENT SIDE white=Cu •
Drawing 541200030


ACTIVE FILTER SECTION
AER\FILT 7 OCT 86 +12V
IN
OUT
1
3.00 INCHES (SCALE 4/1)
192 plated-thru holes 0.035" diam
CIRCUIT SIDE black=Cu
COMPONENT SIDE white=Cu
Drawing 541200031

GAIN CONTROL SECTION AER\AGC 17 JUL 87

IN

CIRCUIT SIDE
black=Cu

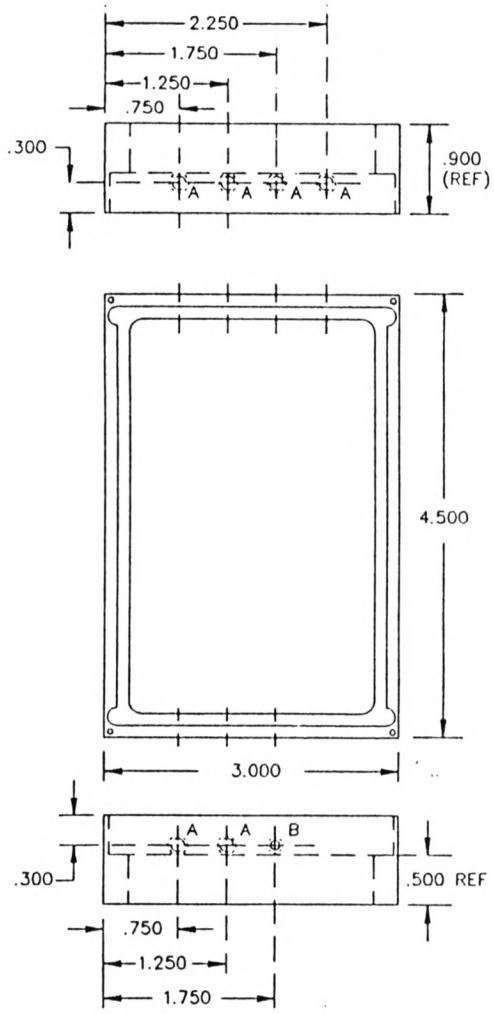
3.00 INCHES (SCALE 4/1)

251 plated-thru holes 0.035" diam.

COMPONENT SIDE white=Cu

Drawing 541200032

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. # 10-32 TAPPED THRU (6) "A" HOLES
2. # 8-32 TAPPED THRU "B" HOLE

C—54120M033

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL XX ± .01
   DECIMAL XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

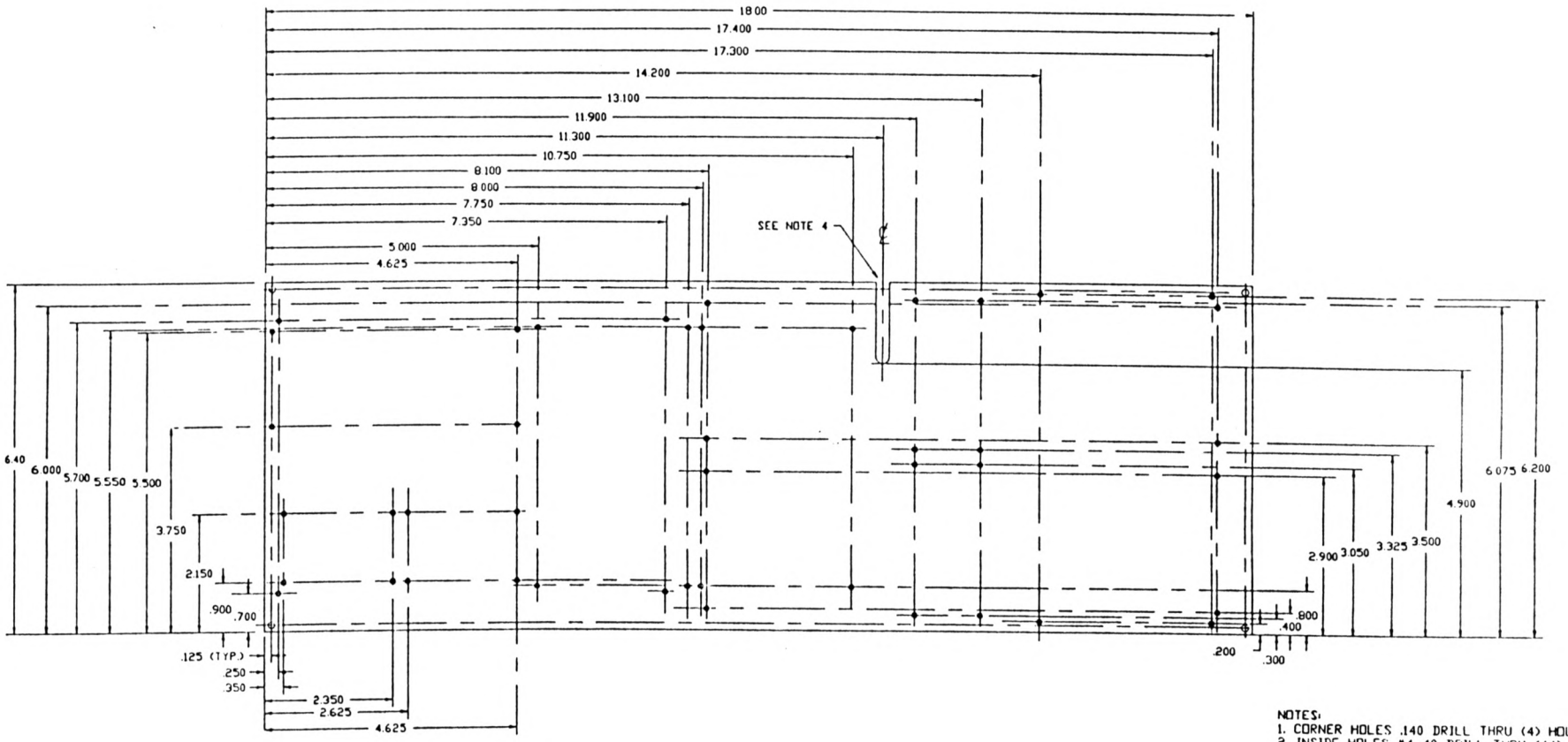
DRAWN FOR	A.E.ROGERS	DATE 12-85
DRAWN BY	A.PHILBROOK	12-85
CHECKED BY		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
SYNTHESIZER DIVIDER

AER\SYNDRILL	C	54120M033
	DWG	

CHANGE LETTER	BY	CHK'D BY	APP'D BY	DATE	DESCRIPTION



NOTES:
1. CORNER HOLES .140 DRILL THRU (4) HOLES.
2. INSIDE HOLES #4-40 DRILL THRU (44) HOLES.
3. MOUNTING SPACER .06 LONG (AT ASS'Y).
4. CUT-OUT SLOT IS .25 DIA.

D- 54120M034

NOTES:

MATERIAL:
.125 ALUM. 6061-T6

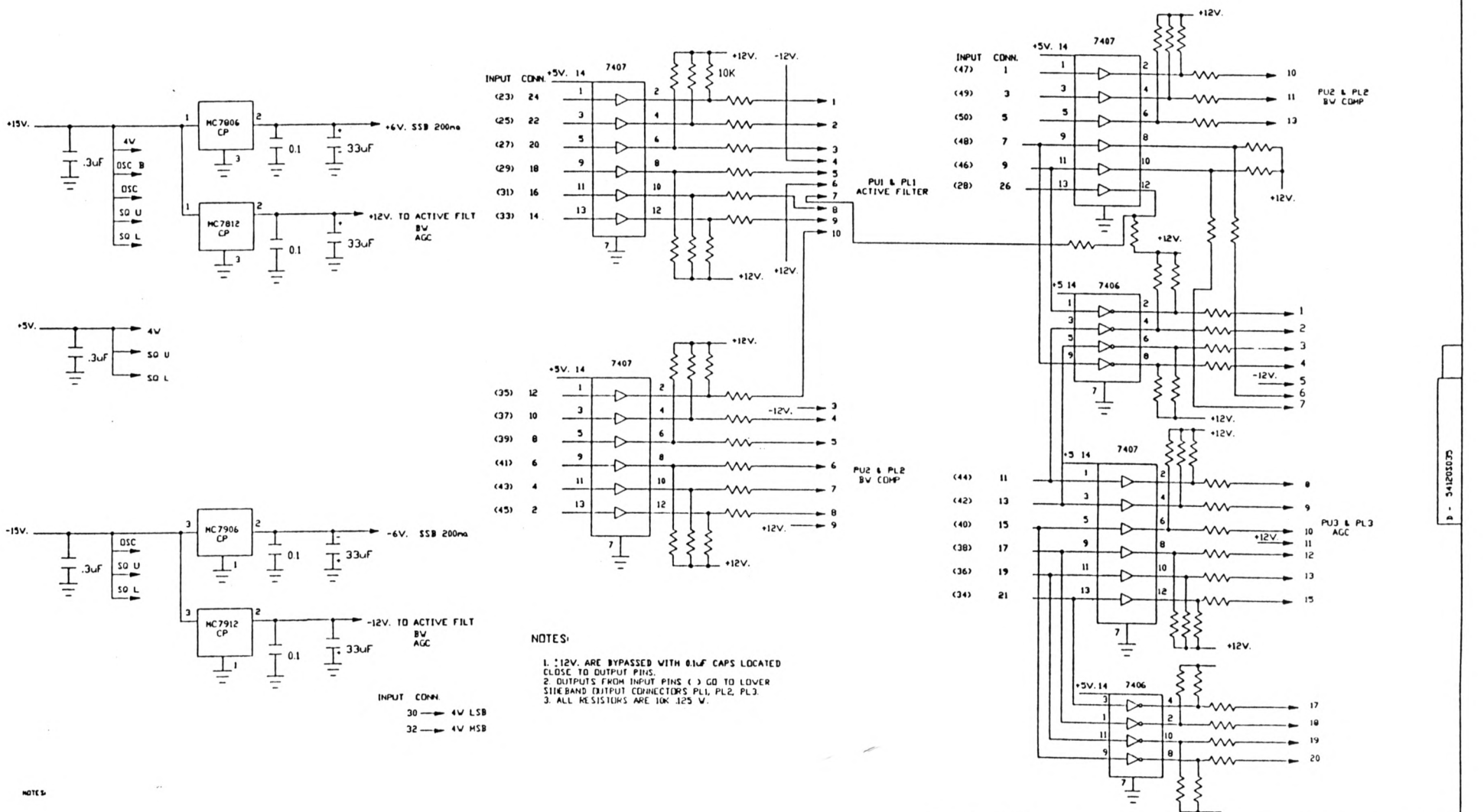
FINISH AND/OR HEAT TREATMENT:
ALODINE

DRAWN	A.E.ROGERS	11/86
CHECKED	A.PHILBROOK	11/86
ENGR APPR.		
MFG APPR.		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

BASEBAND CONVERTER
MOUNTING PLATE

SIZE D | 54120M034

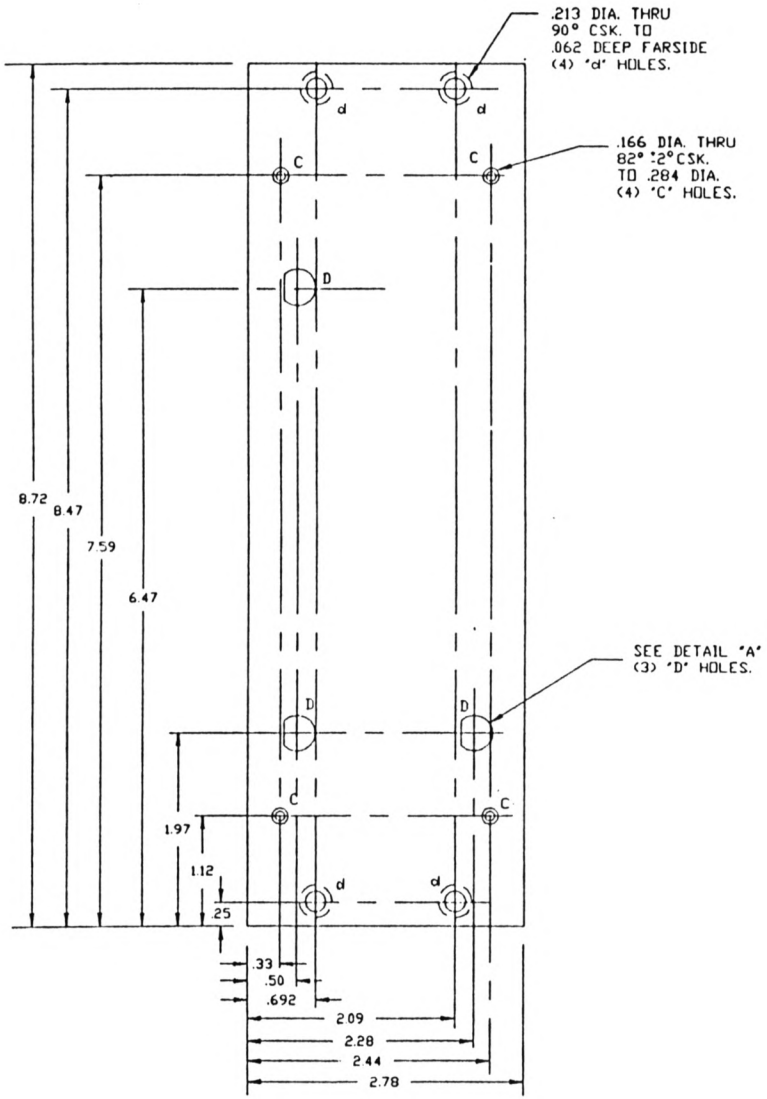


ELECTRONICS NOTES: UNLESS OTHERWISE NOTED RESISTORS: INDUCTORS: CAPACITORS:	USED ON	DRAWN FOR: A.E.ROGERS DRAWN BY: A.PHIL BROOK	DATE: 7-87 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD,MASSACHUSETTS
	SCALE:	APPROVALS: CHECKED BY: ENGINEER: PROJECT:		BASEBAND CONVERTER POWER DISTRIBUTION AND SWITCH DRIVERS
	CLASSIFICATION			ACRSE D 341201035

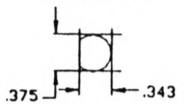
D - 341201035

Drawing 541200036
Drawing 541200037

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	DCN & DESCRIPTION



DETAIL 'A'



CUT-OUT FOR
KINGS-153 BNC
CONNECTOR

C — 54120M038

NOTES

MATERIAL
.125 THICK ALUM. 6061-T6
REMOVE ALL BURRS AND
SHARP EDGES.

FINISH AND/OR HEAT TREATMENT
YELLOW CHROMATE
CONVERSION ALL OVER

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS
   PER MIL-STD-10
4. REMOVE BURRS AND BREAK
   SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY
   BEFORE PLATING OR CON-
   VERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

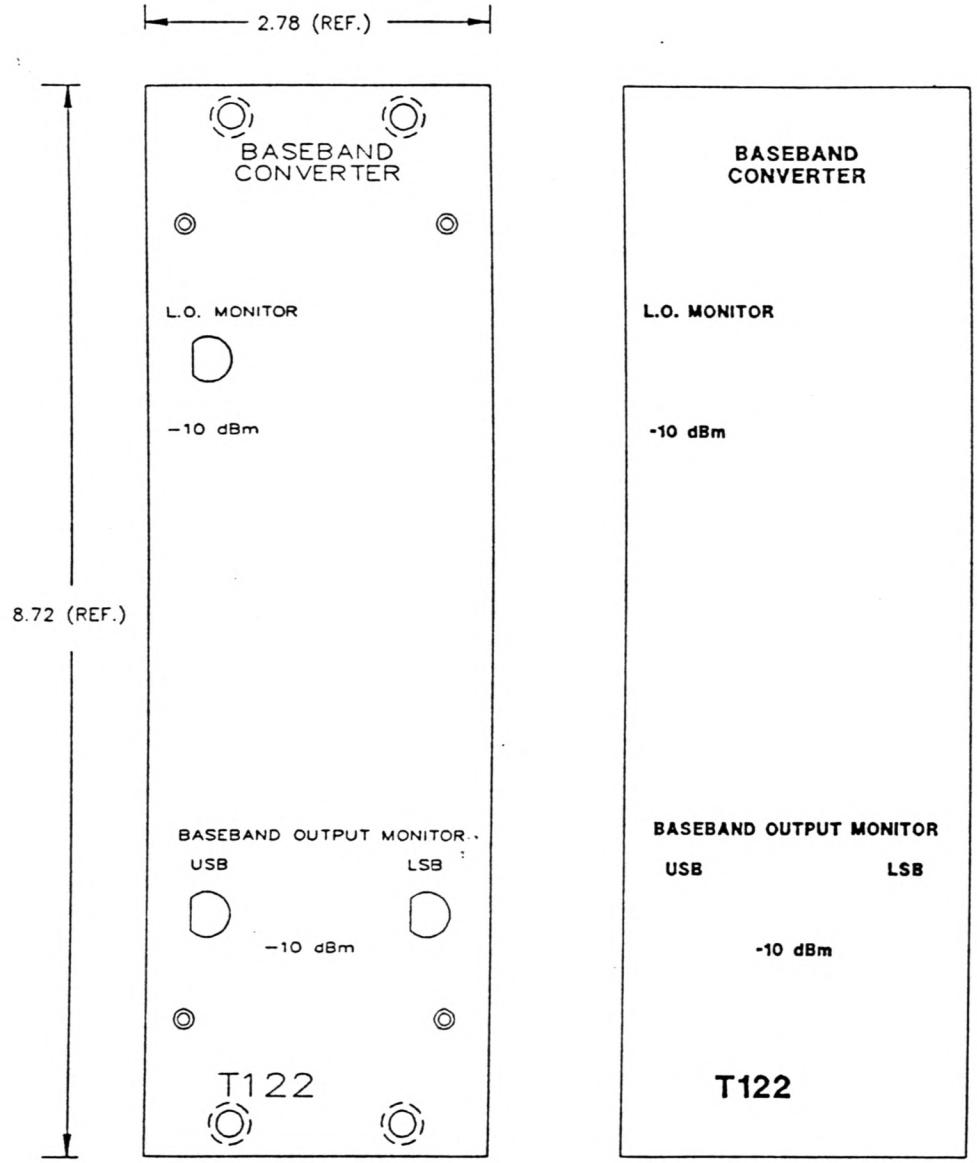
CLASSIFICATION

		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
BASEBAND CONVERTER
FRONT PANEL

		C	54120M038



SILK SCREENED PANEL

ARTWORK

NOTES:
1. SILK SCREEN CHARACTERS AND LINES BLACK.
2. PAINT: HEWLETT PACKARD, MINT GRAY, P/N 6010-0577, FRONT AND EDGES ONLY, PER NRAO SPEC. NO. A13030N1.

D - 541201039

CHANGE LETTER	DWN BY.	CHK'D BY.	APP'D BY.	DATE	DESCRIPTION

ELECTRONICS NOTES: UNLESS OTHERWISE NOTED
RESISTORS:
INDUCTORS:
CAPACITORS:

USED ON

SCALE: 2/1

CLASSIFICATION:

DRAWN FOR: A.E.ROGERS DATE: 7-87
DRAWN BY: A.PHILBROOK 7-87
CHECKED BY:
ENGINEER
PROJECT:

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD,MASSACHUSETTS

SILK SCREENING ARTWORK FOR BASEBAND CONVERTER FRONT PANEL

D 541201039

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

AJ2	1			AJ2	26		
AJ2	2			AJ2	27	GND	
AJ2	3			AJ2	28	ADDR 0	COAXICON
AJ2	4			AJ2	29	ADDR 1	
AJ2	5			AJ2	30	ADDR 2	
AJ2	6			AJ2	31	ADDR 3	COAXICON
AJ2	7			AJ2	32	ADDR 4	
AJ2	8			AJ2	33	ADDR 7	
AJ2	9			AJ2	34		COAXICON
AJ2	10			AJ2	35		
AJ2	11	GND		AJ2	36	GND	
AJ2	12	SYNC	SMC	AJ2	37	STATION SYNC	COAXICON
AJ2	13	GND		AJ2	38	GND	
AJ2	14	GND		AJ2	39	GND	
AJ2	15	5MHz	SMC	AJ2	40	MCB IN	COAXICON
AJ2	16	GND		AJ2	41	GND	
AJ2	17	GND		AJ2	42	GND	
AJ2	18	USB TOTAL POWER FREQ.	SMC	AJ2	43	MCB $\overline{\text{IN}}$	COAXICON
AJ2	19	GND		AJ2	44	GND	
AJ2	20	GND		AJ2	45	GND	
AJ2	21	LSB TOTAL POWER	SMC	AJ2	46	MCB OUT	COAXICON
AJ2	22	GND		AJ2	47	GND	
AJ2	23	LOCK		AJ2	48	GND	
AJ2	24			AJ2	49	MCB $\overline{\text{OUT}}$	COAXICON
AJ2	25			AJ2	50	GND	

AJ1	1	USB GAIN COMPENSATION BIT 3		AJ1	26	USB ACTIVE FILTER 16MHZ	
AJ1	2	USB GAIN COMPENSATION BIT 0		AJ1	27	LSB ACTIVE FILTER 250KHz	
AJ1	3	USB GAIN COMPENSATION BIT 1		AJ1	28	LSB ACTIVE FILTER 16MHZ	
AJ1	4	USB GAIN COMPENSATION BIT 4		AJ1	29	LSB ACTIVE FILTER 500KHz	
AJ1	5	USB GAIN COMPENSATION BIT 2		AJ1	30	IF SELECT LSB	
AJ1	6	USB GAIN COMPENSATION BIT 5		AJ1	31	LSB ACTIVE FILTER 8MHz	
AJ1	7	USB GAIN CONTROL G1		AJ1	32	IF SELECT MSB	
AJ1	8	USB GAIN COMPENSATION BIT 7		AJ1	33	LSB ACTIVE FILTER 2MHz	
AJ1	9	USB GAIN CONTROL G0		AJ1	34	LSB GAIN CONTROL G5	
AJ1	10	USB GAIN COMPENSATION BIT 6		AJ1	35	LSB ACTIVE FILTER 4MHz	
AJ1	11	USB GAIN CONTROL G2		AJ1	36	LSB GAIN CONTROL G6	
AJ1	12	USB ACTIVE FILTER 4MHz		AJ1	37	LSB GAIN COMPENSATION BIT 6	
AJ1	13	USB GAIN CONTROL G3		AJ1	38	LSB GAIN CONTROL G4	
AJ1	14	USB ACTIVE FILTER 2MHz		AJ1	39	LSB GAIN COMPENSATION BIT 7	
AJ1	15	USB GAIN CONTROL G7		AJ1	40	LSB GAIN CONTROL G7	
AJ1	16	USB ACTIVE FILTER 8MHz		AJ1	41	LSB GAIN COMPENSATION BIT 5	
AJ1	17	USB GAIN CONTROL G4		AJ1	42	LSB GAIN CONTROL G3	
AJ1	18	USB ACTIVE FILTER 500KHz		AJ1	43	LSB GAIN COMPENSATION BIT 4	
AJ1	19	USB GAIN CONTROL G6		AJ1	44	LSB GAIN CONTROL G2	
AJ1	20	USB ACTIVE FILTER 250KHz		AJ1	45	LSB GAIN COMPENSATION BIT 0	
AJ1	21	USB GAIN CONTROL G5		AJ1	46	LSB GAIN CONTROL G0	
AJ1	22	USB ACTIVE FILTER 1MHz		AJ1	47	LSB GAIN COMPENSATION BIT 3	
AJ1	23	LSB ACTIVE FILTER 125KHz		AJ1	48	LSB GAIN CONTROL G1	
AJ1	24	USB ACTIVE FILTER 125KHz		AJ1	49	LSB GAIN COMPENSATION BIT 1	
AJ1	25	LSB ACTIVE FILTER 1MHz		AJ1	50	LSB GAIN COMPENSATION BIT 2	

ACTIVE FILTER CONTROL	PU1	1	LEAST MOST SIGNIFICANT SWITCH "A" (125KHz)
	PU1	2	SWITCH "D" (1MHz)
	PU1	3	SWITCH "B" (250KHz)
	PU1	4	-12 VOLTS TO ACTIVE FILTER
	PU1	5	SWITCH "C" (500KHz)
	PU1	6	+12 VOLTS TO ACTIVE FILTER
	PU1	7	ACTIVE FILTER (16MHz) "H"
	PU1	8	ACTIVE FILTER (8MHz) "G"
	PU1	9	SWITCH "E" (2MHz)
	PU1	10	SWITCH "F" (4MHz)

SYNTHESIZER CONTROL	BJ1	1	LSB	F0
	BJ1	2		F2
	BJ1	3		F1
	BJ1	4		F3
	BJ1	5		F6
	BJ1	6		F7
	BJ1	7		F5
	BJ1	8		F4
	BJ1	9		F11
	BJ1	10		F10
	BJ1	11		F9
	BJ1	12		F8
	BJ1	13		F15
	BJ1	14		F14
	BJ1	15		F13
	BJ1	16		F12
	BJ1	17		F18
	BJ1	18		F16
	BJ1	19		F19
	BJ1	20		F17

GAIN CONTROL FOR BANDWIDTH COMPENSATION	PU2	1	
	PU2	2	
	PU2	3	-12V. FOR BW COMPENSATION
	PU2	4	BIT B
	PU2	5	BIT A (LSB)
	PU2	6	BIT C
	PU2	7	BIT D
	PU2	8	GAIN COMPENSATION BIT H (MSB)
	PU2	9	+12V. FOR BW COMPENSATION
	PU2	10	BIT E
	PU2	11	BIT G
	PU2	12	
	PU2	13	BIT F
	PU2	14	
	PU2	15	
	PU2	16	

8-BIT DIGITAL GAIN CONTROL	PU3	1	$\overline{\text{A}}$
	PU3	2	$\overline{\text{C}}$
	PU3	3	$\overline{\text{D}}$
	PU3	4	$\overline{\text{B}}$
	PU3	5	-12V. TO GAIN CONTROL
	PU3	6	BIT B
	PU3	7	LEAST SIGNIFICANT BIT A
	PU3	8	BIT C
	PU3	9	BIT D
	PU3	10	MOST SIGNIFICANT GAIN BIT H
	PU3	11	+12V. TO GAIN CONTROL
	PU3	12	BIT E
	PU3	13	BIT G
	PU3	14	-12V. TO GAIN CONTROL
	PU3	15	BIT F
	PU3	16	
	PU3	17	$\overline{\text{F}}$
	PU3	18	$\overline{\text{E}}$
	PU3	19	$\overline{\text{G}}$
	PU3	20	$\overline{\text{H}}$

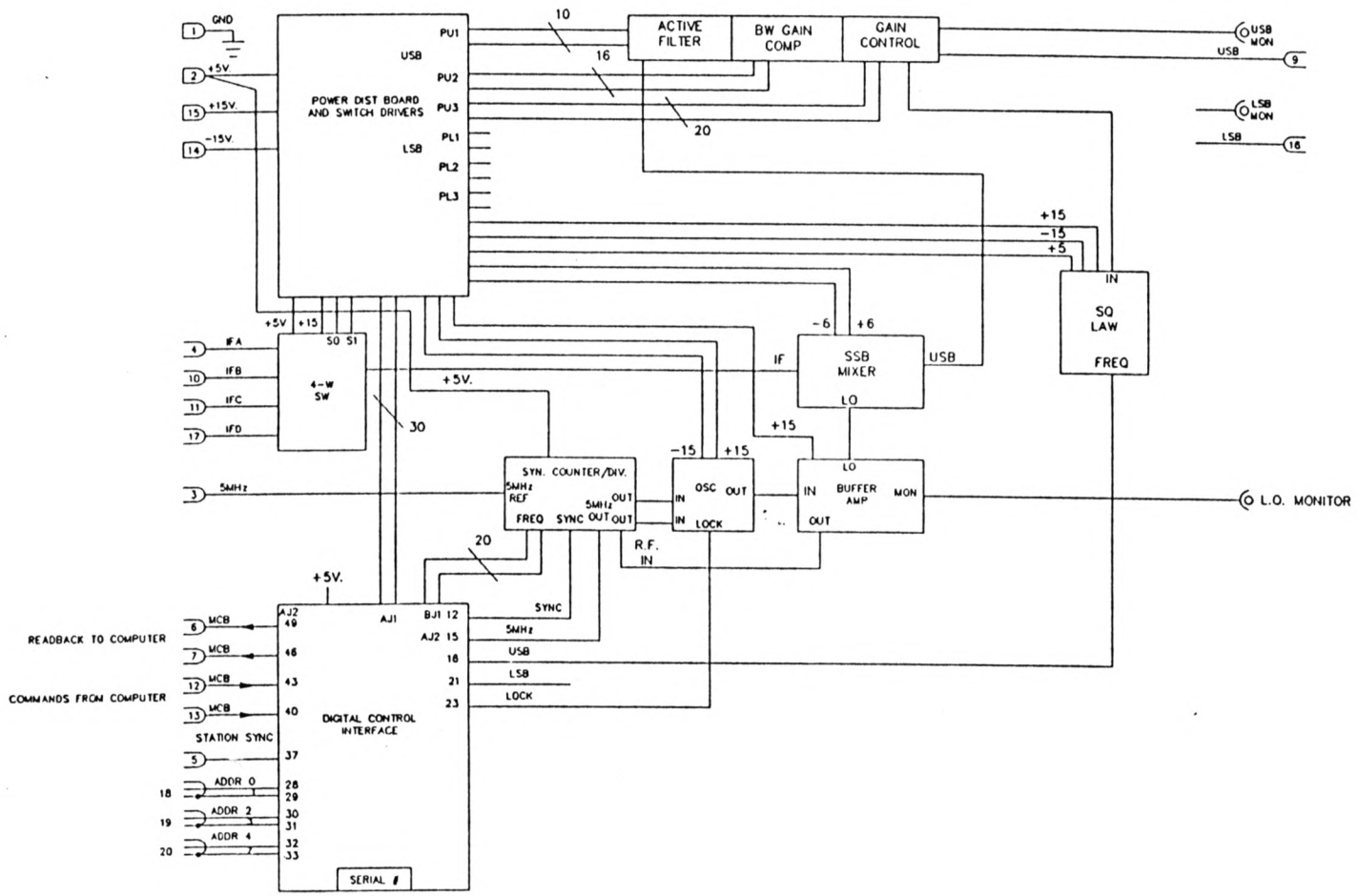
C- 54120D040

NOTES:

1. PL1,PL2,PL3 HAVE SAME ASSIGNMENTS AS PU1,PU2, AND PU3.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 1-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	1-87	VLBA BASEBAND CONVERTER MULITCONDUCTOR CABLE FUNCTIONS
		CHECKED BY:		
	SCALE	APPROVAL PROJECT		AER\CABFUN C 54120D040
	CLASSIFICATION	ENGINEER		

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	DESCRIPTION



NOTES:

1. +5V. WIRE TO POWER DIST. AND SYNC COUNTER/DIV SHOULD BE #22 MIN.
2. SEPARATE CONTROL LINES TO FILTER BOARD FROM OTHER UNSHEILDED LINES (ESPECIALLY 5MHz TO AJ2-15)
3. LINES FROM BUFFER AMP TO SYN. DIVIDER AND SSB MIXER ARE DOUBLE SHIELDED.
4. CABLES GOING TO REAR CONNECTOR HAVE ENOUGH SLACK TO PREVENT "MISALIGNMENT" OF COAXICONS

ELECTRONICS NOTES: UNLESS OTHERWISE NOTED: RESISTORS: INDUCTORS: CAPACITORS:	USED ON: SCALE: CLASSIFICATION:	DRAWN FOR: A.E. ROGERS	DATE: 7-87
		DRAWN BY: A. PHILBROOK	7-87
		CHECKED BY:	
		ENGINEER:	
		PROJECT:	

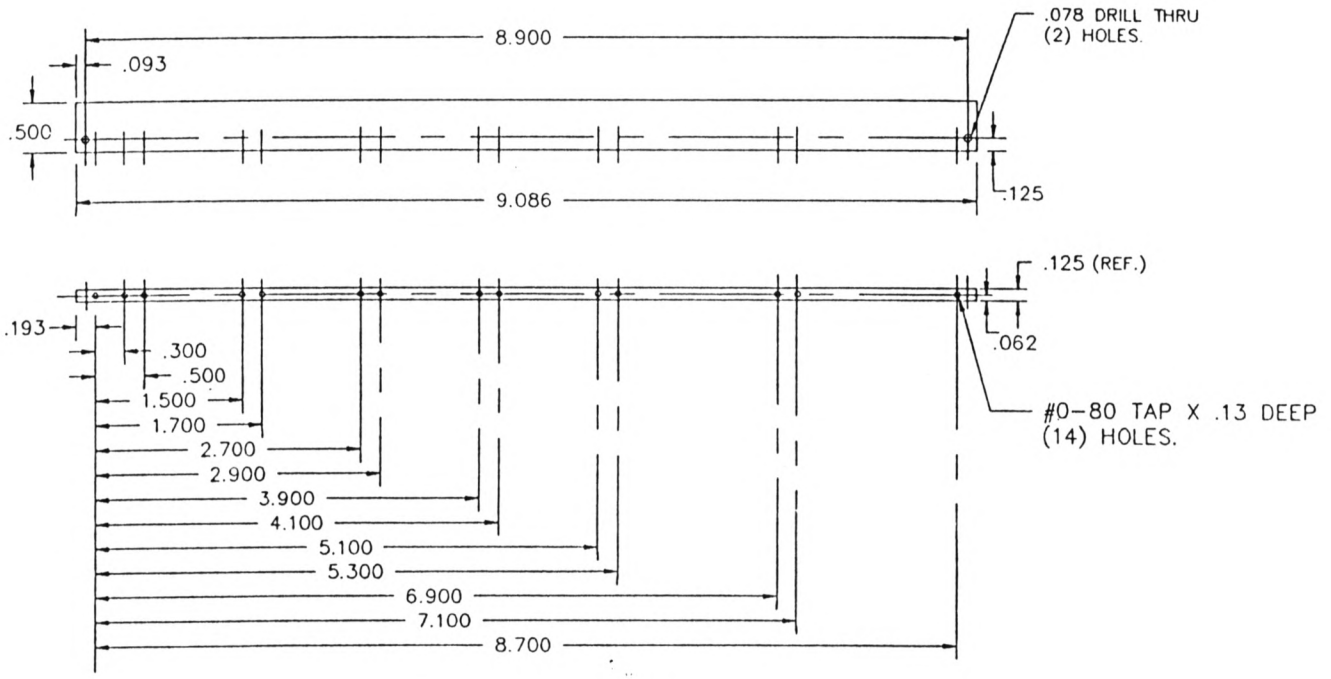
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

VLBA BASEBAND CONVERTER
WIRING DIAGRAM

SIZE	DWG. NO.	REV
D	341205041	

B-341205041

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



C-54120M042

NOTES

MATERIAL
.125 ALUM. 6061-T6

FINISH AND/OR HEAT TREATMENT
CLEAR ALODINE

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0.30'
3. SURFACE ROUGHNESS PER MIL-STD-10 125
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

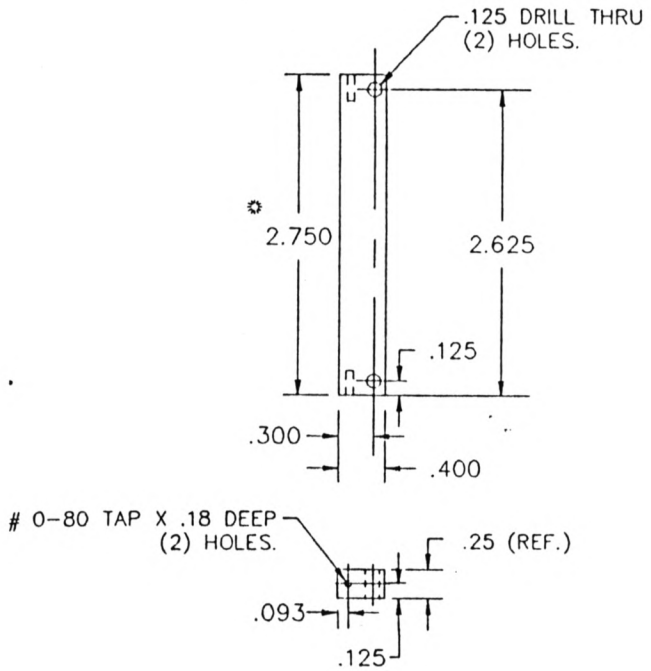
APPROVALS		DATE
DRAWN FOR	A.E ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

LONG BAR
P.C. BOARDS SUPPORT
BASEBAND FILTER AMP

C 54120M042

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



ALL SHORT BARS TO BE SAME LENGTH - MACHINE TOGETHER.

1. MATERIAL: .25 ALUM. 6061-T6
2. FINISH: CLEAR ALODINE

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 125
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

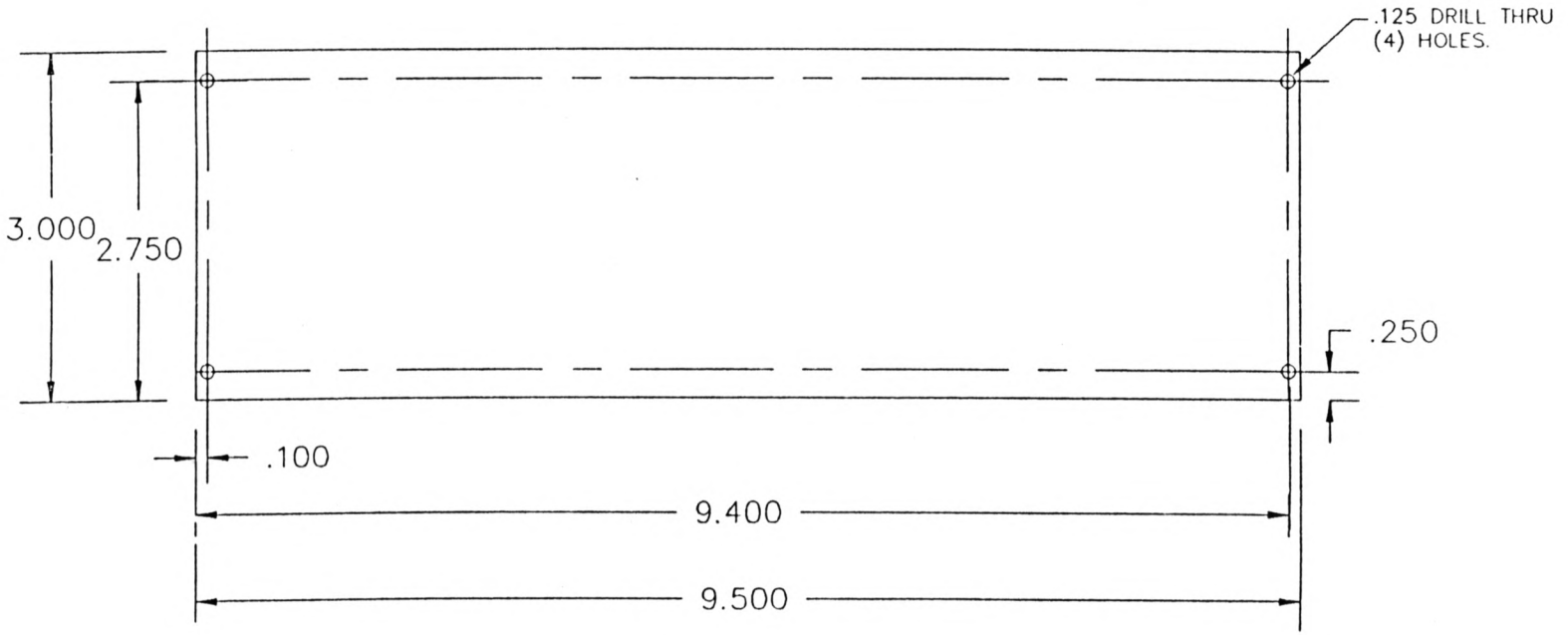
DRAWN FOR	A.E ROGERS	DATE 7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

SHORT BAR
P.C. BOARDS SUPPORT
BASEBAND FILTER AMP

AER\FILTBAR	B	54120M043	
	DWG. SIZE	DWG. NO.	REV.

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. MATERIAL: .062 ALUM. 6061-T6
2. FINISH: CLEAR ALODINE

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 125
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

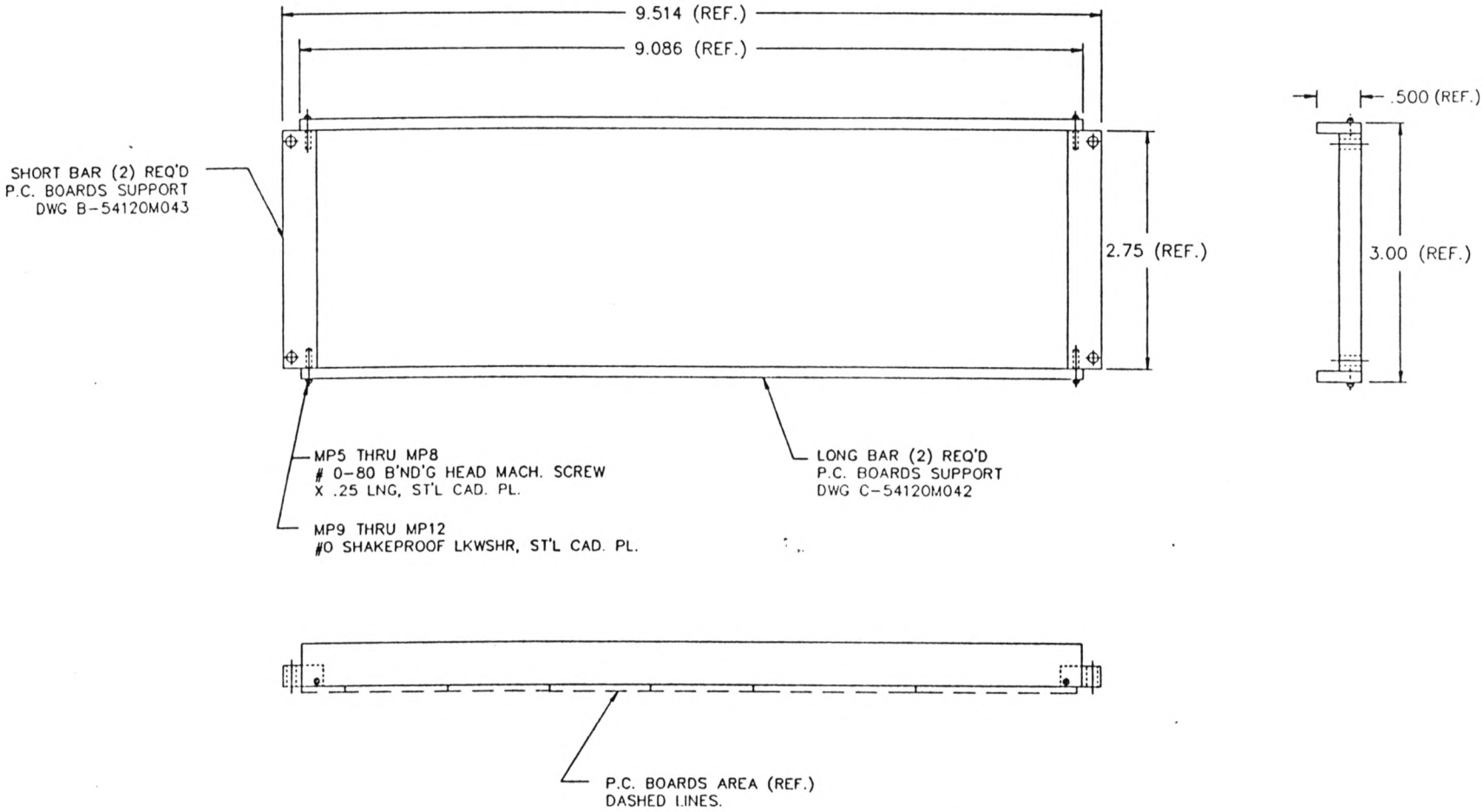
APPROVALS			DATE
	DRAWN FOR	A.E.ROGERS	7-87
	DRAWN BY	A.PHILBROOK	7-87
	CHECKED BY		
	PROJECT		
	ENGINEER		
	MATL. & PROCESS		
	STRUCTURES		
	THERMAL		
	MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

BASEPLATE
BASEBAND FILTER AMP

AER\FILPLATE	B	54120M044	
	DWG. SIZE	DWG. NO.	REV.

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



C-54120M045

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

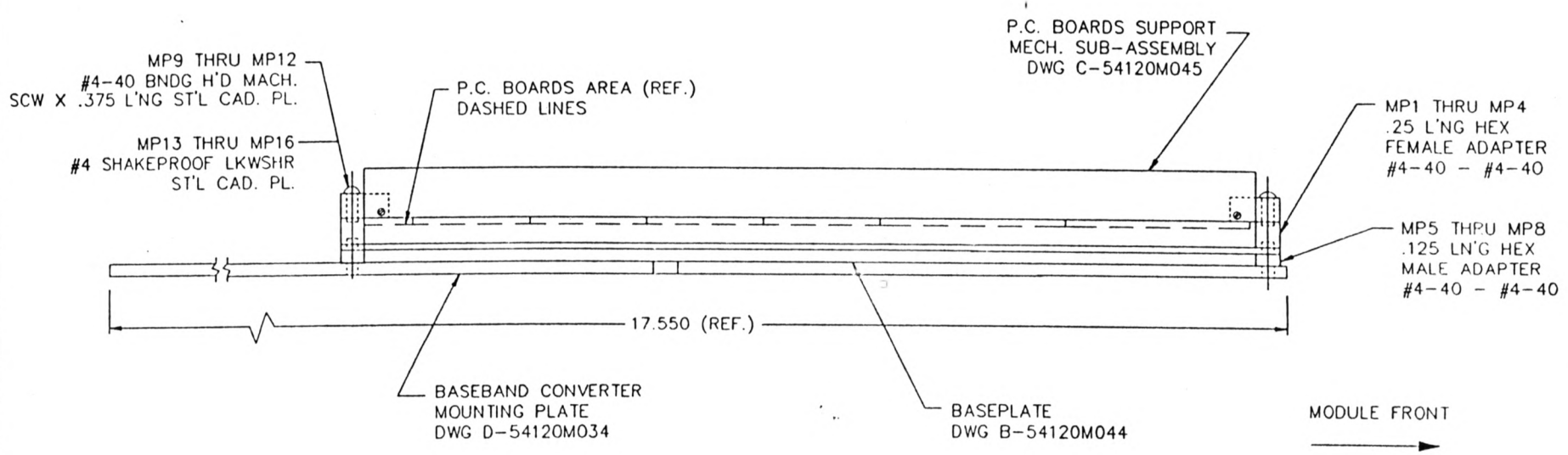
		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

P.C. BOARDS SUPPORT MECH. SUB-ASSEMBLY BASEBAND FILTER AMP

AFR\ASSMPLT	DWG. SIZE	DWG. NO.	REV.
	C	54120M045	

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



TOP VIEW

NOTES:
1) THREADS ON TOP SIDE OF MP5-MP8 NEED TO BE TRIMMED TO BE 0.125 LONG.

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 ✓
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

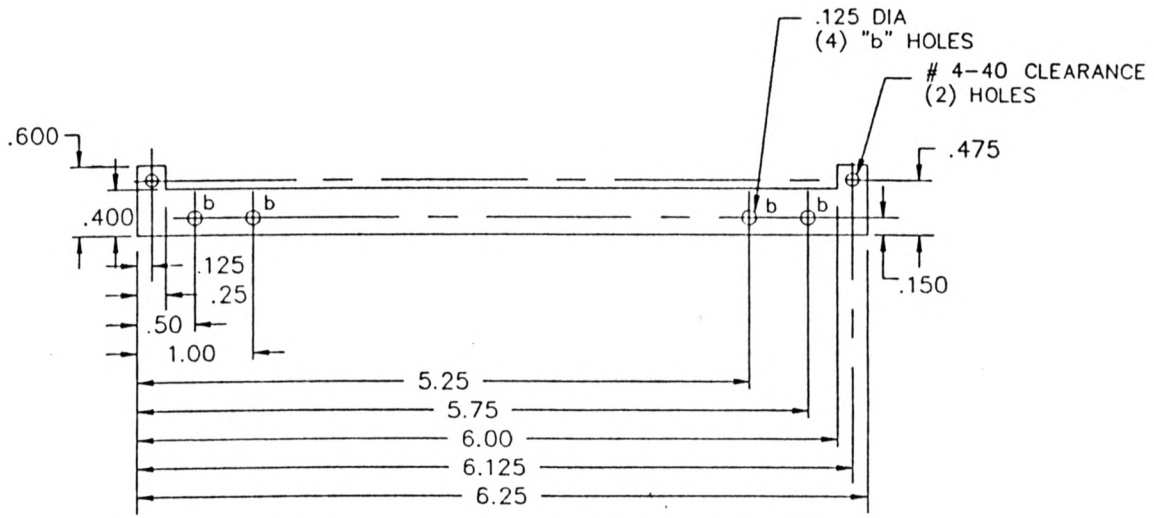
		DATE
DRAWN FOR	A.E ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

FILTER AMP
MECH. ASSEMBLY
BASEBAND FILTER AMP

AER\ASSMBAS	B	54120M046	
	DWG. SIZE	DWG. NO.	REV

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



NOTES:
WHEN MOUNTING TO BASEPLATE
USE #4-40 BRASS SCREWS
FOR GOOD HEAT CONDUCTION.

MATERIAL: ALUM. .125 THICK
FINISH: CLEAR ALODINE

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS 63 PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

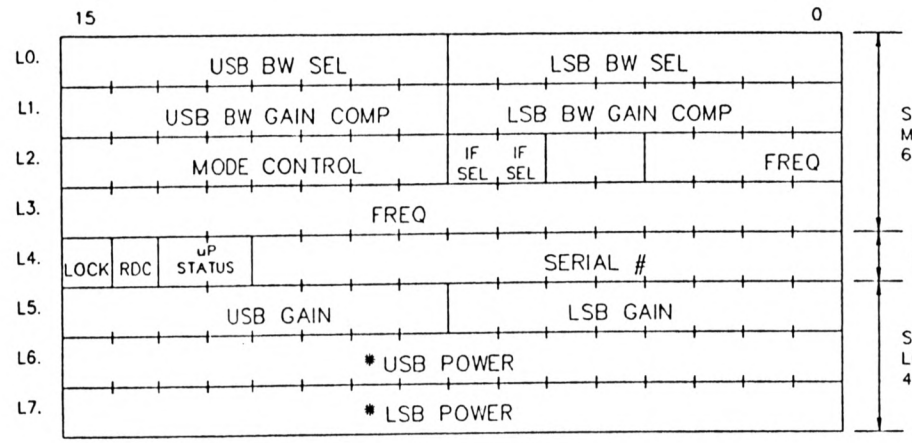
DRAWN FOR	A.E.ROGERS	DATE 7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

BASEBAND CONVERTER HEAT SINK
FOR VOLTAGE REGULATORS

AER\HEATSINK	B	54120M047	
	DWG. SIZE	DWG. NO.	REV.

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	DCN & DESCRIPTION



"LATCHED" MEMORY ALLOCATION

	15															0
L0	AJ1 26	AJ1 16	AJ1 12	AJ1 14	AJ1 22	AJ1 18	AJ1 20	AJ1 24	AJ1 28	AJ1 31	AJ1 35	AJ1 33	AJ1 25	AJ1 29	AJ1 27	AJ1 23
1	AJ1 8	AJ1 10	AJ1 6	AJ1 4	AJ1 1	AJ1 5	AJ1 3	AJ1 2	AJ1 39	AJ1 37	AJ1 41	AJ1 43	AJ1 47	AJ1 50	AJ1 49	AJ1 45
2									AJ1 32	AJ1 30			BJ1 19	BJ1 17	BJ1 20	BJ1 18
3	BJ1 13	BJ1 14	BJ1 15	BJ1 16	BJ1 9	BJ1 10	BJ1 11	BJ1 12	BJ1 6	BJ1 5	BJ1 7	BJ1 8	BJ1 4	BJ1 2	BJ1 3	BJ1 1
4	AJ2 23															
5	AJ1 15	AJ1 19	AJ1 21	AJ1 17	AJ1 13	AJ1 11	AJ1 7	AJ1 9	AJ1 40	AJ1 36	AJ1 34	AJ1 38	AJ1 42	AJ1 44	AJ1 48	AJ1 46

	MSL							LSL
BOARD PIN	7	8	10	9	2	5	3	1
62.5KHz	0	0	0	0	0	0	0	0
125KHz	0	0	0	0	0	0	0	1
250KHz	0	0	0	0	0	0	1	0
500KHz	0	0	0	0	0	1	0	0
1MHz	0	0	0	0	1	0	0	0
2MHz	0	0	0	1	0	0	0	1
4MHz	0	0	1	0	0	1	0	0
8MHz	0	1	1	0	1	1	1	1
16MHz	1	1	1	1	1	1	0	1
DIST. BOARD PIN	26 28	16 31	12 35	14 33	22 25	18 29	20 27	24 23

ACTIVE FILTER
FUNCTION TABLE (8 LINES)

	5	4	6	7	10	13	11	8	
	0	0	1	0	1	0	1	1	
	0	0	1	0	1	0	0	1	
	0	0	0	0	0	0	0	1	
	0	0	0	0	0	0	1	0	
	0	0	0	0	0	1	0	0	
	0	0	0	0	1	0	0	0	
	0	0	0	1	0	0	0	0	
	0	0	1	0	0	0	0	0	
	0	1	0	0	0	0	0	0	
	8 39	10 37	6 41	4 43	1 47	5 50	3 49	2 45	USB LSB

GAIN COMP
FOR BW (8 LINES)

GAIN FOR AGC IS 8-BIT: ALL ZEROS = $-\infty$ dB
ALL ONES = +12dB
011111111 = +6dB

	MSB							LSB	
P.C. BOARD PINS	10 20	13 19	15 17	12 18	9 3	8 2	6 4	7 1	USB LSB
AJ1	15 40	19 36	21 34	17 38	13 42	11 44	7 48	9 46	USB LSB

C – 541200048

NOTES

1.* SWITCHED POWER AT LE. AND LF.

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 ✓
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE NONE

CLASSIFICATION

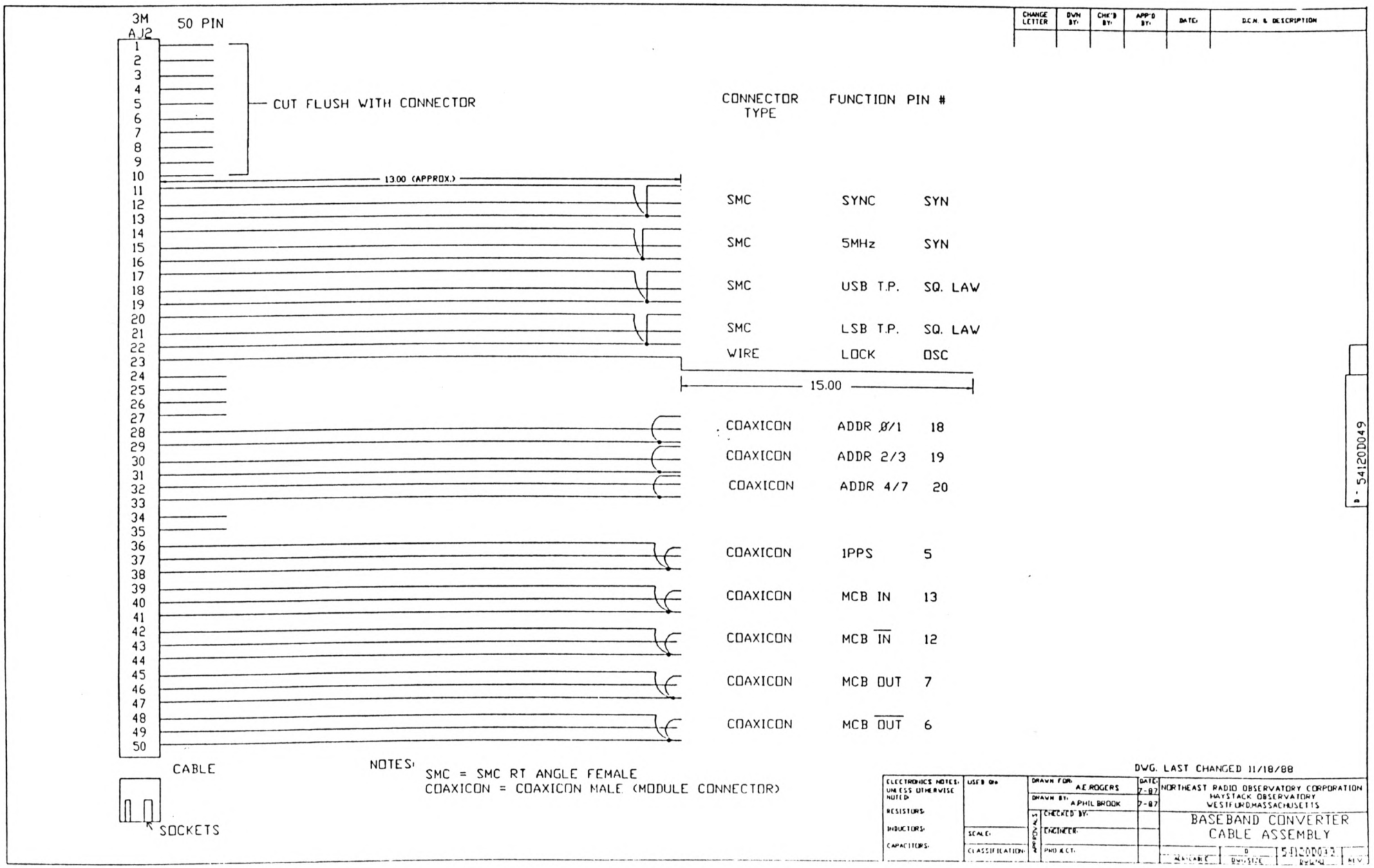
APPROVALS		
DRAWN FOR	A.E ROGERS	3/87
DRAWN BY	A. PHILBROOK	3/87
CHECKED BY		
PROJECT		
ENGINEER		
MATL & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

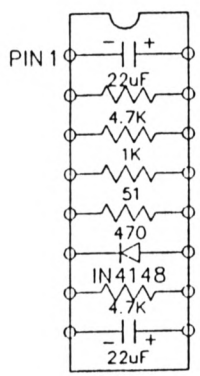
BASEBAND CONVERTER
"LATCHED" MEMORY

C 541200048

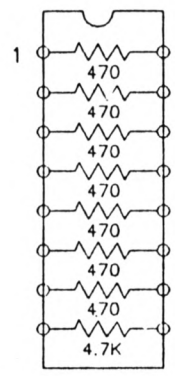
DWG SIZE


3M
AJ2
50 PIN
CUT FLUSH WITH CONNECTOR
13.00 (APPROX.)
15.00
CONNECTOR TYPE
FUNCTION
PIN #
SMC SYNC SYN
SMC 5MHz SYN
SMC USB T.P. SQ. LAW
SMC LSB T.P. SQ. LAW
WIRE LOCK OSC
COAXICON ADDR Ø/1 18
COAXICON ADDR 2/3 19
COAXICON ADDR 4/7 20
COAXICON 1PPS 5
COAXICON MCB IN 13
COAXICON MCB $\overline{\text{IN}}$ 12
COAXICON MCB OUT 7
COAXICON MCB $\overline{\text{OUT}}$ 6
CABLE
SOCKETS
NOTES:
SMC = SMC RT ANGLE FEMALE
COAXICON = COAXICON MALE (MODULE CONNECTOR)
CHANGE LETTER
DWN BY:
CHK'D BY:
APP'D BY:
DATE:
D.C.N. & DESCRIPTION
D-541200049
DWG. LAST CHANGED 11/18/88
ELECTRONICS NOTES: UNLESS OTHERWISE NOTED:
RESISTORS:
INDUCTORS:
CAPACITORS:
USED ON
SCALE:
CLASSIFICATION:
DRAWN FOR: A.E.ROGERS
DATE: 7-87
DRAWN BY: A.PHIL BROOK
DATE: 7-87
APPROVALS
CHECKED BY:
ENGINEER:
PROJECT:
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD,MASSACHUSETTS
BASEBAND CONVERTER
CABLE ASSEMBLY
SIZE
D
DWG.NO.
541200032
REV

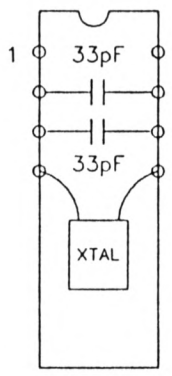
CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



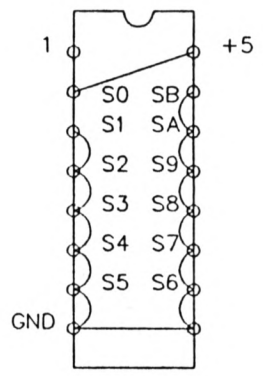
B11



B21



A41 AND B31

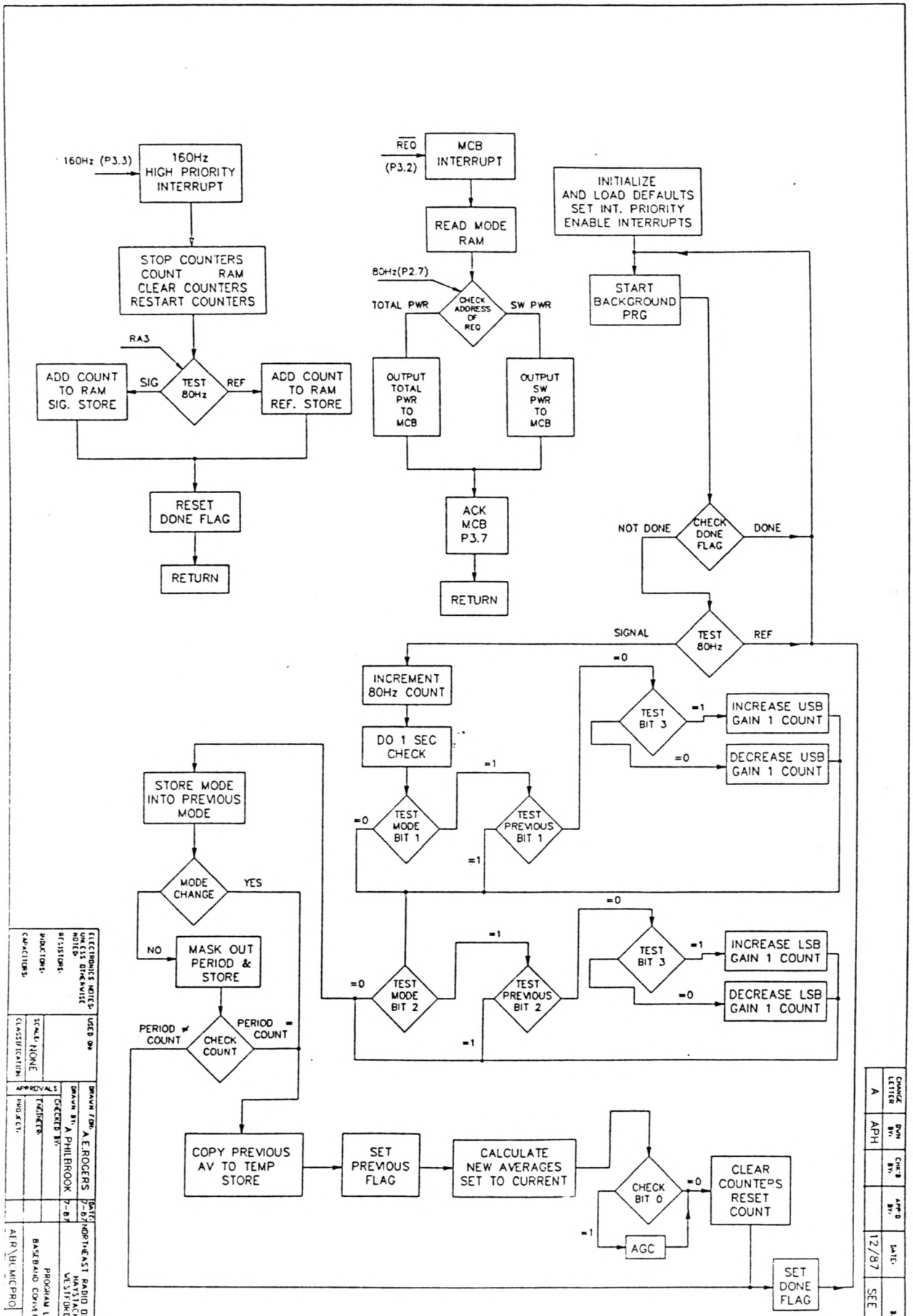


A21
(SHOWN FOR SERIAL # 1)

C - 54120S050

NOTES:
1. CUT POWER (PIN 20) ON A61,A63,A65,B64.
2. CUT GND (PIN 10) ON A52,A54,A56,B55.
3. SOLDER ON LUG TO GROUND PLANE UNDERSIDE TO ENSURE GROUND CONTACT IS MADE WHEN BOARD IS MOUNTED.
4. 1uF DIRECTLY BETWEEN B47-1 AND B36-10.
5. ADD SHORT GROUND WIRE B11-8 TO B11-10 AND A31-7 TO A31-10.
6. 0.1uF ACROSS +5V TO GND AT 5V. INPUT.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	7-87	DISCRETE COMPONENT HEADERS FOR BASEBAND CONVERTER DIGITAL INTERFACE BOARD
		CHECKED BY:		
	SCALE 4=1	APPROVAL PROJECT		AER\INTER C 54120S050
	CLASSIFICATION	ENGINEER:		



ELECTRONICS NOTES:
UNLESS OTHERWISE NOTED
RESISTORS:
INDUCTORS:
CAPACITORS:

USED ON

SCALE: NONE
CLASSIFICATION:

APPROVALS:
PROJECT ENGINEER:

DRAWN BY: A.E.ROGERS 7-87
CHECKED BY: A.PHILBROOK 7-87

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD MASSACHUSETTS

PROGRAM LOGIC FLOW FOR VLBA
BASEBAND CONVERTER 8751 MICROPROCESSOR

AERY\BLMICPRO | D | 54120L051 | A

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	DCN & DESCRIPTION
A	APH			12/87	SEE ARCHIVED DISKS

D - 54120L051 | A

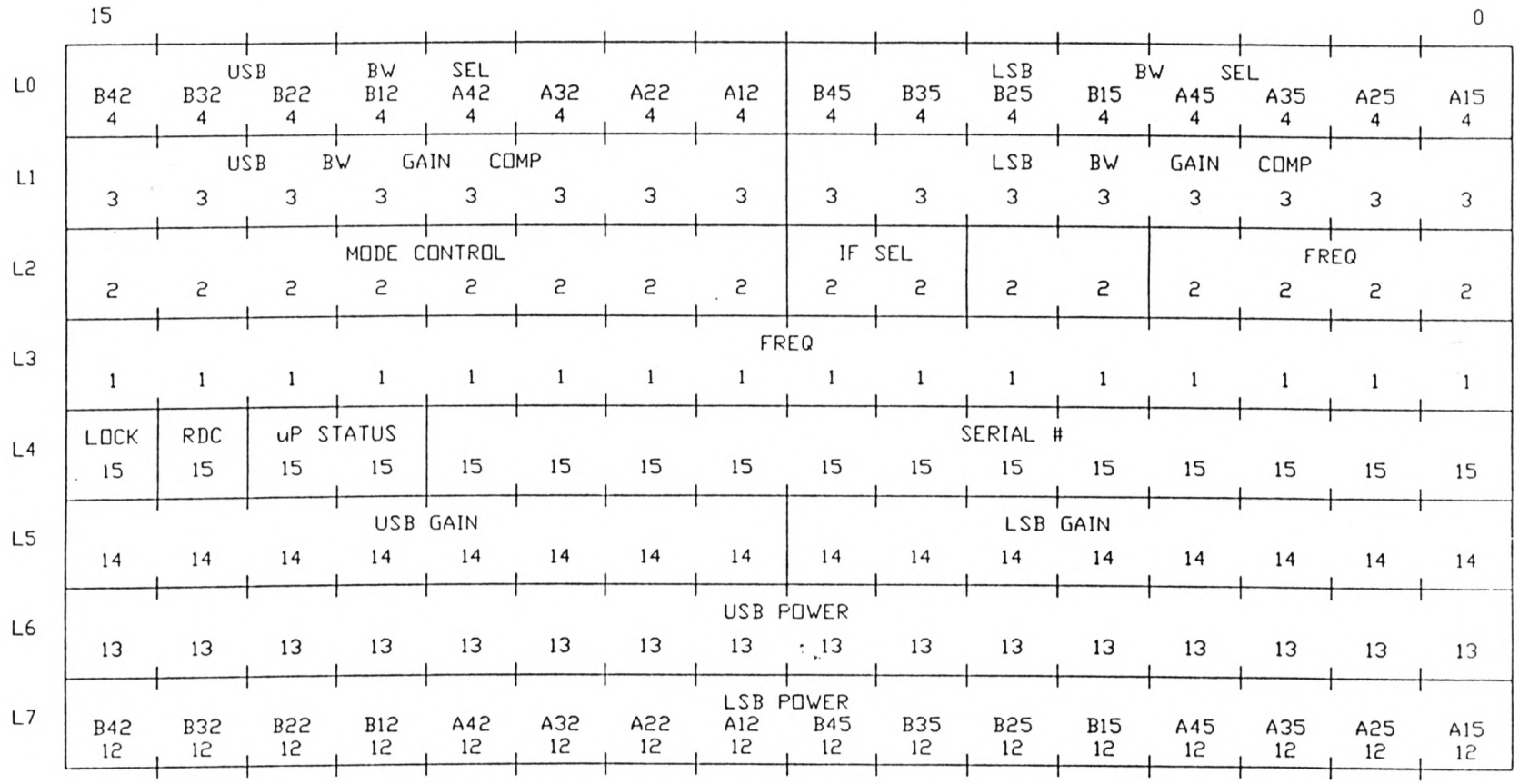
CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

30H-31H	USB POWER - TEMP STORE	312.5	
32H-33H	LSB POWER - TEMP STORE	312.5	
34H-37H	USB SIGNAL TOTAL (32 BITS)	20*10**6 (24 BITS FOR 819 SEC.)	
38H-3BH	LSB SIGNAL TOAL (32 BITS)	20*10**6 (24 BITS FOR 819 SEC.)	
3CH-3FH	USB REF TOTAL (32 BITS)	20*10**6 (24 BITS FOR 819 SEC.)	
40H-43H	LSB REF TOTAL (32 BITS)	20*10**6 (24 BITS FOR 819 SEC.)	
44H	USB REF. GAIN (8 BITS)	128 (6dB FROM MAX.)	
45H	LSB REF. GAIN (8 BITS)	128 (6dB FROM MAX.)	
46H-47H	USB TOTAL POWER REF.	4000 H (16384)	FOR AUTOLEVEL
48H-49H	LSB TOTAL POWER REF.	4000 H (16384)	FOR AUTOLEVEL
4AH-4DH	MULTI FACTOR TEMP STORE	26*2**24/k	
50H-53H	"A" REGISTER 32-BIT		FOR ARITH. SUBROUTINES
54H-57H	"B" REGISTER 32-BIT		FOR ARITH SUBROUTINES
58H-5FH	"C" REGISTER 64-BIT		FOR ARITH SUBROUTINES
60H-67H	PREVIOUS STORE		
70H-71H	USB SIG + REF		NORMALIZED
72H-73H	LSB SIG + REF		NORMALIZED
74H-75H	USB SIG - REF		NORMALIZED
76H-77H	LSB SIG - REF		NORMALIZED
20H BITS 0-7	MODE TEMP STORE		
20H BIT 8	DONE FLAG		
20H BIT 9	SIGN FLAG		
20H BIT A	PREVIOUS=0,CURRENT=1		
22H	PREVIOUS MODE STORE		
78H-79H	PERIOD		
7AH	80Hz COUNT		1 SEC CHECK

NOTES:

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 3/87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	3/87	8751 RAM STORAGE ASSIGNMENTS FOR VLBA BASEBND CONVERTER RADIOMETRY SOFTWARE
		CHECKED BY:		
	SCALE	APPROVAL PROJECT		AER\8751RAM C 54[illegible]052
	CLASSIFICATION	ENGINEER:		

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



C-54120D053

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE NONE

CLASSIFICATION

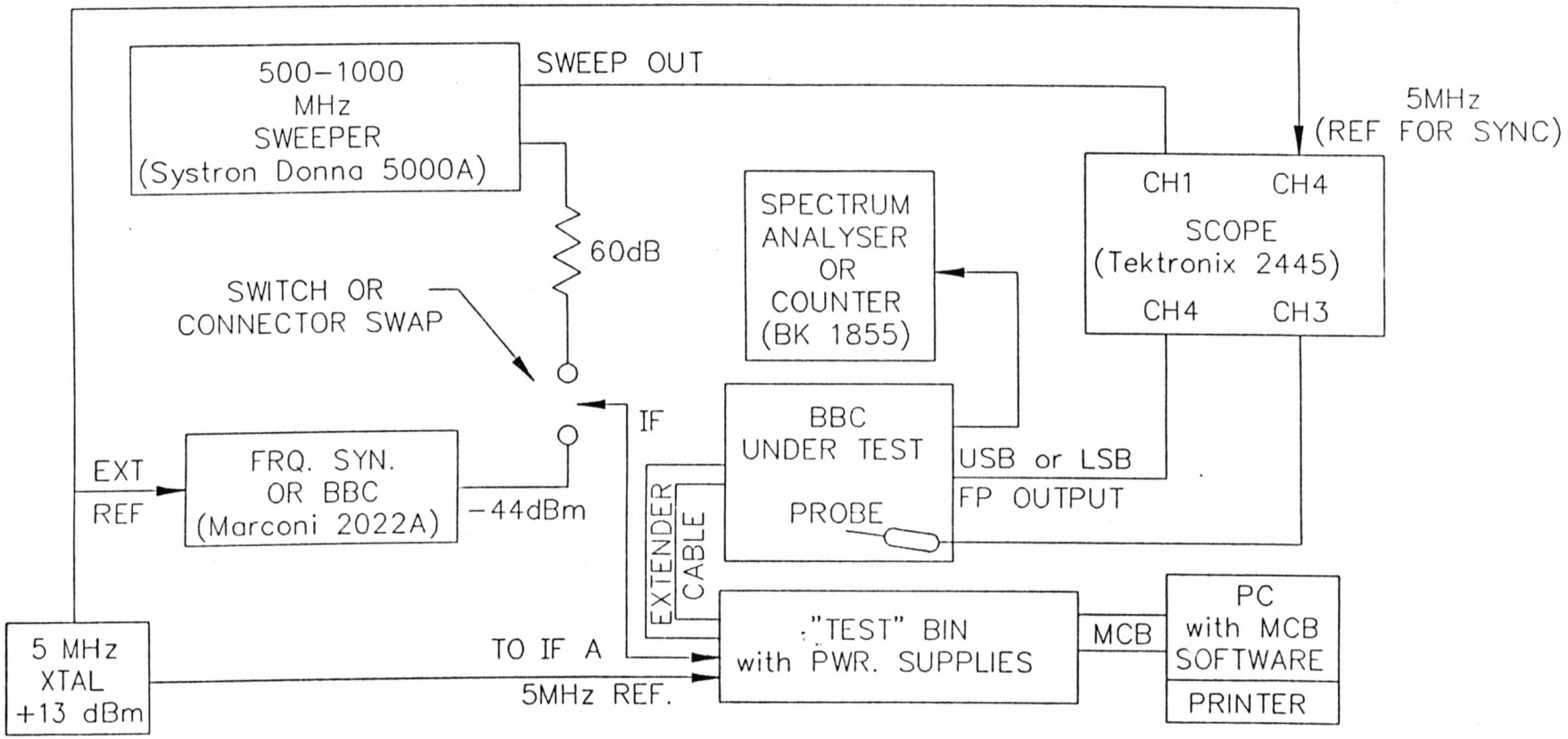
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHIL BROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

LATCHED MEMORY
BIT LOCATIONS

AERSLATCH	C	54120D053	
	DWG SIZE	DWG NO	REV

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE NONE

CLASSIFICATION

		DATE
DRAWN FOR	A.E.ROGERS	10/88
DRAWN BY	C.KOSTKA	10/88
CHECKED BY		

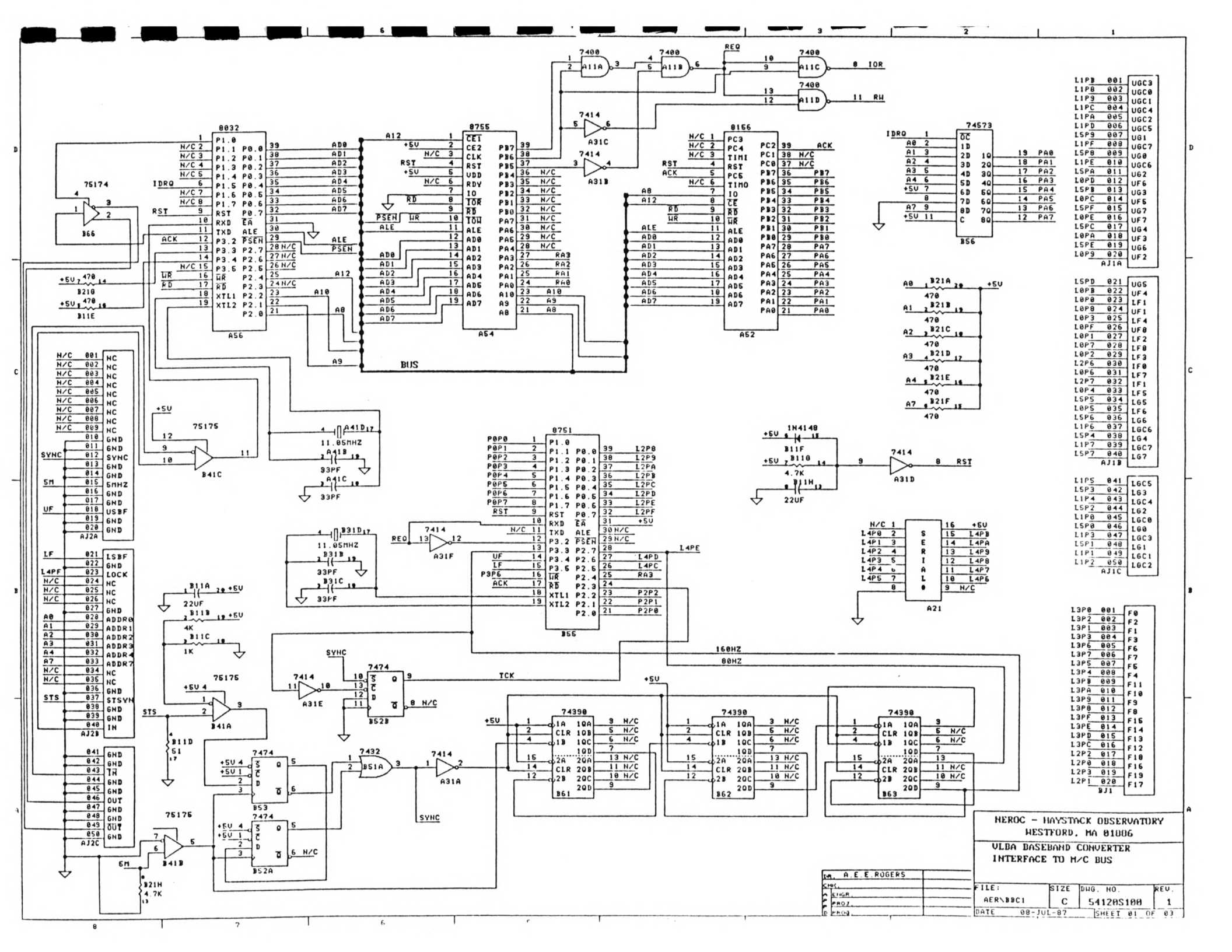
APPROVALS

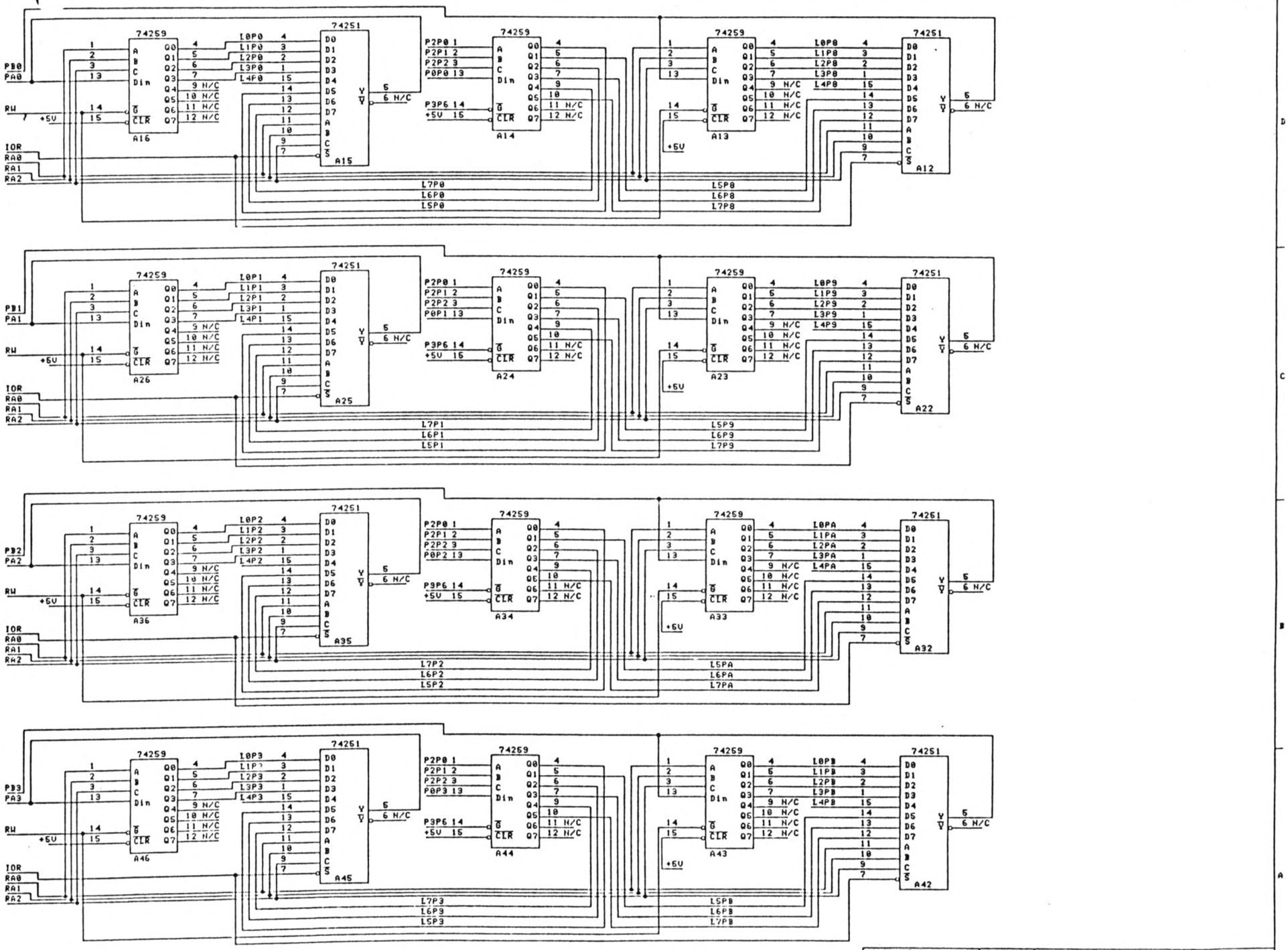
PROJECT	
ENGINEER	
MATL. & PROCESS	
STRUCTURES	
THERMAL	
MECH. ANALYSIS	

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

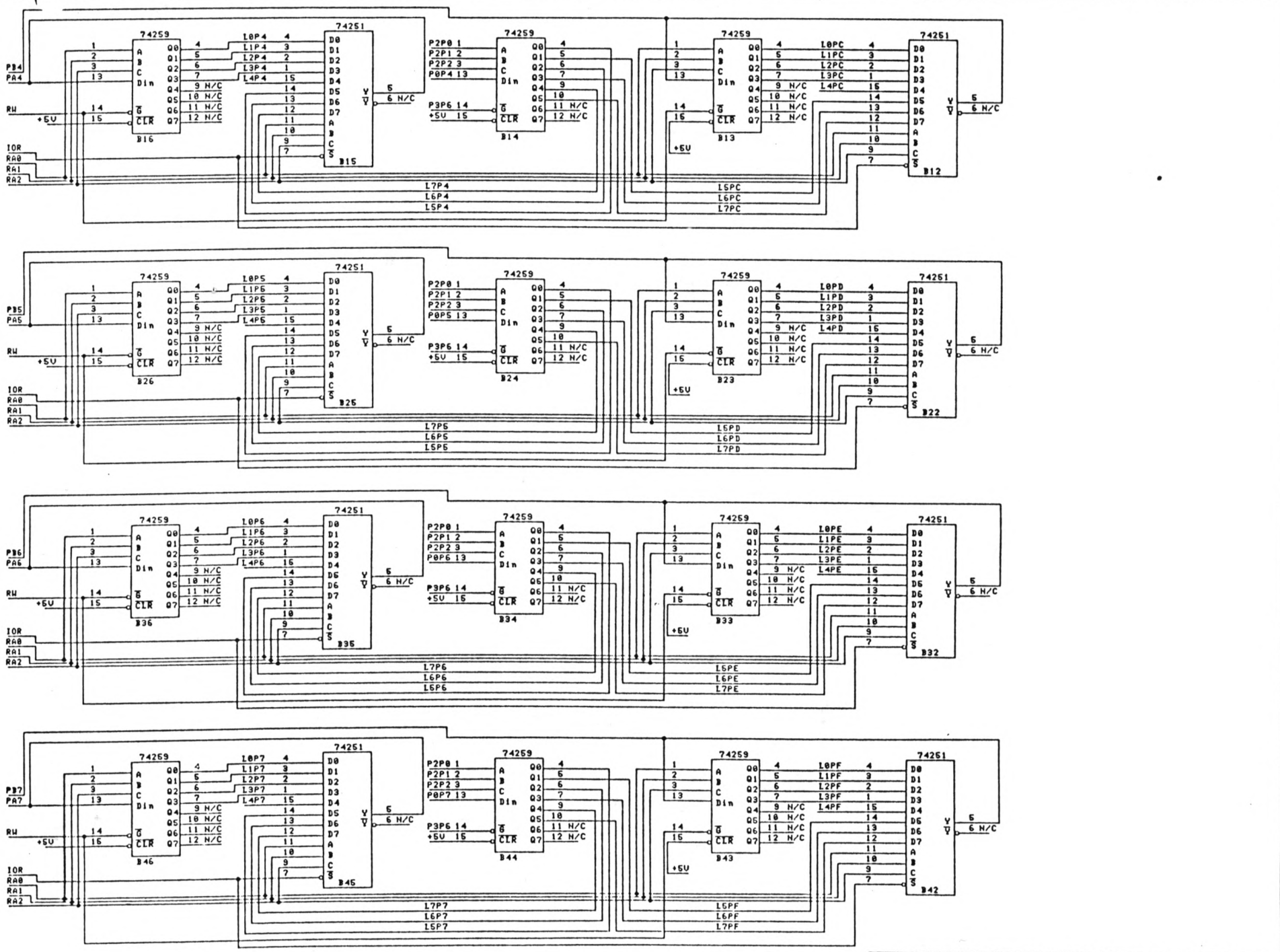
VLBA BASEBAND CONVERTER CHECK-OUT / TEST SET-UP

BCCHOTST	A	54120K054	
	DWG. SIZE	DWG. NO.	REV.

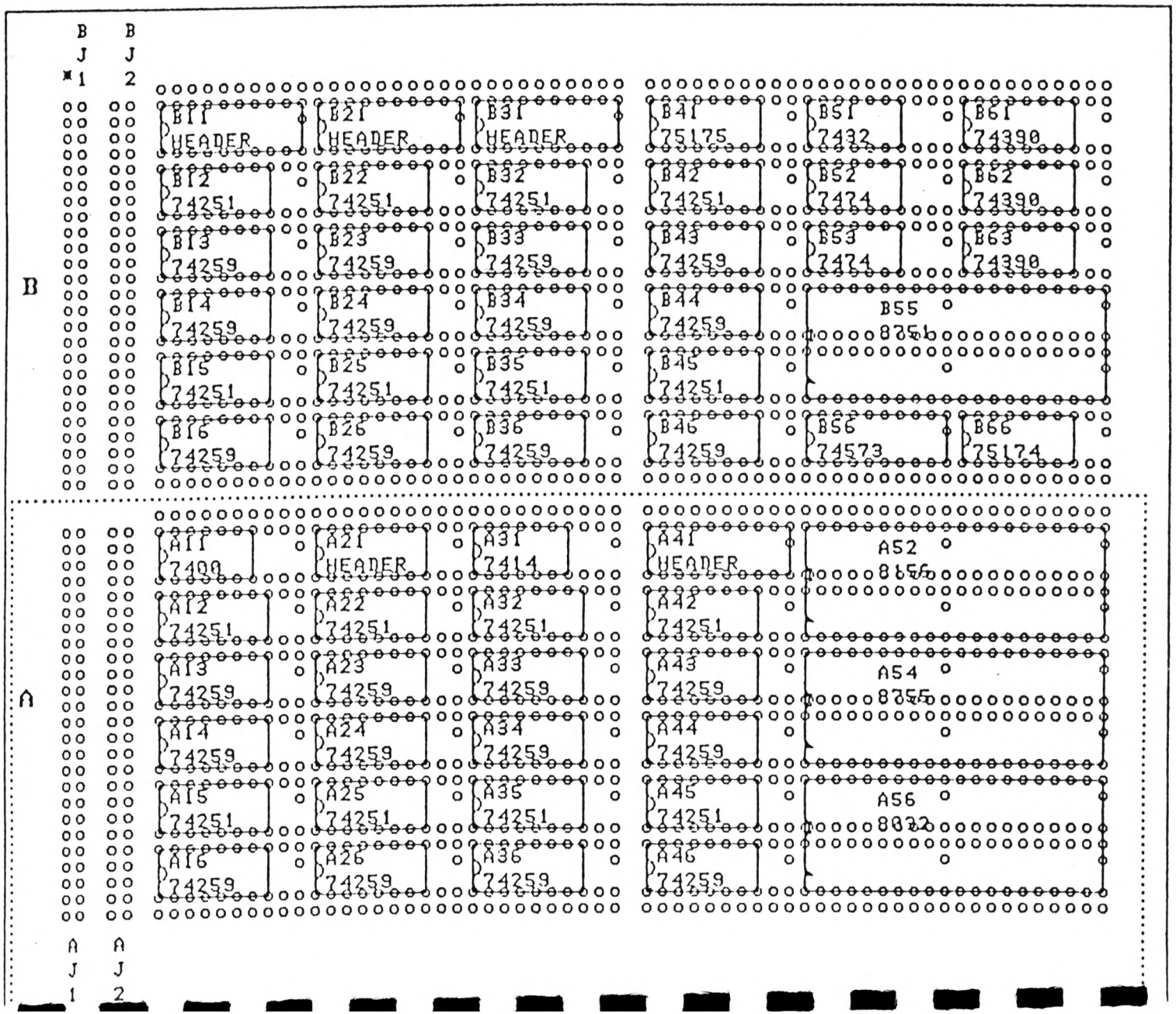

HEROC - HAYSTACK OBSERVATORY
WESTFORD, MA 01886
VLBA BASEBAND CONVERTER
INTERFACE TO M/C BUS
DR. A.E.E.ROGERS
FILE: AER\BBC1
SIZE C
DWG. NO. 54128S100
REV. 1
DATE 08-JUL-87
SHEET 01 OF 03
BUS
11.05MHZ
33PF
22UF
4.7K
1K
160HZ
80HZ
TCK
SYNC
IDRQ
RST
ACK
IOR
RH
RST
PSEN
ALE

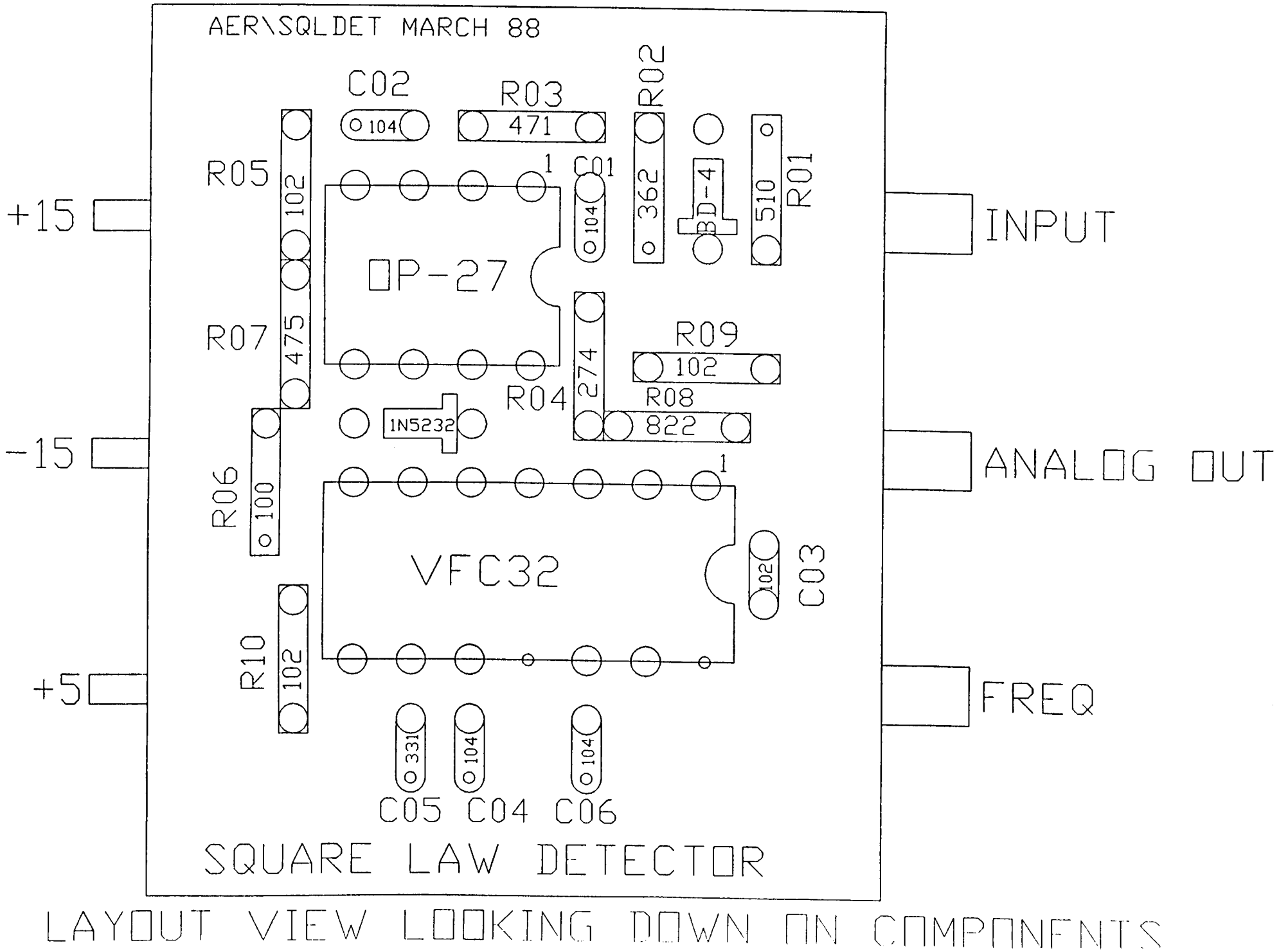


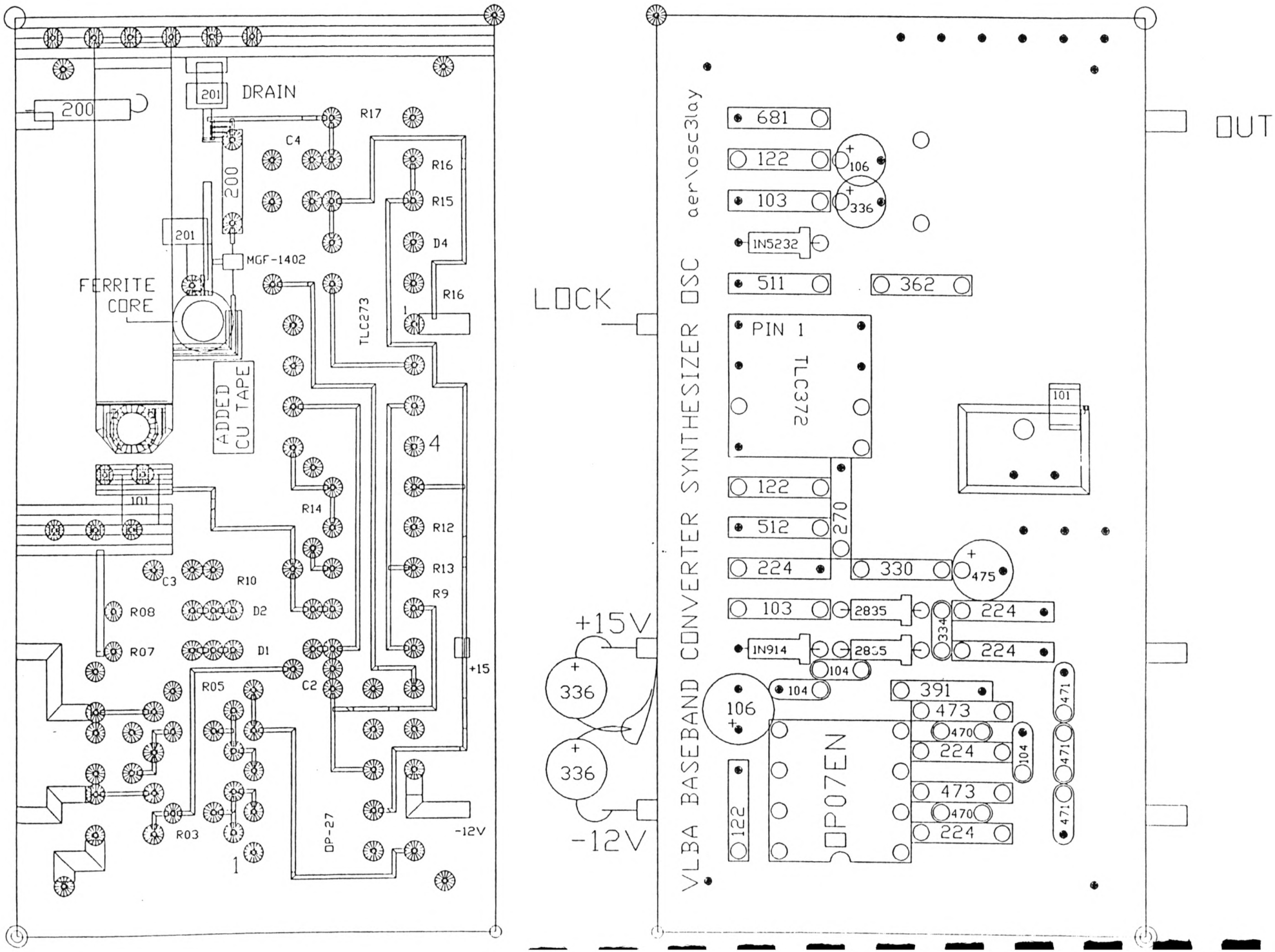
DR. A.E.E.ROGERS		VLBA BASEBAND CONVERTER DIGITAL INTERFACE TO M/C BUS	
CHK.			
ENGR.		FILE: AER\BBC2	C 5412BS101
PROJ.		6 JUN 86	
MGR.			



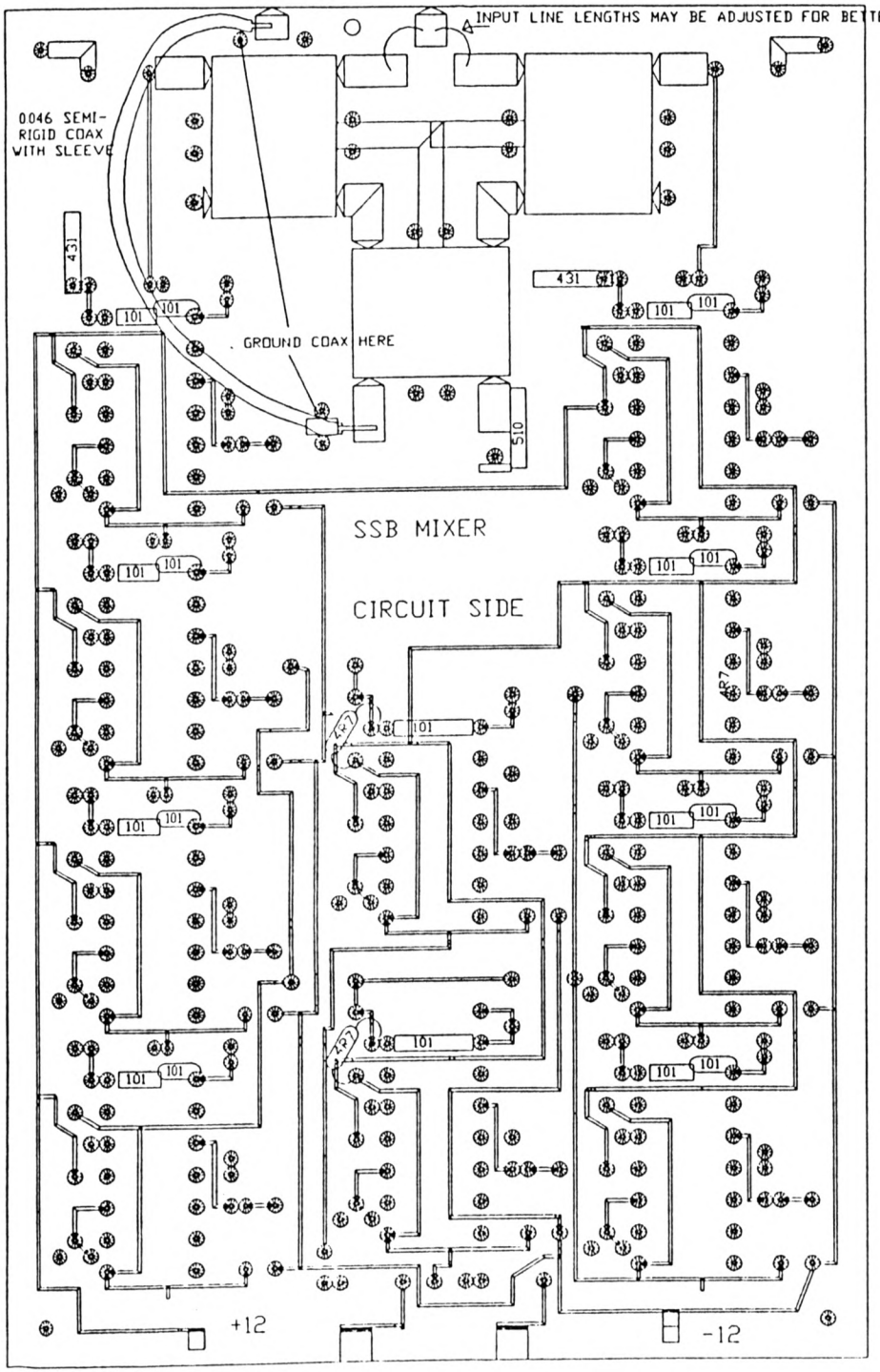
DR. A.E.E.ROGERS		VLBA BASEBAND CONVERTER DIGITAL INTERFACE TO M/C BUS	
CHK.			
ENGR.			
PROJ.		FILE: AER\BBC3	C 54120S102
MGR.		6 JUN 86	

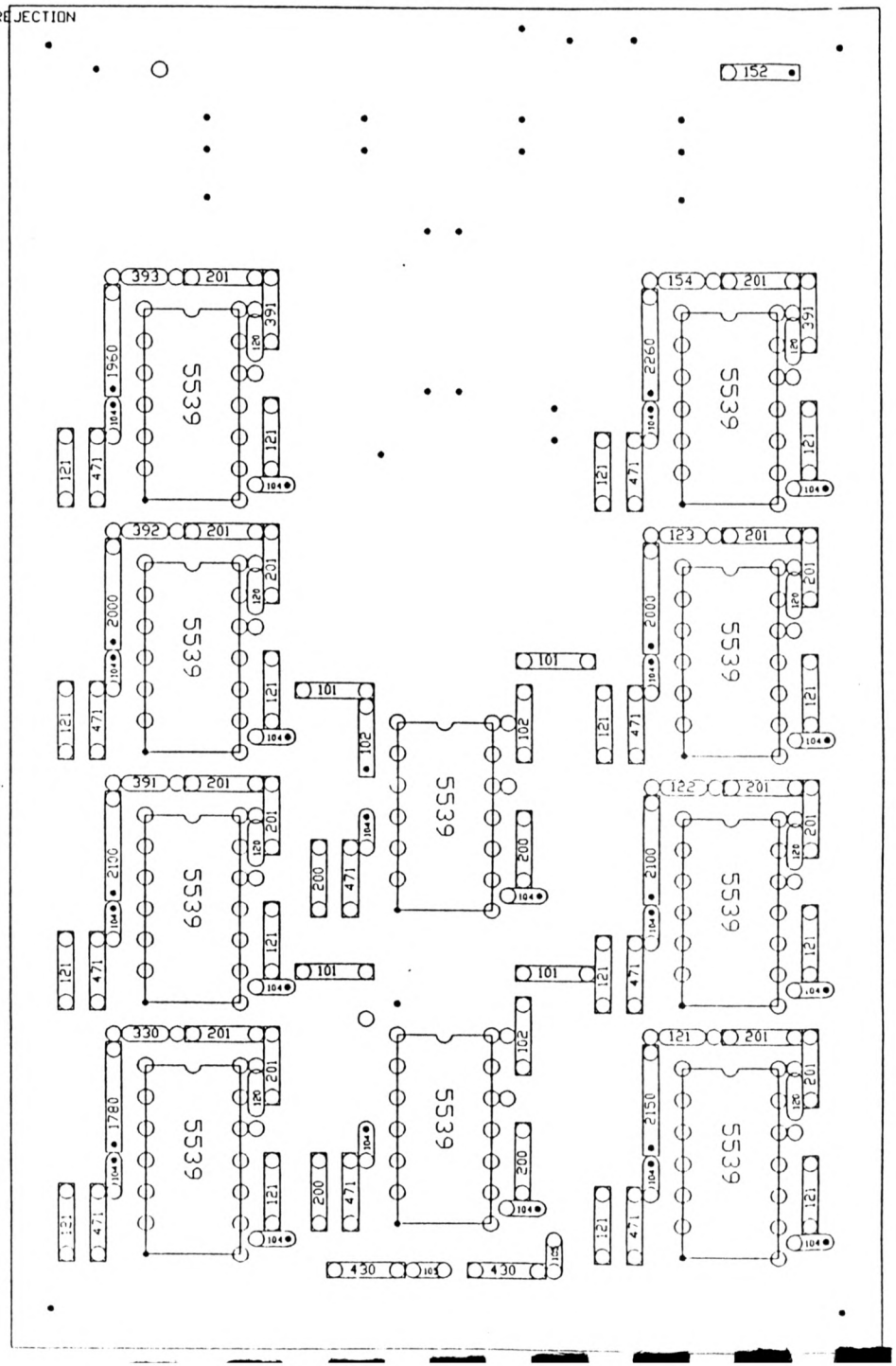

B
J
1
B
J
2
B11
HEADER
B21
HEADER
B31
HEADER
B41
75175
B51
7432
B61
74390
B12
74251
B22
74251
B32
74251
B42
74251
B52
7474
B62
74390
B13
74259
B23
74259
B33
74259
B43
74259
B53
7474
B63
74390
B14
74259
B24
74259
B34
74259
B44
74259
B55
8256
B15
74251
B25
74251
B35
74251
B45
74251
B16
74259
B26
74259
B36
74259
B46
74259
B56
74573
B66
75174
A
A11
7400
A21
HEADER
A31
7414
A41
HEADER
A52
8256
A12
74251
A22
74251
A32
74251
A42
74251
A13
74259
A23
74259
A33
74259
A43
74259
A54
8255
A14
74259
A24
74259
A34
74259
A44
74259
A15
74251
A25
74251
A35
74251
A45
74251
A56
8032
A16
74259
A26
74259
A36
74259
A46
74259
A
J
1
A
J
2


AER\SQLDET MARCH 88
C02
104
R03
471
R02
362
BD-4
R01
510
R05
102
C01
104
+15
OP-27
INPUT
R07
475
R09
102
R04
274
R08
822
1N5232
-15
ANALOG OUT
R06
100
VFC32
C03
102
R10
102
+5
FREQ
331
104
104
C05 C04 C06
SQUARE LAW DETECTOR
LAYOUT VIEW LOOKING DOWN ON COMPONENTS

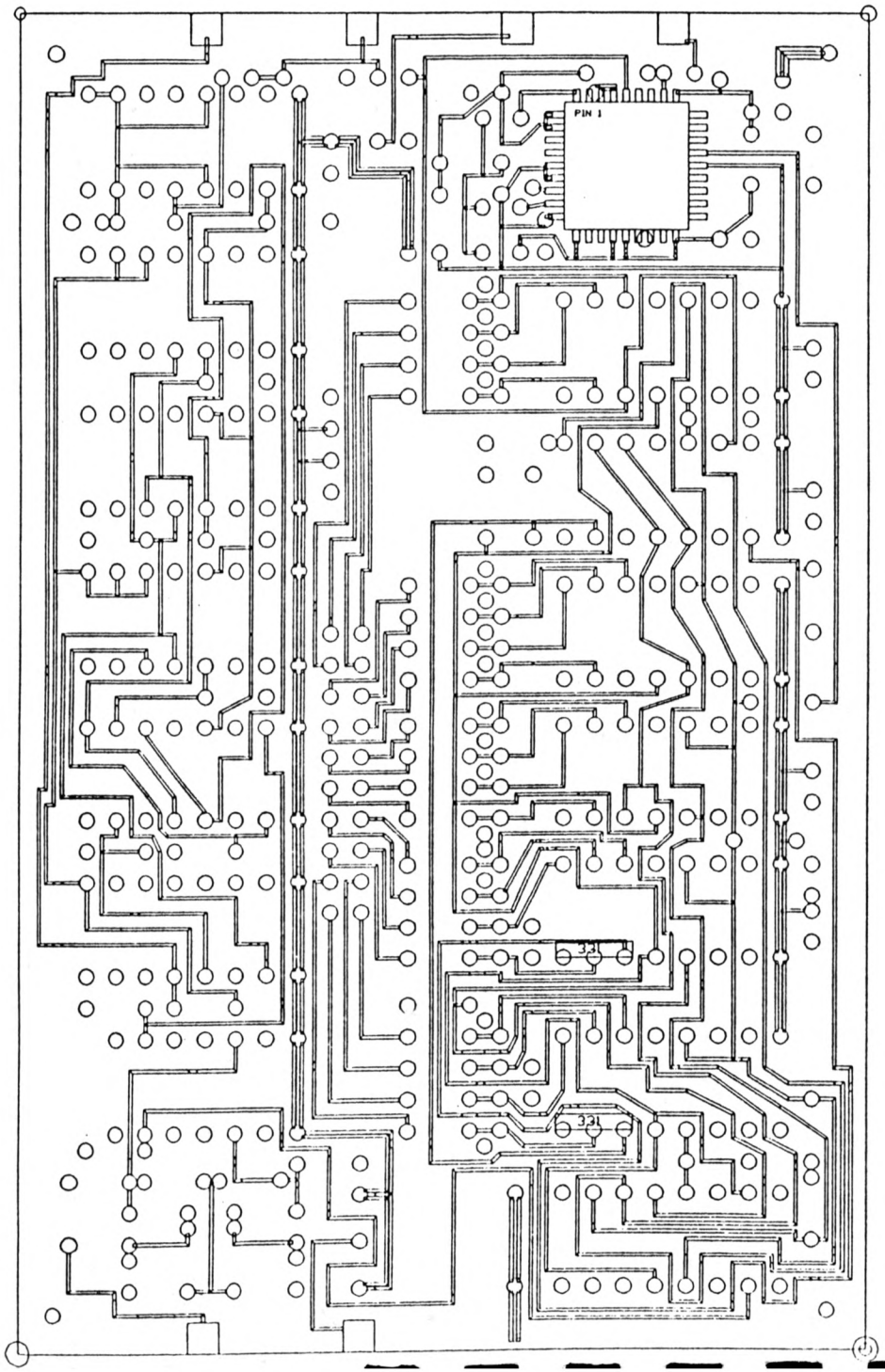

VLBA BASEBAND CONVERTER SYNTHESIZER OSC
aer\osc3lay
LOCK
+15V
-12V
OUT
DRAIN
FERRITE CORE
ADDED CU TAPE
MGF-1402
TLC273
TLC372
OP07EN
OP-27
PIN 1
200
201
101
681
122
103
1N5232
511
362
106
336
512
224
270
330
475
2835
334
1N914
104
391
473
470
471
R17
R16
R15
D4
R14
R12
R13
R9
R10
R08
D2
R07
D1
R05
C2
C3
C4
R03
+15
-12V
1
4

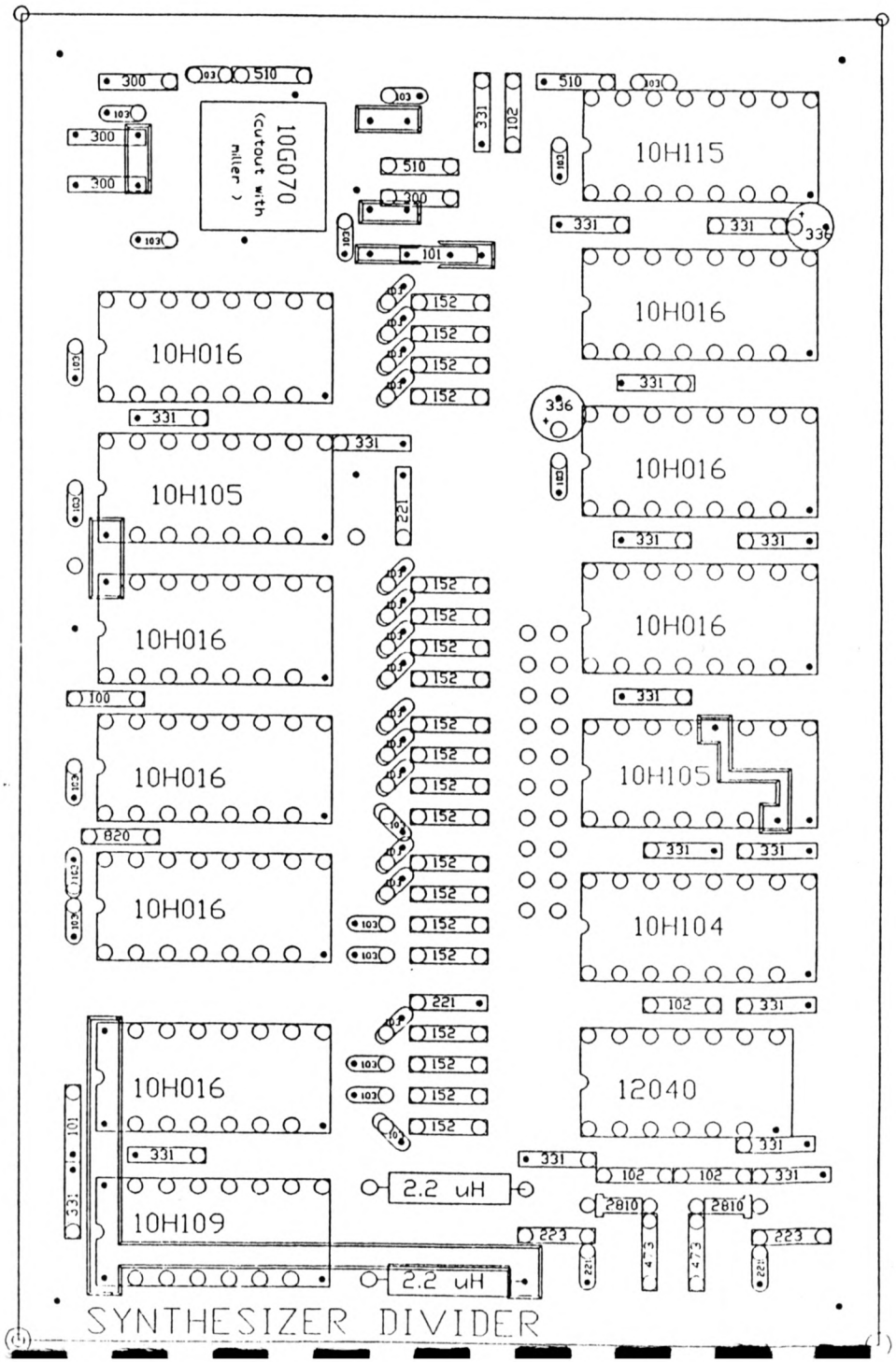
5539
LH0033
SDS002
JUMPER
COMPONENT SIDE


INPUT LINE LENGTHS MAY BE ADJUSTED FOR BETTER IMAGE REJECTION
0046 SEMI-
RIGID COAX
WITH SLEEVE
GROUND COAX HERE
SSB MIXER
CIRCUIT SIDE
+12
-12


5539

+15
7806
7812
4W
OSC
OSCB
SQ
SQ
+5
4W
DIV
SQ
SQ
LSB
MSB
-15
OSC
SQ
SQ
7906
INSULATED
FROM HEAT SINK
-6
7912
INSULATED
FROM HEAT SINK
7407
7406


PIN 1
331
331
331


10G070
(cutout with miller)
10H016
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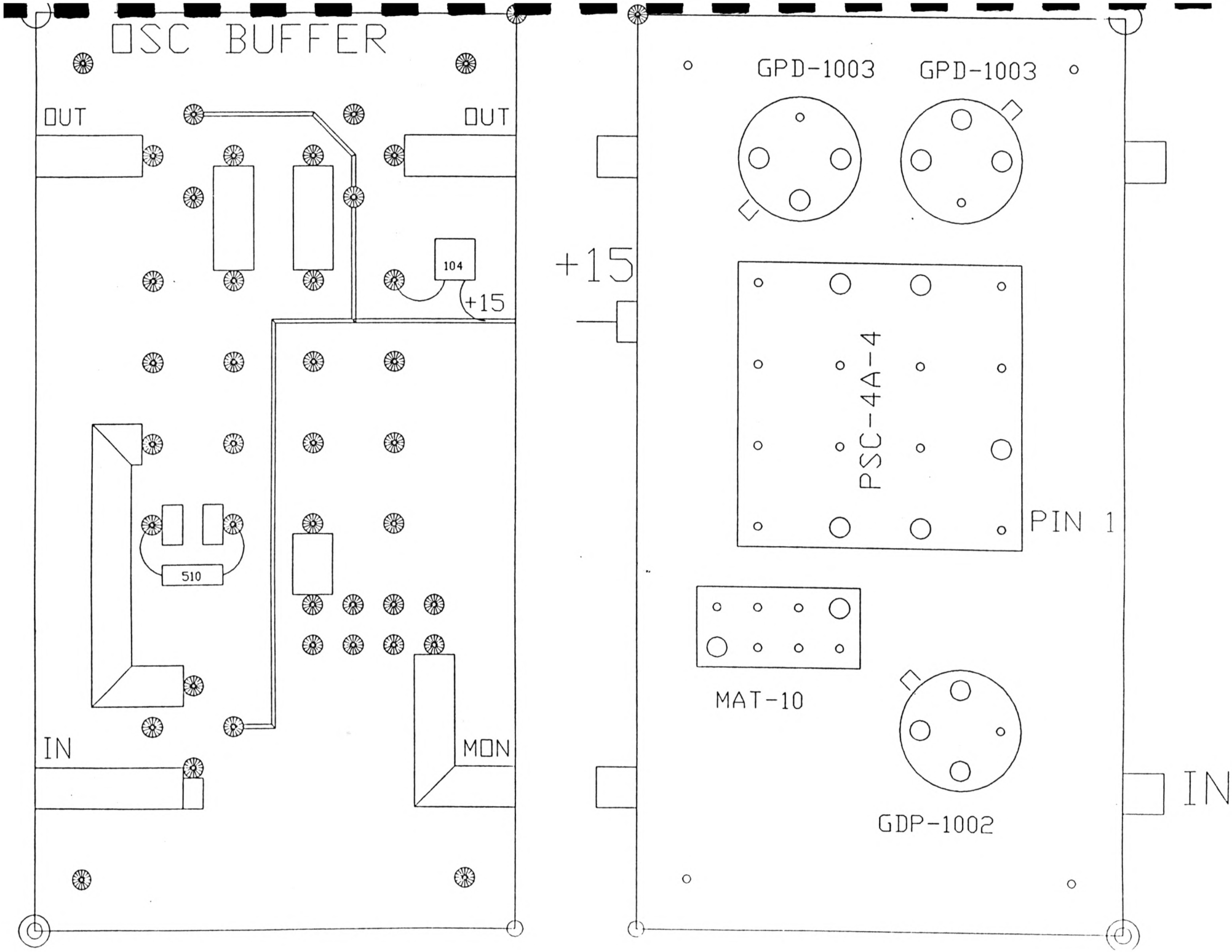
OSC BUFFER
OUT
OUT
104
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510
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MON
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GPD-1003
GPD-1003
PSC-4A-4
PIN 1
MAT-10
GDP-1002
IN

PARTS LIST FROM DBASE FILE:PARTS.DBF

REF	SUBMOD	PART	DESC	MFR	COST	QTY	TOTAL COST
C01	BBC-4WAY	100B201JMS50	200 PF MICROWAVE	ATC	2.87	10	28.70
C	BBC-4WAY	100B470K-Ca-500	47 PF MICROWAVE	ATC	2.87	2	5.74
MP4	BBC-4WAY	1019-1511-000	SMC BULKHEAD	AEP	1.77	5	8.85
C	BBC-4WAY	105K	1.0 UF	AVX	0.32	2	0.64
MP3	BBC-4WAY	1250-003	FEED-THRU	ERIE	1.53	4	6.12
MS	BBC-4WAY	54120M015	BOX DRILLING	HAYSTACK	20.00	1	20.00
U02	BBC-4WAY	74HC139	74139	RCA	0.77	1	0.77
U03	BBC-4WAY	74HC4049	744049	RCA	0.78	1	0.78
U04	BBC-4WAY	74HC4050	744050	RCA	0.47	1	0.47
PC	BBC-4WAY	AER\4WAY2	PC BOARD	PACLAB	40.00	1	40.00
U01	BBC-4WAY	GPD-1003	AMP	AVANTEK	23.00	1	23.00
MS	BBC-4WAY	HAY42520	BOX WITH COVERS	PREC.MACHINE	40.00	1	40.00
MP2	BBC-4WAY	MAT-3	3 DB ATTEN	MINICIRCUITS	5.00	1	5.00
MP1	BBC-4WAY	PSW-1211	DIODE SWITCH	MINICIRCUITS	24.00	7	168.00
MP20	BBC-A	1105-7521-003	SMC CABLE PLUG	AEP	2.49	34	84.66
MP12	BBC-A	200458-1	BLOCK	AMP	3.00	1	3.00
MP13	BBC-A	200833-4	GUIDE PINS	AMP	0.36	2	0.72
MP14	BBC-A	200835-4	GUIDE SOCKETS	AMP	0.48	2	0.96
MP18	BBC-A	201142-2	SPRING	AMP	0.05	11	0.55
MP17	BBC-A	201143-5	COAXICON PIN	AMP	2.70	11	29.70
MP15	BBC-A	202394-2	HOOD	AMP	1.04	1	1.04
MP16	BBC-A	202422-1	POWER PINS	AMP	0.50	4	2.00
MP17	BBC-A	328666	FERRULE	AMP	0.08	11	0.88
MP22	BBC-A	3421-6000	20 PIN CONN	3M	4.04	6	24.24
MP21	BBC-A	3425-6000	50 PIN CONN	3M	6.70	4	26.80
MP22	BBC-A	3452-6000	16 PIN CONN	3M	2.45	4	9.80
MP23	BBC-A	3473-6000	10 PIN CONN	3M	2.15	4	8.60
SS	BBC-A	54120I039	F.P.SILK SCREEN	NYES	100.00	1	100.00
MS	BBC-A	54120M028 BOTTOM	BAR SUPPORT MOD	HAYSTACK	20.00	1	20.00
MS	BBC-A	54120M028 TOP	BAR SUPPORT MOD	HAYSTACK	20.00	1	20.00
MS	BBC-A	54120M034	MOUNTING PLATE	HAYSTACK	20.00	1	20.00
MS	BBC-A	54120M038	FRONT PANEL	HAYSTACK	100.00	1	100.00
MS	BBC-A	54120M047	HEAT SINK	HAYSTACK	100.00	1	100.00
MS	BBC-A	C53306M013-2UA	FRONT PANEL	PREC.MACHINE	20.00	1	20.00
MS	BBC-A	C53306M014-2UA	PERFORATED COVER	PREC.MACHINE	10.00	2	20.00
MS	BBC-A	C53306M015-2UA	MODULEREAR PANEL	PREC.MACHINE	20.00	1	20.00
MS	BBC-A	C53306M016	BAR SUPPORT	PREC.MACHINE	10.00	4	40.00
MS	BBC-A	C53306M017	SIDE PLATE	PREC.MACHINE	10.00	2	20.00
WORK	BBC-A	ENGINEER	CHECKOUT	HAYSTACK	100.00	8	800.00
MP19	BBC-A	KC19-153	F.P.BNC	KINGS	6.76	3	20.28
MPX	BBC-A	RT/DUROID 5880	0.062 THK 1 OZ	ROGERS	143.87	1	143.87
WORK	BBC-A	TECH	ASSEMBLY	HAYSTACK	10.00	40	400.00
MP4	BBC-BUF	1019-1511-000	SMC BULKHEAD	AEP	1.77	4	7.08
C	BBC-BUF	104K	0.1 UF	AVX	0.10	1	0.10
MP3	BBC-BUF	1250-003	FEED THRU	ERIE	1.53	1	1.53
MS	BBC-BUF	54120M018	BOX DRILLING	HAYSTACK	20.00	1	20.00
PC	BBC-BUF	AER\OSCBUF	PC BOARD	PACLAB	40.00	1	40.00
U01	BBC-BUF	GPD-1002	AMP	AVANTEK	22.00	1	22.00
U02	BBC-BUF	GPD-1003	AMP	AVANTEK	23.00	2	46.00
MS	BBC-BUF	HAY25014	BOX WITH COVERS	PREC.MACHINE	39.25	1	39.25
MP2	BBC-BUF	MAT-10	10 DB ATTEN	MINICIRCUITS	5.00	1	5.00
MP1	BBC-BUF	PSC-4A-4	POWER SPLIT	MINICIRCUITS	60.00	1	60.00
R01	BBC-BUF	RCR05G510J	51 OHM 1/8W	AB	0.20	1	0.20
MP2	BBC-DIB	1874010446	40 PIN ADAPTOR	EMC	10.00	4	40.00
D	BBC-DIB	1N4148	DIODE		0.20	1	0.20
C	BBC-DIB	226K	22 UF		0.20	2	0.40
C	BBC-DIB	330J	33 PF		0.20	4	0.80
MP3	BBC-DIB	616-CG1	HOLDERS	AUGAT	0.50	5	2.50
U006	BBC-DIB	74HCT00N	7400	RCA	1.40	1	1.40
U007	BBC-DIB	74HCT14N	7414	RCA	1.50	1	1.50
U014	BBC-DIB	74HCT251N	74251	RCA	1.62	16	25.92
U004	BBC-DIB	74HCT259N	74259	RCA	1.90	24	45.60
U008	BBC-DIB	74HCT32N	7432	TI	1.58	1	1.58
U003	BBC-DIB	74HCT390N	74390	SIGNETICS	2.60	3	7.80
U009	BBC-DIB	74HCT573N	74573		2.89	1	2.89
U005	BBC-DIB	74HCT74N	7474	RCA	1.50	2	3.00
U001	BBC-DIB	75174N	75174	TI	1.00	1	1.00
U002	BBC-DIB	75175N	75175	TI	1.00	1	1.00
U010	BBC-DIB	D8751H	8751	INTEL	65.95	1	65.95
U013	BBC-DIB	D8755A-2	8755	INTEL	30.00	1	30.00
MP1	BBC-DIB	EM09388-A2T-2SF	WIRE WRAP PANEL	EMC	253.97	1	253.97
U011	BBC-DIB	P8032AH	8032	INTEL	24.80	1	24.80
U012	BBC-DIB	P8156H	8156	INTEL	6.00	1	6.00
R	BBC-DIB	RCR05G102J	1 K OHMS 1/8W	AB	0.20	1	0.20
R	BBC-DIB	RCR05G471J	470 OHMS 1/8W	AB	0.20	8	1.60
R	BBC-DIB	RCR05G472J	4.7 K OHMS 1/8W	AB	0.20	2	0.40
R	BBC-DIB	RCR05G510J	51 OHMS 1/8W	AB	0.20	1	0.20
X	BBC-DIB	U49-S1105	11.05 MHZ XTAL	USC	2.85	2	5.70
WIRE	BBC-DIB	WIRE	WIRE WRAP	DATACON	0.14	999	139.86
MP4	BBC-DIV	1019-1511-000	SMC BULKHEAD	AEP	1.77	6	10.62
C01	BBC-DIV	103K	0.01 UF	AVX	0.10	33	3.30
U07	BBC-DIV	10G070-4F	DIV 10/11	GIGABITLOGIC	297.00	1	297.00
MP3	BBC-DIV	1250-003	FEED THRU	ERIE	1.53	1	1.53
C02	BBC-DIV	221J	220 PF	AVX	0.12	2	0.24
C03	BBC-DIV	336K	33 UF	SPRAGUE	0.70	2	1.40
D01	BBC-DIV	5082-2810	DIODE	HP	1.55	2	3.10
MS	BBC-DIV	54120M033	BOX DRILLING	HAYSTACK	20.00	1	20.00
MP5	BBC-DIV	87215-7	20 PIN CONN	AMP	3.20	1	3.20

PARTS LIST FROM DBASE FILE:PARTS.DBF

REF	SUBMOD	PART	DESC	MFR	COST	QTY	TOTAL COST
PC	BBC-DIV	AER\DIV	PC BOARD	PACLAB	40.00	1	40.00
MS	BBC-DIV	HAY45030	BOX WITH COVERS	PREC.MACHINE	43.60	1	43.60
U01	BBC-DIV	MC10H016L	10016	MOTOROLA	5.53	8	44.24
U03	BBC-DIV	MC10H104L	10104	MOTOROLA	0.69	1	0.69
U02	BBC-DIV	MC10H105L	10105	MOTOROLA	0.69	2	1.38
U04	BBC-DIV	MC10H109L	10H109	MOTOROLA	1.00	1	1.00
U05	BBC-DIV	MC10H115L	MC10H115	MOTOROLA(RQ)	0.59	1	0.59
U06	BBC-DIV	MC12040L	12040	MOTOROLA	8.80	1	8.80
R06	BBC-DIV	RCR05G100J	10 OHM 1/8W	AB	0.20	1	0.20
R08	BBC-DIV	RCR05G101J	100 OHM 1/8W	AB	0.20	1	0.20
R04	BBC-DIV	RCR05G102J	1K OHM 1/8W	AB	0.20	4	0.80
R02	BBC-DIV	RCR05G152J	1.5K OHM 1/8W	AB	0.20	20	4.00
R	BBC-DIV	RCR05G221J	220 OHM 1/8W	AB	0.10	2	0.20
R10	BBC-DIV	RCR05G222J	22K OHM 1/8W	AB	0.20	2	0.40
R05	BBC-DIV	RCR05G300J	30 OHM 1/8W	AB	0.20	4	0.80
R01	BBC-DIV	RCR05G331J	330 OHM 1/8W	AB	0.20	19	3.80
R09	BBC-DIV	RCR05G473J	47K OHM 1/8W	AB	0.20	2	0.40
R03	BBC-DIV	RCR05G510J	51 OHM 1/8W	AB	0.20	3	0.60
L01	BBC-DIV	WEE 2.2	2.2 UH	NYTRONICS	1.70	2	3.40
MP1	BBC-FILT	1009-1511-000	SMC PC CONN	AEP	2.25	4	9.00
C005	BBC-FILT	101J	100 PF	AVX	0.13	5	0.65
C011	BBC-FILT	102J	1000PF	AVX	1.95	1	1.95
C003	BBC-FILT	103K	0.01 UF	AVX	0.10	24	2.40
C003	BBC-FILT	104K	0.1 UF	AVX	0.10	17	1.70
C002	BBC-FILT	105K	1 UF	AVX	0.32	5	1.60
C006	BBC-FILT	151J	150 PF	AVX	0.13	1	0.13
C	BBC-FILT	181J	180 PF	AVX	0.10	2	0.20
C007	BBC-FILT	201J	200 PF	AVX	0.73	1	0.73
C004	BBC-FILT	220J	22 PF	AVX	0.10	1	0.10
C008	BBC-FILT	221J	220 PF	AVX	0.12	1	0.12
C012	BBC-FILT	2R2J	2.7 PF	AVX	0.50	2	1.00
C010	BBC-FILT	391J	390 PF	METUCHIN	0.95	1	0.95
C001	BBC-FILT	470J	47 PF	AVX	0.12	3	0.36
C013	BBC-FILT	4R7J	4.7 PF	AVX	0.50	2	1.00
MS	BBC-FILT	54120M042	LONG BAR	HAYSTACK	20.00	2	40.00
MS	BBC-FILT	54120M043	SHORT BAR	HAYSTACK	20.00	2	40.00
MS	BBC-FILT	54120M044	FILT BASEPLATE	HAYSTACK	20.00	1	20.00
MP3	BBC-FILT	87215-2	10 PIN CONN	AMP	1.73	1	1.73
MP2	BBC-FILT	87215-7	20 PIN CONN	AMP	3.20	1	3.20
MP4	BBC-FILT	87215-8	16 PIN	AMP	2.00	1	2.00
PC	BBC-FILT	AER\AGC	PC BOARD	PACLAB	40.00	2	80.00
PC	BBC-FILT	AER\FILT	PC BOARD	PACLAB	40.00	4	160.00
PC	BBC-FILT	AER\INPUT	PC BOARD	PACLAB	40.00	1	40.00
C	BBC-FILT	C312C109D2G5CA	1 PF	KEMET	0.10	2	0.20
U003	BBC-FILT	LH0033CG	LH0033	ANALOG DEV	22.00	1	22.00
U002	BBC-FILT	NE5539N	NE5539N	SIGNETICS	2.50	7	17.50
R040	BBC-FILT	RCR05G105J	1M OHM 1/8W	AB	0.20	8	1.60
R012	BBC-FILT	RCR05G121J	120 OHM 1/8W	AB	0.20	2	0.40
R015	BBC-FILT	RCR05G161J	160 OHM 1/8W	AB	0.20	1	0.20
R011	BBC-FILT	RCR05G201J	200 OHM 1/8W	AB	0.20	3	0.60
R014	BBC-FILT	RCR05G202J	2000 OHM 1/8W	AB	0.20	2	0.40
R	BBC-FILT	RCR05G221J	220 OHMS 1/8W	AB	0.95	1	0.95
R008	BBC-FILT	RCR05G240J	240 OHM 1/8W	AB	0.20	12	2.40
R	BBC-FILT	RCR05G272J	2.7 K OHMS 1/8W	AB	0.20	2	0.40
R019	BBC-FILT	RCR05G332J	3.3K OHM 1/8W	AB	0.20	2	0.40
R	BBC-FILT	RCR05G360J	36 OHM 1/8W	AB	0.20	1	0.20
R010	BBC-FILT	RCR05G470J	47 OHM 1/8W	AB	0.20	4	0.80
R009	BBC-FILT	RCR05G471J	470 OHM 1/8W	AB	0.20	10	2.00
R013	BBC-FILT	RCR05G510J	51 OHM 1/8W	AB	0.20	8	1.60
R018	BBC-FILT	RCR05G513J	51K OHM 1/8W	AB	0.20	1	0.20
R	BBC-FILT	RCR05G621J	620 OHMS 1/8W	AB	0.20	1	0.20
R016	BBC-FILT	RCR05G750J	75 OHM 1/8W	AB	0.20	1	0.20
R039	BBC-FILT	RCR07G200J	20 OHM 1/4W	AB	0.30	1	0.30
R023	BBC-FILT	RN55D1051F	1050 OHM 1%	CORNING	0.10	1	0.10
R	BBC-FILT	RN55D10R0F	10.0 OHM 1%	CORNING	0.10	1	0.10
R001	BBC-FILT	RN55D1272F	12.7K OHM 1%	CORNING	0.10	16	1.60
R027	BBC-FILT	RN55D1540F	154 OHM 1%	CORNING	0.10	1	0.10
R006	BBC-FILT	RN55D1620F	162 OHM 1%	CORNING	0.10	16	1.60
R003	BBC-FILT	RN55D1781F	1.78K OHM 1%	CORNING	0.10	8	0.80
R037	BBC-FILT	RN55D1961F	1960 OHM 1%	CORNING	0.10	3	0.30
R020	BBC-FILT	RN55D2001F	2000 OHM 1%	CORNING	0.10	1	0.10
R026	BBC-FILT	RN55D2430F	243 OHM 1%	CORNING	0.10	1	0.10
R005	BBC-FILT	RN55D3740F	374 OHM 1%	CORNING	0.10	8	0.80
R025	BBC-FILT	RN55D3830F	383 OHM 1%	CORNING	0.10	1	0.10
R036	BBC-FILT	RN55D3921F	3920 OHM 1%	CORNING	0.10	2	0.20
R002	BBC-FILT	RN55D4221F	4.22K OHM 1%	CORNING	0.10	8	0.80
R021	BBC-FILT	RN55D4751F	4750 OHM 1%	CORNING	0.10	1	0.10
R	BBC-FILT	RN55D51R1F	51.1 OHM 1%	CORNING	0.10	7	0.70
R024	BBC-FILT	RN55D6190F	619 OHM 1%	CORNING	0.10	1	0.10
R035	BBC-FILT	RN55D7871F	7870 OHM 1%	CORNING	0.10	2	0.20
R004	BBC-FILT	RN55D8060F	806 OHM 1%	CORNING	0.10	8	0.80
R028	BBC-FILT	RN55D93R1F	93.1 OHM 1%	CORNING	0.10	1	0.10
R038	BBC-FILT	RN55D9530F	953 OHM 1%	CORNING	0.10	2	0.20
U001	BBC-FILT	SD5002N	SD5002N	SILICONIX	3.20	22	70.40
C09	BBC-OSC	100-B-101-J-P-50	100 PF MICROWAVE	ATC	2.50	2	5.00
C06	BBC-OSC	100-B-201-J-P-50	200 PF MICROWAVE	ATC	2.80	2	5.60
MP1	BBC-OSC	1019-1511-000	SMC BULKHEAD	AEP	1.77	3	5.31
C01	BBC-OSC	104K	0.1 UF	AVX	0.10	3	0.30

PARTS LIST FROM DBASE FILE:PARTS.DBF

REF	SUBMOD	PART	DESC	MFR	COST	QTY	TOTAL COST
C04	BBC-OSC	106K	10 UF		1.00	2	2.00
MP2	BBC-OSC	1250-003	FEED THRU	ERIE	1.53	3	4.59
MP	BBC-OSC	135CT050/4C4	FERRITE CORE	FERROXCUBE	0.10	1	0.10
D04	BBC-OSC	1N5232	ZENER DIODE		0.40	1	0.40
D03	BBC-OSC	1N914A	DIODE		0.40	1	0.40
R11	BBC-OSC	334K	0.33 UF	AVX	0.20	1	0.20
C05	BBC-OSC	336K	33 UF	SPRAGUE	0.70	3	2.10
C08	BBC-OSC	470J	47 PF	AVX	0.12	2	0.24
C07	BBC-OSC	471J	470 PF	AVX	0.14	3	0.42
C03	BBC-OSC	475K	4.7 UF		0.80	1	0.80
D01	BBC-OSC	5082-2835	SCHOTTKY DIODE	HP	0.42	2	0.84
MS	BBC-OSC	54120M016	BOX DRILLING	HAYSTACK	20.00	1	20.00
PC	BBC-OSC	AER\OSC3	PC BOARD	PACLAB	40.00	1	40.00
MS	BBC-OSC	HAY25014	BOX WITH COVERS	PREC.MACHINE	39.25	1	39.25
D05	BBC-OSC	MA46577B-30	VARACTOR DIODE	MACOM	87.00	1	87.00
Q03	BBC-OSC	MGF-1402	FET	MITSUBISHI	11.75	1	11.75
U01	BBC-OSC	OP-07EN	OP AMP	ANALOG DEV	7.15	1	7.15
R09	BBC-OSC	RCR05G103J	10K OHM 1/8W	AB	0.20	2	0.40
R06	BBC-OSC	RCR05G122J	1200 OHM 1/8W	AB	0.20	3	0.60
R21	BBC-OSC	RCR05G200J	20 OHMS 1/8W	AB	0.20	2	0.40
R03	BBC-OSC	RCR05G224J	220K OHM 1/8W	AB	0.20	5	1.00
R14	BBC-OSC	RCR05G270J	27 OHMS 1/8W	AB	0.20	1	0.20
R10	BBC-OSC	RCR05G330J	33 OHM 1/8W	AB	0.20	1	0.20
R18	BBC-OSC	RCR05G362J	3.6K OHM 1/8W	AB	0.20	1	0.20
R05	BBC-OSC	RCR05G391J	390 OHM 1/8W	AB	0.20	1	0.20
R01	BBC-OSC	RCR05G473J	47 K OHM 1/8W	AB	0.20	2	0.40
R12	BBC-OSC	RCR05G511J	510 OHM 1/8W	AB	0.20	1	0.20
R17	BBC-OSC	RCR05G681J	680 OHM 1/8W	AB	0.20	1	0.20
U2	BBC-OSC	TLC372CP	DUAL COMPARATOR		0.50	1	0.50
C001	BBC-PWR	104K	0.1 UF	AVX	0.10	16	1.60
MP1	BBC-PWR	2-87215-5	50 PIN CONN	AMP	6.93	1	6.93
C002	BBC-PWR	334M	0.33 UF		0.70	3	2.10
C002	BBC-PWR	336K	33 UF	SPRAGUE	0.70	4	2.80
MPX	BBC-PWR	54120M047	HEAT SINK	HAYSTACK	20.00	1	20.00
U001	BBC-PWR	7406N	7406	SIGNETICS	0.49	4	1.96
U002	BBC-PWR	7407N	7407		0.46	8	3.68
MP2	BBC-PWR	87215-2	10 PIN CONN	AMP	1.73	2	3.46
MP3	BBC-PWR	87215-7	20 PIN CONN	AMP	3.20	2	6.40
MP4	BBC-PWR	87215-8	16 PIN CONN	AMP	2.00	2	4.00
PC	BBC-PWR	AER\PWRDIS	PC BOARD	PACLAB	40.00	1	40.00
U003	BBC-PWR	MC7806CT	+6V REG	MOTOROLA	0.35	1	0.35
U005	BBC-PWR	MC7812CT	+12V REG	MOTOROLA	0.69	1	0.69
U004	BBC-PWR	MC7906CT	-6V REG	MOTOROLA	0.45	1	0.45
U006	BBC-PWR	MC7912CT	-12V REG	MOTOROLA	0.69	1	0.69
R001	BBC-PWR	RCR05G103J	10K OHM 1/8W	AB	0.20	124	24.80
MP5	BBC-PWR	TS-120-G-A	PINS	SAMTEC	0.36	16	5.76
MP2	BBC-SQL	1019-1511-000	SMC BULKHEAD	AEP	1.77	3	5.31
C03	BBC-SQL	102J	1000 PF	AVX	0.50	1	0.50
C01	BBC-SQL	104K	0.1 UF	AVX	0.10	4	0.40
MP1	BBC-SQL	1250-003	FEED THRU	ERIE	1.53	3	4.59
CR	BBC-SQL	1N5232	ZENER DIODE	MOTOROLA	0.50	1	0.50
C05	BBC-SQL	331J	330 PF	AVX	0.08	1	0.08
MS	BBC-SQL	54120M019	BOX DRILLING	HAYSTACK	20.00	1	20.00
U02	BBC-SQL	ADVFC32KN	VOLT TO FREQ CON	ANALOG DEV	8.95	1	8.95
PC	BBC-SQL	AER\SQDET	PC BOARD	PACLAB	40.00	1	40.00
CR1	BBC-SQL	BD-4	BACK DIODE	CUSTOM COMP.	6.00	1	6.00
MS	BBC-SQL	HAY17515	BOX WITH COVERS	PREC.MACHINE	34.50	1	34.50
U01	BBC-SQL	OP-27EN	OP AMP	ANALOG DEV	7.15	1	7.15
R06	BBC-SQL	RCR05G100J	10 OHM 1/8W	AB	0.20	1	0.20
R05	BBC-SQL	RCR05G102J	1000 OHM 1/8W	AB	0.20	3	0.60
R04	BBC-SQL	RCR05G274J	270K OHM 1/8W	AB	0.20	1	0.20
R02	BBC-SQL	RCR05G362J	3.6K OHM 1/8W	AB	0.20	1	0.20
R03	BBC-SQL	RCR05G471J	470 OHM 1/8W	AB	0.20	1	0.20
R07	BBC-SQL	RCR05G475J	4.7M OHM 1/8W	AB	0.20	1	0.20
R01	BBC-SQL	RCR05G510J	51 OHM 1/8W	AB	0.20	1	0.20
R08	BBC-SQL	RCR05G822J	8.2K OHM 1/8W	AB	0.20	1	0.20
MP3	BBC-SSB	1019-1511-000	SMC BULKHEAD	AEP	1.77	4	7.08
C12	BBC-SSB	101J	100 PF	AVX	0.12	8	0.96
C02	BBC-SSB	104K	0.1 UF	AVX	0.10	20	2.00
C13	BBC-SSB	105K	1 UF	AVX	0.32	2	0.64
C03	BBC-SSB	120J	12 PF		0.50	8	4.00
C08	BBC-SSB	121J	120 PF		0.50	1	0.50
C09	BBC-SSB	122J	1200 PF	AVX	1.95	1	1.95
C10	BBC-SSB	123J	0.012 UF	AVX	0.12	1	0.12
MP4	BBC-SSB	1250-003	FEED THRU	ERIE	1.53	2	3.06
C11	BBC-SSB	154J	0.15 UF	METUCHIN	2.10	1	2.10
C04	BBC-SSB	330J	33 PF	AVX	0.12	1	0.12
C05	BBC-SSB	391J	390 PF	AVX	0.13	1	0.13
C06	BBC-SSB	392J	3900 PF		0.50	1	0.50
C07	BBC-SSB	393J	0.039 UF		0.70	1	0.70
C	BBC-SSB	4R7J	4.7 PF	AVX	0.20	2	0.40
MS	BBC-SSB	54120M020	BOX DRILLING	HAYSTACK	20.00	1	20.00
PC	BBC-SSB	AER\SSB2	PC BOARD	PACLAB	40.00	1	40.00
MS	BBC-SSB	HAY45030	BOX WITH COVERS	PREC.MACHINE	43.60	1	43.60
MP2	BBC-SSB	JH-140	HYBRID	ANZAC	86.00	1	86.00
MP1	BBC-SSB	LMX-113	MIXER	MINICIRCUITS	14.95	2	29.90
U01	BBC-SSB	NE5539N	5539 OP AMP	SIGNETICS	2.50	10	25.00
R005	BBC-SSB	RCR05G101J	100 OHM 1/8W	AB	0.20	14	2.80

PARTS LIST FROM DBASE FILE:PARTS.DBF

REF	SUBMOD	PART	DESC	MFR	COST	QTY	TOTAL COST
R14	BBC-SSB	RCR05G102J	1K OHMS	AB	0.20	3	0.60
R003	BBC-SSB	RCR05G121J	120 OHM 1/8W	AB	0.20	16	3.20
R	BBC-SSB	RCR05G152J	1500 OHM 1/8W	AB	0.10	1	0.10
R15	BBC-SSB	RCR05G200J	20 OHMS 1/8W	AB	0.20	4	0.80
R001	BBC-SSB	RCR05G201J	200 OHM 1/8W	AB	0.20	14	2.80
R005	BBC-SSB	RCR05G391J	390 OHM 1/8W	AB	0.20	2	0.40
R	BBC-SSB	RCR05G430J	43 OHM 1/8W	AB	0.10	1	0.10
R007	BBC-SSB	RCR05G431J	430 OHM 1/8W	AB	0.20	2	0.40
R002	BBC-SSB	RCR05G471J	470 OHM 1/8W	AB	0.20	10	2.00
R004	BBC-SSB	RCR05G510J	51 OHM 1/8W	AB	0.20	3	0.60
R013	BBC-SSB	RN55D1780F	178 OHM 1%	CORNING	0.10	1	0.10
R012	BBC-SSB	RN55D1960F	196 OHM 1%	CORNING	0.10	1	0.10
R009	BBC-SSB	RN55D2000F	200 OHM 1%	CORNING	0.10	2	0.20
R010	BBC-SSB	RN55D2100F	210 OHM 1%	CORNING	0.10	2	0.20
R011	BBC-SSB	RN55D2150F	215 OHM 1%	CORNING	0.10	1	0.10
R008	BBC-SSB	RN55D2260F	226 OHM 1%	CORNING	0.10	1	0.10
*** Total ***							5103.72

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2500 A.D. 8051 Macro Assembler  -  Version 4.00h
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        Input  Filename : RAD3.asm
        Output Filename : RAD3.obj


 1  0000                          ORG     0000H       ; RESET VECTOR
 2  0000  02 01 70                LJMP    INIT        ;JUMP TO INIT
 3  0003                          ORG     0003H       ;JUMP TO THIS ADDRESS UPON MCB
 4  0003  02 C0 A8                LJMP    MCB
 5  0013                          ORG     0013H       ;JUMP TO THIS ADDRESS UPON 160 HZ
 6  0013  C0 D0                   PUSH    PSW
 7  0015  C0 E0                   PUSH    A
 8  0017  C2 8C                   CLR     8CH         ;STOP COUNTER 0
 9  0019  C2 8E                   CLR     8EH         ;STOP COUNTER 1
10  001B  85 8A 30                MOV     30H,8AH     ;MOVE COUNTER 0 LOW BYTE TO RAM
11  001E  85 8C 31                MOV     31H,8CH     ;MOVE COUNTER 0 HIGH BYTE TO RAM
12  0021  85 8B 32                MOV     32H,8BH     ;MOVE COUNTER 1 LOW BYTE TO RAM
13  0024  85 8D 33                MOV     33H,8DH     ;MOVE COUNTER 1 HIGH BYTE TO RAM
14  0027  75 8A 00                MOV     8AH,#00H    ;CLEAR COUNTERS
15  002A  75 8C 00                MOV     8CH,#00H
16  002D  75 8B 00                MOV     8BH,#00H
17  0030  75 8D 00                MOV     8DH,#00H
18  0033  D2 8C                   SETB    8CH         ;START COUNTER 0
19  0035  D2 8E                   SETB    8EH         ;START COUNTER 1
20  0037  30 A7 37                JNB     A7H,LAB1    ;IF FROM REF. JUMP TO LAB1
21  003A  E5 30                   MOV     A,30H       ;USB - ADD 16-BIT INTO 32-BIT
22  003C  25 34                   ADD     A,34H
23  003E  F5 34                   MOV     34H,A
24  0040  E5 31                   MOV     A,31H
25  0042  35 35                   ADDC    A,35H
26  0044  F5 35                   MOV     35H,A
27  0046  74 00                   MOV     A,#0
28  0048  35 36                   ADDC    A,36H
29  004A  F5 36                   MOV     36H,A
30  004C  74 00                   MOV     A,#0
31  004E  35 37                   ADDC    A,37H
32  0050  F5 37                   MOV     37H,A
33  0052  E5 32                   MOV     A,32H       ;REPEAT FOR LSB
 ;  0054  25 38                   ADD     A,38H
35  0056  F5 38                   MOV     38H,A
36  0058  E5 33                   MOV     A,33H
37  005A  35 39                   ADDC    A,39H
38  005C  F5 39                   MOV     39H,A
39  005E  74 00                   MOV     A,#0
40  0060  35 3A                   ADDC    A,3AH
41  0062  F5 3A                   MOV     3AH,A
42  0064  74 00                   MOV     A,#0
43  0066  35 3B                   ADDC    A,3BH
44  0068  F5 3B                   MOV     3BH,A
45  006A  C2 08                   CLR     8H          ;CLEAR DONE
46  006C  D0 E0                   POP     A
47  006E  D0 D0                   POP     PSW
48  0070  32                      RETI
```

```
 49  0071  E5 30          LAB1:   MOV     A,30H       ;USB - ADD 16-BIT INTO 32-BIT STORE FOR REF.
 50  0073  25 3C                  ADD     A,3CH
 51  0075  F5 3C                  MOV     3CH,A
 52  0077  E5 31                  MOV     A,31H
  3  0079  35 3D                  ADDC    A,3DH
 54  007B  F5 3D                  MOV     3DH,A
 55  007D  74 00                  MOV     A,#0
 56  007F  35 3E                  ADDC    A,3EH
 57  0081  F5 3E                  MOV     3EH,A
 58  0083  74 00                  MOV     A,#0
 59  0085  35 3F                  ADDC    A,3FH
 60  0087  F5 3F                  MOV     3FH,A
 61  0089  E5 32                  MOV     A,32H       ;LSB
 62  008B  25 40                  ADD     A,40H
 63  008D  F5 40                  MOV     40H,A
 64  008F  E5 33                  MOV     A,33H
 65  0091  35 41                  ADDC    A,41H
 66  0093  F5 41                  MOV     41H,A
 67  0095  74 00                  MOV     A,#0
 68  0097  35 42                  ADDC    A,42H
 69  0099  F5 42                  MOV     42H,A
 70  009B  74 00                  MOV     A,#0
 71  009D  35 43                  ADDC    A,43H
 72  009F  F5 43                  MOV     43H,A
 73  00A1  C2 08                  CLR     8H
 74  00A3  D0 E0                  POP     A
 75  00A5  D0 D0                  POP     PSW
 76  00A7  32                     RETI                ;RETURN TO BACKGROUND
 77  00A8  85 80 20       MCB:    MOV     20H,80H     ;READ MODE
 78  00AB  20 A4 60               JB      A4H,SWPW    ;IF RA3 JUMP TO SWPW
 79  00AE  30 0A 2F               JNB     AH,PREV1    ;JUMP IF PREVIOUS
 80  00B1  C2 A0                  CLR     A0H
 81  00B3  D2 A1                  SETB    A1H
 82  00B5  C2 A2                  CLR     A2H
 83  00B7  85 70 90               MOV     90H,70H
 84  00BA  C2 B6                  CLR     B6H
 85  00BC  D2 B6                  SETB    B6H
 86  00BE  D2 A0                  SETB    A0H
  7  00C0  85 71 90               MOV     90H,71H
 88  00C3  C2 B6                  CLR     B6H
 89  00C5  D2 B6                  SETB    B6H
 90  00C7  C2 A0                  CLR     A0H
 91  00C9  C2 A1                  CLR     A1H
 92  00CB  D2 A2                  SETB    A2H
 93  00CD  85 72 90               MOV     90H,72H
 94  00D0  C2 B6                  CLR     B6H
 95  00D2  D2 B6                  SETB    B6H
 96  00D4  D2 A0                  SETB    A0H
 97  00D6  85 73 90               MOV     90H,73H
 98  00D9  C2 B6                  CLR     B6H
 99  00DB  D2 B6                  SETB    B6H
100  00DD  02 01 6B               LJMP    ACK
101  00E0  C2 A0          PREV1:  CLR     A0H
102  00E2  D2 A1                  SETB    A1H
103  00E4  C2 A2                  CLR     A2H
104  00E6  85 60 90               MOV     90H,60H
105  00E9  C2 B6                  CLR     B6H
```

```
106   00EB   D2 B6              SETB    B6H
107   00ED   D2 A0              SETB    A0H
108   00EF   85 61 90           MOV     90H,61H
109   00F2   C2 B6              CLR     B6H
110   00F4   D2 B6              SETB    B6H
111   00F6   C2 A0              CLR     A0H
112   00F8   C2 A1              CLR     A1H
113   00FA   D2 A2              SETB    A2H
114   00FC   85 62 90           MOV     90H,62H
115   00FF   C2 B6              CLR     B6H
116   0101   D2 B6              SETB    B6H
117   0103   D2 A0              SETB    A0H
118   0105   85 63 90           MOV     90H,63H
119   0108   C2 B6              CLR     B6H
120   010A   D2 B6              SETB    B6H
121   010C   80 5D              SJMP    ACK
122   010E   30 0A 2E    SWPW:  JNB     AH,PREV2
123   0111   C2 A0              CLR     A0H         ;SIG-REF
124   0113   D2 A1              SETB    A1H
125   0115   C2 A2              CLR     A2H
126   0117   85 74 90           MOV     90H,74H
127   011A   C2 B6              CLR     B6H
128   011C   D2 B6              SETB    B6H
129   011E   D2 A0              SETB    A0H
130   0120   85 75 90           MOV     90H,75H
131   0123   C2 B6              CLR     B6H
132   0125   D2 B6              SETB    B6H
133   0127   C2 A0              CLR     A0H
134   0129   C2 A1              CLR     A1H
135   012B   D2 A2              SETB    A2H
136   012D   85 76 90           MOV     90H,76H
137   0130   C2 B6              CLR     B6H
138   0132   D2 B6              SETB    B6H
139   0134   D2 A0              SETB    A0H
140   0136   85 77 90           MOV     90H,77H
141   0139   C2 B6              CLR     B6H
142   013B   D2 B6              SETB    B6H
143   013D   80 2C              SJMP    ACK
144   013F   C2 A0      PREV2:  CLR     A0H
145   0141   D2 A1              SETB    A1H
146   0143   C2 A2              CLR     A2H
147   0145   85 64 90           MOV     90H,64H
148   0148   C2 B6              CLR     B6H
149   014A   D2 B6              SETB    B6H
150   014C   D2 A0              SETB    A0H
151   014E   85 65 90           MOV     90H,65H
152   0151   C2 B6              CLR     B6H
153   0153   D2 B6              SETB    B6H
154   0155   C2 A0              CLR     A0H
155   0157   C2 A1              CLR     A1H
156   0159   D2 A2              SETB    A2H
157   015B   85 66 90           MOV     90H,66H
158   015E   C2 B6              CLR     B6H
159   0160   D2 B6              SETB    B6H
160   0162   D2 A0              SETB    A0H
161   0164   85 67 90           MOV     90H,67H
162   0167   C2 B6              CLR     B6H
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163  0169  D2 B6              SETB    B6H
164  016B  C2 B7        ACK:  CLR     B7H         ;STROBE LOW
165  016D  D2 B7              SETB    B7H         ;RETURN TO HI STATE
166  016F  32                RETI
 57  0170  75 89 55    INIT: MOV     89H,#055H   ;CONFIGURE TIMER
168  0173  75 88 55          MOV     88H,#055H   ;START COUNTERS AND INTERRUPT EDGE DETECT
169  0176  75 B0 7F          MOV     B0H,#07FH   ;SET PORT 3 TO READ (EXCEPT P3.7)
170  0179  75 A0 FF          MOV     A0H,#0FFH   ;SET PORT 2 TO READ
171  017C  75 44 80          MOV     44H,#80H    ;DEFAULT VALUE -6 DB FROM MAX GAIN
172  017F  75 45 80          MOV     45H,#80H
173  0182  75 46 00          MOV     46H,#00H
174  0185  75 47 40          MOV     47H,#40H
175  0188  75 48 00          MOV     48H,#00H
176  018B  75 49 40          MOV     49H,#40H
177  018E  75 20 00          MOV     20H,#0      ;SET INITIAL MODE=0
178  0191  75 22 00          MOV     22H,#0
179  0194  75 B8 04          MOV     B8H,#04H    ;SET 160 HZ TO HIGH PRIORITY
180  0197  75 A8 85          MOV     A8H,#085H   ;ENABLE INTERRUPTS
181  019A  20 B0 02    START: JB      B0H,USB
182  019D  D2 B7              SETB    B7H         ;ENSURE ACH IS HIGH
183  019F  20 08 F8    USB:  JB      8H,START    ;JUMP IF DONE
184  01A2  20 A7 F5          JB      A7H,START   ;JUMP IF REF
185  01A5  A3                INC     DPTR        ;INC COUNT
186  01A6  D1 12              ACALL   TCHK        ;DO 1 SEC TICK CHECK
187  01A8  30 01 05           JNB     1H,LSB
188  01AB  20 11 02           JB      11H,LSB     ;JUMP UNLESS 0 GOES TO 1
189  01AE  51 5E              ACALL   READ1       ;ADJUST USB GAIN
190  01B0  30 02 05    LSB:  JNB     2H,STOR
191  01B3  20 12 02          JB      12H,STOR
192  01B6  51 73              ACALL   READ2       ;ADJUST LSB GAIN
193  01B8  E5 22        STOR: MOV     A,22H
194  01BA  85 20 22          MOV     22H,20H     ;STORE PREVIOUS MODE
195  01BD  B5 20 56          CJNE    A,20H,OUT   ;FORCE END OF AV FOR MODE CHANGE
196  01C0  E5 20             MOV     A,20H
197  01C2  54 70             ANL     A,#70H      ;MASK OUT PERIOD BITS
198  01C4  B4 00 06          CJNE    A,#0H,PER0
199  01C7  75 78 01          MOV     78H,#1      ;1/80 SEC
200  01CA  75 79 00          MOV     79H,#0
  1  01CD  B4 10 06    PER0: CJNE    A,#10H,PER1
202  01D0  75 78 50          MOV     78H,#80     ;1 SEC
203  01D3  75 79 00          MOV     79H,#0
204  01D5  B4 20 06    PER1: CJNE    A,#20H,PER2
205  01D9  75 78 A0          MOV     78H,#160    ;2 SEC
206  01DC  75 79 00          MOV     79H,#0
207  01DF  B4 30 06    PER2: CJNE    A,#30H,PER3
208  01E2  75 78 40          MOV     78H,#64     ;4 SEC
209  01E5  75 79 01          MOV     79H,#1
210  01E8  B4 40 06    PER3: CJNE    A,#40H,PER4
211  01EB  75 78 20          MOV     78H,#32     ;10 SEC
212  01EE  75 79 03          MOV     79H,#3
213  01F1  B4 50 06    PER4: CJNE    A,#50H,PER5
214  01F4  75 78 40          MOV     78H,#64     ;20 SEC
215  01F7  75 79 06          MOV     79H,#6
216  01FA  B4 60 06    PER5: CJNE    A,#60H,PER6
217  01FD  75 78 80          MOV     78H,#128    ;40 SEC
218  0200  75 79 0C          MOV     79H,#12
219  0203  B4 70 06    PER6: CJNE    A,#70H,PER7
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220  0206  75 78 C0          MOV     78H,#192    ;60 SEC
221  0209  75 79 12          MOV     79H,#18
222  020C  E5 82      PER7:   MOV     A,82H       ;DPL
223  020E  B5 78 48          CJNE    A,78H,DONE
  4  0211  E5 83              MOV     A,83H
225  0213  B5 79 43          CJNE    A,79H,DONE
226  0216  71 BF      OUT:    ACALL   SCALE
227  0218  85 70 60          MOV     60H,70H     ;COPY TO PREVIOUS
228  021B  85 71 61          MOV     61H,71H
229  021E  85 72 62          MOV     62H,72H
230  0221  85 73 63          MOV     63H,73H
231  0224  85 74 64          MOV     64H,74H
232  0227  85 75 65          MOV     65H,75H
233  022A  85 76 66          MOV     66H,76H
234  022D  85 77 67          MOV     67H,77H
235  0230  C2 0A              CLR     AH          ;SET FLAG TO PREVIOUS
236  0232  51 92              ACALL   SUMM        ;CALC. NEW AVERAGES
237  0234  D2 0A              SETB    AH          ;SET TO CURRENT
238  0236  30 00 02          JNB     0H,LABB
239  0239  71 E6              ACALL   REFCAL      ;AGC
240  023B  C2 A0      LABB:   CLR     A0H         ;SET ADDR TO 0 TO OUTPUT GAIN
241  023D  C2 A1              CLR     A1H
242  023F  C2 A2              CLR     A2H
243  0241  85 45 90          MOV     90H,45H
244  0244  C2 B6              CLR     B6H
245  0246  D2 B6              SETB    B6H         ;STROBE
246  0248  D2 A0              SETB    A0H         ;SET ADDR TO 1
247  024A  85 44 90          MOV     90H,44H     ;USB GAIN ON P1
248  024D  C2 B6              CLR     B6H
249  024F  D2 B6              SETB    B6H
250  0251  51 88              ACALL   CLRAM
251  0253  75 83 00          MOV     DPH,#0
252  0256  75 82 00          MOV     DPL,#0
253  0259  D2 08      DONE:   SETB    8H          ;DONE
254  025B  02 01 9A          LJMP    START       ;GO BACK TO START
255  025E  30 03 09   REFAD1: JNB     3H,L1AB1    ;JUMP TO L1AB1 IF BIT 3=0
256  0261  E5 44              MOV     A,44H
257  0263  B4 FF 01          CJNE    A,#FFH,L1AB2;CONTINUE IF 44H()FFH
  3  0266  22                RET
259  0267  05 44      L1AB2:  INC     44H         ;ADD 1 TO USB REF. GAIN
260  0269  22                RET
261  026A  E5 44      L1AB1:  MOV     A,44H
262  026C  B4 00 01          CJNE    A,#0,L1AB3
263  026F  22                RET
264  0270  15 44      L1AB3:  DEC     44H         ;SUBTRACT 1 FROM USB REF.
265  0272  22                RET
266  0273  30 03 09   REFAD2: JNB     3H,L2AB1
267  0276  E5 45              MOV     A,45H
268  0278  B4 FF 01          CJNE    A,#FFH,L2AB2
269  027B  22                RET
270  027C  05 45      L2AB2:  INC     45H         ;ADD1 TO LSB REF. GAIN
271  027E  22                RET
272  027F  E5 45      L2AB1:  MOV     A,45H
273  0281  B4 00 01          CJNE    A,#0,L2AB3
274  0284  22                RET
275  0285  15 45      L2AB3:  DEC     45H
276  0287  22                RET
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277  0288  7A 10        CLRAM:  MOV     R2,#10H     ;SUBROUTINE TO CLEAR ACCUMULATION
278  028A  79 33                MOV     R1,#33H
279  028C  09            LOOP1:  INC     R1
280  028D  77 00                 MOV     @R1,#0H
281  028F  DA FB                 DJNZ    R2,LOOP1
282  0291  22                    RET
283  0292  85 34 50      SUMM:   MOV     50H,34H     ;SUBROUTINE TO SUM SIG+REF
284  0295  85 35 51              MOV     51H,35H     ;AND NORMALIZE PUTTING OUTPUT
285  0298  85 36 52              MOV     52H,36H     ;IN 70H-77H
286  029B  85 37 53              MOV     53H,37H
287  029E  E5 50                 MOV     A,50H
288  02A0  25 3C                 ADD     A,3CH
289  02A2  F5 50                 MOV     50H,A
290  02A4  E5 51                 MOV     A,51H
291  02A6  35 3D                 ADDC    A,3DH
292  02A8  F5 51                 MOV     51H,A
293  02AA  E5 52                 MOV     A,52H
294  02AC  35 3E                 ADDC    A,3EH
295  02AE  F5 52                 MOV     52H,A
296  02B0  E5 53                 MOV     A,53H
297  02B2  35 3F                 ADDC    A,3FH
298  02B4  F5 53                 MOV     53H,A
299  02B6  85 4A 54              MOV     54H,4AH
300  02B9  85 4B 55              MOV     55H,4BH
301  02BC  85 4C 56              MOV     56H,4CH
302  02BF  85 4D 57              MOV     57H,4DH
303  02C2  91 57                 ACALL   MUL32       ;MULTIPLY BY SCALE FACTOR
304  02C4  85 5B 70              MOV     70H,5BH     ;USB SUM(S+R)*26*2**24/K /2**24
305  02C7  85 5C 71              MOV     71H,5CH
306  02CA  E5 5D                 MOV     A,5DH
307  02CC  70 0A                 JNZ     SUMA
308  02CE  E5 5E                 MOV     A,5EH
309  02D0  70 06                 JNZ     SUMA
310  02D2  E5 5F                 MOV     A,5FH
311  02D4  70 02                 JNZ     SUMA
312  02D6  80 06                 SJMP    SUMB
313  02D8  75 70 FF      SUMA:   MOV     70H,#FFH    ;IF OVERFLOW SET ALL ONES
314  02DB  75 71 FF              MOV     71H,#FFH
315  02DE  85 34 50      SUMB:   MOV     50H,34H
316  02E1  85 35 51              MOV     51H,35H
317  02E4  85 36 52              MOV     52H,36H
318  02E7  85 37 53              MOV     53H,37H
319  02EA  E5 50                 MOV     A,50H
320  02EC  C3                    CLR     C
321  02ED  95 3C                 SUBB    A,3CH
322  02EF  F5 50                 MOV     50H,A
323  02F1  E5 51                 MOV     A,51H
324  02F3  95 3D                 SUBB    A,3DH
325  02F5  F5 51                 MOV     51H,A
326  02F7  E5 52                 MOV     A,52H
327  02F9  95 3E                 SUBB    A,3EH
328  02FB  F5 52                 MOV     52H,A
329  02FD  E5 53                 MOV     A,53H
330  02FF  95 3F                 SUBB    A,3FH
331  0301  F5 53                 MOV     53H,A
332  0303  C2 09                 CLR     9H
333  0305  50 16                 JNC     SUM1        ;JUMP IF CARRY IS NOT SET
```

```
334  0307  D2 09              SETB    9H          ;SET SIGN FLAG
335  0309  E5 50              MOV     A,50H
336  030B  F4                 CPL     A
337  030C  F5 50              MOV     50H,A
338  030E  E5 51              MOV     A,51H
339  0310  F4                 CPL     A
340  0311  F5 51              MOV     51H,A
341  0313  E5 52              MOV     A,52H
342  0315  F4                 CPL     A
343  0316  F5 52              MOV     52H,A
344  0318  E5 53              MOV     A,53H
345  031A  F4                 CPL     A
346  031B  F5 53              MOV     53H,A
347  031D  91 57        SUM1: ACALL   MUL32
348  031F  85 5B 74           MOV     74H,5BH
349  0322  85 5C 75           MOV     75H,5CH
350  0325  30 09 06           JNB     9H,SUM2     ;JUMP IF CARRY IS NOT SET
351  0328  E5 75              MOV     A,75H
352  032A  24 80              ADD     A,#80H      ;SET MSB TO INDICATE -VE SIGN
353  032C  F5 75              MOV     75H,A
354  032E  85 38 50     SUM2: MOV     50H,38H     ;REPEAT FOR LOWER SB
355  0331  85 39 51           MOV     51H,39H
356  0334  85 3A 52           MOV     52H,3AH
357  0337  85 3B 53           MOV     53H,3BH
358  033A  E5 50              MOV     A,50H
359  033C  25 40              ADD     A,40H
360  033E  F5 50              MOV     50H,A
361  0340  E5 51              MOV     A,51H
362  0342  35 41              ADDC    A,41H
363  0344  F5 51              MOV     51H,A
364  0346  E5 52              MOV     A,52H
365  0348  35 42              ADDC    A,42H
366  034A  F5 52              MOV     52H,A
367  034C  E5 53              MOV     A,53H
368  034E  35 43              ADDC    A,43H
369  0350  F5 53              MOV     53H,A
370  0352  91 57              ACALL   MUL32
371  0354  85 5B 72           MOV     72H,5BH
372  0357  85 5C 73           MOV     73H,5CH
373  035A  E5 5D              MOV     A,5DH
374  035C  70 0A              JNZ     SUMC
375  035E  E5 5E              MOV     A,5EH
376  0360  70 06              JNZ     SUMC
377  0362  E5 5F              MOV     A,5FH
378  0364  70 02              JNZ     SUMC
379  0366  80 06              SJMP    SUMD
380  0368  75 72 FF     SUMC: MOV     72H,#FFH
381  036B  75 73 FF           MOV     73H,#FFH
382  036E  85 38 50     SUMD: MOV     50H,38H
383  0371  85 39 51           MOV     51H,39H
384  0374  85 3A 52           MOV     52H,3AH
385  0377  85 3B 53           MOV     53H,3BH
386  037A  E5 50              MOV     A,50H
387  037C  C3                 CLR     C
388  037D  95 40              SUBB    A,40H
389  037F  F5 50              MOV     50H,A
390  0381  E5 51              MOV     A,51H
```

```
391  0383  95 41              SUBB    A,41H
392  0385  F5 51              MOV     51H,A
393  0387  E5 52              MOV     A,52H
394  0389  95 42              SUBB    A,42H
395  038B  F5 52              MOV     52H,A
396  038D  E5 53              MOV     A,53H
397  038F  95 43              SUBB    A,43H
398  0391  F5 53              MOV     53H,A
399  0393  C2 09              CLR     9H
400  0395  50 16              JNC     SUM3
401  0397  D2 09              SETB    9H
402  0399  E5 50              MOV     A,50H
403  039B  F4                 CPL     A
404  039C  F5 50              MOV     50H,A
405  039E  E5 51              MOV     A,51H
406  03A0  F4                 CPL     A
407  03A1  F5 51              MOV     51H,A
408  03A3  E5 52              MOV     A,52H
409  03A5  F4                 CPL     A
410  03A6  F5 52              MOV     52H,A
411  03A8  E5 53              MOV     A,53H
412  03AA  F4                 CPL     A
413  03AB  F5 53              MOV     53H,A
414  03AD  91 57        SUM3: ACALL   MUL32
415  03AF  85 58 76           MOV     76H,58H
416  03B2  85 5C 77           MOV     77H,5CH
417  03B5  30 09 06           JNB     9H,SUM4
418  03B8  E5 77              MOV     A,77H
419  03BA  24 80              ADD     A,#80H
420  03BC  F5 77              MOV     77H,A
421  03BE  22           SUM4: RET
422  03BF  75 50 00     SCALE: MOV     50H,#0
423  03C2  75 51 00            MOV     51H,#0
424  03C5  75 52 00            MOV     52H,#0
425  03C8  75 53 1A            MOV     53H,#26     ;PUT 26*2**24 IN NUMERATOR
426  03CB  85 82 54            MOV     54H,DPL     ;80 HZ COUNT INTO DENOMINATOR
427  03CE  85 83 55            MOV     55H,DPH
428  03D1  75 56 00            MOV     56H,#0
429  03D4  75 57 00            MOV     57H,#0
430  03D7  B1 B9               ACALL   DIV32
431  03D9  85 58 4A            MOV     4AH,58H     ;MOVE 4 LOW ORDER BYTES
432  03DC  85 59 4B            MOV     4BH,59H
433  03DF  85 5A 4C            MOV     4CH,5AH
434  03E2  85 5B 4D            MOV     4DH,5BH
435  03E5  22                  RET
436  03E6  E5 44        REFCAL: MOV     A,44H
437  03E8  C3                  CLR     C
438  03E9  13                  RRC     A           ;GAIN/2
439  03EA  70 01               JNZ     REFCA
440  03EC  04                  INC     A           ;ADD 1 IF ZERO
441  03ED  F5 F0        REFCA: MOV     B,A
442  03EF  E5 71               MOV     A,71H
443  03F1  84                  DIV     AB          ;POWER*2/G
444  03F2  B4 FF 01            CJNE    A,#FFH,REFCB
445  03F5  14                  DEC     A
446  03F6  04           REFCB: INC     A           ;ADD ONE
447  03F7  F5 50               MOV     50H,A
```

```
448   03F9  C3                        CLR     C
449   03FA  E5 46                     MOV     A,46H
450   03FC  95 70                     SUBB    A,70H
451   03FE  E5 47                     MOV     A,47H
 52   0400  95 71                     SUBB    A,71H       ;TAKE REF - POWER
453   0402  40 0C                     JC      REFC1
454   0404  85 50 F0                  MOV     B,50H
455   0407  84                        DIV     AB          ;[R-P]/([P]/((G/2)+1)
456   0408  25 44                     ADD     A,44H       ;POWER(REF
457   040A  50 10                     JNC     REFC2       ;DONE IF CARRY NOT SET
458   040C  74 FF                     MOV     A,#FFH      ;MUST HAVE OVERFLOWED SET ALL ONES
459   040E  80 0C                     SJMP    REFC2
460   0410  F4              REFC1:    CPL     A           ;MAKE POSITIVE
461   0411  85 50 F0                  MOV     B,50H
462   0414  84                        DIV     AB
463   0415  F4                        CPL     A           ;MAKE NEGATIVE
464   0416  25 44                     ADD     A,44H       ;POWER)REF
465   0418  40 02                     JC      REFC2       ;DONE IF CARRY SET
466   041A  74 00                     MOV     A,#0        ;UNDERFLOW SET TO ZERO
467   041C  F5 44           REFC2:    MOV     44H,A
468   041E  E5 45                     MOV     A,45H
469   0420  C3                        CLR     C
470   0421  13                        RRC     A
471   0422  70 01                     JNZ     REFCC
472   0424  04                        INC     A
473   0425  F5 F0           REFCC:    MOV     B,A
474   0427  E5 73                     MOV     A,73H
475   0429  84                        DIV     AB
476   042A  B4 FF 01                  CJNE    A,#FFH,REFCD
477   042D  14                        DEC     A
478   042E  04              REFCD:    INC     A
479   042F  F5 50                     MOV     50H,A
480   0431  C3                        CLR     C
481   0432  E5 48                     MOV     A,48H
482   0434  95 72                     SUBB    A,72H
483   0436  E5 49                     MOV     A,49H
484   0438  95 73                     SUBB    A,73H
485   043A  40 0C                     JC      REFC3
  6   043C  85 50 F0                  MOV     B,50H
 37   043F  84                        DIV     AB
488   0440  25 45                     ADD     A,45H
489   0442  50 10                     JNC     REFC4
490   0444  74 FF                     MOV     A,#FFH
491   0446  80 0C                     SJMP    REFC4
492   0448  F4              REFC3:    CPL     A
493   0449  85 50 F0                  MOV     B,50H
494   044C  84                        DIV     AB
495   044D  F4                        CPL     A
496   044E  25 45                     ADD     A,45H
497   0450  40 02                     JC      REFC4
498   0452  74 00                     MOV     A,#0
499   0454  F5 45           REFC4:    MOV     45H,A
500   0456  22                        RET
501   0457  75 5A 00        MUL32:    MOV     5AH,#0
502   045A  75 5B 00                  MOV     5BH,#0
503   045D  75 5C 00                  MOV     5CH,#0
504   0460  75 5D 00                  MOV     5DH,#0
```

```
505   0463   75 5E 00          MOV     5EH,#0
506   0466   75 5F 00          MOV     5FH,#0
507   0469   E5 50             MOV     A,50H
508   046B   85 54 F0          MOV     B,54H
509   046E   A4                MUL     AB
510   046F   F5 58             MOV     58H,A       ;MOVE DIRECTLY TO C
511   0471   85 F0 59          MOV     59H,B
512   0474   E5 50             MOV     A,50H
513   0476   85 55 F0          MOV     B,55H
514   0479   A4                MUL     AB
515   047A   25 59             ADD     A,59H       ;ADD IN PARTIAL PRODUCT
516   047C   F5 59             MOV     59H,A
517   047E   E5 F0             MOV     A,B
518   0480   35 5A             ADDC    A,5AH       ;ADD AND CARRY INTO 5A
519   0482   F5 5A             MOV     5AH,A
520   0484   E5 5B             MOV     A,5BH
521   0486   34 00             ADDC    A,#0
522   0488   F5 5B             MOV     5BH,A
523   048A   E5 51             MOV     A,51H
524   048C   85 54 F0          MOV     B,54H
525   048F   A4                MUL     AB
526   0490   25 59             ADD     A,59H
527   0492   F5 59             MOV     59H,A
528   0494   E5 F0             MOV     A,B
529   0496   35 5A             ADDC    A,5AH
530   0498   F5 5A             MOV     5AH,A
531   049A   E5 5B             MOV     A,5BH
532   049C   34 00             ADDC    A,#0
533   049E   F5 5B             MOV     5BH,A       ;GETS CARRY INTO 5B
534   04A0   E5 50             MOV     A,50H
535   04A2   85 56 F0          MOV     B,56H
536   04A5   A4                MUL     AB
537   04A6   25 5A             ADD     A,5AH
538   04A8   F5 5A             MOV     5AH,A
539   04AA   E5 F0             MOV     A,B
540   04AC   35 5B             ADDC    A,5BH
541   04AE   F5 5B             MOV     5BH,A
542   04B0   E5 5C             MOV     A,5CH
543   04B2   34 00             ADDC    A,#0
544   04B4   F5 5C             MOV     5CH,A
545   04B6   E5 51             MOV     A,51H
546   04B8   85 55 F0          MOV     B,55H
547   04BB   A4                MUL     AB
548   04BC   25 5A             ADD     A,5AH
549   04BE   F5 5A             MOV     5AH,A
550   04C0   E5 F0             MOV     A,B
551   04C2   35 5B             ADDC    A,5BH
552   04C4   F5 5B             MOV     5BH,A
553   04C6   E5 5C             MOV     A,5CH
554   04C8   34 00             ADDC    A,#0
555   04CA   F5 5C             MOV     5CH,A
556   04CC   E5 52             MOV     A,52H
557   04CE   85 54 F0          MOV     B,54H
558   04D1   A4                MUL     AB
559   04D2   25 5A             ADD     A,5AH
560   04D4   F5 5A             MOV     5AH,A
561   04D6   E5 F0             MOV     A,B
```

```
562   04D8   35 5B          ADDC    A,5BH
563   04DA   F5 5B          MOV     5BH,A
564   04DC   E5 5C          MOV     A,5CH
565   04DE   34 00          ADDC    A,#0
566   04E0   F5 5C          MOV     5CH,A
567   04E2   E5 50          MOV     A,50H
568   04E4   85 57 F0       MOV     B,57H
569   04E7   A4             MUL     AB
570   04E8   25 5B          ADD     A,5BH
571   04EA   F5 5B          MOV     5BH,A
572   04EC   E5 F0          MOV     A,B
573   04EE   35 5C          ADDC    A,5CH
574   04F0   F5 5C          MOV     5CH,A
575   04F2   E5 5D          MOV     A,5DH
576   04F4   34 00          ADDC    A,#0
577   04F6   F5 5D          MOV     5DH,A
578   04F8   E5 51          MOV     A,51H
579   04FA   85 56 F0       MOV     B,56H
580   04FD   A4             MUL     AB
581   04FE   25 5B          ADD     A,5BH
582   0500   F5 5B          MOV     5BH,A
583   0502   E5 F0          MOV     A,B
584   0504   35 5C          ADDC    A,5CH
585   0506   F5 5C          MOV     5CH,A
586   0508   E5 5D          MOV     A,5DH
587   050A   34 00          ADDC    A,#0
588   050C   F5 5D          MOV     5DH,A
589   050E   E5 52          MOV     A,52H
590   0510   85 55 F0       MOV     B,55H
591   0513   A4             MUL     AB
592   0514   25 5B          ADD     A,5BH
593   0516   F5 5B          MOV     5BH,A
594   0518   E5 F0          MOV     A,B
595   051A   35 5C          ADDC    A,5CH
596   051C   F5 5C          MOV     5CH,A
597   051E   E5 5D          MOV     A,5DH
598   0520   34 00          ADDC    A,#0
599   0522   F5 5D          MOV     5DH,A
600   0524   E5 53          MOV     A,53H
601   0526   85 54 F0       MOV     B,54H
602   0529   A4             MUL     AB
603   052A   25 5B          ADD     A,5BH
604   052C   F5 5B          MOV     5BH,A
605   052E   E5 F0          MOV     A,B
606   0530   35 5C          ADDC    A,5CH
607   0532   F5 5C          MOV     5CH,A
608   0534   E5 5D          MOV     A,5DH
609   0536   34 00          ADDC    A,#0
610   0538   F5 5D          MOV     5DH,A
611   053A   E5 51          MOV     A,51H
612   053C   85 57 F0       MOV     B,57H
613   053F   A4             MUL     AB
614   0540   25 5C          ADD     A,5CH
615   0542   F5 5C          MOV     5CH,A
616   0544   E5 F0          MOV     A,B
617   0546   35 5D          ADDC    A,5DH
618   0548   F5 5D          MOV     5DH,A
```

```
619  054A  E5 5E              MOV     A,5EH
620  054C  34 00              ADDC    A,#0
621  054E  F5 5E              MOV     5EH,A
622  0550  E5 52              MOV     A,52H
623  0552  85 56 F0           MOV     B,56H
624  0555  A4                 MUL     AB
625  0556  25 5C              ADD     A,5CH
626  0558  F5 5C              MOV     5CH,A
627  055A  E5 F0              MOV     A,B
628  055C  35 5D              ADDC    A,5DH
629  055E  F5 5D              MOV     5DH,A
630  0560  E5 5E              MOV     A,5EH
631  0562  34 00              ADDC    A,#0
632  0564  F5 5E              MOV     5EH,A
633  0566  E5 53              MOV     A,53H
634  0568  85 55 F0           MOV     B,55H
635  056B  A4                 MUL     AB
636  056C  25 5C              ADD     A,5CH
637  056E  F5 5C              MOV     5CH,A
638  0570  E5 F0              MOV     A,B
639  0572  35 5D              ADDC    A,5DH
640  0574  F5 5D              MOV     5DH,A
641  0576  E5 5E              MOV     A,5EH
642  0578  34 00              ADDC    A,#0
643  057A  F5 5E              MOV     5EH,A
644  057C  E5 52              MOV     A,52H
645  057E  85 57 F0           MOV     B,57H
646  0581  A4                 MUL     AB
647  0582  25 5D              ADD     A,5DH
648  0584  F5 5D              MOV     5DH,A
649  0586  E5 F0              MOV     A,B
650  0588  35 5E              ADDC    A,5EH
651  058A  F5 5E              MOV     5EH,A
652  058C  E5 5F              MOV     A,5FH
653  058E  34 00              ADDC    A,#0
654  0590  F5 5F              MOV     5FH,A
655  0592  E5 53              MOV     A,53H
656  0594  85 56 F0           MOV     B,56H
657  0597  A4                 MUL     AB
658  0598  25 5D              ADD     A,5DH
659  059A  F5 5D              MOV     5DH,A
660  059C  E5 F0              MOV     A,B
661  059E  35 5E              ADDC    A,5EH
662  05A0  F5 5E              MOV     5EH,A
663  05A2  E5 5F              MOV     A,5FH
664  05A4  34 00              ADDC    A,#0
665  05A6  F5 5F              MOV     5FH,A
666  05A8  E5 53              MOV     A,53H
667  05AA  85 57 F0           MOV     B,57H
668  05AD  A4                 MUL     AB
669  05AE  25 5E              ADD     A,5EH
670  05B0  F5 5E              MOV     5EH,A
671  05B2  E5 F0              MOV     A,B
672  05B4  35 5F              ADDC    A,5FH
673  05B6  F5 5F              MOV     5FH,A
674  05B8  22                 RET
675  05B9  75 58 00   DIV32:  MOV     58H,#0
```

```
676   05BC   75 59 00            MOV     59H,#0
677   05BF   7A 20                MOV     R2,#32
678   05C1   E5 50        LSHFT:  MOV     A,50H
679   05C3   25 50                ADD     A,50H
680   05C5   F5 50                MOV     50H,A
681   05C7   E5 51                MOV     A,51H
682   05C9   35 51                ADDC    A,51H
683   05CB   F5 51                MOV     51H,A
684   05CD   E5 52                MOV     A,52H
685   05CF   35 52                ADDC    A,52H
686   05D1   F5 52                MOV     52H,A
687   05D3   E5 53                MOV     A,53H
688   05D5   35 53                ADDC    A,53H
689   05D7   F5 53                MOV     53H,A
690   05D9   E5 58                MOV     A,58H
691   05DB   35 58                ADDC    A,58H
692   05DD   F5 58                MOV     58H,A
693   05DF   E5 59                MOV     A,59H
694   05E1   35 59                ADDC    A,59H
695   05E3   F5 59                MOV     59H,A
696   05E5   E5 58                MOV     A,58H       ;SUBTRACT 15 BIT DIVISOR
697   05E7   95 54                SUBB    A,54H
698   05E9   F5 58                MOV     58H,A
699   05EB   E5 59                MOV     A,59H
700   05ED   95 55                SUBB    A,55H
701   05EF   F5 59                MOV     59H,A
702   05F1   05 50                INC     50H         ;ADD 1 TO QUOTIENT
703   05F3   50 0E                JNC     NEXT        ;JUMP TO NEXT IF CARRY NOT SET
704   05F5   E5 58                MOV     A,58H       ;ADD DIVISOR BACK IN
705   05F7   25 54                ADD     A,54H
706   05F9   F5 58                MOV     58H,A
707   05FB   E5 59                MOV     A,59H
708   05FD   35 55                ADDC    A,55H
709   05FF   F5 59                MOV     59H,A
710   0601   15 50                DEC     50H         ;SUBTRACT 1 FROM QUOTIENT
711   0603   DA BC        NEXT:   DJNZ    R2,LSHFT
712   0605   85 50 58            MOV     58H,50H
713   0608   85 51 59            MOV     59H,51H
714   060B   85 52 5A            MOV     5AH,52H
715   060E   85 53 5B            MOV     5BH,53H
716   0611   22                  RET
717   0612   05 7A        TCHK:  INC     7AH         ;ROUTINE TO CHECK 1 SEC
718   0614   30 A3 0A            JNB     A3H,TIC1    ;JUMP TO TIC1 WHEN TICK ABSENT
719   0617   E5 7A                MOV     A,7AH
720   0619   B4 80 02            CJNE    A,#80,TIC2
721   061C   D2 A5                SETB    A5H         ;TICK O.K.
722   061E   75 7A 00      TIC2:  MOV     7AH,#0      ;RESET COUNTER
723   0621   E5 7A        TIC1:  MOV     A,7AH
724   0623   B4 81 05            CJNE    A,#81,TIC3
725   0626   C2 A5                CLR     A5H         ;TICK NOT O.K.
726   0628   75 7A 00            MOV     7AH,#0
727   062B   22          TIC3:   RET
728   062C                        END
729   062C                        END
```

Defined	Symbol Name	Value	References			
164	ACK	016B	100	121	143	
Pre	BSECT	0000				
277	CLRAM	0288	250			
Pre	CODE	0013	1	3	5	
?e	DATA	0000				
/5	DIV32	0559	430			
253	DONE	0259	223	225		
167	INIT	0170	2			
261	L1AB1	026A	255			
259	L1AB2	0267	257			
264	L1AB3	0270	262			
272	L2AB1	027F	266			
270	L2AB2	027C	268			
275	L2AB3	0285	273			
49	LAB1	0071	20			
240	LABB	023B	238			
279	LOOP1	028C	281			
190	LSB	01B0	187	188		
678	LSHFT	05C1	711			
77	MCB	00A8	4			
501	MUL32	0457	303	347	370	414
711	NEXT	0603	703			
225	OUT	0216	195			
201	PER0	01CD	198			
204	PER1	01D6	201			
207	PER2	01DF	204			
210	PER3	01E8	207			
213	PER4	01F1	210			
216	PER5	01FA	213			
219	PER6	0203	216			
222	PER7	020C	219			
101	PREV1	00E0	79			
144	PREV2	013F	122			
255	REFAD1	025E	189			
266	REFAD2	0273	192			
460	REFC1	0410	453			
467	REFC2	041C	457	459	465	
492	REFC3	0448	485			
?9	REFC4	0454	489	491	497	
1	REFCA	03ED	439			
436	REFCAL	03E6	239			
446	REFCB	03F6	444			
473	REFCC	0425	471			
478	REFCD	042E	476			
Pre	RSECT	0000				
422	SCALE	03BF	226			
181	START	019A	183	184	254	
193	STOR	01B8	190	191		
347	SUM1	031D	333			
354	SUM2	033E	350			
414	SUM3	03AD	400			
421	SUM4	03BE	417			
313	SUMA	02D8	307	309	311	
315	SUMB	02DE	312			
380	SUMC	0368	374	376	378	
382	SUMD	036E	379			

Defined	Symbol Name	Value	References
283	SUMM	0292	236
122	SWPW	010E	79
717	TCHK	0612	186
723	TIC1	0621	718
722	TIC2	061E	720
727	TIC3	062B	724
183	USB	019F	181

Lines Assembled : 728 Assembly Errors : 0

MANUFACTURERS' DATA SHEETS

MOTOROLA

MC12040/ MC12540

PHASE-FREQUENCY DETECTOR

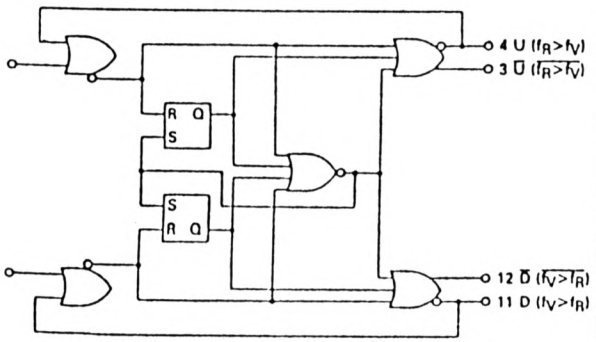
The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

P SUFFIX
PLASTIC PACKAGE
CASE 646

L SUFFIX
CERAMIC PACKAGE
CASE 632-02

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

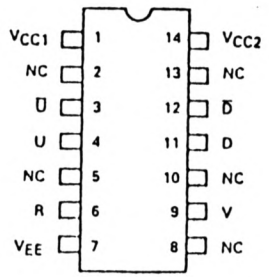
TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

INPUT		OUTPUT			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = Don't Care

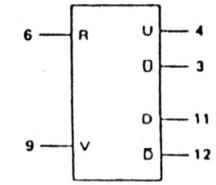
PIN ASSIGNMENT



NC — No Connection

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to −2.0 V for −5.2 V tests.



Supply Voltage = −5.2 V

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	MC12040 0°C Max	MC12040 25°C Min	MC12040 25°C Max	MC12040 +75°C Min	MC12040 +75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	-	-	-120	-60	-	-	mAdc					7	1,14
Input Current	I_{INH}	6 9	- -	- -	- -	350 350	- -	- -	μAdc μAdc	6 9	-	-	-	7 7	1,14 1,14
Logic "1" Output Voltage	V_{OH} ①	3 4 11 12	-1.000 - - -	-0.840 - - -	-0.960 - - -	-0.810 - - -	-0.900 - - -	-0.720 - - -	Vdc	- - - -	- - - -	- - - -	- - - -	7	1,14
Logic "0" Output Voltage	V_{OL} ①	3 4 11 12	-1.870 - - -	-1.635 - - -	-1.850 - - -	-1.620 - - -	-1.830 - - -	-1.595 - - -	Vdc	- - - -	- - - -	- - - -	- - - -	7	1,14
Logic "1" Threshold Voltage	V_{OHA} ②	3 4 11 12	-1.020 - - -	- - - -	-0.980 - - -	- - - -	-0.920 - - -	- - - -	Vdc	- -	-	6,9 -	-	7	1,14
Logic "0" Threshold Voltage	V_{OLA} ②	3 4 11 12	- - - -	-1.615 - - -	- - - -	-1.600 - - -	- - - -	-1.575 - - -	Vdc	- - - -	- - - -	9 6 9 6	6 9 6 9	7	1,14

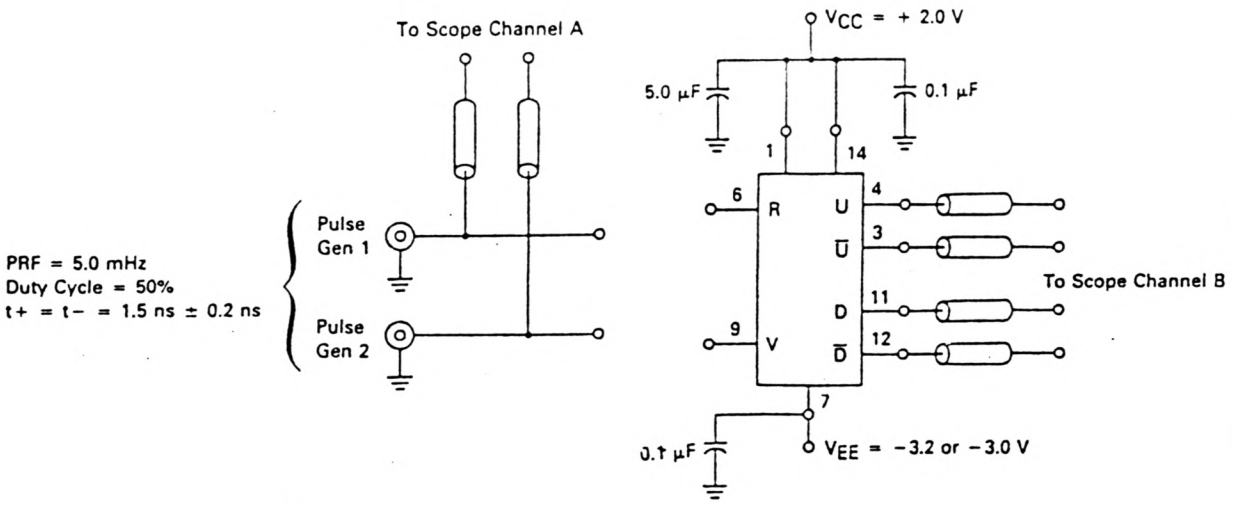
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Supply Voltage = +5.0 V

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	MC12040 0°C Max	MC12040 25°C Min	MC12040 25°C Max	MC12040 +75°C Min	MC12040 +75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7			-115	-60			mAdc					1,14	7
Input Current	I_{INH}	6 9				350 350			μAdc μAdc	6 9				1,14 1,14	7 7
Logic "1" Output Voltage	V_{OH} ①	3 4 11 12	4.000 - - -	4.160 - - -	4.040 - - -	4.180 - - -	4.100 - - -	4.280 - - -	Vdc					1,14	7
Logic "0" Output Voltage	V_{OL} ①	3 4 11 12	3.190 - - -	3.430 - - -	3.210 - - -	3.440 - - -	3.230 - - -	3.470 - - -	Vdc					1,14	7
Logic "1" Threshold Voltage	V_{OHA} ②	3 4 11 12	3.980 - - -	- - - -	4.020 - - -	- - - -	4.080 - - -	- - - -	Vdc			6,9		1,14	7
Logic "0" Threshold Voltage	V_{OLA} ②	3 4 11 12	- - - -	3.450 - - -	- - - -	3.460 - - -	- - - -	3.490 - - -	Vdc			9 6 9 6	6 9 6 9	1,14	7

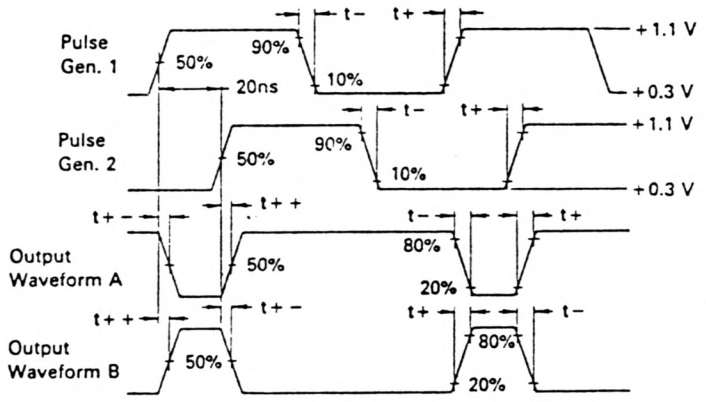
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12540 −55°C Max	MC12540 +25°C Max	MC12540 +125°C Max	MC12040 0°C Max	MC12040 +25°C Max	MC12040 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	VEE −3.0 or −3.2 V	VCC +2.0 V
Propagation Delay	t_{6+4+}	6,4	B	4.6	4.6	5.6	4.6	4.6	5.0	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	6.0	6.0	7.2	6.0	6.0	6.6		9	6		
	t_{6+3-}	6,3	A	4.5	4.5	5.5	4.5	4.5	4.9		6	9		
	t_{6+11-}	6,11	B	6.4	6.4	7.7	6.4	6.4	7.0		9	6		
	t_{9+11+}	9,11	B	4.6	4.6	5.6	4.6	4.6	5.0		9	6		
	t_{9+3+}	9,3	A	6.0	6.0	7.2	6.0	6.0	6.6		6	9		
	t_{9+12-}	9,12	A	4.5	4.5	5.5	4.5	4.5	4.9		9	6		
	t_{9+4-}	9,4	B	7.4	6.4	7.7	6.4	6.4	7.0		6	9		
Output Rise Time	t_{3+}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4+}	4	B								6	9		
	t_{11+}	11	B								9	6		
	t_{12+}	12	A								9	6		
Output Fall Time	t_{3-}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4-}	4	B								6	9		
	t_{11-}	11	B								9	6		
	t_{12-}	12	A								9	6		

DMOS FET Quad Analog Switch Arrays

designed for Military and Industrial Applications . . .

Siliconix

FEATURES

- Low "ON" Resistance
- Low Input Capacitance
- Low Output Capacitance
- Low Feedback Capacitance
- High Channel-to-Channel Isolation

BENEFITS

- "OFF Isolation of −107 dB
- Low Insertion Loss
- Glitch Free Signals
- Fast Switching

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- Choppers
- Crosspoint Switches

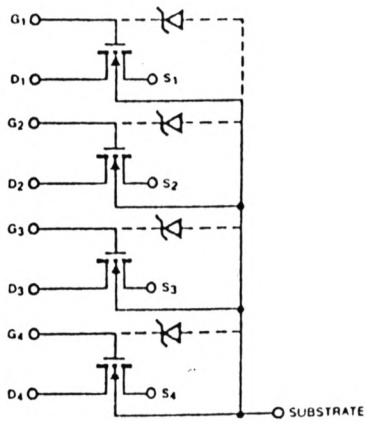
DESCRIPTION

The Siliconix SD5000 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video, and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5000 is rated for analog signals of ±10 V, while the SD5001 and SD5002 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and ON resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

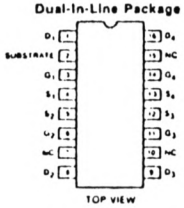
The SD5000 family is available in 16-pin plastic and side braze dual-in-line packages, and is rated for operation over the −55° to 125°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



Order Part Numbers:
SD5000I, SD5001I, SD5002I
Plastic
SD5000N, SD5001N, SD5002N
Ceramic
See Section 8

SD5000/SD5001/SD5002

ABSOLUTE MAXIMUM RATINGS

	SD5000	SD5001	SD5002
V_{DS}	20 V	10 V	15 V
V_{SD}[1]	20 V	10 V	15 V
V_{DB}	25 V	15 V	22.5 V
V_{SB}	25 V	15 V	22.5 V
V_{GS}	30/−25 V	25/−15 V	30/−22.5 V
V_{GB}	30/−0.3 V	25/−0.3 V	30/−0.3 V
V_{GD}	30/−25 V	25/−15 V	30/−22.5 V

I_D ..... 50 mA
Operating Temperature ..... −55° to +125°C
Storage Temperature ..... −55 to 150°C
Power Dissipation (Package)[2] ..... 640 mW
(Each Device) ..... 300 mW

ELECTRICAL CHARACTERISTICS[3]

T_A = 25°C

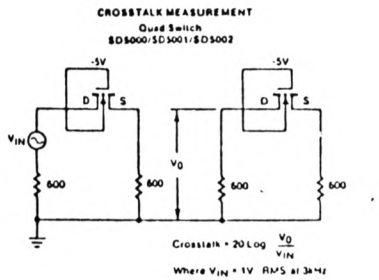
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:		SD5000 MIN[4]	SD5000 TYP[5]	SD5000 MAX	SD5001 MIN[4]	SD5001 TYP[5]	SD5001 MAX	SD5002 MIN[4]	SD5002 TYP[5]	SD5002 MAX	UNIT
Analog Signal Range	V_{ANALOG}			-10		10	-5		5	-7.5		7.5	V
Drain-Source Breakdown Voltage	BV_{DS}	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		20	25		10	25		15	25		V
Source-Drain Breakdown Voltage	BV_{SD}	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		20			10			15			V
Drain-Substrate Breakdown Voltage	BV_{DB}	$V_{GB} = 0$ V, $I_D = 10$ nA, Source Open		25			15			22.5			V
Source-Substrate Breakdown Voltage	BV_{SB}	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain Open		25			15			≤22.5			V
Drain-Source Leakage Current	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 20$ V		1	10							nA
			$V_{DS} = 10$ V					1	10				nA
			$V_{DS} = 15$ V								1	10	nA
Source-Drain Leakage Current	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 20$ V		1	10							nA
			$V_{SD} = 10$ V					1	10				nA
			$V_{SD} = 15$ V								1	10	nA
Gate Leakage Current	I_{GBS}	$V_{DB} = V_{SB} = 0$ V	$V_{GB} = 30$ V		1								µA
			$V_{GB} = 25$ V						1				µA
			$V_{GB} = 30$ V									1	µA
Threshold Voltage	V_T	$V_{DS} = V_{GS} = V_T$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
Drain-Source ON Resistance	$r_{DS(on)}$	$I_D = 1$ mA, $V_{SB} = 0$ V	$V_{GS} = 5$ V		50	70		50	70		50	70	Ω
			$V_{GS} = 10$ V		30			30			30		Ω
			$V_{GS} = 15$ V		23			23			23		Ω
			$V_{GS} = 20$ V		19			19			19		Ω
Resistance Match[6]	$r_{DS(on)}$	I_D 1 mA, V_{SB} = 0 V, V_{GS} = 5 V			1	5		1	5		1	5	Ω
Forward Transconductance	g_{fs}	V_{DS} 10 V, I_D 20 mA, V_{SB} 0 V, f 1 kHz		10	15		10	15		10	15		mS[7]
Gate Node Capacitance	C_G	V_{DS} = 10 V, V_{GS} = V_{BS} = −15 V, f = 1 MHz, See Capacitance Model Figure 1			24	35		24	35		24	35	pF
Drain Node Capacitance	C_D				13	16		13	16		13	16	pF
Source Node Capacitance	C_S				35	5		35	5		35	5	pF
Reverse Transfer Capacitance	C_{DG}				0.3	5		0.3	5		0.3	5	pF
Crosstalk		See Test Circuits 1 and 2, f = 3 kHz			-107			107			107		dB

DMCAI

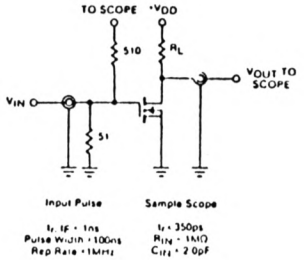
NOTES:

1. Refer to test conditions specified in Electrical Characteristics Tables
2. Derate 5 mW/°C above 25°C
3. Refer to PROCESS OPTION FLOWCHART for additional information
4. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet
5. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
6. This untested parameter is guaranteed by design
7. 1 mS = 1 m-mho (Ω)

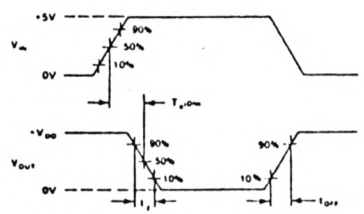
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS

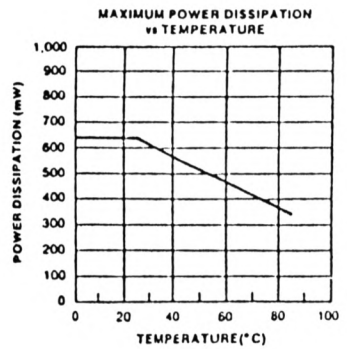


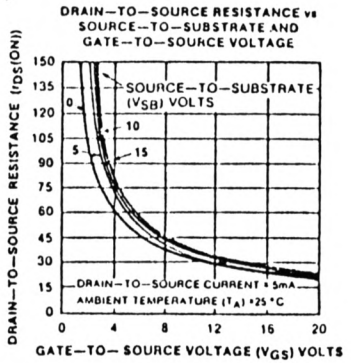
SWITCHING CHARACTERISTICS

		$t_{d(ON)}$ (ns)		t_r (ns)		* t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

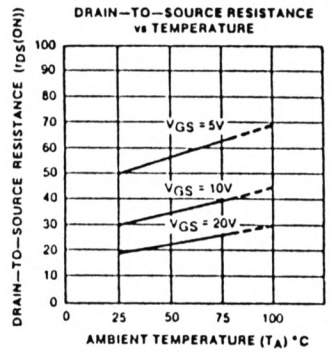
*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

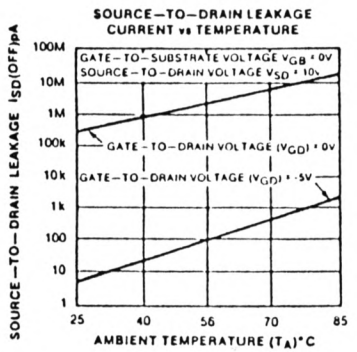
TYPICAL CHARACTERISTICS

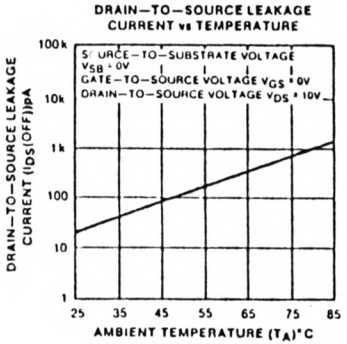


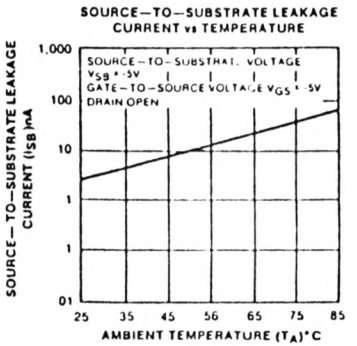


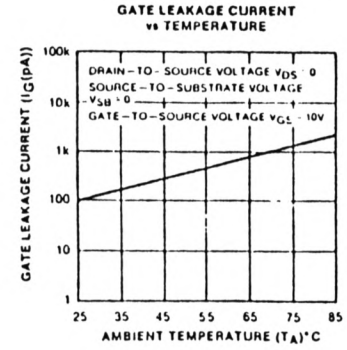
TYPICAL CHARACTERISTICS (Cont.)

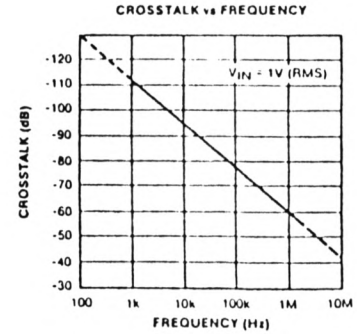












ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER — SE/NE5539

DESCRIPTION

The Signetics SE/NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

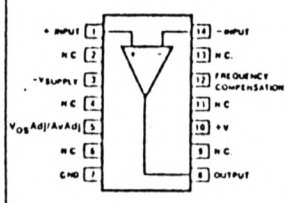
- Gain bandwidth product: 1.2GHz at 17dB
- Slew rate: 600/V$_\mu$sec
- Full power response: 48MHz
- A_{VOL}: 52dB typical
- 350MHz unity gain

APPLICATIONS

- Fast pulse amplifiers
- RF oscillators
- Fast sample and hold
- High gain video amplifiers (BW > 20MHz)

PIN CONFIGURATION

D,F,N PACKAGE



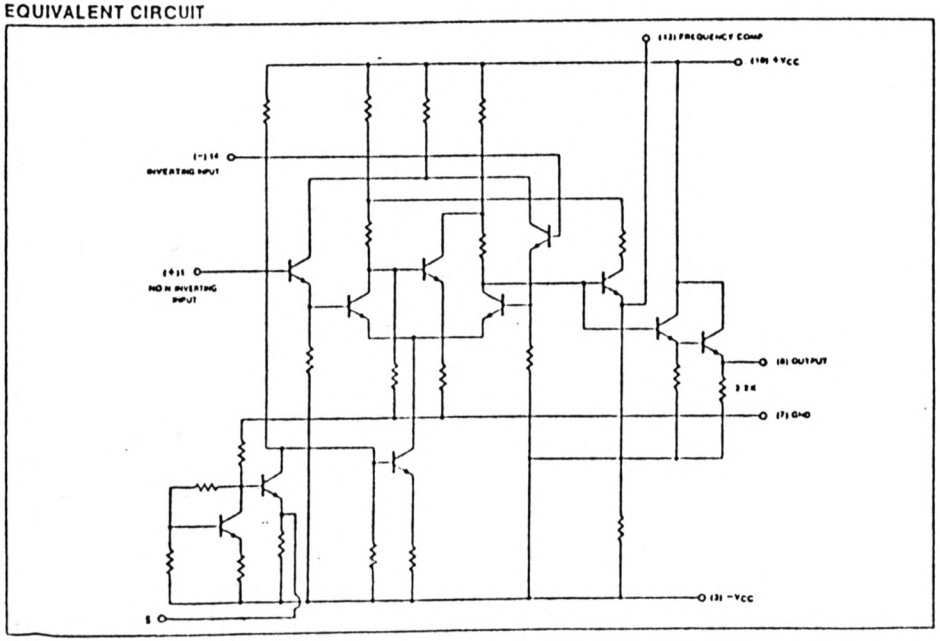
TOP VIEW

ORDER NUMBERS
SE/NE5539F SE/NE5539N
NE5539D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	± 12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to + 150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to + 125	°C
	Lead temperature	300	°C

EQUIVALENT CIRCUIT



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER — SE/NE5539

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ± 8V, T_A = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS		SE5539 Min	SE5539 Typ	SE5539 Max	NE5539 Min	NE5539 Typ	NE5539 Max	UNIT
V_{OS}	Input offset voltage	V_O = 0V, R_S = 100Ω	Over temp		2	5				mV
			T_A = 25°C		2	3		2.5	5	
$\Delta V_{OS}/\Delta T$					5			5		µV/°C
I_{OS}	Input offset current		Over temp		.1	3				µA
			T_A = 25°C		.1	1			2	
$\Delta I_{OS}/\Delta T$					.5			.5		nA/°C
I_B	Input bias current		Over temp		8	25				µA
			T_A = 25°C		5	13		5	20	
$\Delta I_B/\Delta T$					10			10		nA/°C
CMRR	Common mode rejection ratio	F = 1kHz, R_S = 100Ω, V_{CM} ± 1.7V		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to $-V_{CC}$	+Swing				+2.3	+2.7		V
			−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	R_L = 2kΩ to GND	Over temp +Swing	+2.3	+3.0					V
			Over temp −Swing	−1.5	−2.1					
			T_A = 25°C +Swing	+2.5	+3.1					V
			T_A = 25°C −Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	V_O = 0, R_1 = ∞	Over temp		14	18				mA
			T_A = 25°C		14	17		14	18	
$I_{CC}-$	Negative supply current	V_O = 0, R_1 = ∞	Over temp		11	15				mA
			T_A = 25°C		11	14		11	15	
PSRR	Power supply rejection ratio	ΔV_{CC} = ± 1V	Over temp		300	1000				µV/V
			T_A = 25°C					200	1000	
A_{VOL}	Large signal voltage gain	V_O = +2.3V, −1.7V R_L = 150Ω to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, −1.7V R_L = 2K to GND								dB
			T_A = 25°C				47	52	57	
A_{VOL}	Large signal voltage gain	V_O = +2.5V, −2.0V R_L = 2kΩ to GND	Over temp	46		60				dB
			T_A = 25°C	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER SE/NE5539

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$ $V_O = 0.1$ Vp-p		1200			1200		MHz
Small signal bandwidth	$A_{CL} = 2$ $R_L = 150\Omega$[1]		110			110		MHz
Settling time	$A_{CL} = 2$ $R_L = 150\Omega$[1]		15			15		nSec
Slew rate	$A_{CL} = 2$ $R_L = 150\Omega$[1]		600			600		V/μSec
Propagation delay	$A_{CL} = 2$ $R_L = 150\Omega$[1]		7			7		nSec
Full power response	$A_{CL} = 2$ $R_L = 150\Omega$[1]		48			48		MHz
Full power response	$A_V = 7$, $R_L = 150\Omega$		20			20		MHz
Input noise voltage	$R_S = 50\Omega$		4			4		$nV/\sqrt{Hz}$

NOTE 1. External compensation.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$ unless otherwise specified

PARAMETERS	TEST CONDITIONS		SE5539			UNIT
			Min	Typ	Max	
V_{OS} Input offset voltage		Over temp		2	5	mV
		$T_A = 25°C$		2	3	
I_{OS} Input offset current		Over temp		.1	3	μA
		$T_A = 25°C$		.1	1	
I_B Input bias current		Over temp		5	20	μA
		$T_A = 25°C$		4	10	
CMRR Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$		70	85		dB
$I_{CC}+$ Positive supply current		Over temp		11	14	mA
		$T_A = 25°C$		11	13	
$I_{CC}-$ Negative supply current		Over temp		8	11	mA
		$T_A = 25°C$		8	10	
PSRR Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000	μV/V
		$T_A = 25°C$				
V_{OUT} Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp + Swing	+ 1.4	+ 2.0		V
		Over temp − Swing	− 1.1	− 1.7		
		$T_A = 25°C$ + Swing	+ 1.5	+ 2.0		
		$T_A = 25°C$ − Swing	− 1.4	− 1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

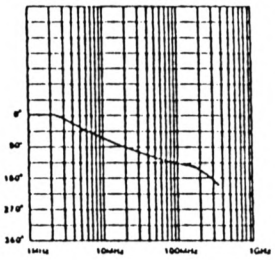
PARAMETER	TEST CONDITIONS	SE5539			UNIT
		Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$		700		MHz
Small signal bandwidth	$A_{CL} = 2$[1]		120		MHz
Settling time	$A_{CL} = 2$[1]		23		ns
Slew rate	$A_{CL} = 2$[1]		330		V/μs
Propagation delay	$A_{CL} = 2$[1]		4.5		ns
Full power response	$A_{CL} = 2$[1]		20		MHz

NOTE 1: External compensation

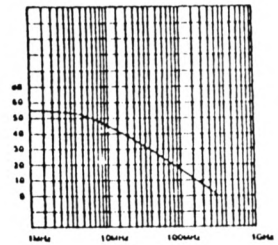
LINEAR LSI PRODUCTS

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER SE/NE5539

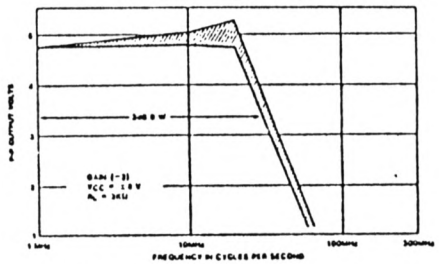
NE5539 OPEN LOOP PHASE



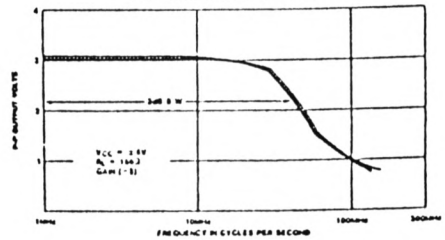
NE5539 OPEN LOOP GAIN



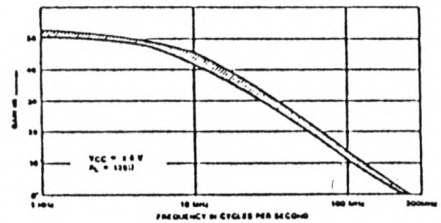
POWER BANDWIDTH (SE)



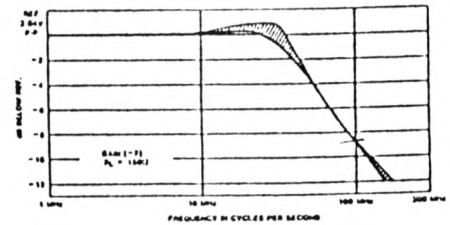
POWER BANDWIDTH (NE)



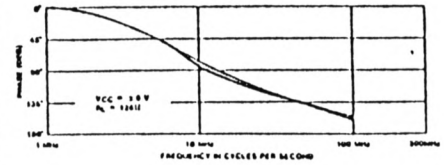
SE5539 OPEN LOOP GAIN vs FREQUENCY



POWER BANDWIDTH



SE5539 OPEN LOOP PHASE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs FREQUENCY

NOTE

Indicates typical distribution $-55°C \le T_A \le 125°C$

ANALOG DEVICES

Voltage-to-Frequency and Frequency-to-Voltage Converter

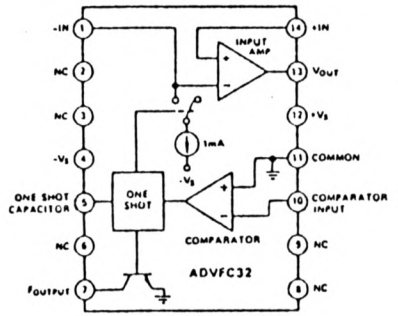
ADVFC32

FEATURES

High Linearity
- ±0.01% max at 10kHz FS
- ±0.05% max at 100kHz FS
- ±0.2% max at 500kHz FS

Output TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction

ADVFC32 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage-to-frequency (V/F) converter or frequency-to-voltage (F/V) converter with good linearity (0.01% max error at 10kHz) and operating frequency up to 0.5MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using only a few external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15V or +5V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8mA. A larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full scale calibration drift is held to a maximum of 100ppm/°C (ADVFC32BH) due to a low T.C. zener diode.

The ADVFC32 is available in commercial, industrial, and extended temperature grades. The commercial grade is packaged in a 14-pin plastic DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans.

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to high accuracy voltage-to-frequency conversion. The full-scale operating frequency is determined by only one precision resistor and capacitor. The tolerance of other support components (including the integration capacitor) is not critical. Inexpensive ± 20% resistors and capacitors can be used without affecting linearity or temperature drift.
2. The ADVFC32 is easily configured to satisfy a wide range of system requirements. Input voltage scaling is set by selecting the input resistor which sets the input current to 0.25mA at the maximum input voltage.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. The ADVFC32 is intended as a pin-for-pin replacement for VFC32 devices from other manufacturers.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V, unless otherwise noted)

Model	ADVFC32KN	ADVFC32BH	ADVFC32SH
DYNAMIC PERFORMANCE			
Full Scale Frequency Range	0 to 500kHz	•	•
Nonlinearity[1]			
f_{max} = 10kHz	±0.01% max	•	•
f_{max} = 100kHz	±0.05% max	•	•
f_{max} = 0.5MHz	±0.2% max, ±0.05% typ	•	•
Full Scale Calibration Error (adjustable to zero)	±5%	•	•
vs. Supply (Full Scale Frequency = 100kHz)	±0.015% of FSR/%max	•	•
vs. Temperature (Full Scale Frequency = 10kHz)	±75ppm/°C	±100ppm/°C max	±150ppm/°C
DYNAMIC RESPONSE			
Max Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1µs	•	•
Overload Recovery Time	1 Pulse of New Frequency Plus 1µs	•	•
ANALOG INPUT AMPLIFIER (V/F Conversion)			
Current Input Range	0 to +0.25mA	•	•
Voltage Input Range	0 to -10V[2], 0 to 0.25mA X R_{IN}[3]	•	•
Differential Impedance	2MΩ‖10pF (300kΩ‖10pF min)		
Common Mode Impedance	750MΩ‖3pF (300MΩ‖3pF min)		
Input Bias Current			
Noninverting Input	40nA (250nA max)	•	•
Inverting Input	±8nA (±100nA max)	•	•
Input Offset Voltage (trimmable to zero)[2,3]	4mV max	•	•
vs. Temperature (T_{min} to T_{max})	30µV/°C	•	•
Safe Input Voltage	±V_S	•	•
COMPARATOR (F/V Conversion)			
Logic "0" Level	-V_S to -0.6V	•	•
Logic "1" Level	+1V to +V_S	•	•
Pulse Width Range	0.1µs to (0.15/f_{max})	•	•
Input Impedance	250kΩ (50kΩ‖10pF min)	•	•
OPEN COLLECTOR OUTPUT (V/F Conversion)			
Output Voltage, Logic "0" I_{SINK} = 8mA	0.4V max	•	•
Output Leakage Current in Logic "1"	1µA max	•	•
Voltage Range	0 to +30V	•	•
Fall Times (Load = 500pF and I_{SINK} = 5mA)	400ns max	•	•
AMPLIFIER OUTPUT (F/V Conversion)			
Voltage Range (0mA≤I_O≤7mA)	0 to +10V	•	•
Source Current (0≤V_O≤7V)	+10mA min	•	•
Capacitive Load (without oscillation)	100pF max	•	•
Closed Loop Output Impedance	1Ω max	•	•
POWER SUPPLY			
Rated Voltage	±15V	•	•
Voltage Range	±9V to ±18V	•	•
Quiescent Current	6mA typ, 8mA max	•	•
TEMPERATURE RANGE			
Specified Range	0 to +70°C	-25°C to +85°C	-55°C to +125°C
Operating Range	-25°C to +85°C	-55°C to +125°C	-55°C to +125°C
Storage	-25°C to +85°C	-65°C to +150°C	-65°C to +150°C
PACKAGE OPTIONS[4]			
Plastic DIP – N14A	ADVFC32KN	N/A	N/A
TO-100	N/A	ADVFC32BH	ADVFC32SH

NOTES
[1] Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.
[2] See Figure 3.
[3] See Figure 1.
[4] See Section 19 for package outline information.
[5] Specifications same as ADVFC32KN.

Specifications subject to change without notice.

GigaBit Logic

10G070

PRELIMINARY

Variable Modulus Divider
2 GHz Clock Rate
10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 2 GHz operation
- Divide by 5 and 6, 10 and 11, 20 and 21, or 40 and 41
- 10G PicoLogic and ECL compatible inputs and outputs
- Divide by N or N + 1 mode control timing allows use of TTL, CMOS or ECL control logic
- Wire-OR output capability
- Temperature and voltage compensation capability
- Member of GigaBit's 10G Gallium Arsenide PicoLogic Family
- Available in leadless chip carrier, flatpack or dice form
- Decoupling capacitors in LCC and flatpack package facilitate high frequency operation
- All devices, including dice, tested to meet AC and DC specs

FUNCTIONAL DESCRIPTION

The 10G070 is a high performance 2 GHz variable modulus prescaler for use in frequency synthesis applications. By strapping the S10/11, S20/21 and S40/41 pins to V_{SS} or V_{EE}, one of the following four division ratio pairs can be programmed: 5 and 6, 10 and 11, 20 and 21 or 40 and 41. When the MODE input is set to 1, the counter will divide by N (5, 10, 20 or 40). When the MODE input is set to 0, the counter will divide by N + 1 (6, 11, 21, 41).

In a typical system, MODE will be driven from 10G, ECL, TTL or CMOS logic. The state transitions of the 10G070 have been optimized to allow the maximum amount of time to establish the appropriate level on the MODE input, simplifying the use of slower logic, such as ECL, TTL or CMOS, to generate the MODE input. In order to handle all types of MODE generation logic, the 10G070 has both a 10G/ECL compatible MODE input—MODE (10G/ECL)—and a TTL compatible MODE input—MODE (TTL). When driving the MODE (10G/ECL) input from 10G or ECL logic, the MODE (TTL) input should be left unconnected. Similarly, when the MODE (TTL) input is driven from TTL or CMOS logic, the MODE (10G/ECL) signal should be left unconnected.

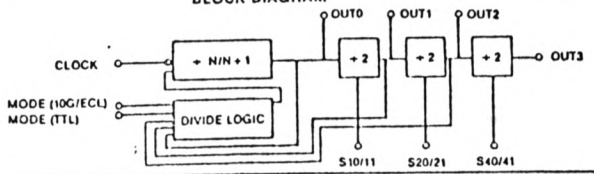
When the 10G070 is used to divide by 5 or 6, the OUT0 pin should be used. For division by 10/11, 20/21 and 40/41, the OUT1, OUT2, and OUT3 pins respectively should be used.

The 10G070 features special input clamps (V_{ICH} and V_{ICL}) which, when connected to −1.3V, allow the 10G070 to be driven with large peak-to-peak input signals or large overshoots without damage to the internal gates. This is particularly useful when the 10G070 CLOCK pin is driven directly from a voltage controlled oscillator (VCO). When not used, the input clamps can be left unconnected. Alternatively, V_{ICH} and V_{ICL} can be connected to V_{DDO} (ground) and V_{SS} (−3.3V) respectively for enhanced static protection.

The V_{TRIM} input can be used as a temperature and voltage compensation input for matching the thermal and logic threshold of the 10G070 to surrounding ECL components for maximum noise immunity and performance. When not used, V_{TRIM} should be connected to V_{EE} (−5.2V).

The 10G070 is available packaged in a leadless chip carrier (LCC), packaged in a flatpack, or in dice form. The LCC and flatpack include on-board decoupling capacitors for maximum noise immunity, even at high operating frequencies.

BLOCK DIAGRAM



10G070 ORDERING INFORMATION

PACKAGE TYPE	SPEED		
	2.00 GHz	1.75 GHz	1.25 GHz
LEADLESS CHIP CARRIER	10G070-2L	10G070L	10G070-4L
FLATPACK	10G070-2F	10G070F	10G070-4F
DICE	10G070-2X	10G070X	10G070-4X

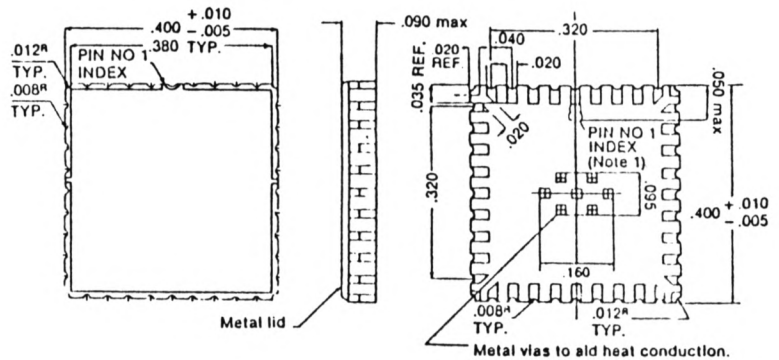
1908 Oak Terrace Lane, Newbury Park, CA 91320 (805) 498-9664 • Telex 6711358

GigaBit Logic

10G070

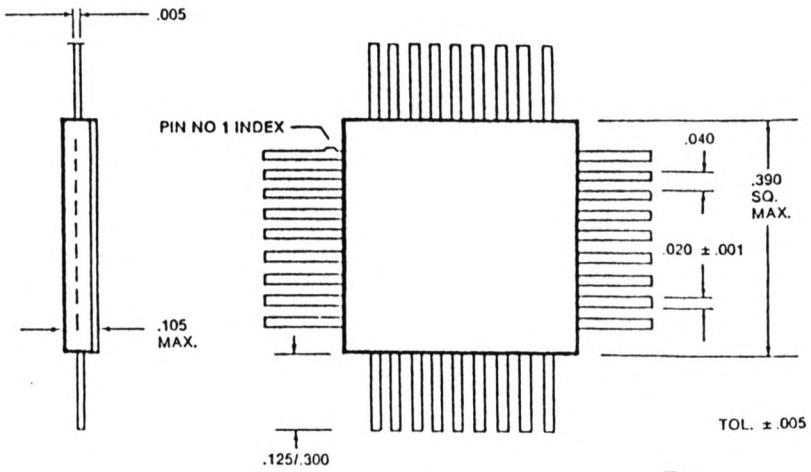
PACKAGE DRAWINGS

40 PIN LEADLESS CHIP CARRIER



NOTES: To avoid shorts, do not run uninsulated traces under pin 1 index mark or under heat conduction vias.

36 LEAD FLATPACK



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PROGRAMMING					
S40/41	S20/21	S10/11	Mode	Division Ratio	Output Pin
V_{SS}	V_{SS}	V_{SS}	0	6	OUT0
V_{SS}	V_{SS}	V_{SS}	1	5	OUT0
V_{SS}	V_{SS}	V_{EE}	0	11	OUT1
V_{SS}	V_{SS}	V_{EE}	1	10	OUT1
V_{SS}	V_{EE}	V_{EE}	0	21	OUT2
V_{SS}	V_{EE}	V_{EE}	1	20	OUT2
V_{EE}	V_{EE}	V_{EE}	0	41	OUT3
V_{EE}	V_{EE}	V_{EE}	1	40	OUT3

STATE TRANSITIONS

DIVIDE BY 5/6 MODE

N/N + 1 DIVIDER

OUT0	Q1	Q0	
1	1	1	
1	1	0	MODE = 1 DIVIDE BY 5
1	0	0	MODE = 0 DIVIDE BY 6
0	0	0	
0	0	1	
0	1	1	

OUT1 = OUT2 = OUT3 = 0. Q0 and Q1 are internal flip-flops in the N/N + 1 divider.

Use OUT0 as chip output.

DIVIDE BY 10/11 MODE

N/N + 1 DIVIDER

OUT1	OUT0	Q1	Q2	
1	1	1	1	
1	1	1	0	MODE = 1 DIVIDE BY 10
1	1	0	0	MODE = 0 DIVIDE BY 11
1	0	0	0	
1	0	0	1	
1	0	1	1	
0	1	1	0	
0	1	0	0	
0	0	0	0	
0	0	0	1	
0	0	1	1	

OUT2 = OUT3 = 0. Q0 and Q1 are internal flip-flops in the N/N + 1 divider.

Use OUT1 as chip output.

DIVIDE BY 20/21 MODE

N/N + 1 DIVIDER

OUT2	OUT1	OUT0	Q1	Q0	
1	1	1	1	1	
1	1	1	1	0	
1	1	1	0	0	MODE = 1 DIVIDE BY 20
1	1	0	0	0	MODE = 0 DIVIDE BY 21
1	1	0	0	1	
1	1	0	1	1	
1	0	5 count subcycle (Note 1)			
0	1	5 count subcycle (Note 1)			
0	0	1	1	0	
0	0	1	0	0	
0	0	0	0	0	
0	0	0	0	1	
0	0	0	1	1	

OUT3 = 0. Q0 and Q1 are internal flip-flops in the N/N + 1 divider.

Use OUT2 as chip output.

DIVIDE BY 40/41 MODE

N/N + 1 DIVIDER

OUT3	OUT2	OUT1	OUT0	Q1	Q0	
1	1	1	1	1	1	
1	1	1	1	1	0	
1	1	1	1	0	0	MODE = 1 DIVIDE BY 40
1	1	1	0	0	0	MODE = 0 DIVIDE BY 41
1	1	1	0	0	1	
1	1	1	0	1	1	
1	1	0	5 Count Subcycle (Note 1)			
1	0	1	5 Count Subcycle (Note 1)			
1	0	0	5 Count Subcycle (Note 1)			
0	1	1	5 Count Subcycle (Note 1)			
0	1	0	5 Count Subcycle (Note 1)			
0	0	1	5 Count Subcycle (Note 1)			
0	0	0	1	1	0	
0	0	0	1	0	0	
0	0	0	0	0	1	
0	0	0	0	1	1	

Q0 and Q1 are internal flip-flops in the N/N + 1 divider.

Use OUT3 as chip output.

NOTES: 1. To avoid unnecessarily long State Transition Tables, the five count subcycle on Q0, Q1 and OUT3 has been omitted. The State Transition Table for this subcycle is:

N/N + 1 DIVIDER

OUT0	Q1	Q0
1	1	1
1	1	0
1	0	0
0	0	0
0	0	1
0	1	1

Pins OUT1, OUT2 and OUT3 do not change during this five count subcycle.

Q0 and Q1 are internal flip-flops in the N/N + 1 divider.

ABSOLUTE MAXIMUM RATINGS (Note 1)
(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
V_{OOL}	Supply Voltage	−3.5V to 4.0V
V_{OOO}	Supply Voltage (Note 2)	V_{OOL} − 1.0V to 4.0V
V_{EE}	Supply Voltage	−7.0V to −3.5V
V_{TRIM}	Input Threshold Trim Voltage	V_{EE} − 6.0V to V_{EE} + 6.0V
V_{TT}	Load Termination Supply (Notes 2, 3)	−10V to V_{OOO}
V_{OUT}	Voltage Applied to Any Output In Low State In High State (Note 2)	−4.0V to 5.0V −2.0V to 5.0V
V_{IN}	Voltage Applied to any Input; Continuous @ V_{SS} = −3.3V, V_{EE} = −5.2V, V_{OOO} = V_{OOL} = 0V	−6.0V to 0V
I_{OUT}	Current From Any Output Continuous Surge	70mA TBD
I_{IN}	Current into Any Input; Continuous	−0.5mA to 1.0mA
P_D	Total Power Dissipation (T_C = 70°C)	1.5W
P_{OUT}	Power Dissipation Per Output P_{OUT} = (V_{OOO} − V_{OUT}) × I_{OUT}	200mW
T_{STOR}	Storage Temperature	−65°C to 150°C

NOTES: 1. All voltages are specified with V_{SS} defined as −3.3V.
2. Subject to power dissipation limitations.
3. In operation in TTL or CMOS systems, where positive load resistor termination voltages are used, the V_{TT} pins on the packaged devices must be left unconnected or connected to V_{SS}.

RECOMMENDED OPERATING CONDITIONS (Note 1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{SS}	Supply Voltage, defined as −3.3V		−3.3V		V
V_{OOL}	Supply Voltage	−0.25	0	3.5	V
V_{OOO}	Supply Voltage	V_{OOL} − 0.5	0	3.5	V
V_{EE}	Supply Voltage Interface to ECL Interface to TTL/CMOS		−5.2 −5.0		V V
V_{TRIM}	Input Threshold Trim Voltage	V_{EE} − 1.8	V_{EE}	V_{EE} + 1.8	V
V_{TT}	Load Termination Supply Voltage (Note 2) Interface to ECL Interface to TTL/CMOS (Note 3)	−5.2	−2.0 V_{SS}	−2.0	V V
T_C	Case Temperature				°C

NOTES: 1. All voltages are specified with V_{SS} defined as −3.3V.
2. The R_{LOAD} and V_{TT} combination used is subject to maximum output current and output power restrictions.
3. In operation in TTL or CMOS systems, when positive load resistor termination voltages are used, the V_{TT} pins on the packaged devices must be left unconnected or connected to V_{SS}.

DC CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IH}	Input Voltage High	All inputs (except input under test: −2.0V≤V_{IN}≤−0.4V, and MODE (TTL) Open.	−1.100		0	V
V_{IL}	Input Voltage Low	All inputs (except input under test: −2.0V≤V_{IN}≤−0.4V, and MODE (TTL) Open.	−2.500		−1.500	V
V_{IHTTL}	Input Voltage High MODE (TTL)	All inputs (except input under test: −2.0V≤V_{IN}≤−0.4V, and MODE (10G/ECL) Open.	2.0		3.5	V
V_{ILTTL}	Input Voltage Low MODE (TTL)	All inputs (except input under test: −2.0V≤V_{IN}≤−0.4V, and MODE (10G/ECL) Open.	−1.0		0.8	V
I_{IH}	Input Current High	V_{IH} = −0.8V		60		μA
I_{IL}	Input Current Low	V_{IH} = −2.0V		60		μA
V_{OH}	Output Voltage High		−0.900			V
V_{OL}	Output Voltage Low				−1.700	V
I_{OH}	Output Current High (Note 2)	V_{OH} = −0.950V, V_{OCH} = 0V		−70		mA
		V_{OH} = −0.800V, V_{OCH} = 0V		−60		mA
I_{OL}	Output Current Low (output leakage current) (Note 3)	V_{OL} = −1.800V		−100		μA
I_{EE}	Power Supply Current			15		mA
I_{SS}	Power Supply Current			150		mA
P_D	Power Dissipation				800	mW

NOTES: 1. Test conditions for all tests (except as noted otherwise).
T_A = 25°C, V_{OOL} = V_{OOO} = 0V, V_{EE} = −5.2V, V_{SS} = −3.3V, V_{TRIM} = V_{EE}, R_{LOAD} = 50 ohms to −2.0V, V_{OCH} = 0V, V_{OCL} = V_{SS}, V_{OCH} = 0V, V_{OCL} = V_{SS}, V_{LCH} = −1.7V, V_{LCL} = −0.95V
2. Parameter I_{OH} is the maximum current the output can source under any R_{LOAD} and V_{TT} combination.
3. For any R_{LOAD} and V_{TT} combination.

10G070-2L, 10G070-2F, 10G070-2X

AC CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	DICE			PACKAGED			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
T1	$\overline{CLOCK}$ Maximum Toggle Frequency (Notes 2, 3)	2.0	2.5		2.0	2.5		GHz
	(Notes 2, 4)	1.6			1.6			GHz
T2	$\overline{CLOCK}$ Low Time (Notes 2, 3)	250			250			ps
	(Notes 2, 4)	310			310			ps
T3	$\overline{CLOCK}$ High Time (Notes 2, 3)	250			250			ps
	(Notes 2, 4)	310			310			ps
T4	MODE High or Low to $\overline{CLOCK}$ Low (Mode Setup Time) (Note 5)	500			500			ps
T5	$\overline{CLOCK}$ Low to MODE High or Low (Mode Hold Time) (Note 5)	250			250			ps
T6	$\overline{CLOCK}$ Low to OUT0 High or Low (Note 6)			1.5			1.6	ns
T7	$\overline{CLOCK}$ Low to OUT1 High or Low (Note 6)			2.5			2.6	ns
T8	$\overline{CLOCK}$ Low to OUT2 High or Low (Note 6)			3.5			3.6	ns
T9	$\overline{CLOCK}$ Low to OUT3 High or Low (Note 6)			4.5			4.6	ns

10G070-L, 10G070-F, 10G070-X

AC CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	DICE			PACKAGED			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
T1	$\overline{CLOCK}$ Maximum Toggle Frequency (Notes 2, 3)	1.75			1.75			GHz
	(Notes 2, 4)	1.4			1.4			GHz
T2	$\overline{CLOCK}$ Low Time (Notes 2, 3)	285			285			ps
	(Notes 2, 4)	355			355			ps
T3	$\overline{CLOCK}$ High Time (Notes 2, 3)	285			285			ps
	(Notes 2, 4)	355			355			ps
T4	MODE High or Low to $\overline{CLOCK}$ Low (Mode Setup Time) (Note 5)	575			575			ps
T5	$\overline{CLOCK}$ Low to MODE High or Low (Mode Hold Time) (Note 5)	285			285			ps
T6	$\overline{CLOCK}$ Low to OUT0 High or Low (Note 6)			1.8			1.9	ns
T7	$\overline{CLOCK}$ Low to OUT1 High or Low (Note 6)			2.9			3.0	ns
T8	$\overline{CLOCK}$ Low to OUT2 High or Low (Note 6)			4.0			4.1	ns
T9	$\overline{CLOCK}$ Low to OUT3 High or Low (Note 6)			5.2			5.3	ns

ADDENDUM

AC CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	10G070-2			UNIT
		MIN	TYP	MAX	
T1	$\overline{CLOCK}$ Maximum Toggle Frequency (Notes 2,3)	2.0			GHz
T2	$\overline{CLOCK}$ Low Time (Notes 2,3)	250			ps
T3	$\overline{CLOCK}$ High Time (Notes 2,3)	250			ps
T4	MODE High or Low to $\overline{CLOCK}$ Low (Mode Setup Time-Note 4)	500			ps
T5	$\overline{CLOCK}$ Low to MODE High or Low (Mode Hold Time-Note 4)	250			ps
T6	$\overline{CLOCK}$ Low to OUT0 High or Low (Note 5)			1.5	ns
T7	$\overline{CLOCK}$ Low to OUT1 High or Low (Note 5)			2.5	ns
T8	$\overline{CLOCK}$ Low to OUT2 High or Low (Note 5)			3.5	ns
T9	$\overline{CLOCK}$ Low to OUT3 High or Low (Note 5)			4.5	ns

NOTES:
1. See page 7 of the 10G070 datasheet for test conditions.
2. See page 7 of the 10G070 datasheet for Clock input conditions.
3. See page 7 of the 10G070 datasheet for Clock input test conditions.
4. See page 7 of the 10G070 datasheet for Mode control input conditions.
5. See page 7 of the 10G070 datasheet for Output selection data.

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AC CHARACTERISTICS

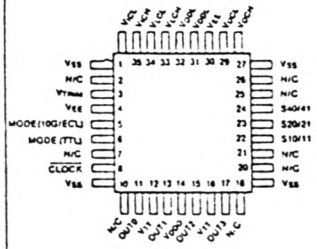
NOTES: 1. Test Conditions, unless otherwise stated:

T_A = 25°C	V_{OCH} = 0V	Input signal rise time:
V_{OOL} = V_{OOO} = 0V	V_{OCL} = V_{SS}	Packaged = 150 ps, Dice = 100 ps
V_{EE} = −5.2V	V_{TRIM} = V_{EE}	Input signal fall time:
V_{SS} = −3.3V	V_{IH} = −0.8V	Packaged = 150 ps, Dice = 100 ps
V_{ICH} = 0V	V_{IL} = −1.8V	Rise and fall times are measured
V_{ICL} = V_{SS}	V_{OH} = −0.8V	between the 20% and 80% points.
V_{LCH} = −1.70V	V_{OL} = −1.8V	
V_{LCL} = −0.95V	R_{LOAD} = 50 ohms to −2.0V	

2. The CLOCK rise and fall times must be 2ns or faster (measured from the 20% and 80% points).
3. Test conditions: Clock input = 2V peak-to-peak sine wave, −1.3V DC offset (i.e. −0.3 to −2.3 sine wave) with V_{ICH} = V_{ICL} = −1.3V. This specification also applies when the Clock input is driven with a −0.8V to −1.8V square wave with 50 ps rise and fall times (between the 20% and 80% points), and V_{ICH} = 0V, V_{ICL} = V_{SS}.
4. Test conditions: Clock input = 1V peak-to-peak sine wave, −1.3V DC offset (i.e. −0.8 to −1.8V sine wave) with V_{ICH} = 0V, V_{ICL} = V_{SS}.
5. The MODE control input may be arbitrarily changed throughout almost the full 5, 6, 10, 11, 20, 21, 40 or 41 count cycle without affecting the output. However, the MODE input must be stable at the desired level (High or Low) for the indicated setup time (T4) before the last input clock edge of the cycle. The MODE input must also be held stable for the indicated hold time (T5) after the last input clock edge of the cycle. The "last input clock edge of the cycle" is the High-to-Low clock transition which occurs while the counter is in the state OUT3 = 0, OUT2 = 0, OUT1 = 0, OUT0 = 0, Q1 = 1 and Q0 = 1.
6. Only the single output selected by appropriately strapping the S10/11, S20/21 and S40/41 pins to V_{EE} or V_{SS} is valid.

PACKAGE PINOUT DIAGRAM

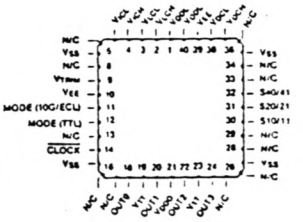
36 LEAD FLATPACK



N/C = No Connection

Note: Pin 1 is marked for orientation.

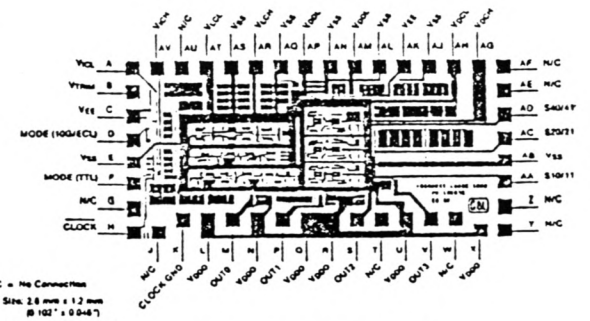
40 PIN LEADLESS CHIP CARRIER



N/C = No Connection

Note: Pin 1 is marked for orientation.

DICE BONDING PAD DIAGRAM



N/C = No Connection

Die Size: 2.8 mm x 1.2 mm (0.102" x 0.046")

Pad Size: 100 µm x 100 µm (0.004" x 0.004")

Note: Pad A has a cut corner for orientation.

HEWLETT PACKARD

SCHOTTKY BARRIER DIODES FOR GENERAL PURPOSE APPLICATIONS

1N5711
1N5712
5082-2800/10/11/35
HSCH-1001 (1N6263)
5082-2301
5082-2302
5082-2303
5082-2305
5082-2900

Features

LOW TURN-ON VOLTAGE: AS LOW AS 0.34V AT 1mA

PICO-SECOND SWITCHING SPEED

HIGH BREAKDOWN VOLTAGE: UP TO 70V

MATCHED CHARACTERISTICS AVAILABLE

Description/Applications

The 1N5711, 1N5712, 5082-2800/10/11 are passivated Schottky barrier diodes which use a patented "guard ring" design to achieve a high breakdown voltage. Packaged in a low cost glass package, they are well suited for high level detecting, mixing, switching, gating, log or A-D converting, video detecting, frequency discriminating, sampling and wave shaping.

The 5082-2835 is a passivated Schottky diode in a low cost glass package. It is optimized for low turn-on voltage. The 5082-2835 is particularly well suited for the UHF mixing needs of the CATV marketplace.

The 5082-2300 and 2900 Series devices are unpassivated Schottky diodes in a glass package. These diodes have extremely low 1/f noise and are ideal for low noise mixing, and high sensitivity detecting. They are particularly well suited for use in Doppler or narrow band video receivers.

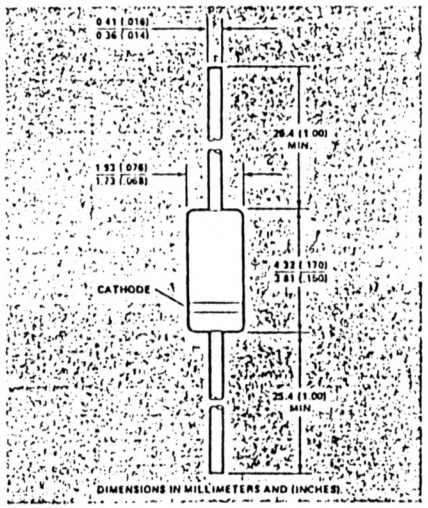
Application Bulletins 13, 14, 15, and 16 describe applications in which these diodes are used for speed up of a transistor, clipping, clamping, and sampling, respectively. Other digital and RF applications are described in Application Bulletins 26, 27, 28, 30, 31 and 36.

Maximum Ratings

Junction Operating and Storage Temperature Range
5082-2305, 2301, 2302, 2303, 2900 ..... -60°C to +100°C
1N5711, 1N5712, 5082-2800/10/11, ... -65°C to +200°C
5082-2835 ..... -60°C to +150°C

DC Power Dissipation (Measured in an infinite heat sink at T_{CASE} = 25°C)
Derate linearly to zero at maximum rated temperature
5082-2305, 2301, 2302, 2303, 2900 ..... 100 mW
1N5711, 1N5712, 5082-2800/10/11 ..... 250 mW
5082-2835 ..... 150 mW

Peak Inverse Voltage ..... V_{BR}



OUTLINE 15

Package Characteristics

	Outline 15
Lead Material:	Dumet
Lead Finish:	1N5711, 1N5712: 95-5% Tin Lead 2800 Series: 95-5% Tin Lead 2300 Series: Gold 2900 Series: 95-5% Tin Lead
Maximum Soldering Temperature:	230°C for 5 sec.
Minimum Lead Strength:	4 lb. Pull
Typical Package Inductance:	1N5711, 1N5712: 2.0 nH 2800 Series: 2.0 nH 2300, 2900 Series: 3.0 nH
Typical Package Capacitance:	1N5711, 1N5712: 0.2 pF 2800 Series: 0.2 pF 2300, 2900 Series: 0.07 pF

The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch from the glass body.

Outline 12 and 15 diodes are available on tape and reel. The tape and reel specification is patterned after RS-296-D.

Electrical Specifications at T_A = 25°C

GENERAL PURPOSE DIODES

Part Number 5082-	Package Outline	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	V_F = 1 V Max at Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA) at V_R (V)		Maximum Capacitance C_T (pF)
2800	15	70	410	15	200	50	2.0
1N5711	15	70	410	15	200	50	2.0
2810	15	20	410	35	100	15	1.2
1N5712	15	20	550	35	150	16	1.2
2811	15	15	410	20	100	8	1.2
2835	15	8	340	10†	100	1	1.0
HSCH-1001 (1N6263)	12	60	410	15	200	50	2.2
Test Conditions		I_R = 10 μA I_R = 100 μA	I_F = 1 mA	†V_F = .45 V			V_R = 0 V f = 1.0 MHz

Note: *For further information, see HSCH-1001 (1N6263) data sheet in "Switching Diodes" section, page 000.
Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA except for 5082-2835 which is measured at 20 mA.

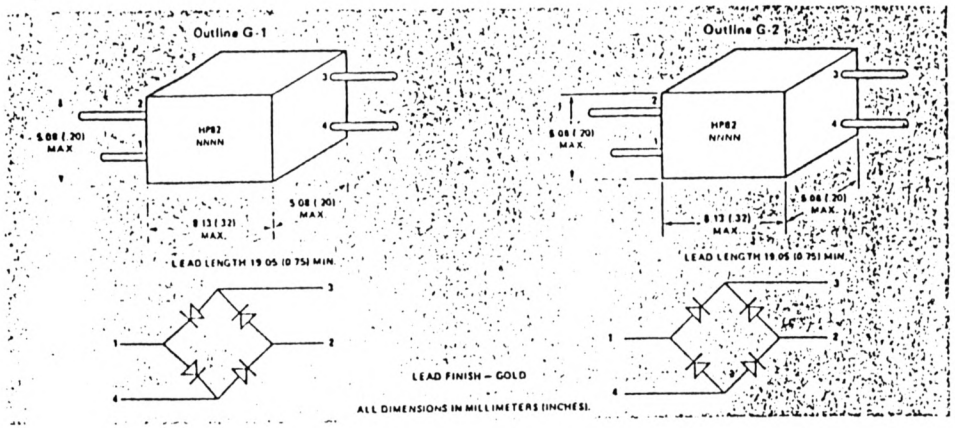
LOW V_F (FLICKER) NOISE DIODES

Part Number 5082-	Package Outline	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	V_F = 1 V Max at Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA) at V_R (V)		Maximum Capacitance C_T (pF)
2305	15	30	400	75	300	15	1.0
2301	15	30	400	50	300	15	1.0
2302	15	30	400	35	300	15	1.0
2303	15	20	400	35	500	15	1.0
2900	15	10	400	20	100	5	1.2
Test Conditions		I_R = 10 μA	I_F = 1 mA				V_R = 0 V f = 1.0 MHz

Note: Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 20 mA.

Matched Pairs and Quads

Basic Part Number 5082-	Matched Pair Unconnected	Matched Quad Unconnected	Matched Ring Quad Encapsulated G-1 Outline	Matched Bridge Quad Encapsulated G-2 Outline	Batch Matched	Test Conditions
2301	5082-2306 ΔV_F = 20 mV ΔC_O = 0.2 pF					ΔV_F at I_F = 0.75, 20 mA ΔC_O at f = 1.0 MHz
2303	5082-2308 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2370 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2396 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2356 ΔV_F = 20 mV ΔC_O = 0.2 pF		ΔV_F at I_F = 0.75, 20 mA ΔC_O at f = 1.0 MHz
2900	5082-2912 ΔV_F = 30 mV	5082-2970 ΔV_F = 30 mV		5082-2997 ΔV_F = 30 mV		ΔV_F at I_F = 1.0, 10 mA
2800	5082-2804 ΔV_F = 20 mV	5082-2805 ΔV_F = 20 mV			5082-2836* ΔV_F = 20 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 0.5, 5 mA I_F = 10 mA ΔC_O at f = 1.0 MHz
2811		5082-2815 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2814 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2813 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2826 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz
2835					5082-2080 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA at f = 1.0 MHz



Typical Parameters

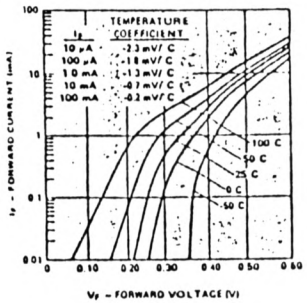


Figure 1. I-V Curve Showing Typical Temperature Variation for 5082-2300 and 5082-2900 Series Schottky Diodes.

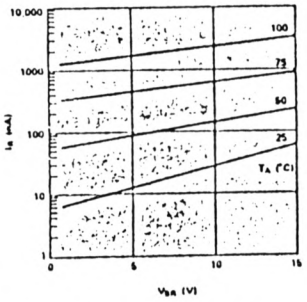


Figure 2. 5082-2300 Series Typical Reverse Current vs. Reverse Voltage at Various Temperatures.

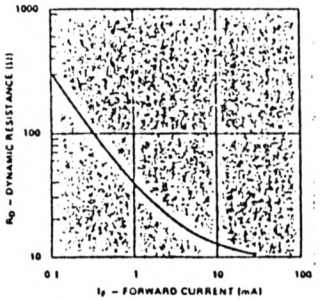


Figure 3. 5082-2300 Series and 5082-2900 Series Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

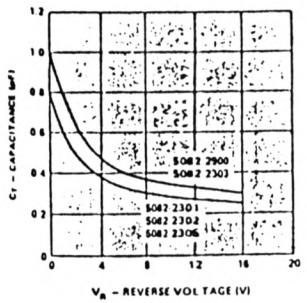


Figure 4. 5082-2300 and 5082-2900 Series Typical Capacitance vs. Reverse Voltage.

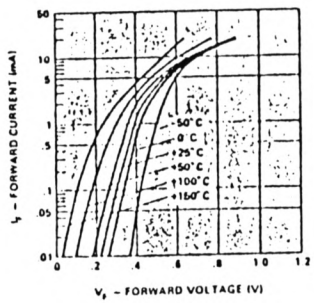


Figure 5. I-V Curve Showing Typical Temperature Variation for 5082-2800 or 1N5711 Schottky Diodes.

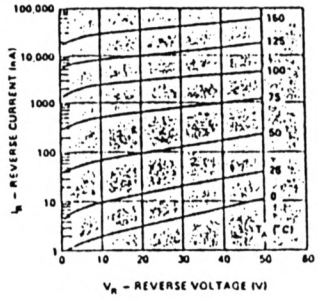


Figure 6. (5082-2800 or 1N5711) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

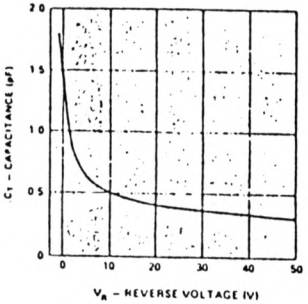


Figure 7. (5082-2800 or 1N5711) Typical Capacitance (C_T) vs. Reverse Voltage (V_R).

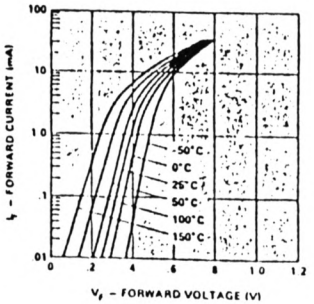


Figure 8. I-V Curve Showing Typical Temperature Variation for the 5082-2810 or 1N5712 Schottky Diode.

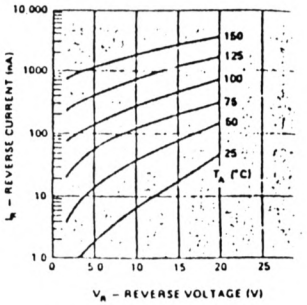


Figure 9. (5082-2810 or 1N5712) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

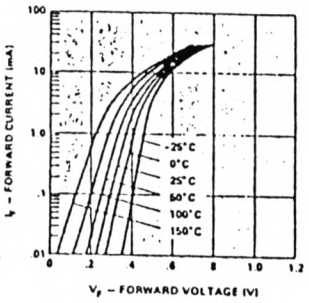


Figure 10. I-V Curve Showing Typical Temperature Variation for the 5082-2811 Schottky Diode.

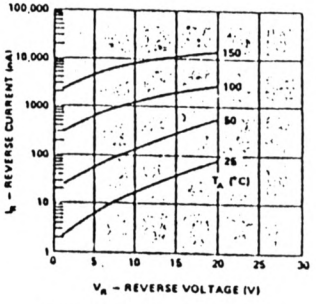


Figure 11. (5082-2811) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

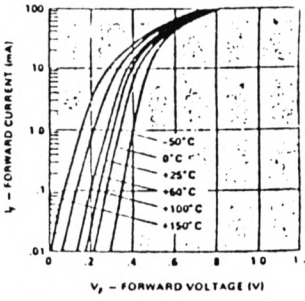


Figure 12. I-V Curve Showing Typical Temperature Variations for 5082-2835 Schottky Diode.

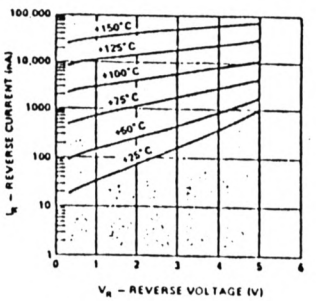


Figure 13. (5082-2835) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

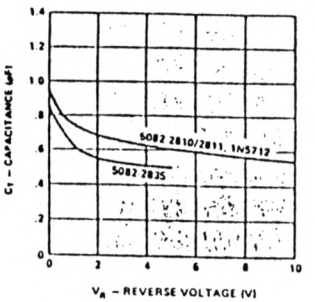


Figure 14. Typical Capacitance (C_T) vs. Reverse Voltage (V_R).

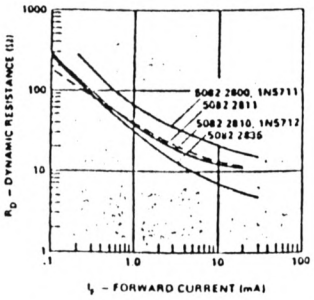


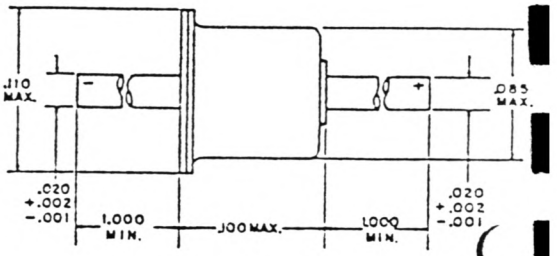
Figure 15. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

SPECIFICATIONS

70.51 2/62
Back Diodes
Germanium Types
BD1, 2, 3, 4, 5, 6 & 7

types 4JFBD1-7 are germanium back diodes which make use of the quantum mechanical tunneling phenomenon, thereby attaining a very low forward voltage drop and eliminating charge storage effects. They feature closely controlled forward voltage characteristics with very small temperature coefficients. The very low forward voltage and low capacity of the back diode make it ideal for use in high frequency applications and in transistor and tunnel diode switching circuits. The germanium back diodes are characterized in seven types according to the forward current at a forward voltage of 90 millivolts and according to the maximum reverse leakage current.

AXIAL DIODE OUTLINE



ALL DIMENSIONS IN INCHES.
DIMENSIONS ARE REFERENCE UNLESS TOLERANCED.

ABSOLUTE MAXIMUM RATINGS

Part Number	1	2	3	4	5	6	7	units
Forward Current (-55 to +100°C)	30	15	10	5	5	5	5	ma
Reverse Current (-55 to +100°C)	10	5	5	5	5	5	5	ma
Lead Temperature, 1/16" ± 1/32" from case for 10 seconds				260°C				

ELECTRICAL CHARACTERISTICS(25°C)

	Sym.	BD1	BD2	BD3	BD4	BD5	BD6	BD7	Units
Forward Voltage, V_{F1}=90mv±10mv at I_{F1}=		10	5	2	1	.5	.2	.1	ma
Forward Voltage at I_{F2}(I_{F2}=3I_{F1})	V_{F2}	120	130	170	170	170	160	160	mv typ
Reverse Voltage, I_R=I_p max	V_{R1}	440	420	400	380	350	330	300	mv min
Reverse Voltage, I_R=1 ma	V_{R2}	440	465	465	465	465	465	465	mv min
Reverse Peak Point Current	I_P	1	.5	.2	.1	.05	.02	.01	ma max
Series Inductance (Measured at case)	L_S	1.5	1.5	1.5	1.5	1.5	1.5	1.5	nh typ
Total Terminal Capacity	C	8	6	4	3	3	3	3	pf typ
(V_R=350mv)		20	10	10	10	10	10	10	pf max
Recovery Time*	t_r	1.0	0.7	0.5	0.4	0.4	0.4	0.4	ns typ

* The recovery time is measured to a reverse current of 1 ma. when switching from 0.1 volt forward to 0.4 volt reverse from a 50 ohm source. Since the back diode does not exhibit charge storage, the recovery time is determined by the charging time of the total device capacity.

Shetland Industrial Center, Building 4 / York Street / Box 3065 / Shawsheen Village Station
Andover, Massachusetts 01810 / Telephone (617) 475-5982 / Telex 94-7150 GPD ANDR

most widely used

Frequency Mixers

Model LMX-113

LEVEL 7 (+7dBm LO, up to +1dBm RF)

computer-automated performance data

typical production unit / for data of other models consult factory

mixer conversion loss and isolation

RF MHz	LO MHz	Conversion Loss (dB) LO +4dBm	LO +7dBm	LO +10dBm	Isolation L-R (dB) LO +4dBm	LO +7dBm	LO +10dBm	Isolation L-I (dB) LO +4dBm	LO +7dBm	LO +10dBm
5 000	35 00	5 91	5 65	5 56	>64 00	>67 00	>70 00	>64 00	>67 00	66 32
20 000	50 00	5 89	5 61	5 48	>64 00	>67 00	61 87	>64 00	62 02	59 19
35 152	65 15	5 92	5 64	5 53	60 03	57 88	56 63	58 71	56 44	54 61
125 610	95 61	5 82	5 57	5 49	46 89	46 48	45 46	45 35	44 58	43 84
185 910	155 91	5 96	5 72	5 64	43 87	43 05	42 13	41 58	41 18	40 70
246 220	216 22	6 01	5 74	5 60	41 50	40 66	39 94	38 94	38 80	38 49
276 370	246 37	5 87	5 63	5 53	40 52	39 62	38 78	37 83	37 70	37 41
336 670	306 67	5 91	5 67	5 58	38 97	38 07	37 08	35 92	35 92	35 71
396 980	366 98	5 96	5 70	5 59	37 25	36 60	36 42	34 15	34 27	34 26
457 280	427 28	6 08	5 75	5 58	36 91	35 82	35 22	32 75	32 94	33 17
547 740	517 74	5 89	5 61	5 50	35 02	34 91	35 11	30 52	30 94	31 22
577 890	547 89	5 94	5 67	5 56	34 28	34 22	34 40	30 10	30 50	30 57
638 190	608 19	6 05	5 78	5 64	33 94	33 14	33 31	29 54	29 84	30 16
698 500	668 50	6 24	5 92	5 75	32 51	32 74	33 27	28 28	29 14	29 61
758 800	728 80	6 36	6 05	5 88	32 01	32 38	32 46	27 06	28 02	28 98
819 100	789 10	6 60	6 23	6 00	31 16	31 58	31 51	26 00	26 86	27 83
879 410	849 41	6 95	6 51	6 22	30 32	31 42	32 98	25 07	25 95	26 81
939 710	909 71	7 23	6 84	6 46	29 33	30 71	32 19	24 54	25 32	25 90
969 860	939 86	7 38	6 93	6 47	28 95	30 28	31 36	24 46	25 18	25 69
1000 000	970 00	7 67	7 18	6 78	28 75	29 68	30 61	24 43	25 06	25 57

mixer VSWR

Freq. MHz	VSWR, RF port LO +4dBm	LO +7dBm	LO +10dBm	VSWR, LO port LO +4dBm	LO +7dBm	LO +10dBm	VSWR, IF port LO +4dBm	LO +7dBm	LO +10dBm
5 002	1 26	1 22	1 20	1 91	2 86	4 24	1 63	1 44	1 34
35 152	1 16	1 08	1 02	1 92	2 81	4 01	1 60	1 44	1 32
50 000	1 15	1 08	1 03	1 88	2 77	4 03	1 60	1 43	1 33
100 000	1 13	1 07	1 03	1 82	2 57	3 53	1 59	1 42	1 31
155 760	1 13	1 06	1 05	1 74	2 51	3 42	1 58	1 42	1 31
200 000	1 12	1 07	1 07	1 81	2 49	3 50	1 56	1 41	1 31
246 210	1 12	1 08	1 09	1 80	2 56	3 52	1 54	1 40	1 31
306 520	1 13	1 12	1 13	1 86	2 59	3 57	1 54	1 41	1 32
366 820	1 15	1 17	1 18	1 97	2 54	3 56	1 53	1 41	1 33
427 120	1 20	1 23	1 24	2 03	2 69	3 56	1 51	1 42	1 36
500 000	1 29	1 33	1 34	2 12	2 72	3 56	1 54	1 49	1 42
547 730	1 35	1 40	1 44	2 20	2 88	3 75	1 61	1 62	1 57
608 030	1 45	1 51	1 56	2 29	2 92	3 70	1 59	1 57	1 51
668 330	1 54	1 62	1 67	2 39	3 00	3 93	1 62	1 63	1 56
728 640	1 67	1 76	1 79	2 45	3 03	3 99	1 67	1 70	1 62
788 940	1 79	1 92	1 90	2 61	3 21	4 14	1 72	1 78	1 69
849 240	1 93	2 11	2 01	2 82	3 40	4 39	1 79	1 87	1 76
909 550	2 12	2 35	2 16	2 93	3 42	4 54	1 87	1 98	1 86
939 700	2 20	2 46	2 25	3 03	3 52	4 57	1 90	2 01	1 89
1000 000	2 37	2 76	2 46	3 14	3 59	4 73	1 95	2 11	1 97

ϕ detection

Freq. (MHz)	max. DC output mV	DC offset mV
5 000	+227 25	- 05
35 152	+224 63	- 06
50 000	+224 13	- 06
100 000	+223 22	- 06
155 760	+225 03	- 08
200 000	+224 89	- 11
246 220	+227 12	- 09
306 520	+227 61	- 20
366 820	+210 22	- 35
427 130	+204 85	- 17
500 000	+210 09	- 34
547 740	+213 64	- 36
608 040	+217 93	- 15
668 340	+199 95	- 26
728 650	+187 17	- 09
788 950	+191 49	- 80
849 260	+185 75	- 1 33
909 560	+177 95	- 2 13
939 710	+172 51	- 2 98
1000 000	+166 85	- 2 78

Measurements at RF & LO Power +7 dBm

Mini-Circuits P.O BOX 166, Brooklyn, New York 11235 (718) 934-4500

5 to 1000 MHz

Mini-Circuits

00-39

mixer harmonic intermodulation

(relative to desired IF output)

RF CAL	0	1	2	3	4	5	6	7	8	9	10
0	-	-	17	40	25	35	25	41	30	48	41	61
1		19	-	28	12	34	22	45	42	43	59	49
2	80	58	46	63	44	66	47	56	45	51	43	60
3	95	41	51	37	46	57	82	68	45	60	54	55
4	96	78	69	70	75	65	66	68	57	73	66	62
5	96	68	75	64	60	64	54	62	54	68	55	69
6	94	86	85	86	81	78	71	78	68	77	70	75
7	96	82	84	85	80	79	74	75	73	71	75	76
8	97	86	85	87	84	85	86	85	85	81	93	81
9	96	86	85	86	85	86	84	85	83	85	80	81
10	95	86	85	86	87	85	87	85	85	85	84	84

RF ORDER HARMONIC

Harmonic LO Order

Test conditions: fR RF FREQ 500 1 MHz LEVEL 4 03 DBM
LO RF FREQ 470 01 MHz LEVEL 7 01 DBM
IF MEASURED FREQ 30 092 MHz AMP -10 25 DBM

RF CAL	0	1	2	3	4	5	6	7	8	9	10
0	-	-	8	30	14	25	11	28	16	37	24	51
1		18	-	27	11	33	21	39	39	36	52	41
2	96	66	56	69	54	68	52	64	52	57	49	56
3	94	61	66	68	62	72	66	76	63	75	69	74
4	96	75	75	77	77	76	77	75	76	74	75	76
5	95	75	75	75	76	78	76	76	75	75	76	75
6	95	74	74	75	75	77	75	76	76	77	76	74
7	97	76	75	75	76	75	75	77	77	76	75	75
8	95	75	75	75	75	75	75	77	75	77	76	75
9	96	76	75	75	75	75	75	75	75	75	76	76
10	96	75	75	76	77	75	75	75	76	76	76	76

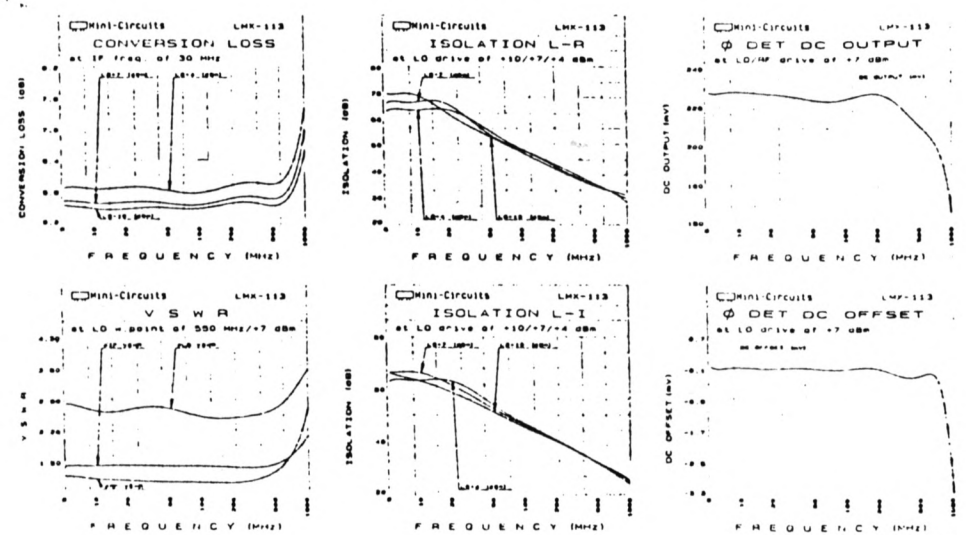
RF ORDER HARMONIC

Harmonic LO Order

Test conditions: fR RF FREQ 500 1 MHz LEVEL 4 03 DBM
LO RF FREQ 470 01 MHz LEVEL 7 01 DBM
IF MEASURED FREQ 30 092 MHz AMP -20 08 DBM

typical performance curves

(production unit)



ERAMIC GaAs HYPERABRUPT TUNING VARACTORS — ONSTANT GAMMA ≅ 1.25

: MA-46560 and MA-46570 series of microwave
ing varactors are hyperabrupt junction gallium
enide devices featuring a constant gamma of 1.25.
ecially high Q factors (up to 4000) permit extremely
ar broadband tuning performance through Ka-band.
: Q of these devices is similar to that of abrupt
ction varactors. Standard capacitance matching is
0%. All diode types in these series may be sup-
d in a wide selection of ceramic packages as well
in chip form.

se series are especially designed for use in heavily
pled microwave oscillators and filters with wide
dwidth tuning requirements.

MA-46560 Series[1,2] — Constant Gamma GaAs Hyperabrupt Tuning Varactors

Breakdown Voltage[3] = 15 Volts Minimum

	C_{T-4} (pF) Capacitance Range[4,5,6]							
NIMUM Q[7]	0.5 MAX.	0.50 — 0.99	1.00 — 1.49	1.50 — 2.49	2.50 — 3.49	3.50 — 4.99	5.00 — 6.99	7.00 — 10.0
0	—	—	—	—	—	—	MA-46566A	MA-46567A
00	—	—	—	MA-46563B	MA-46564B	MA-46565B	MA-46566B	MA-46567B
00	MA-46560C	MA-46561C	MA-46562C	MA-46563C	MA-46564C	MA-46565C	MA-46566C	MA-46567C
00	MA-46560D	MA-46561D	MA-46562D	MA-46563D	MA-46564D	MA-46565D	—	—
00	MA-46560E	MA-46561E	MA-46562E	MA-46563E	—	—	—	—
00	MA-46560F	MA-46561F	—	—	—	—	—	—
C_{T-2}/C_{T-12}[10] MAX.	2.7	4.0	4.9	5.6	6.0	6.3	6.5	6.6
TYP.	2.3	3.4	4.1	4.6	4.9	5.1	5.3	5.4
MIN.	2.0	2.9	3.5	3.9	4.2	4.4	4.5	4.6

MA-46570 Series[1,2] — Constant Gamma GaAs Hyperabrupt Tuning Varactors

Breakdown Voltage[3] = 22 Volts Minimum

	C_{T-4} (pF) Capacitance Range[4,5,6]							
	0.5 MAX.	0.50 — 0.99	1.00 — 1.49	1.50 — 2.49	2.50 — 3.49	3.50 — 4.99	5.00 — 6.99	7.00 — 10.0
00	—	—	—	—	—	—	MA-46576A	MA-46577A
00	—	—	—	MA-46573B	MA-46574B	MA-46575B	MA-46576B	MA-46577B
500	MA-46570C	MA-46571C	MA-46572C	MA-46573C	MA-46574C	MA-46575C	MA-46576C	MA-46577C
000	MA-46570D	MA-46571D	MA-46572D	MA-46573D	MA-46574D	MA-46575D	—	—
000	MA-46570E	MA-46571E	MA-46572E	MA-46573E	—	—	—	—
000	MA-46570F	MA-46571F	—	—	—	—	—	—
C_{T-2}/C_{T-20}[10] MAX.	3.2	5.3	7.1	8.7	10.0	11.0	11.5	12.0
TYP.	2.6	4.3	5.7	6.9	7.8	8.4	8.9	9.3
MIN.	2.2	3.6	4.8	6.6	6.4	6.8	7.2	7.5

ee notes on page 53.

CERAMIC GaAs HYPERABRUPT TUNING VARACTORS— CONSTANT GAMMA ≅ 1.25 (CONT'D)

NOTES:

1. All GaAs tuning varactors in these series are available in case style 30 and many other ceramic case styles as well as in chip form. When ordering specify the desired case by adding the case designation as a suffix to the type number. For example: an MA-46561D-30 specifies a 15 volt tuning diode in case style 30 with C_{T-4} between 0.50 and 0.99 pF and a minimum Q (at −4 volts and 50 MHz) of 2000. Case style 30 is a ceramic to metal axial pronged hermetic package. For other package styles, contact factory representative.

2. Case parasitics (C_p and L_s) are given along with case outlines at the rear of this catalog. The C_p values listed typically have tolerances of ±0.02 pF. However, the actual case capacitance of each diode is measured to within ±0.0025 pF.

3. Breakdown voltage (V_B) is measured at 10 μA of reverse bias current.

4. Capacitance is measured at 1 MHz on a bridge which has been balanced with a shielded test holder connected in place, but open circuited. These shielded test holders are available for purchase. Contact the factory for further information.

5. Customer should specify, within the range indicated, the required capacitance. The nominal tolerance at −4 volts is ±10% of the customer requested value. Closer tolerances are available on request.

6. All junctions are hyperabrupt with nominal $\gamma \cong 1.25$, where:

$$C_J(V) = \frac{K}{(V + \phi)^{\gamma}}$$

and:

$C_J(V)$ = voltage dependent junction capacitance
V_R = applied reverse voltage
ϕ = built-in potential (1.2 volts)
γ = capacitance-voltage slope exponent (gamma)
K = constant

γ is within the limits $1.13 < \gamma < 1.40$ over the voltage range 2-12 volts for the MA-46560 series and 2-20 volts for the MA-46570 series. Total capacitance of packaged diodes will deviate from constant gamma characteristics depending on the value of the required junction capacitance and the package choice due to differences in case capacitance (C_p). The figures below illustrate typical total capacitance versus applied voltage for the MA-46570 series when case style 30 is selected and typical capacitance ratios versus applied voltage using case style 30.

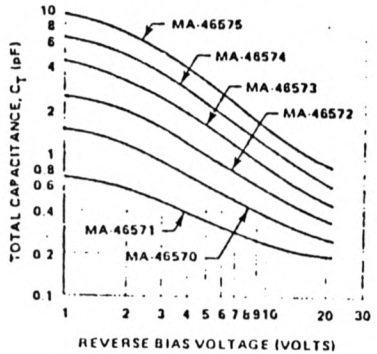
7. Diode Q is measured by a modified DeLoach technique at −4 volts and extrapolated to 50 MHz. (A copy of the article "Determination of Varactor Parameters by a Modified DeLoach Method" is available on request.)

8. All GaAs tuning diodes are subjected to a 48-hour 100°C electrical burn-in before final tests. During this period, each device is stressed 60 times per second with 30 mA in the forward direction and 5 volts in the back direction.

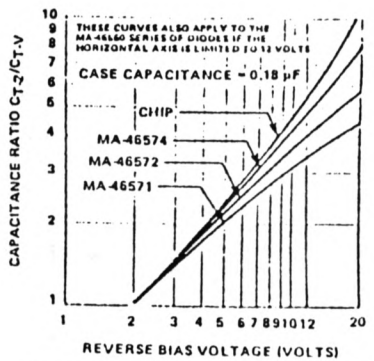
9. Parasitic inductance (L_s) has been determined at X-Band using a DeLoach method measurement.

10. The total capacitance ratios shown in the specifications are for devices housed in case style 30. Total capacitance ratios will vary with choice of case style.

TYPICAL PERFORMANCE



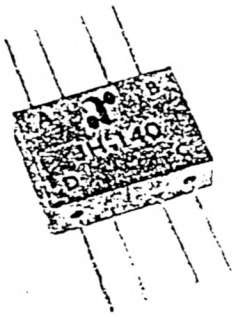
MA-46570 SERIES TOTAL CAPACITANCE VS REVERSE BIAS VOLTAGE (CASE STYLE 30)



MA-46570 SERIES CAPACITANCE RATIO VS REVERSE BIAS VOLTAGE (CASE STYLE 30)

MODEL JH-140 HIGH FREQUENCY QUADRATURE HYBRID 500-1000 MHz

- Octave Bandwidth
- Low VSWR — 1.2:1 Typical
- Miniature Size — ½" x ⅜" Flatpack



Guaranteed Specifications*

(From −55°C to +85°C)

Frequency Range	500-1000 MHz
Insertion Loss (Less coupling)	0.3 dB Max Avg**
Isolation	20 dB Min
Amplitude Balance	1.0 dB Max
VSWR	1.2:1 Max
Deviation from Quadrature	2° Max

Operating Characteristics

Impedance	50 Ohms Nominal
Input Power	25 Watts Max @ 25°C; Derated to 1 Watt @ 85°C
Package Type	Flatpack (FP-2) (See pages 340 to 349 for physical dimensions.)

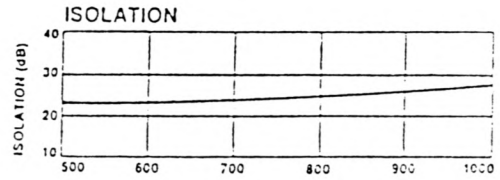
Environmental
These units are designed to meet the environmental requirements of Table 1A, page 358 of the Adams-Russell Electronics catalog.

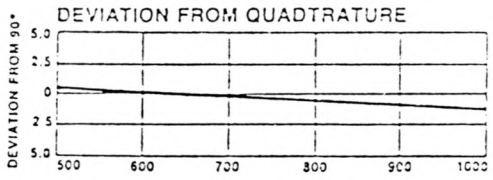
Pin Configuration	A; P1, B; P4, C, P8, D; P5. All other pins are ground.

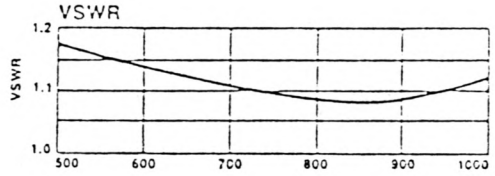
*All specifications apply with 50 ohm source and load impedance.

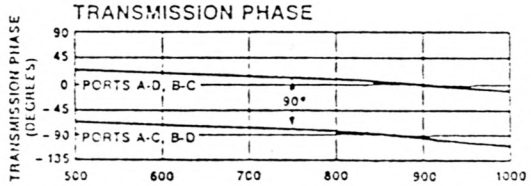
**Average of coupled outputs less 3 dB.

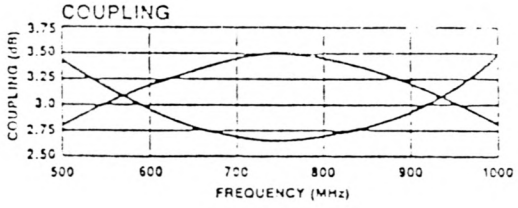
Typical Performance











Phasing Diagram

IN \ OUT	A	B	C	D
A		180	-90°	0°
B	180		0°	-90°
C	-90°	0°		180
D	0°	-90°	180	

Ordering Information

Model No.	Part No.	Connectors	Unit Price (5-9 Units)
JH-140	6619	Pin	$76

Delivery is from stock.

Adams Russell
ANZAC DIVISION

ANZAC...Make the Connection
80 Cambridge Street, Burlington, Mass. 01803-4107 (617) 273-3333 TWX 710•332•0258

ATC 100 UHF/MICROWAVE CAPACITORS

american technical ceramics
DIVISION OF PHASE IND., INC.

Performance Curves

ULTRA HIGH Q

is characteristic of the ATC 100 capacitors through microwave frequencies, even at high ambient temperatures, and under extremely high currents, permitting reliable operation at high power levels. Output power increases of greater than 20% per stage are reported when ATC 100's, with their negligible I^2R losses, are substituted for conventional capacitors. The reduction of losses also produces greater DC-to-RF conversion efficiency, improvements of 35% being reported. Improvements in Noise Figure are also attainable in receiver applications.

HIGH-POWER

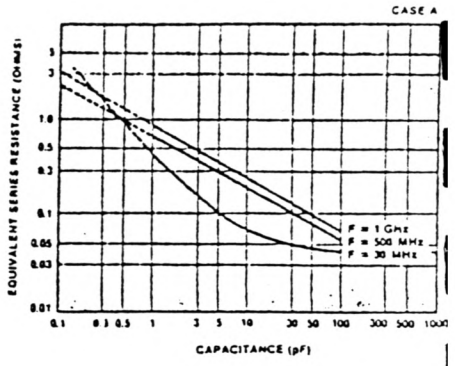
operation through microwave frequencies. Extremely low Equivalent Series Resistance (ESR) and high dielectric strength permit 15 KW pulse operation (900 watts average) at 500 MHz (3000 volts, 17 amps RF) in a 50 ohm system. Other typical applications are 500 watts (CW) at 1 GHz and 1 KW (avg.) at 50 ohms up to 3 GHz.

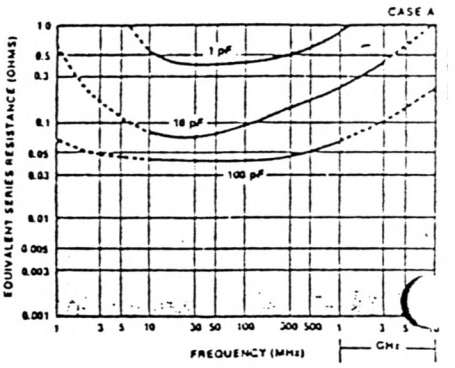
LOW NOISE FIGURE

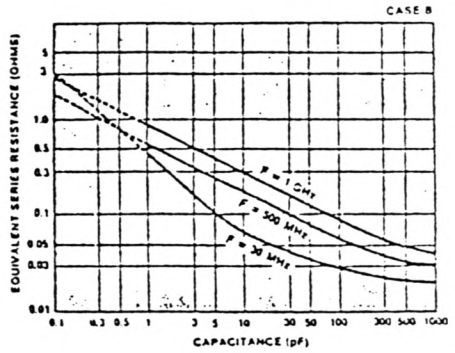
in receiving systems is achieved by the very low equivalent series resistance and extremely high Insulation Resistance (I.R.) of the ATC 100's. In an RF preamplifier, their low ESR helped attain a N.F. of 1.4 dB with a 1.2 dB transistor N.F. at 500 MHz. The high Insulation Resistance (ultra-low leakage) of an ATC 100 used as a calibration capacitor at the input of a charge storage amplifier on an X-Ray Spectrometer made possible a threshold sensitivity of 150 eV.

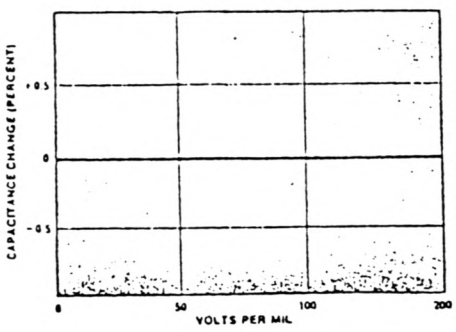
HIGH SELF-RESONANCE

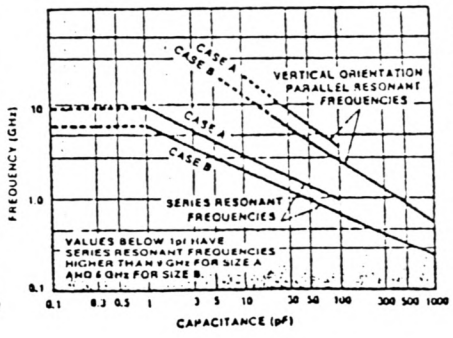
is shown by test data taken on a Hewlett Packard 8542A Network Analyzer covering S-Parameters, VSWR, Reactance, and Insertion Loss over the frequency range of 100 to 3000 MHz. Request **THE RF CAPACITOR HANDBOOK** for actual S-Parameter computer print-outs.

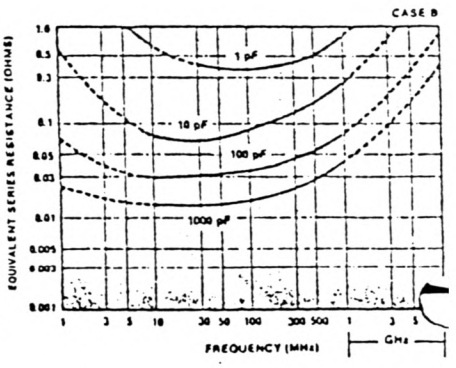












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Specifications

ELECTRICAL CHARACTERISTICS:

QUALITY FACTOR: (Qcap), greater than 10,000 at 1 MHz.

CAPACITANCE VALUES AND TOLERANCES:

Case A: standard values and tolerances from 0.1 pF to 100 pF.
Case B: standard values and tolerances from 0.1 pF to 1000 pF.

TEMPERATURE COEFFICIENT OF CAPACITANCE: +90 ±20 PPM/°C (−55°C to 125°C).

DIELECTRIC TEST VOLTAGE: 250% of WVDC rating for 5 secs.

RETRACE: Less than ±0.02% or 0.02 pF, whichever is greater.

AGING EFFECTS: None.

PIEZOELECTRIC EFFECTS: None (No capacitance variation with voltage or pressure).

CAPACITANCE DRIFT: ±0.02% or 0.02 pF, whichever is greater.

CAPACITANCE RANGE, INSULATION RESISTANCE, AND OPERATING VOLTAGE (WVDC) BY CASE SIZE

Case A: 0.1 pF to 100 pF (50 WVDC), 10^4 Megohms Min @ 25°C, 10^2 Megohms Min @ 125°C

Case B: 0.1 pF to 100 pF (500 WVDC), 10^4 Megohms Min @ 25°C, 10^2 Megohms Min @ 125°C
110 pF to 200 pF (300 WVDC), 10^4 Megohms Min @ 25°C, 10^2 Megohms Min @ 125°C
220 pF to 470 pF (200 WVDC), 10^4 Megohms Min @ 25°C, 10^2 Megohms Min @ 125°C
510 pF to 820 pF (100 WVDC), 10^4 Megohms Min @ 25°C, 10^2 Megohms Min @ 125°C
680 pF to 1000 pF (50 WVDC), 10^4 Megohms Min @ 25°C, 10^2 Megohms Min @ 125°C

LIFE TEST: 150% rated voltage for 2000 hours at 125°C as per MIL-STD-202C, method 108A (test condition F).

CHANGE IN CAPACITANCE: At 25°C; ±0.02% or 0.02 pF, whichever is greater.

QUALITY FACTOR: greater than 10,000 at frequency of 1 MHz.

INSULATION RESISTANCE: See table above; no degradation. Standard frequency measurements, 1 MHz, unless otherwise noted.

MECHANICAL CHARACTERISTICS:

HERMETICITY: The porcelain dielectric is non-porous and impervious to moisture and commonly used cleaning solvents.

TERMINATION STYLES: available in Case A as chips and pellets; Case B units as chips, pellets, and leaded devices.

TERMINAL STRENGTH: Microstrip, Axial Ribbon, and Radial Ribbon leaded capacitors withstand a lead pull of 5 lbs. for 5 seconds in the axis of the lead per MIL-STD-202, method 211.

OUTLINE DIMENSIONS: See Mechanical Configurations on page 7.

MARKING: All ATC Case A and Case B capacitors may be laser marked with manufacturer's identification, capacity and tolerance code.

ENVIRONMENTAL CHARACTERISTICS:

TEMPERATURE RANGE: From −55°C to +125°C (no derating of working voltage); above 125°C, derate linearly to 50% DCWV @ 200°C.

ATC 100 porcelain capacitors are designed and manufactured to meet or exceed the requirements of MIL-C-11272C, according to the methods of MIL-STD-202. ATC 100 series capacitors are available in all CY80D styles. See QPL list of MIL-C-11272C:FSC-5910.

Barometric pressure	(method 105, cond. B)
Shock	(method 213, cond. J)
Vibration	(method 204, cond. B)
Temperature Cycling	(method 102, cond. C)
Immersion	(method 104, cond. B)
Moisture resistance	(method 106)
Solderability	(method 208)
Terminal Strength	(method 211)
Salt Spray	(method 101, cond. B)

ATC SW 100 BOILING SALT WATER TEST:

Thermal Shock and Hermeticity Test

PURPOSE: To provide a non-destructive simulation of the thermal shock and degradation caused by contaminant absorption experienced during normal circuit mounting and cleaning.

PROCEDURE: With plastic tweezers, drop capacitors into a boiling salt water solution. Remove after two hours, wash thoroughly (distilled water), then dry at 150°C for 10 minutes.

MEASURE: I.R., capacity, and Q shall be within published specifications.

MILITARY SPECIFICATIONS:

ATC is on the QPL List for MIL-C-55681/4 and /5, BG (+90 ±20 PPM/°C) characteristic, and the QPL List for MIL-C-11272. Refer to the ATC Military Products Manual.

Capacity Values

CASE A mini-cube® capacitors are available only as chips and pellets from 0.1 pF through 100 pF in the values and tolerances listed below; working voltages 50 VDC.

CASE B MAXI-"Q"-UBE® capacitors are available in all values and tolerances at the working voltages shown in the table below. The Case B size may be ordered with a rating of 1000 WVDC, 0.1 pF to 47 pF, or with a rating of 100 WVDC, 680 pF to 1000 pF. To order, specify new WVDC in the ordering code.

CAP CODE	CAP (pF)	TOL.	WVDC 125°C
0R1	0.1	B	500
0R2	0.2		
0R3	0.3	BC	500
0R4	0.4		
0R5	0.5	BCD	500
0R6	0.6		
0R7	0.7		
0R8	0.8		
0R9	0.9		
1R0	1.0		
1R1	1.1		
1R2	1.2		
1R3	1.3		
1R4	1.4		
1R5	1.5		
1R6	1.6		
1R7	1.7		
1R8	1.8		
1R9	1.9		
2R0	2.0		
2R1	2.1		
2R3	2.3		
2R4	2.4		
2R7	2.7		
3R0	3.0		
3R3	3.3		
3R6	3.6		
3R9	3.9		

CAP CODE	CAP (pF)	TOL.	WVDC 125°C
4R3	4.3	BCD	500
4R7	4.7		
5R1	5.1		
5R6	5.6		
6R2	6.2		
6R8	6.8	BCJKM	500
7R5	7.5		
8R2	8.2		
9R1	9.1		
100	10	FGJKM	500
110	11		
120	12		
130	13		
150	15		
160	16		
180	18		
200	20		
220	22		
240	24		
270	27		
300	30		
330	33		
360	36		
390	39		
430	43		
470	47		
510	51		
560	56		
620	62		

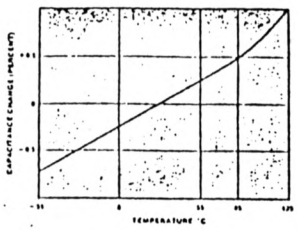
CAP CODE	CAP (pF)	TOL.	WVDC 125°C
680	68	FGJKM	500
750	75		
820	82		
910	91		
101	100		
111	110	FGJKM	300
121	120		
131	130		
151	150		
161	160		
181	180		
201	200		
221	220	FGJKM	200
241	240		
271	270		
301	300		
331	330		
361	360		
391	390		
431	430		
471	470		
511	510	FGJKM	100
561	560		
621	620		
681	680	FGJKM	50
751	750		
821	820		
911	910		
102	1000		

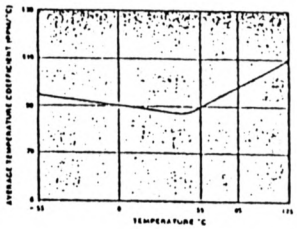
TOLERANCE CODE:

B = ±0.1 pF
C = ±0.25 pF
D = ±0.5 pF
F = ±1%
G = ±2%
J = ±5%
K = ±10%
M = ±20%

*MAXI-"Q"-UBE® and mini-cube® are registered trademarks of ATC.

Stability





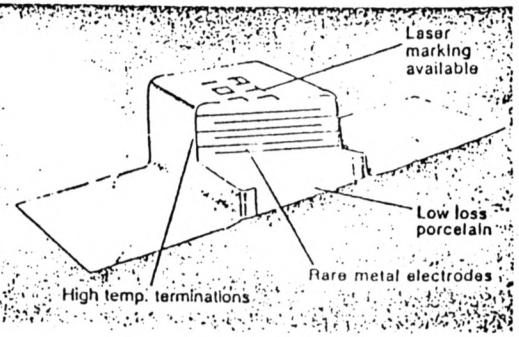
ULTRA-STABLE

performance is assured by the self-encapsulating porcelain construction. ATC 100's provide absolute retrace, no measurable drift, and complete stability under extremes of voltage, frequency, time and temperature. They are ideal for high-power, high-current, tuning, or impedance-matching applications.

Structure

SELF-ENCAPSULATING PORCELAIN CONSTRUCTION

Rare metal internal electrodes are molecularly bonded and sealed in a monolith of non-porous porcelain. The ATC 100 is a hermetic, microminiature, self-encapsulated, high voltage, porcelain chip capacitor matched to the thermal coefficient of expansion of commonly used substrate materials.



RUGGED TERMINATIONS

The ATC barrierCap® termination is now standard on all pellets (Pre-tinned capacitors). The terminations remain intact under the most severe thermal shock, and are not dissolved away even by the most careless soldering. They easily withstand a 5 minute submersion in 375°F solder pot without leaching, while retaining complete solderability. Migration is virtually eliminated and a bond strength greater than 30 lbs. is typical for "B" Case capacitors (110 mils square) with nail head leads.

HERMETIC

The severe thermal shock to which capacitors are subjected by direct soldering during circuit assembly can destroy the integrity of conventional capacitors, permitting flux and solvents to penetrate the dielectric. ATC porcelain capacitors are hermetic and are not degraded by the assembly process.

A simple and easy hermeticity test to simulate the thermal shock of soldering and subsequent absorption of contaminants is to drop the capacitor into boiling salt water. Remove, wash and verify hermeticity by retesting I.R., capacity, and Q. (For details, see ATC SW 100 Boiling Salt Water Test on page 4.)

RELIABILITY

Reliability after circuit assembly is outstanding due to the rugged and hermetic structure provided by the self-encapsulated porcelain construction. ATC's design of the chip capacitor internal structure and dielectric has resulted in the most reliable porcelain capacitors available proven by extensive testing programs of approximately 2 million component hours per month.

ATC has complete Government approved Hi-Rel testing facilities as well as RF production testing capability through 2.5 GHz.

LASER MARKING

Is available on ATC capacitors for quick and complete identification of capacitor source, value and tolerance. This highly legible and permanent marking results in no degradation of performance or reliability and is impervious to all cleaning solvents.

barrierCap® is a registered trademark of American Technical Ceramics

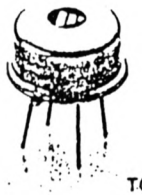
GPD-1002/-1062

Thin Film Cascadable Amplifier Module 5-1000 MHz

AVANTEK

FEATURES

- Medium Output Level: +6 dBm (Typ)
- Low Cost
- Small Size



TO-12 Case
(p. 403)

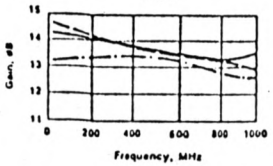
ELECTRICAL SPECIFICATIONS (Measured in a 50-ohm system @ +15 VDC nominal)

Symbol	Characteristic	Typical T_C = 25°C	Guaranteed Specifications T_C = 0°-50°C	Guaranteed Specifications T_C = -55°- +85°C	Unit
BW	Frequency Range	5-1000	5-1000	5-1000	MHz
GP	Small Signal Gain	13.0	12.0 Min.	11.0 Min.	dB
—	Gain Flatness	±1.0	—	—	dB
NF	Noise Figure	7.0	—	—	dB
—	Reverse Isolation	18.0			dB
$P_{1\,dB}$	Power Output @ +1 dB Compression	+6.0	—	—	dBm
—	Input VSWR	—	—	2.0:1 Max.	—
—	Output VSWR	—	—	2.0:1 Max.	—
IP_3	Two Tone 3rd Order Intercept Point	+16.0	—	—	dBm
IP_2	Two Tone 2nd Order Intercept Point	+19.0	—	—	dBm
I_D	DC Current	27		—	mA

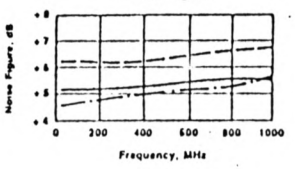
TYPICAL PERFORMANCE OVER TEMPERATURE (@ +15 VDC unless otherwise noted)

KEY: +25°C ——— +85°C — — — -55°C —·—·—

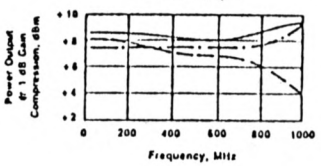
Gain



Noise Figure



Power Output



MAXIMUM RATINGS

DC Voltage	+17 Volts
Continuous RF Input Power	+13 dBm
Operating Case Temperature	-55°C to +125°C
Storage Temperature	-62°C to +150°C
"R" Series Burn-In Temperature	+125°C

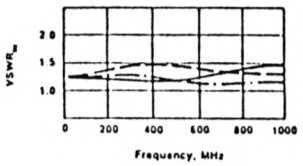
THERMAL CHARACTERISTICS*

θ_{JC}	160°C/W
Active Transistor Power Dissipation	81.6 mW
Junction Temperature Above Case Temperature	13°C
MTBF	1,639,228 (1002)/1,882,476 (1062) Hrs.

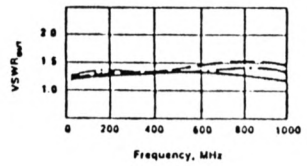
*For further information, see High Reliability section.

WEIGHT: (typical) — 1.5 grams

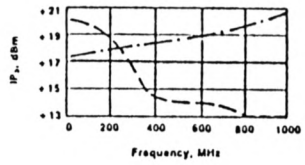
Input VSWR



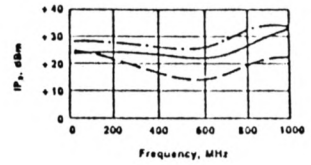
Output VSWR



Third-Order Intercept Point



Second-Order Intercept Point



AUTOMATIC NETWORK ANALYZER MEASUREMENTS (Typical production unit at +25°C ambient)

NUMERICAL READINGS — BIAS = 15.00 VOLTS

FREQ MHz	VSWR IN	GAIN dB	PHASE DEG	PHASE DEV	GPDEL NSEC	VSWR OUT	ISOL dB
100.0	1.29	14.23	174.38	-.18	.00	1.26	24.09
200.0	1.28	14.06	167.94	-.52	.18	1.27	23.33
300.0	1.21	13.97	161.47	-.93	.18	1.29	23.49
400.0	1.17	13.83	156.06	-.27	.14	1.30	23.05
500.0	1.18	13.67	150.80	.53	.14	1.31	22.61
600.0	1.23	13.57	145.27	1.08	.16	1.30	22.14
700.0	1.30	13.44	139.93	1.82	.17	1.29	21.64
800.0	1.39	13.43	133.32	1.29	.18	1.28	21.23
900.0	1.44	13.41	125.77	-.18	.26	1.20	20.79
1000.0	1.49	13.53	115.90	-3.99	.33	1.18	18.94
1100.0	1.76	13.51	100.89		.48	1.25	18.43
1200.0	2.74	12.87	80.86		.59	1.43	18.56
1300.0	5.08	10.21	60.92		.44	1.57	21.81

S-PARAMETERS, MAGNITUDES AND ANGLES — BIAS = 15.00 VOLTS

FREQ	11		21		12		22	
MHz	RATIO	ANGLE	dB	ANGLE	dB	ANGLE	RATIO	ANGLE
100.00	.130	177.2	14.212	174.2	-23.883	10.1	.114	1.0
200.00	.115	174.5	14.090	168.1	-23.830	14.4	.118	9.1
300.00	.094	177.6	13.974	161.6	-23.220	23.4	.127	9.4
400.00	.081	-166.4	13.831	156.2	-22.778	31.2	.130	9.0
500.00	.081	-150.8	13.638	150.9	-22.618	36.0	.134	8.5
600.00	.102	-139.1	13.535	145.2	-22.092	41.8	.132	3.1
700.00	.131	-138.6	13.423	139.8	-21.605	45.5	.127	-1.0
800.00	.162	-150.8	13.412	133.3	-21.127	48.1	.115	-6.2
900.00	.178	-171.3	13.416	126.0	-20.662	48.3	.097	-5.4
1000.00	.197	151.2	13.496	116.0	-19.983	47.6	.084	10.0
1100.00	.272	95.7	13.510	101.1	-19.447	42.2	.112	29.1
1200.00	.462	40.7	12.865	81.0	-20.068	34.7	.175	19.4
1300.00	.868	-4.2	10.191	60.9	-21.823	26.8	.225	-4.7
1400.00	.793	-37.1	6.343	51.1	-24.091	28.3	.213	-28.4
1500.00	.837	-58.2	2.570	50.1	-25.353	36.2	.174	-48.3

GPD-1003/-1063

Thin Film Cascadable Amplifier 5-1000 MHz

AVANTEK

FEATURES

- +14.0 dBm Output Power
- Low Cost
- Small Size

TO-12 Case
(p. 403)

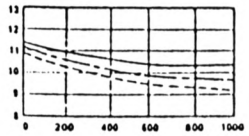
ELECTRICAL SPECIFICATIONS (Measured in a 50-ohm system @ +15 VDC nominal)

Symbol	Characteristic	Typical T_C = 25°C	Guaranteed Specifications T_C = 0°-50°C	Guaranteed Specifications T_C = -55°- +85°C	Unit
BW	Frequency Range	5-1000	5-1000	5-1000	MHz
GP	Small Signal Gain	10.5	10.0 Min.	9.0 Min.	dB
—	Gain Flatness	±1.0	—	—	dB
NF	Noise Figure	7.0	—	—	dB
—	Reverse Isolation	18.0			dB
$P_{1\ dB}$	Power Output @ +1 dB Compression	+14.0	—	—	dBm
—	Input VSWR	1.50:1	—	2.0:1 Max.	—
—	Output VSWR	1.30:1	—	2.0:1 Max.	—
IP_3	Two Tone 3rd Order Intercept Point	+25.0	—	—	dBm
IP_2	Two Tone 2nd Order Intercept Point	+37.0	—	—	dBm
I_D	DC Current	55		—	mA

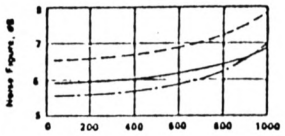
TYPICAL PERFORMANCE OVER TEMPERATURE (@ +15 VDC unless otherwise noted)

KEY: +25°C ——— +85°C — — — -55°C —·—·—

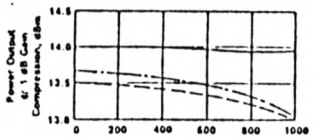
Gain



Noise Figure



Power Output



MAXIMUM RATINGS

DC Voltage	+17 Volts
Continuous RF Input Power	+13 dBm
Operating Case Temperature	-55°C to +125°C
Storage Temperature	-62°C to +150°C
"R" Series Burn-In Temperature	+125°C

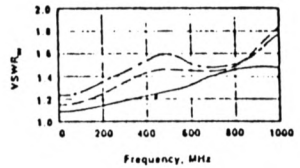
THERMAL CHARACTERISTICS*

θ_{JC}	105°C/W
Active Transistor Power Dissipation	225 mW
Junction Temperature Above Case Temperature	23.7°C
MTBF	869,341 (1003)/2,101,101 (1063) Hrs.

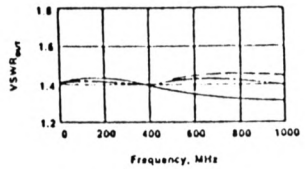
*For further information, see High Reliability section.

WEIGHT: (typical) — 1.5 grams

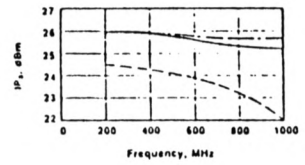
Input VSWR



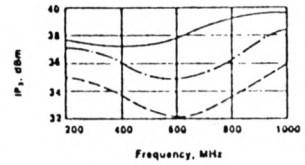
Output VSWR



Third-Order Intercept Point



Second-Order Intercept Point



AUTOMATIC NETWORK ANALYZER MEASUREMENTS (Typical production unit @ +25°C ambient)

NUMERICAL READINGS — BIAS = 15.00 VOLTS

FREQ MHz	VSWR IN	GAIN dB	PHASE DEG	PHASE DEV	GPDEL NSEC	VSWR OUT	ISOL dB
100.0	1.13	11.32	161.40	-.80	.00	1.46	22.29
200.0	1.17	11.18	141.34	-1.28	.54	1.43	22.12
300.0	1.23	11.14	122.54	-.66	.51	1.39	21.89
400.0	1.27	10.98	104.21	.36	.51	1.34	21.62
500.0	1.31	10.84	86.05	1.58	.53	1.29	21.29
600.0	1.36	10.72	66.56	1.47	.52	1.26	21.00
700.0	1.41	10.74	47.59	1.88	.57	1.28	21.02
800.0	1.53	10.67	26.70	.38	.56	1.22	19.34
900.0	1.50	10.75	6.68	-.23	.59	1.24	18.98
1000.0	1.54	10.88	-16.41	-3.94	.00	1.28	18.61

LINEARIZATION RANGE 100.0 TO 1000.0

S-PARAMETERS, MAGNITUDES AND ANGLES — BIAS = 15.00 VOLTS

FREQ	11		21		12		22	
MHz	RATIO	ANGLE	dB	ANGLE	dB	ANGLE	RATIO	ANGLE
100.00	.053	-123.2	11.016	171.9	-21.498	11.5	.149	-9.5
200.00	.086	-119.4	11.120	167.0	-22.603	5.8	.125	-18.6
300.00	.082	-127.5	11.249	160.5	-20.865	26.2	.148	-22.0
400.00	.104	-130.2	10.824	154.6	-21.173	25.7	.139	-36.5
500.00	.113	-132.5	10.857	148.1	-21.142	33.8	.141	-49.3
600.00	.137	-146.1	10.755	141.8	-21.214	33.8	.136	-64.1
700.00	.144	-157.4	10.768	135.9	-20.690	39.1	.147	-77.8
800.00	.153	-169.4	10.778	127.8	-20.598	43.3	.156	-83.8
900.00	.186	169.2	10.973	120.2	-19.731	40.8	.157	-109.0
1000.00	.207	136.3	11.218	109.3	-18.887	36.1	.160	-126.3
1100.00	.293	88.5	11.458	95.4	-20.163	40.2	.165	-152.0
1200.00	.455	32.3	10.592	76.2	-19.339	31.5	.144	-175.6
1300.00	.646	-15.4	8.449	55.5	-18.965	24.1	.132	166.3
1400.00	.763	-50.0	5.442	43.9	-21.462	20.8	.133	154.4
1500.00	.820	-75.6	2.852	38.0	-22.083	25.1	.133	138.6
1600.00	.862	-94.2	.174	37.8	-22.710	30.8	.145	117.1
1700.00	.892	-109.5	-2.115	35.7	-24.489	22.8	.163	102.4

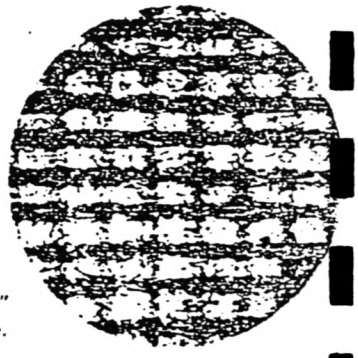
16"x10" RT/duroid 5880
Nominal thickness 0.062"
1 oz copper
AEEK 12 OCT 85

RT/duroid®

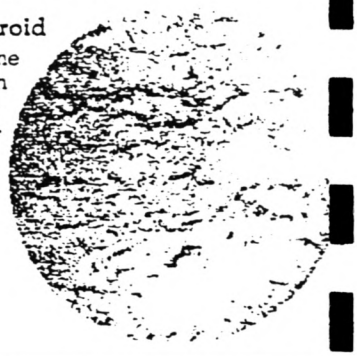
The Non-Woven Glass Microfiber-Reinforced PTFE Structure

ROGERS
MICROWAVE MATERIALS DIVISION
BOX 700 CHANDLER, ARIZONA 85224
PHONE (602) 961-1382
TWX 910-950-1961

G-10
1 oz electrodeposited



Woven Glass Laminate
Photomicrograph (55X) of typical woven glass laminate. Note "window" effect in fiber structure.



RT/duroid
Rogers material at same magnification. Note even dispersion of glass microfibers, uniform structure.

Availability

Thickness:
Standard and close tolerance laminates available in thicknesses ranging from .005" to .375"

Typical Thickness Tolerances, RT/duroid 5000 series

Nominal	Close	Extra Close
.010"	±.0007"	±.0005"
.031"	±.001"	±.0007"
.062"	±.002"	±.0015"
.125"	±.0035"	±.003"

Cladding:
1/2-, 1- and 2-ounce rolled and electrodeposited copper is standard. 1/8- and 1/4-ounce ED copper is available. 1/32", 1/16" and 1/8" aluminum standard; other foils and thicknesses on request.

Sheet Sizes:
Standard for RT/duroid 5000 series 16"x10", 16"x20", 16"x30" and 16"x40".
Standard for RT/duroid 6000 series 10"x10", 10"x20", and 20"x20".

Material	Dielectric Constant	Dissipation Factor
RT/duroid 5880	2.20 ± .02	.0009 typical
RT/duroid 5220	2.20 ± .02	.0011 typical
RT/duroid 5870	2.33 ± .02	.0012 typical
RT/duroid 5233	2.33 ± .02	.0014 typical
RT/duroid 5876	2.45 ± .04	.0015 typical
RT/duroid 6006	6.0 ± .25	.0020 typical
RT/duroid 6010.2	10.2 ± .25	.0020 typical
RT/duroid 6010.5	10.5 ± .25	.0020 typical

Design Characteristics

Uniform dielectric constant — Less than ±1% 10^6 through 10^{10} Hz.

Low dissipation factor — RT/duroids have very low dissipation factor at frequencies from 1 MHz up through X-band and beyond. RT/duroid 5880 is superior to all other stripline materials.

Dimensional stability — Withstand temperatures up to 550°F. Lay flat, do not warp.

Close thickness control — Tolerance of ±3% on overall laminate thickness.

Excellent bond strength — Average peel strength over 15 lbs./in. allows fine-line stripline to be made with ease. Excellent adhesion is maintained even after soldering, plating and exposure to elevated temperatures.

Environmental stability — Extremely low water absorption, coupled with 500°F plus temperature resistance, allows its application in the most demanding military or commercial systems.

ANALOG DEVICES

Ultra-Low Noise Precision Op Amp

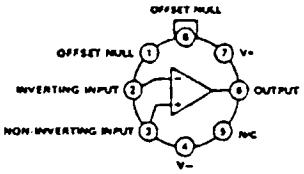
AD OP-27

4

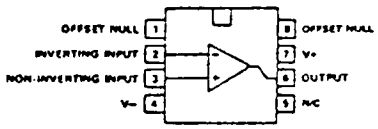
FEATURES

- Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
- Ultra-Low Offset Voltage Drift: 0.2μV/°C
- High Offset Stability Over Time: 0.2μV/month
- High Slew Rate: 2.8V/μs
- High Gain Bandwidth Product: 8MHz
- Low Offset Voltage: 10μV
- High CMRR: 126dB over ±11V Input Voltage Range
- Fits OP-07, OP-05, OP-06, 5534, 725, 714 and 741 Sockets

AD OP-27 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW



8-PIN MINI DIP
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs slew rate and an 8MHz gain bandwidth product are possible without sacrificing dc accuracy. Long term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ±10nA and an input offset current of 7nA. An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ±20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-27 is available in six performance grades. The AD OP-27E, AD OP-27F and AD OP-27G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-27A, AD OP-27B and AD OP-27C are specified for −55°C to +125°C operation. All devices are available in TO-99 hermetically sealed metal cans, while the E, F and G grades are also packaged in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. Precision amplification of very low level, low frequency voltage inputs is enhanced by ultra-low input voltage noise.
2. The AD OP-27 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-27G			AD OP-27F			AD OP-27E		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	700 – 200 450	1,500 1,500 500 1,000		1,000 800 250 700	1,800 1,500 700 1,300		1,000 800 250 750	1,800 1,500 700 1,500	
OUTPUT CHARACTERISTICS Voltage Swing	V_O	±11.5 ±10.0 ±11.0	±13.5 ±11.5 ±13.2		±12.0 ±10.0 ±11.4	±13.8 ±11.5 ±13.5		±12.0 ±10.0 ±11.7	±13.8 ±11.5 ±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE Gain Bandwidth Product Slew Rate	GBW SR	5.0 1.7	8.0 2.8		5.0 1.7	8.0 2.8		5.0 1.7	8.0 2.8	
INPUT OFFSET VOLTAGE Initial	V_{OS}		30 55	100 220		20 40	60 140		10 20	25 50
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	0.6
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT Initial	I_B		±15 ±25	±80 ±150		±12 ±18	±55 ±95		±10 ±14	±40 ±60
INPUT OFFSET CURRENT Initial	I_{OS}		12 20	75 135		9 14	50 85		7 10	35 50
INPUT NOISE Voltage	e_{n} p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	I_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE Common Mode	CMVR	±11.0 ±10.5	±12.3 ±11.8		±11.0 ±10.5	±12.3 ±11.8		±11.0 ±10.5	±12.3 ±11.8	
Common-Mode Rejection Ratio	CMRR	100 96	120 118		106 102	123 121		114 110	126 124	
INPUT RESISTANCE Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	5.6		3.0	4.6		3.0	4.6
Rejection	PSR		2	20		1	10		1	10
			2	32		2	16		2	15
Power Consumption	P_d		100	170		90	140		90	140
OPERATING TEMPERATURE RANGE	T_{MIN}, T_{MAX}	–25		+85	–25		+85	–25		+85

AD OP-27C			AD OP-27B			AD OP-27A			CONDITIONS	UNITS
MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
700 – 200 300	1,500 1,500 500 800		1,000 800 250 500	1,800 1,500 700 1,000		1,000 800 250 600	1,800 1,500 700 1,200		$R_L \geq 2k\Omega$, V_{OUT} = ±10V $R_L \geq 1k\Omega$, V_{OUT} = ±10V R_L = 600Ω, V_{OUT} = ±1V, V_S = ±4V $R_L \geq 2k\Omega$, V_{OUT} = ±10V, T_A = min to max	V/mV V/mV V/mV V/mV
±11.5 ±10.0 ±10.5	±13.5 ±11.5 ±13.0 70		±12.0 ±10.0 ±11.0	±13.8 ±11.5 ±13.2 70		±12.0 ±10.0 ±11.5	±13.8 ±11.5 ±13.5 70		$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$ $R_L \geq 2k\Omega$, T_A = min to max I_{OUT} = 0A, V_{OUT} = 0V	V V V Ω
5.0 1.7	8.0 2.8		5.0 1.7	8.0 2.8		5.0 1.7	8.0 2.8		$R_L \geq 2k\Omega$	MHz V/μs
	30 70 0.4 0.4 ±4.0	100 300 1.8 2.0		20 50 0.3 0.3 ±4.0	60 200 1.3 1.5		10 30 0.2 0.2 ±4.0	25 60 0.6 1.0	(Note 1) T_A = min to max T_A = min to max (Note 2) (Note 3) R_p = 10kΩ	μV μV μV/°C μV/month mV
	±15 ±35	±80 ±150		±12 ±28	±55 ±95		±10 ±20	±40 ±60	T_A = min to max	nA nA
	12 30	75 135		9 22	50 85		7 15	35 50	T_A = min to max	nA nA
	0.09 3.8 3.3 3.2 1.7 1.0 0.4	0.25 8.0 5.6 4.5 – – 0.6		0.08 3.5 3.1 3.0 1.7 1.0 0.4	0.18 5.5 4.5 3.8 4.0 2.3 0.6		0.08 3.5 3.1 3.0 1.7 1.0 0.4	0.18 5.5 4.5 3.8 4.0 2.3 0.6	0.1Hz to 10Hz f_o = 10Hz f_o = 30Hz f_o = 1000Hz f_o = 10Hz f_o = 30Hz f_o = 1000Hz	μV p-p nV/√Hz nV/√Hz nV/√Hz pA/√Hz pA/√Hz pA/√Hz
±11.0 ±10.2	±12.3 ±11.5		±11.0 ±10.3	±12.3 ±11.5		±11.0 ±10.3	±12.3 ±11.5		T_A = min to max	V V
100 94	120 116		106 100	123 119		114 108	126 122		V_{CM} = ±11V V_{CM} = ±10V, T_A = min to max	dB dB
0.8	4 2		1.2	5 2.5		1.5	6 3			MΩ GΩ
	±15 ±(4–18) 3.3 2 4 100	 5.6 20 51 170		±15 ±(4–18) 3.0 1 2 90	 4.6 10 20 140		±15 ±(4–18) 3.0 1 2 90	 4.6 10 16 140	V_S = ±15V V_S = ±4V to ±18V V_S = ±4.5V to ±18V, T_A = min to max V_{OUT} = 0V	V V mA μV/V μV/V mW
–55		+125	–55		+125	–55		+125		°C

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with R_p = 8kΩ to 20kΩ.

[3]Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ANALOG DEVICES

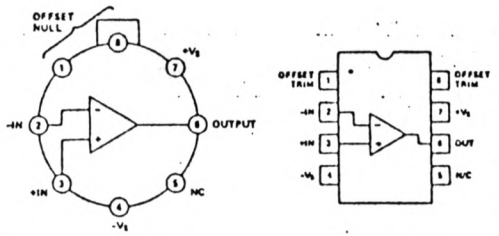
Ultra-Low Offset Voltage Op Amp

AD OP-07

FEATURES

Ten Times More Gain Than Other OP-07 Devices (3.0M min)
Ultra-Low Offset Voltage: 10μV
Ultra-Low Offset Voltage Drift: 0.2μV/°C
Ultra-Stable vs. Time: 0.2μV/month
Ultra-Low Noise: 0.35μV p-p
No External Components Required
Monolithic Construction
High Common Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A Sockets

AD OP-07 FUNCTIONAL BLOCK DIAGRAM



H-PACKAGE N-PACKAGE

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as 10μV, bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C and long-term stability of 0.2μV/month eliminate recalibration or loss of initial accuracy.

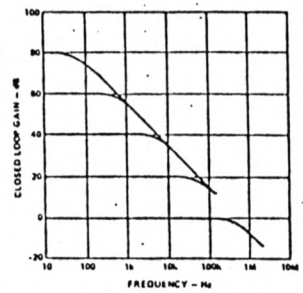
A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range (±14V) high common mode rejection ratio (up to 126dB) and high differential input impedance (50MΩ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. The devices are packaged in either TO-99 hermetically-sealed metal cans or plastic 8-pin mini DIPS.

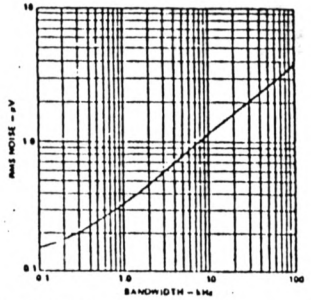
PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

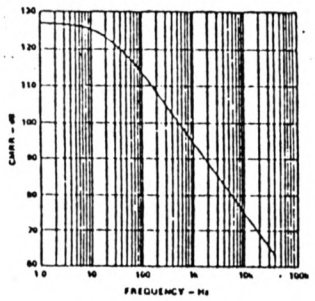
Typical Performance Curves



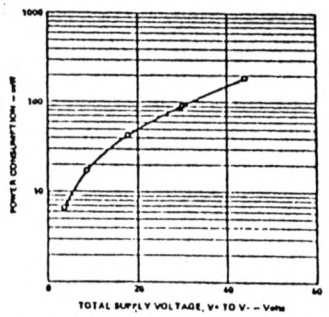
Closed Loop Response for Various Gain Configurations



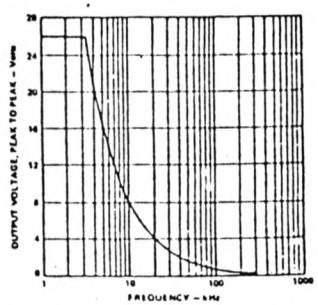
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



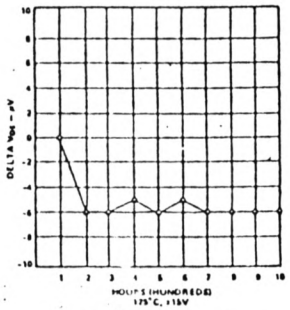
CMRR vs. Frequency



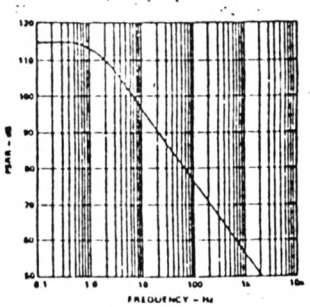
Power Consumption vs. Power Supply



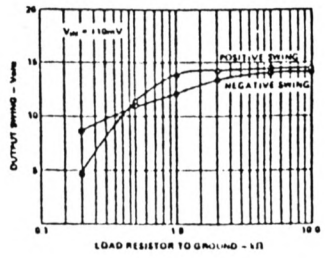
Maximum Undistorted Output vs. Frequency



Offset Voltage vs. Time



PSRR vs. Frequency



Output Voltage vs. Load Resistance

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-07E			AD OP-07C			AD OP-07D		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	2,000	5,000		1,200	4,000		1,200	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0	
		±12.0	±12.8		±11.5	±12.8		±11.5	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	75		60	150		60	150
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift							(Note 2)			(Note 2)
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	(Note 2) 2.0		0.5	(Note 2) 1.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		0	35 (Note 2)		12	50 (Note 2)		12	50 (Note 2)
INPUT BIAS CURRENT										
Initial	I_B		±1.2	±4.0		±1.8	±7.0		±2.0	±12
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13	35 (Note 2)		18	50 (Note 2)		18	50 (Note 2)
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{IN} CM		160			120			120	
INPUT NOISE										
Voltage	e_n P-P		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.2	13.5
			10.0	13.0		10.2	13.5		9.8	11.5
			9.6	11.0		9.8	11.5		9.6	11.0
Current	i_n P-P		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	±13.0	±14.0		±13.0	±14.0		±13.0	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common Mode Rejection Ratio	CMRR	106	123		100	120		94	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	4.0		3.5	5.0		3.5	5.0
Power Consumption	P_D		90	120		105	150		105	150
			6.0	8.4		6.0	8.4		6.0	8.4
Rejection Ratio	PSRR	94	107		90	104		90	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PACKAGE OPTION[4]										
"N" Package										
8 Pin MINI DIP — (N8A)			AD OP-07EN			AD OP-07CN			AD OP-07DN	
"H" Package										
TO 99 — (H08B)			AD OP-07EH			AD OP-07CH			AD OP-07DH	

NOTES

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 23°C, −55°C and +125°C.

[2] Parameter is not 100% tested; 90% of units meet this specification.

[3] Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested; 90% of units meet this specification.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

AD OP-07AH			AD OP-07H				
MIN	TYP	MAX	MIN	TYP	MAX	TEST CONDITIONS	UNITS
3,000	5,000		2,000	5,000		$R_L \geq 2k\Omega$, V_O = ±10V	V/mV
2,000	4,000		1,500	4,000		$R_L \geq 2k\Omega$, V_O = ±10V, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3V	V/mV
±12.5	±13.0		±12.5	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		±12.0	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		±10.5	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		±12.0	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		V_O = 0, I_O = 0	Ω
	0.6			0.6		A_{VCL} = +1.0	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	25		30	75	Note 1	μV
	25	60		60	200	Note 1, T_{min} to T_{max}	μV
	±4			±4		R_P = 20kΩ	mV
	0.2	0.6		0.3	1.3	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	R_P = 20kΩ, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 3	μV/Month
	0.3	2.0		0.4	2.8		nA
	0.8	4.0		1.2	5.6	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	±2.0		±1.0	±3.0		nA
	±1.0	±4.0		±2.0	±6.0	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz, Note 2	μV p-p
	10.3	18.0		10.3	18.0	f_O = 10Hz, Note 2	nV/√Hz
	10.0	13.0		10.0	13.0	f_O = 100Hz, Note 2	nV/√Hz
	9.6	11.0		9.6	11.0	f_O = 1kHz, Note 2	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz, Note 2	pA p-p
	0.32	0.80		0.32	0.80	f_O = 10Hz, Note 2	pA/√Hz
	0.14	0.23		0.14	0.23	f_O = 100Hz, Note 2	pA/√Hz
	0.12	0.17		0.12	0.17	f_O = 1kHz, Note 2	pA/√Hz
±13.0	±14.0		±13.0	±14.0			V
±13.0	±13.5		±13.0	±13.5		T_{min} to T_{max}	V
110	126		110	126		V_{CM} = ±CMVR	dB
106	123		106	123		V_{CM} = ±CMVR, T_{min} to T_{max}	dB
	3.0	4.0		3.0	3.8	V_S = ±15V	mA
	90	120		90	120	V_S = ±15V	mW
	6.0	8.4		6.0	8.4	V_S = ±3V	mW
100	110		100	110		V_S = ±3V to ±18V	dB
94	106		94	106		V_S = ±3V to ±18V, T_{min} to T_{max}	dB
-55		+125	-55		+125		°C
AD OP-07AH			AD OP-07H				

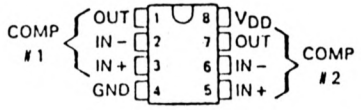
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TYPES TLC372M, TLC372C
DUAL LinCMOS™ DIFFERENTIAL COMPARATORS

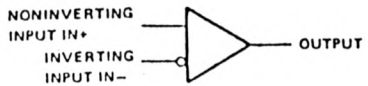
D2821, NOVEMBER 1983

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages
  2 to 18 Volts
- Very Low Supply Current Drain
  0.2 mA Typ
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Ω Typ
- Extremely Low Input Bias Current
  1 pA Typ
- Ultra-Stable Low Input Offset Voltage
- Common-Mode Input Voltage Range Includes Ground
- Output Compatible with TTL, MOS, and CMOS

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol (each comparator)



iption

his device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators designed o operate from a single power supply. Operation from dual supplies is also possible so long as the difference between he two supplies is 2 to 18 volts. Each of these devices features extremely high input impedance (typically greater han 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain onfigurations, and can be connected to achieve positive-logic wired-AND relationships.

hese devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures t voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised n handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

he TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372C s characterized for operation from 0°C to 70°C.

4 4 Voltage Comparators

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PRODUCT PREVIEW
ument contains information on a product under ment. Texas Instruments reserves the right to e discontinue this product without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC374M	TLC374C	UNIT
Supply voltage, V_{DD} (see Note 1)		18	18	V
Differential input voltage (see Note 2)		±18	±18	V
Input voltage, V_I		18	18	V
Output voltage, V_O		18	18	V
Output current, I_O		20	20	mA
Duration of output short-circuit to ground (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, TLC374C chips are glass mounted and TLC374M chips are alloy mounted.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC372M MIN	TLC372M TYP	TLC372M MAX	TLC372C MIN	TLC372C TYP	TLC372C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 5		25°C		2	10		2	10	mV
				Full range			12			12	
I_{IO}	Input offset current	See Note 5		25°C		1			1		pA
				Full range			10			0.3	nA
I_{IB}	Input bias current			25°C		1					pA
				Full range			20			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} − 1.5			0 to V_{CC} − 1.5			V
				Full range	0 to V_{CC} − 2			0 to V_{CC} − 2			
A_{VD}	Large-signal differential voltage amplification	V_{DD} = 15 V, R_L ≥ 15 kΩ to V_{DD}		25°C		200			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} 4 mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		0.2			0.2		mA

†All characteristics are measured with zero common-mode input voltage unless otherwise specified.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output up to 4 V or down to 400 mV with a pull-up resistor of 2.5 kΩ to V_{DD}. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance. Full range for T_A is −55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF†, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

†C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

George/Mark
please order 10 more of these RFR

MITSUBISHI SEMICONDUCTOR <GaAs FET>

MGF-1402 (2SK274)

FOR MICROWAVE LOW NOISE AMPLIFIERS
N-CHANNEL SCHOTTKY BARRIER GATE TYPE

DESCRIPTIONS

The MGF-1402 (2SK274) is a low-noise GaAs FET with an N-channel Schottky gate, which is designed for use in S to X-band amplifiers and oscillators. The hermetically sealed metal-ceramic package assures minimum parasitic losses, and has a configuration suitable for microstrip circuits.

FEATURES

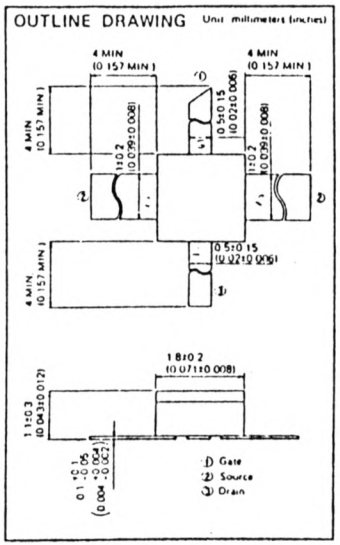
- High maximum frequency of oscillation fmax = 70 GHz (TYP)
- Low noise figure NF = 1.1 dB (TYP) @f = 4GHz
- High associated gain Gs = 13 dB (TYP) @f = 4GHz
- High RF input power capability
- High reliability and stability

APPLICATIONS

S to X-band low noise amplifiers and oscillators

OUTLINE DRAWING

Unit: millimeters (inches)



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Symbol	Parameter	Limits	Unit
V_{GDO}	Gate to drain voltage	−6	V
V_{GSO}	Gate to source voltage	−6	V
V_{DSX}	Drain to source voltage	8	V
I_D	Drain current	100	mA
P_T	Total power dissipation	300	mW
T_{ch}	Channel temperature	150	°C
T_{stg}	Storage temperature	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Symbol	Parameter	Conditions		Values MIN	Values TYP	Values MAX	Unit
$V_{(BR)GSS}$	Gate to source breakdown voltage	I_G = −100μA, V_{DS} = 0V		−6			V
I_{GSS}	Gate to source leakage current	V_{GS} = −3V, V_{DS} = 0V				10	μA
$I_{D(off)}$	Drain cut off current	V_{GS} = −5V, V_{DS} = 5V				200	μA
I_{DSS}	Saturated drain current	V_{GS} = 0V, V_{DS} = 3V		30	70	100	mA
$V_{GS(off)}$	Gate to source cut off voltage	V_{DS} = 3V, I_D = 100μA		−1		−5	V
g_m	Transconductance	V_{DS} = 3V, I_D = 30mA		25	35		mS
G_s	Associated gain	V_{DS} = 3V, I_D = 10mA	f = 4GHz	11	13		dB
			f = 8GHz		10		
			f = 12GHz		8		
NF_{min}	Minimum noise figure	V_{DS} = 3V, I_D = 10mA	f = 4GHz		1.1	1.4	dB
			f = 8GHz		2.0		
			f = 12GHz		3.0		
MAG	Maximum available gain	V_{DS} = 3V, I_D = 30mA	f = 4GHz		18		dB
			f = 8GHz		13		
			f = 12GHz		10		
f_{max}	Maximum frequency of oscillation	V_{DS} = 3V, I_D = 30mA			70		GHz

MITSUBISHI ELECTRIC

MITSUBISHI SEMICONDUCTOR <GaAs FET>

MGF-1402 (2SK274)

FOR MICROWAVE LOW NOISE AMPLIFIERS
N-CHANNEL SCHOTTKY BARRIER GATE TYPE

HANDLING PRECAUTIONS FOR GaAs FETs

1. Check of Electrical Characteristics

(1) Measurement of DC Characteristics by Curve Tracer

Many curve tracers, if not properly grounded, exhibit a high leakage current from the high-voltage transformer, which can be a prime cause of failure or degradation of the FET. Measurement of the DC characteristics using a curve tracer is therefore not recommended. However, when tests using a curve tracer are required, first of all, check that the curve tracer is grounded to earth.

(2) Measurement of RF Characteristics

Before measurement, check that the measuring instruments are grounded to earth. Many instruments to measure RF characteristics such as RF power meters, network analyzers and so on, if not properly grounded to earth, sometimes allow a high AC leakage of up to several tens volts, which can be a cause of failure or degradation of the FET.

2. Installation of GaAs FET

When GaAs FET is soldered on a microstrip circuit, the following should be attended to,

(1) Properly ground the soldering iron to earth.

Leakage current from the soldering iron could cause failure or degradation of the FET.

(2) Solder the FET as promptly as possible at a low temperature. For a criterion, soldering in less than 8 seconds at a temperature of less than 250°C is recommended for each soldering process.

3. Bias Procedure and Conditions

When GaAs FET is biased, the following procedure is recommended.

(1) Slowly adjust the gate to source voltage, V_{GS}, to about −1 V.

(2) Gradually increase the drain to source voltage, V_{DS}, from zero to a desired value.

(3) Adjust the drain current, I_D, to a desired value by controlling the gate to source voltage, V_{GS}.

When bias is released, the reverse procedure is recommended.

Typical bias conditions for MGF-1402 are as follows,

for low noise operation : V_{DS} = 3 V, I_D = 10 mA

for high gain operation : V_{DS} = 3 V, I_D = 30 mA

Be careful that the FET is not operated under conditions exceeding absolute maximum ratings.

4. Guaranteed Characteristics

All the graphic characteristics illustrated in this catalog are typical examples. The characteristics of individual devices as specified in the tables of absolute maximum ratings and electrical characteristics are guaranteed under the specified conditions.

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H E4435 C K1 8201 Printed in Japan (TOT)
Revised publication effective Jun. 1982
Supersedes publication H E4435 B of July 1981

MITSUBISHI ELECTRIC

S PARAMETERS (T_a = 25°C, V_{DS} = 3V)

I_D (mA)	f (GHz)	S Parameters (TYP.) S_{11} Magn	S_{11} Angle (deg.)	S_{12} Magn	S_{12} Angle (deg.)	S_{21} Magn	S_{21} Angle (deg.)	S_{22} Magn	S_{22} Angle (deg.)
10	2	0.935	− 47.4	0.040	54.1	2.848	133.4	0.758	− 33.1
	4	0.835	− 88.4	0.065	21.3	2.469	92.3	0.710	− 62.6
	6	0.800	− 119.1	0.054	13.6	2.333	65.8	0.713	− 75.8
	8	0.709	− 164.5	0.048	− 9.5	2.286	27.7	0.643	− 97.6
	10	0.658	155.7	0.052	− 59.3	1.805	− 13.9	0.599	− 138.7
	12	0.713	130.0	0.044	− 37.4	1.488	− 37.1	0.480	177.3

I_D (mA)	f (GHz)	S Parameters (TYP.) S_{11} Magn	S_{11} Angle (deg.)	S_{12} Magn	S_{12} Angle (deg.)	S_{21} Magn	S_{21} Angle (deg.)	S_{22} Magn	S_{22} Angle (deg.)
20	2	0.923	− 51.1	0.035	54.8	3.544	131.7	0.698	− 32.9
	4	0.801	− 94.9	0.053	23.4	3.003	89.7	0.652	− 61.7
	6	0.759	− 126.2	0.039	28.9	2.737	63.0	0.666	− 72.9
	8	0.675	− 172.5	0.038	12.0	2.624	24.7	0.608	− 93.9
	10	0.643	147.8	0.042	− 42.1	2.068	− 15.0	0.578	− 135.5
	12	0.715	124.0	0.043	− 4.7	1.696	− 37.2	0.440	179.8

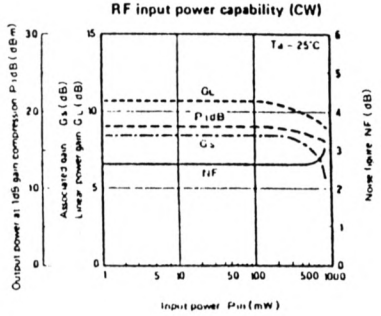
I_D (mA)	f (GHz)	S Parameters (TYP.) S_{11} Magn	S_{11} Angle (deg.)	S_{12} Magn	S_{12} Angle (deg.)	S_{21} Magn	S_{21} Angle (deg.)	S_{22} Magn	S_{22} Angle (deg.)
30	2	0.916	− 53.1	0.032	55.2	3.864	130.8	0.676	− 32.5
	4	0.787	− 98.0	0.048	25.1	3.203	88.3	0.632	− 60.9
	6	0.742	− 129.7	0.034	39.4	2.928	61.8	0.657	− 71.3
	8	0.661	− 176.7	0.035	27.4	2.751	23.3	0.604	− 91.9
	10	0.640	144.1	0.037	− 29.3	2.160	− 15.7	0.580	− 134.0
	12	0.720	121.2	0.046	9.7	1.770	− 37.6	0.433	− 178.0

I_D (mA)	f (GHz)	S Parameters (TYP.) S_{11} Magn	S_{11} Angle (deg.)	S_{12} Magn	S_{12} Angle (deg.)	S_{21} Magn	S_{21} Angle (deg.)	S_{22} Magn	S_{22} Angle (deg.)
40	2	0.912	− 54.5	0.030	55.8	4.027	130.1	0.667	− 32.2
	4	0.777	− 100.5	0.044	26.5	3.319	87.3	0.625	− 60.2
	6	0.731	− 132.6	0.032	48.8	3.006	60.7	0.655	− 70.2
	8	0.653	178.4	0.034	39.1	2.805	22.2	0.610	− 90.6
	10	0.641	141.3	0.035	− 19.4	2.205	− 16.5	0.588	− 133.0
	12	0.725	119.1	0.049	18.3	1.797	− 38.1	0.436	− 175.6

I_D (mA)	f (GHz)	S Parameters (TYP.) S_{11} Magn	S_{11} Angle (deg.)	S_{12} Magn	S_{12} Angle (deg.)	S_{21} Magn	S_{21} Angle (deg.)	S_{22} Magn	S_{22} Angle (deg.)
50	2	0.909	− 55.9	0.029	55.9	4.150	129.4	0.663	− 31.8
	4	0.769	− 102.8	0.041	27.6	3.392	86.3	0.623	− 59.6
	6	0.723	− 135.4	0.030	57.3	3.048	59.6	0.658	− 69.4
	8	0.646	176.3	0.034	47.1	2.822	21.1	0.616	− 89.9
	10	0.642	138.8	0.034	− 11.6	2.218	− 17.5	0.597	− 132.4
	12	0.730	117.0	0.052	24.1	1.805	− 38.8	0.441	− 175.2

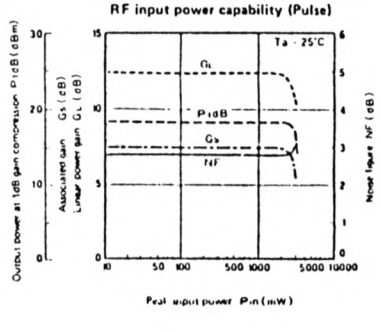
MITSUBISHI SEMICONDUCTOR <GaAs FET>
MGF-1402 (2SK274)
FOR MICROWAVE LOW NOISE AMPLIFIERS
N-CHANNEL SCHOTTKY BARRIER GATE TYPE

RF input power capability (CW)



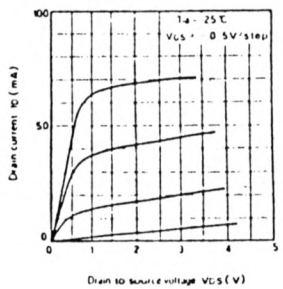
Test conditions
DC Bias
V_{DS} 6V
I_D 40mA
RF input power (CW)
f 8GHz
Input VSWR ≤ 3

RF input power capability (Pulse)

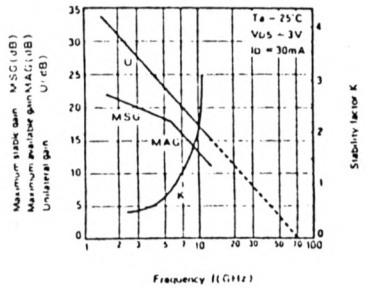


Test conditions
DC Bias
V_{DS} 3V
I_D 10mA
RF input power (Pulse)
f 9.375GHz
Pulse width 1μsec
Repetitive frequency 1KHz
Input VSWR ≤ 3

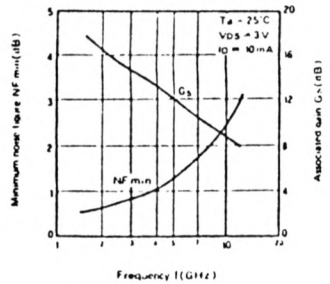
I_D vs. V_{DS}



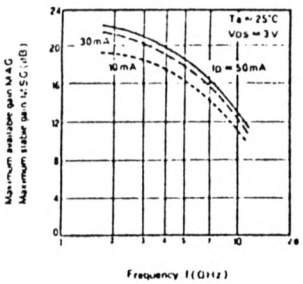
MSG, MAG, U & K vs. f



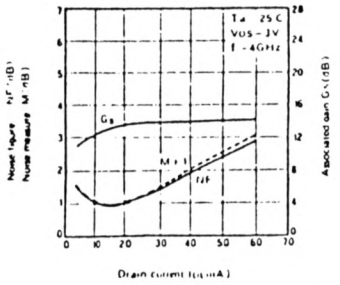
NFmin & Gs vs. f



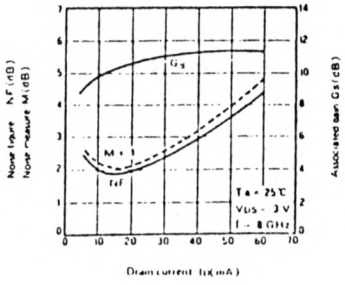
MAG/MSG vs. f



NF, M & Gs vs. I_D
(f = 4GHz)



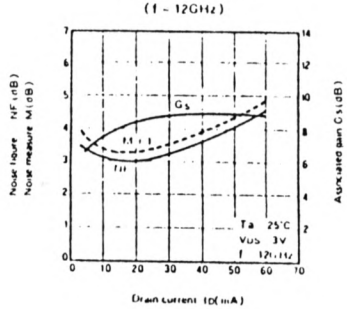
NF, M & Gs vs. I_D
(f = 8GHz)



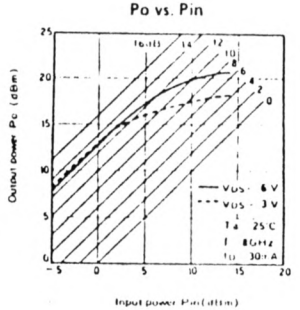
MITSUBISHI SEMICONDUCTOR <GaAs FET>
MGF-1402 (2SK274)

FOR MICROWAVE LOW NOISE AMPLIFIERS
N-CHANNEL SCHOTTKY BARRIER GATE TYPE

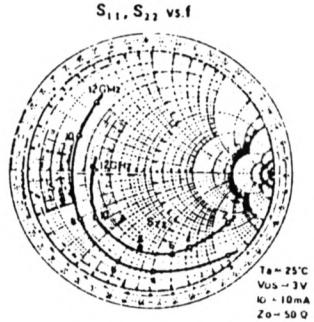
NF, M & Gs vs. I_D
(f = 12GHz)



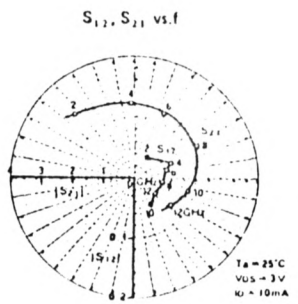
Po vs. Pin



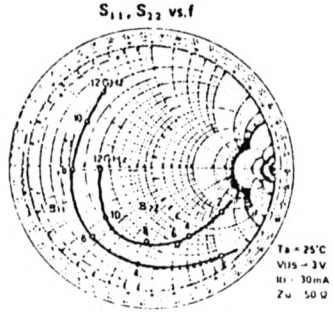
S_{11}, S_{22} vs.f



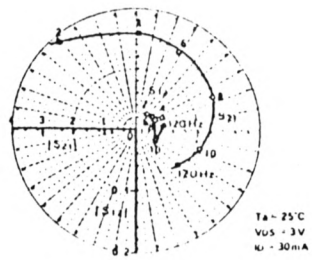
S_{12}, S_{21} vs.f



S_{11}, S_{22} vs.f



S_{12}, S_{21} vs.f



pin diode

Switches

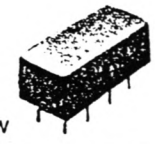
SPST/SPDT

10 to 2500 MHz

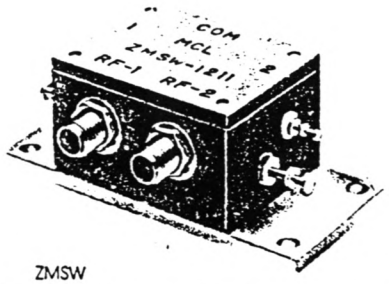
Mini-Circuits

case style selection

outline drawings see section 1



PSW



ZMSW

	MODEL NO.	TYPE	FREQUENCY MHz f_L-f_U	INSERTION LOSS dB low-band lw Typ.	lw Max.	Upper band U Typ.	U Max.	IN-OUT ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	PRICE, $ Ea.	Qty.
PSW case A06	PSW-1111	SPST	10-2500	1.1	1.7	1.7	2.7	50	40	35	30	28	22	29.95	(6-24)
	PSW-1211	SPDT	10-2500	1.1	1.7	1.7	2.7	50	40	35	30	28	22	29.95	(6-24)
ZMSW case JJ77	ZMSW-1111	SPST	10-2500	1.1	1.7	1.7	2.7	50	45	35	30	28	22	59.95	(1-4)
	ZMSW-1211	SPDT	10-2500	1.1	1.7	1.7	2.7	50	45	35	30	28	22	59.95	(1-4)

L = low range (f_L to 10 f_L) M = mid range (10f_L to f_U/2) U = upper range (f_U/2 to f_U)

lw = low-band (f_L to f_U/2)

NOTES:

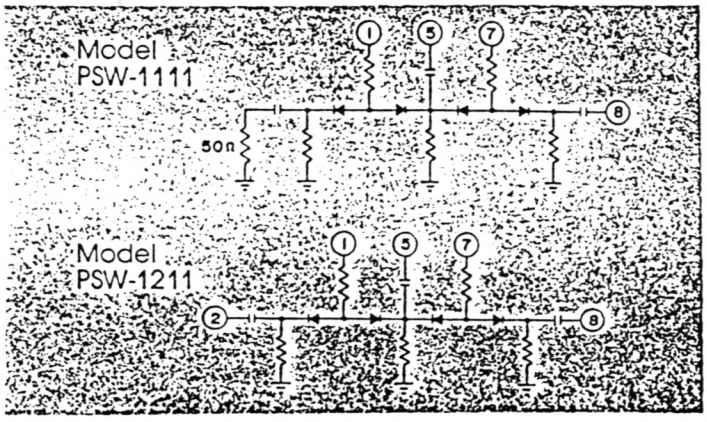
1. Refer to table of contents for quality control procedures, environmental specifications, absolute maximum ratings, and hi-rel testing
2. For PSW and ZMSW models
   a) VSWR 1.5 max. ("on" state)
   b) Switching speed t_μ sec. max.
   c) Maximum RF input + 20 dBm
   d) Control voltage + 5V (5mA max.) on condition
      0V off condition
3. Prices and specifications subject to change without notice.

CAPD PSW-1211

computer-automated performance data

typical production unit / for data of other models consult factory

RF (MHz)	INSERTION LOSS, dB com RF-1	com RF-2	ISOLATION, dB com RF-1	com RF-2
10	-1.29	-1.38	-49.04	-49.44
110	- .93	- .97	-49.74	-49.78
210	- .91	- .90	-48.87	-44.32
310	- .92	- .84	-44.55	-45.50
410	- .83	- .71	-42.88	-44.53
610	-1.09	- .96	-39.47	-39.28
810	-1.13	-1.12	-37.53	-36.80
1010	-1.12	-1.09	-35.83	-34.95
1310	-1.14	-1.10	-33.28	-32.77
1510	-1.16	-1.12	-32.93	-32.41
1810	-1.30	-1.26	-31.80	-31.32
2010	-1.40	-1.32	-30.31	-29.93
2110	-1.45	-1.34	-28.33	-28.99
2310	-1.44	-1.31	-28.08	-28.09
2510	-1.59	-1.45	-27.89	-28.11



pin and coaxial connections

see case style outline drawings

Series	PSW		ZMSW	
Models	1111	1211	1111	1211
RF COMMON	5	5	com	com
RF-1 port	8	2	—	RF-1
RF-2 port	—	8	RF-2	RF-2
CONTROL RF-1	7	1	—	1
CONTROL RF-2	—	7	2	2
CONTROL 50 ohm TERMINATION	1	—	1 —	— —
GND	2,4	4	—	—
CASE GND	3,6	3,6	—	—

In Stock... Immediate Delivery