VLBA Technical Report No. 37

VLBA Sampler
Module D121

Alan E.E. Rogers
November 1988

VLBA SAMPLER MODULE D121

Alan E.E. Rogers
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Specifications:

Sampling Jitter and Drift	< 0.2 ns
Differential Error Between Channels	< 2 ns
Sampling Level Accuracy (after trimming)	< 50 microvolts
"Magnitude" Bit Threshold	200 mv
Encoding (From Most -ve to Most +ve signal)	00,01,10,11

General Description:

The sampler module digitizes the eight baseband signals from four converters (two modules are needed to support eight converters). The

sample clock is derived from the 32 MHz synthesizer module and distributed to each A/D converter section. Each A/D converter/sampler uses three comparators with voltage thresholds of -200,0,+200 mv respectively.

Theory of Operation:

The sign bit is the output of one comparator while the least most significant bit is derived from all three comparators according to the logic equation:

LSB = B.A + (COMPLEMENT(B)).C

where

B = sign bit
A = comparator with 200 mv threshold
C = comparator with -200 mv threshold

Circuit Details:

The comparators are Analog Devices AD9685D. The clock and reference signal are distributed from the center board. Clock signals are terminated in 50 ohms (the Thevenin equivalent) to -2 volts at the end of each line.

I/O Connections - 20 Pin Amp Connector

Pin #	Function
1	GND
2	+5v (350 ma)
3	32 MHz Clock Input (1 Volt p-p)
4	NC
5	SYNC Input (1 Volt p-p)
6	USB from Converter #1
7	LSB from Converter #1
8	-5v (2400 ma)
9	USB from Converter #2
10	LSB from Converter #2
11	USB from Converter #3
12	LSB from Converter #3
13	USB from Converter #4
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	LSB from Converter #4

I/O Connections - 40 Pin (Balanced ECL Outputs)

Pin #	Function
1	SYNC SIGN (-ve)
2	SYNC SIGN (+ve)
3	SYNC MAGN (-ve)
4	SYNC MAGN (+ve)
5	USB1 SIGN (-ve)
6	USB1 SIGN (+ve)
7	USB1 MAGN (-ve)
8	USB1 MAGN (+ve)
9	LSB1 SIGN (-ve)
10	LSB1 SIGN (+ve)
11	LSB1 MAGN (-ve)
12	LSB1 MAGN (+ve)
13	USB3 SIGN (-ve)
14	USB3 SIGN (+ve)
15	USB3 MAGN (-ve)
16	USB3 MAGN (+ve)
17	LSB3 SIGN (-ve)
18	LSB3 SIGN (+ve)
19	LSB3 MAGN (-ve)
20	LSB3 MAGN (+ve)
21	CLOCK (-ve)
22	CLOCK (+ve)
23	GND
24	GND
25	USB2 SIGN (-ve)
26	USB2 SIGN (+ve)
27	USB2 MAGN (-ve)
28	USB2 MAGN (+ve)
29	LSB2 SIGN (-ve)
30	LSB2 SIGN (+ve)
31	LSB2 MAGN (-ve)
32	LSB2 MAGN (+ve)
33	USB4 SIGN (-ve)
34	USB4 SIGN (+ve)
35	USB4 MAGN (-ve)
36	USB4 MAGN (+ve)
37	LSB4 SIGN (-ve)
38	LSB4 SIGN (+ve)
39	LSB4 SIGN (-ve)
40	LSB4 MAGN (+ve)

Test Procedures:

Check symmetry of threshold levels by counting the number of zeroes and ones for each bit of each channel via the decoder/data buffer.

Replacement Instructions

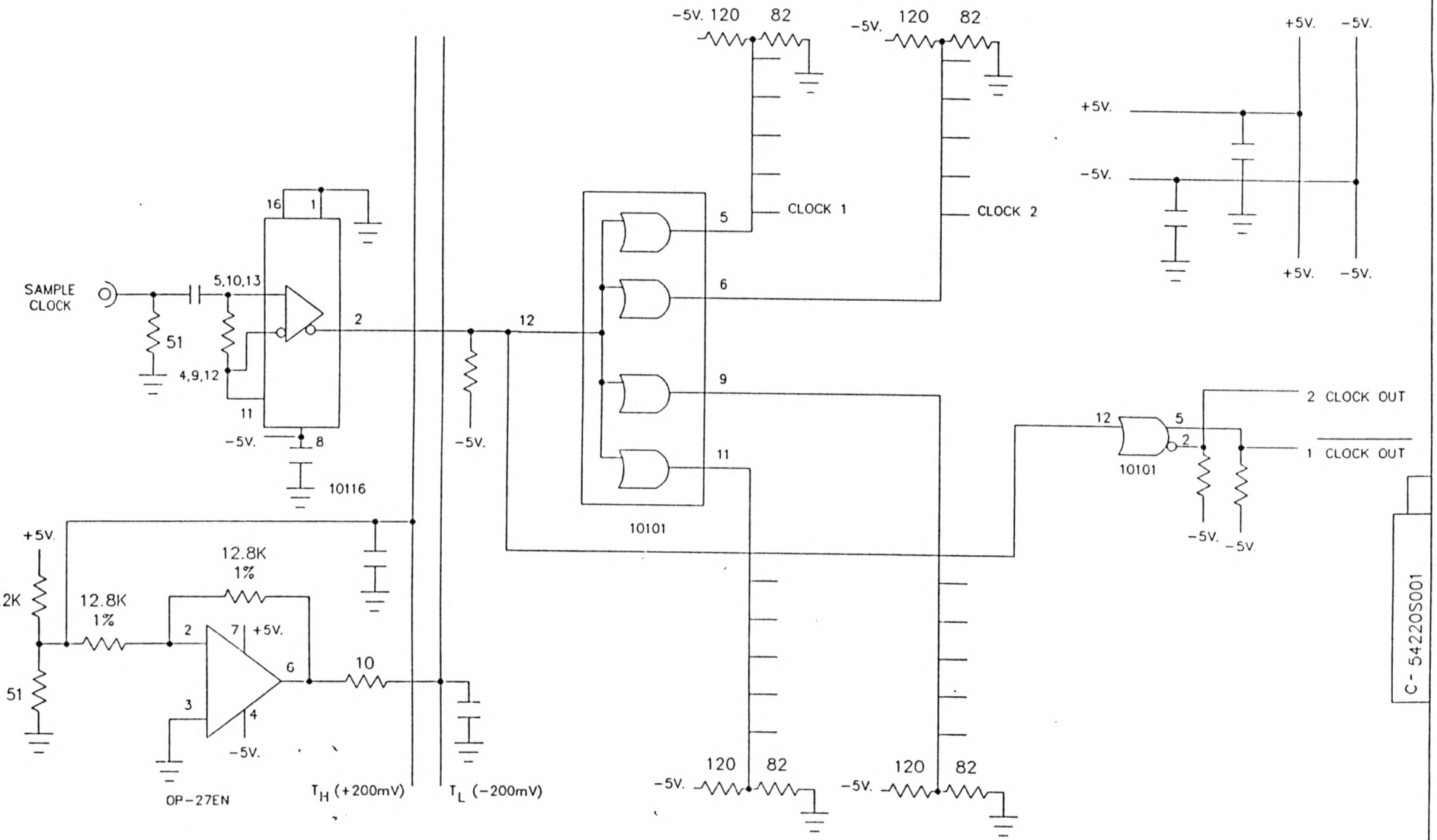
Use "solder wick" to remove defective components.

Parts List:

Data Sheets:

AD9685BD

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

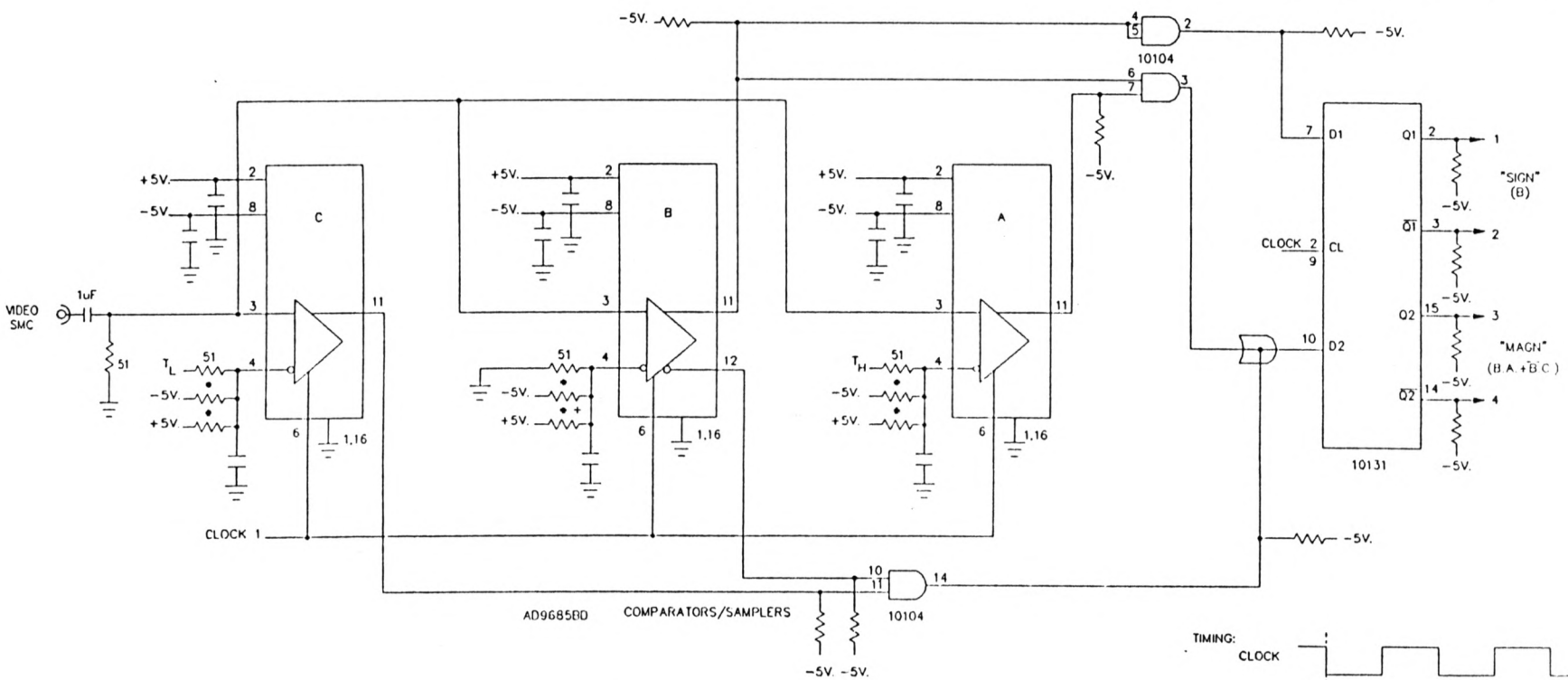


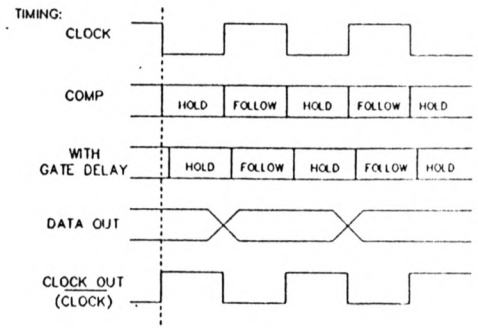
NOTES:

1. ALL CAPACITORS .01uF UNLESS OTHERWISE NOTED.
2. ALL RESISTORS ARE 330 OHMS UNLESS OTHERWISE NOTED.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBROOK	7-87	A/D CONVERTER/SAMPLER CLOCK & REF. VOLTAGE DISTRIBUTION
		CHECKED BY:		
	SCALE NONE	APPROVAL PROJECT		C / 54220S001
	CLASSIFICATION	ENGINEER		AERVADCONSAM / DWG SIZE / DWG NO / REV

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	D.C.N. & DESCRIPTION





NOTES:
1. +OFFSET TRIM APPROXIMATELY 50K.
2. ALL CAPACITORS ARE 0.01uF UNLESS OTHERWISE NOTED.
3. ALL RESISTORS ARE 330 OHMS UNLESS OTHERWISE NOTED.
4. +2.4K OFFSET TRIM TO +5V FOR SYNC CHANNEL (100mV OFFSET).

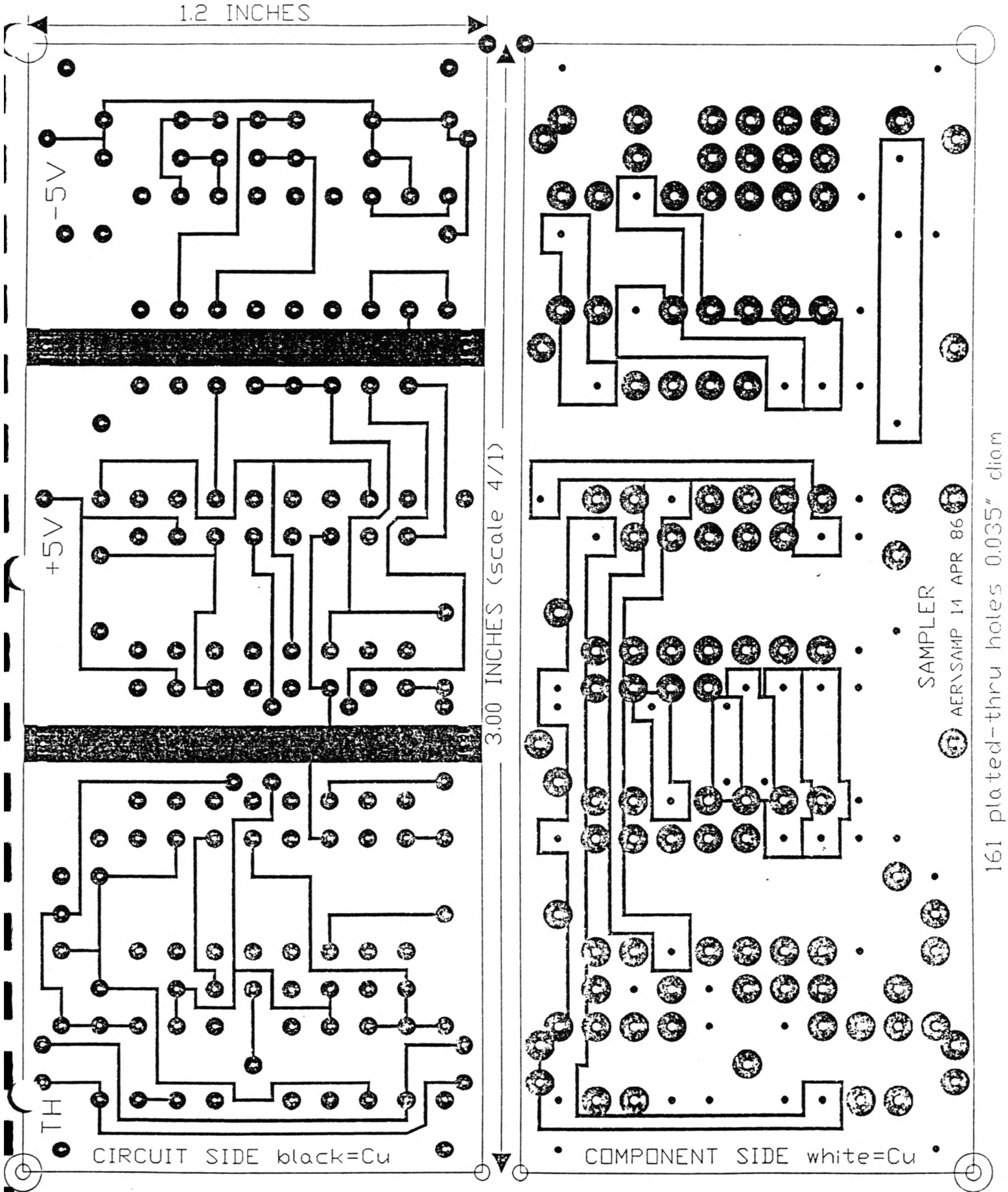
ELECTRONICS NOTES: UNLESS OTHERWISE NOTED:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87
RESISTORS:		DRAWN BY: A.PHILBROOK	7-87
INDUCTORS:	SCALE:	CHECKED BY:	
CAPACITORS:		ENGINEER:	

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

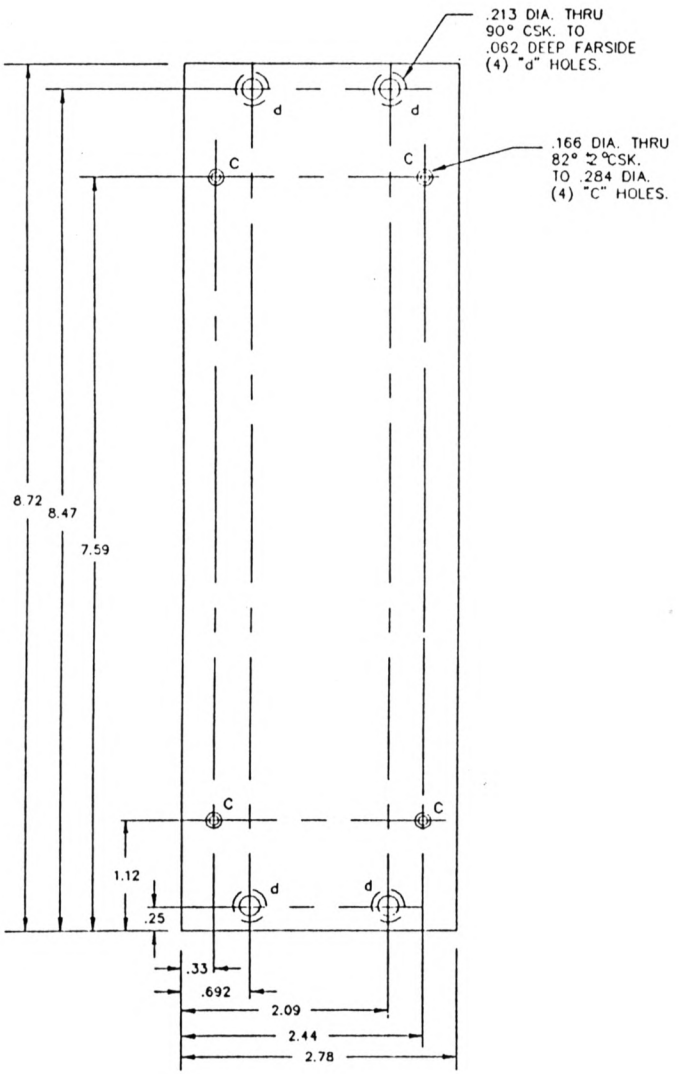
A/D CONVERTER/SAMPLER (SINGLE "VIDEO" CHANNEL TO 2-BIT SAMPLES OUT)

D - 542205002

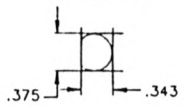
Drawing Number: 542200003



CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



DETAIL "A"



CUT-OUT FOR
KINGS-153 BNC
CONNECTOR

C—54220M004

NOTES

MATERIAL

.125 THICK ALUM. 6061-T6
REMOVE ALL BURRS AND
SHARP EDGES.

FINISH AND/OR HEAT TREATMENT

YELLOW CHROMATE
CONVERSION ALL OVER

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS
   PER MIL-STD-10
4. REMOVE BURRS AND BREAK
   SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY
   BEFORE PLATING OR CON-
   VERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

APPROVALS		
	PROJECT	
	ENGINEER	
	MATL. & PROCESS	
	STRUCTURES	
	THERMAL	
	ELECTRICAL	

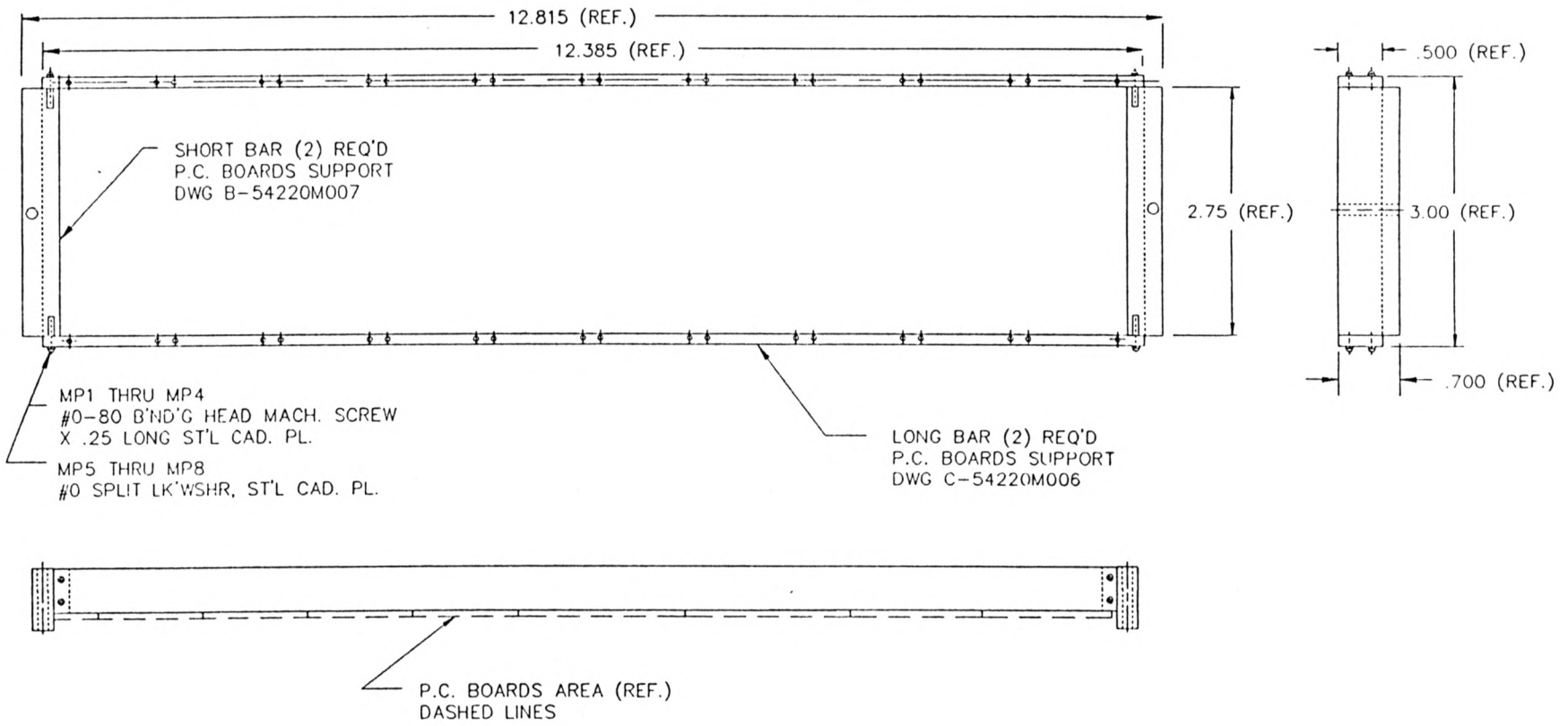
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
SAMPLER
FRONT PANEL

SIZE	DWG NO	REV
C	54220M004	

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



C-54220M005

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-8
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

		DATE
DRAWN FOR	A E ROGERS	7-87
DRAWN BY	A. PHIL BROOK	7-87
CHECKED BY		

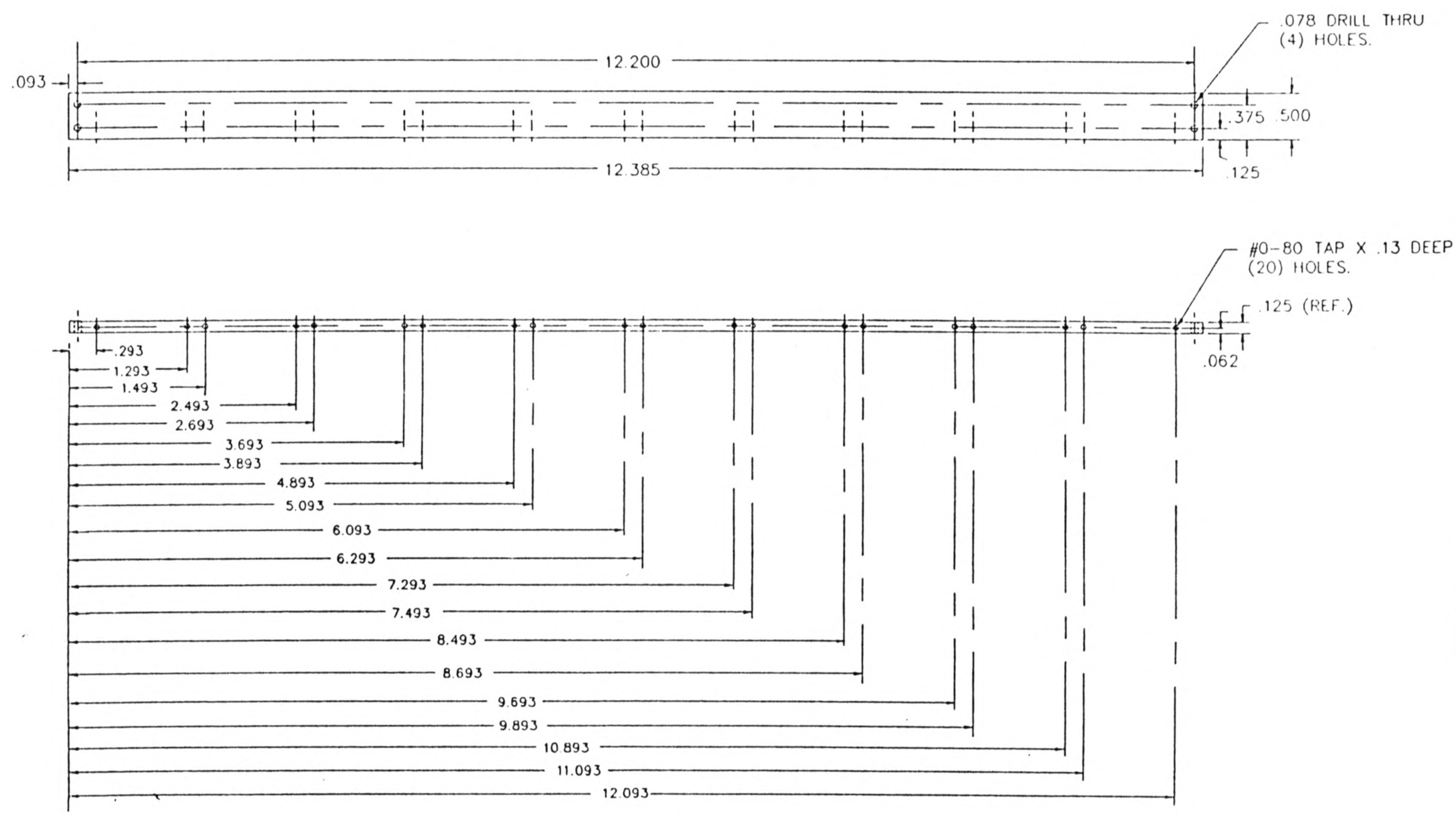
APPROVALS: PROJECT; ENGINEER; MATL. & PROCESS; STRUCTURES; THERMAL; MECH. ANALYSIS

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

P.C. BOARDS SUPPORT MECH. SUB-ASSEMBLY SAMPLER

AERNSUBSAMP	DWG. SIZE: C	DWG. NO: 54220M005	REV

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



C—54220M006

NOTES

MATERIAL
.125 ALUM. 6061-T6

FINISH AND/OR HEAT TREATMENT
CLEAR ALODINE

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS 125 √
   PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON
NEXT ASSEMBLY
WEIGHT
SCALE FULL
CLASSIFICATION

		DATE
DRAWN FOR	A.E.ROGERS	7-87
DRAWN BY	A.PHILBROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
[redacted]		

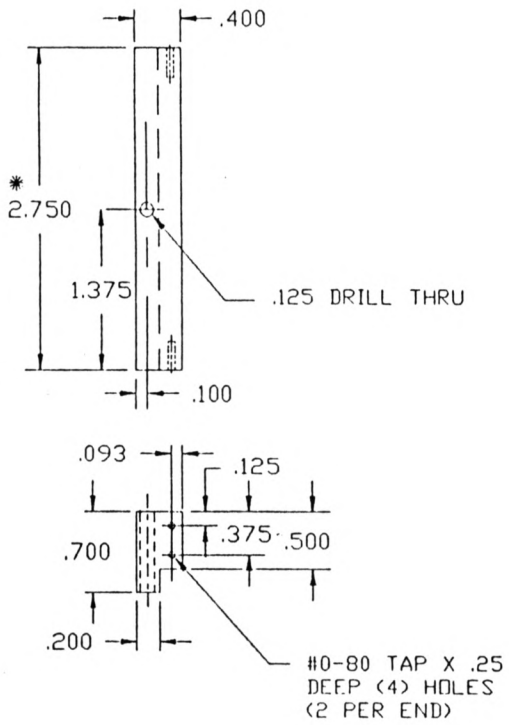
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

LONG BAR
P.C. BOARDS SUPPORT
SAMPLER

C | 54220M006

HARSAM [redacted] ZE [redacted] NO [redacted] REV

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



* 2.750 LENGTH IS THE SAME FOR ALL SHORT BARS - MACHINE TOGETHER

1. MATERIAL: ALUM. 6061-T6
2. FINISH: CLEAR ALODINE

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10 — 63
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

DRAWN FOR	A.E.ROGERS	DATE 12/86
DRAWN BY	A.PHIL.BROOK	12/86
CHECKED BY		

APPROVALS

PROJECT	
ENGINEER	
MATL. & PROCESS	
STRUCTURES	
THERMAL	
MECH. ANALYSIS	

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

SHORT BAR P.C. BOARD SUPPORT SAMPLER

AERSSHARSAMP | B | 54220M007 | REV

DWG. SIZE | DWG. NO

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	D.C.N. & DESCRIPTION

NOTES:

1. SILK SCREEN CHARACTERS AND LINES BLACK.
2. PAINT: HEWLETT PACKARD, MINT GRAY, P/N 6010-0577, FRONT AND EDGES ONLY, PER NRAO SPEC. NO. A13030N1.

D - 542201009

NOTES:

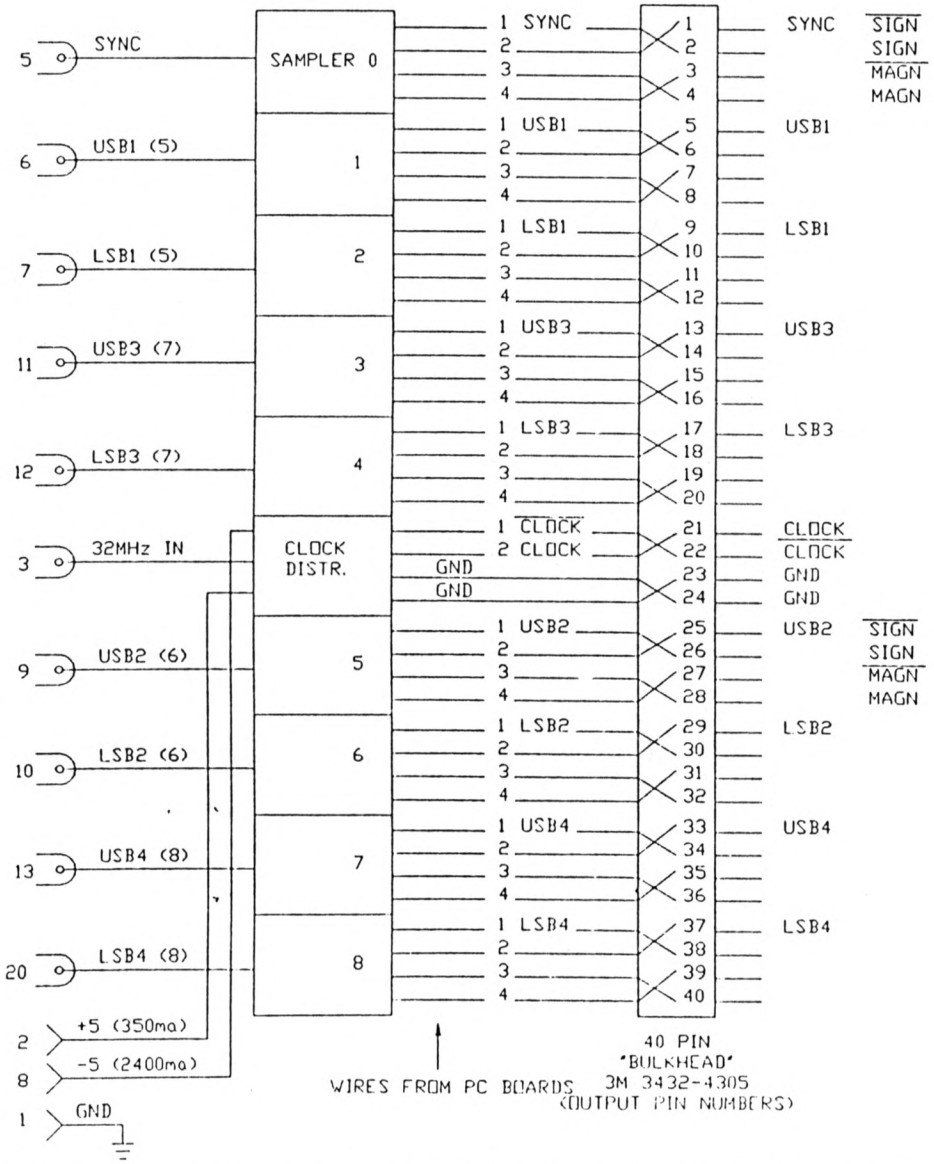
ELECTRONICS NOTES: UNLESS OTHERWISE NOTED: RESISTORS: INDUCTORS: CAPACITORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87
		DRAWN BY: A.PHILBROOK	7-87
	SCALE: 2/1	APPROVALS: CHECKED BY: ENGINEER: PROJECT:	
	SPECIFICAT		

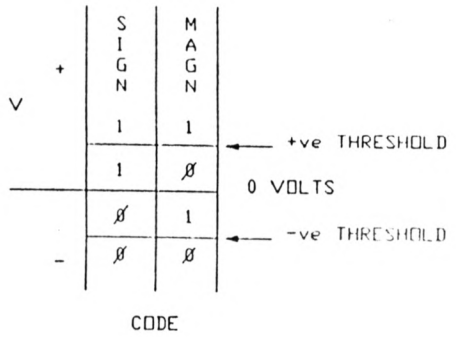
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORDMASSACHUSETTS

SILK SCREENING ARTWORK FOR SAMPLER

[redacted]

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	D.C.N. & DESCRIPTION

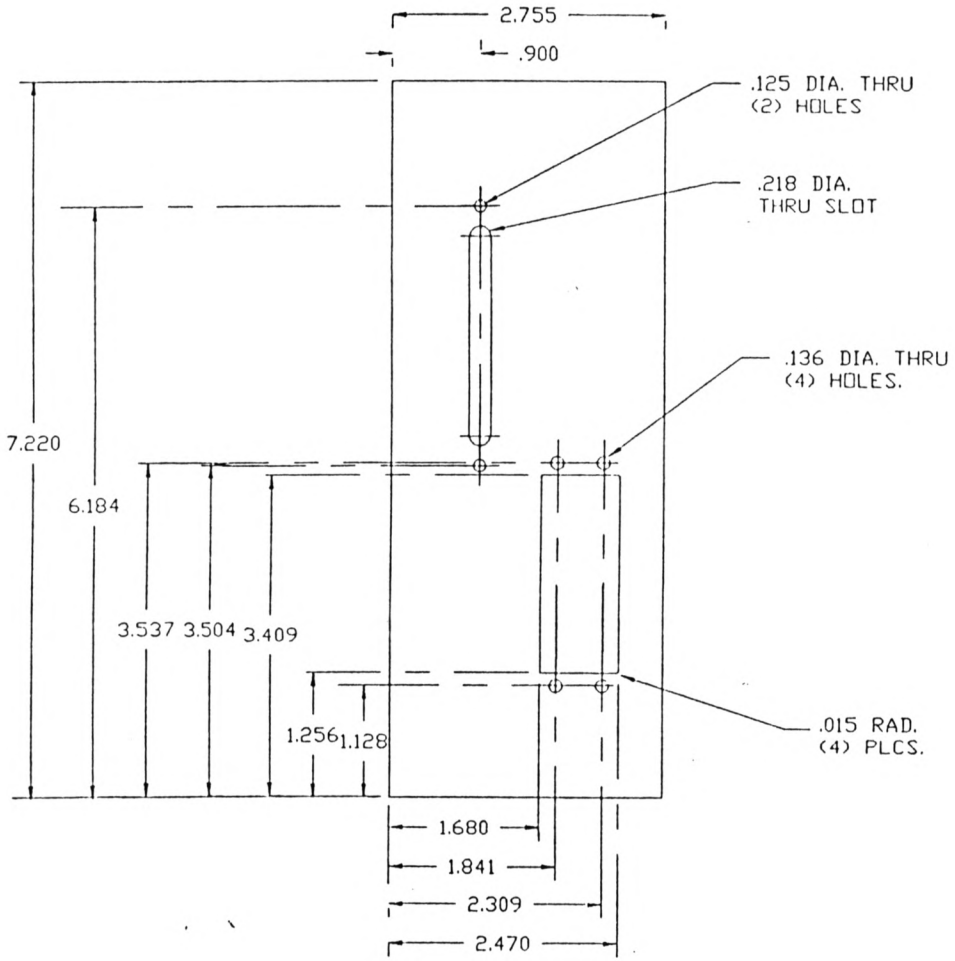


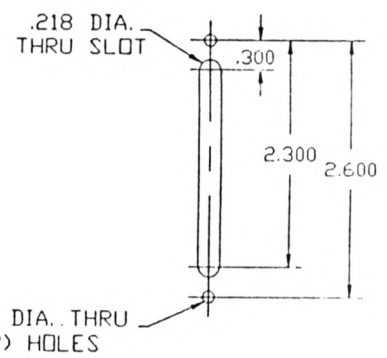


D - 54220S010

ELECTRONICS NOTES: UNLESS OTHERWISE NOTED: RESISTORS: INDUCTORS: CAPACITORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 7-87	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.PHILBRICK	7-87	
		CHECKED BY:		SAMPLER (A/D CONVERTER) 2 WIRE MODULE
	SCALE:	ENGINEER		
	CLASSIFICATION	PROJECT		ACM/SAMP/MOD | 11 | 54220S010

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	DCN & DESCRIPTION





C-54220M011

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE

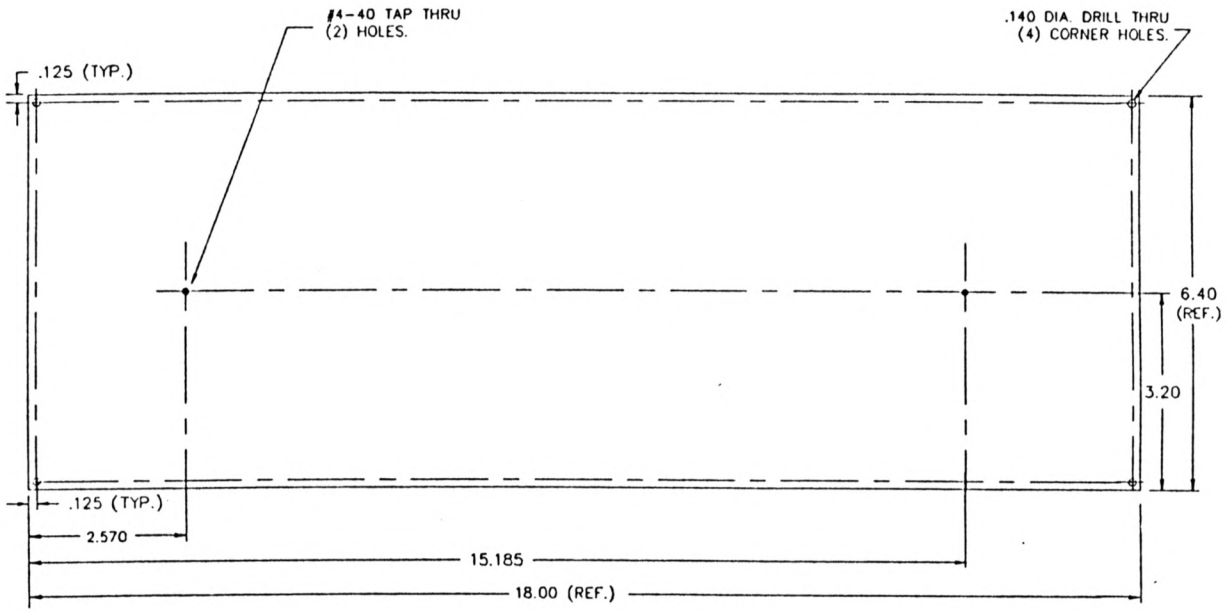
CLASSIFICATION

DRAWN FOR	A.E.ROGERS	DATE 7-87
DRAWN BY	A.PHIL BROOK	7-87
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL & PROCESS		
STRUCTURES		
THERMAL		
[illegible]		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

VLBA SAMPLER
MODULE ASSEMBLY

[redacted] | [redacted] | [redacted] | [redacted]

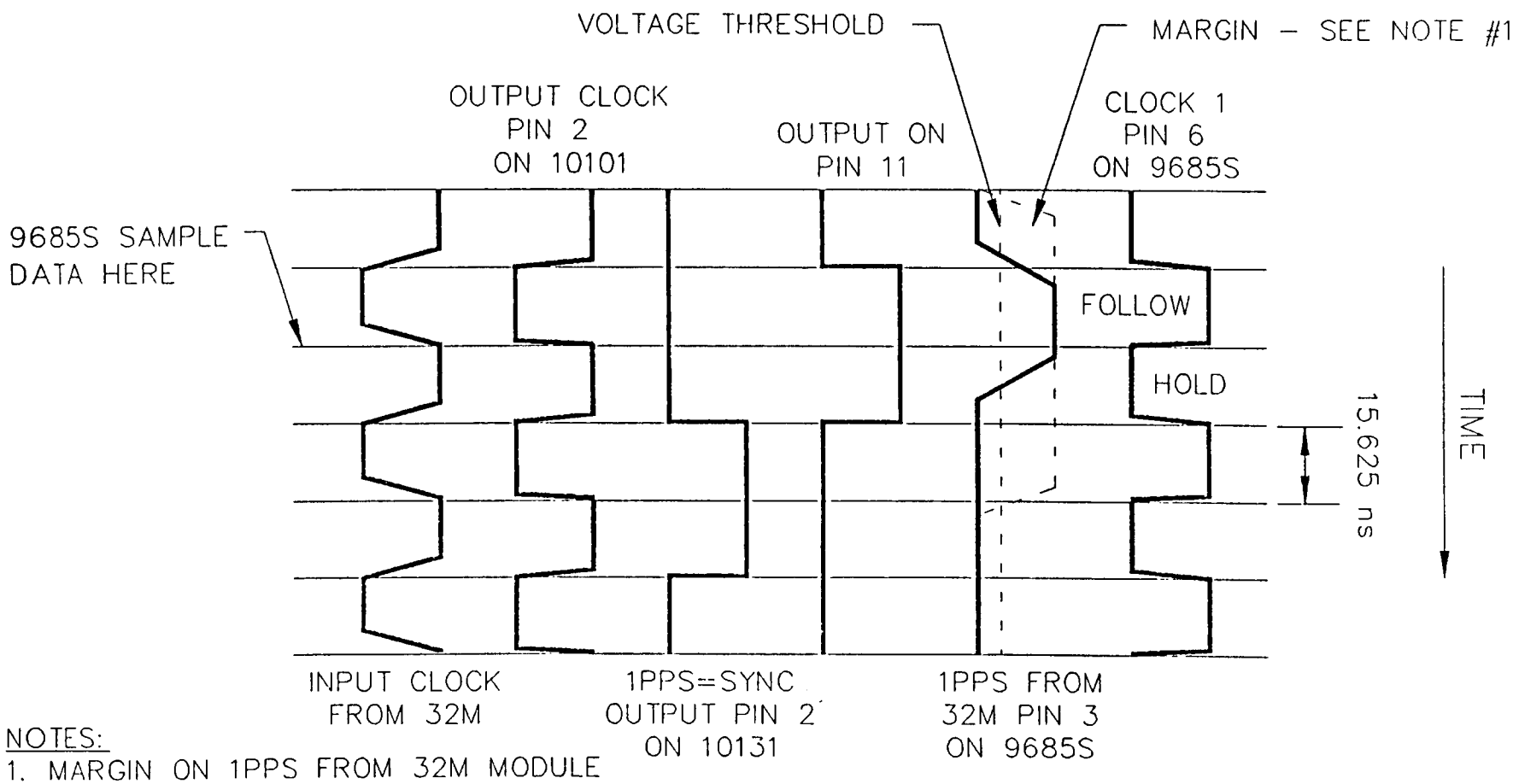


NOTES:

MATERIAL: .125 ALUM. 6061-T6				A.E.ROGERS	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
FINISH AND/OR HEAT TREATMENT: CLEAR ALODINE				A.PHILBRICK	DRILLING PLAN FOR MOUNTING PLATE SAMPLER

D- 54220W012

TH
SAMPLER CLOCK
AER\SCLK 15 APR 86
+5V
-5V
CIRCUIT SIDE black=Cu
1.2 INCHES
3.00 INCHES (SCALE 4/1)
COMPONENT SIDE white=Cu
Drawing Number: 542200013



NOTES:

1. MARGIN ON 1PPS FROM 32M MODULE +15ns (EARLY) TO −20ns (LATE).

DWG. LAST CHANGED −/−/−

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON	
NEXT ASSEMBLY	
WEIGHT	
SCALE	NONE
CLASSIFICATION	

DRAWN FOR	A.E.ROGERS	DATE 11/88
DRAWN BY	C.KOSTKA	11/88
CHECKED BY		
APPROVALS: PROJECT		
APPROVALS: ENGINEER		
APPROVALS: MATL. & PROCESS		
APPROVALS: STRUCTURES		
APPROVALS: THERMAL		
APPROVALS: MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

1PPS TIMING IN SAMPLER MODULE

1PPSTSMD	A	5422OS01	
	DWG. SIZE	DWG. NO.	REV.

PARTS LIST FROM DBASE FILE:PARTS.DBF

REF	SUBMOD	PART	DESC	MFR	COST	QTY	TOTAL COST
U06	SA	10104	10104	FAIRCHILD	0.69	1	0.69
C01	SA	103K	0.01 UF	AVX	0.10	87	8.70
C02	SA	105K	1 UF	AVX	0.32	9	2.88
MP	SA	1105-7521-003	SMC CABLE PLUG	AEP	2.49	10	24.90
MPX	SA	200458-1	BLOCK	AMP	3.00	1	3.00
MPX	SA	200833-4	GUIDE PINS	AMP	0.36	2	0.72
MPX	SA	200835-4	GUIDE SOCKETS	AMP	0.48	2	0.96
MPX	SA	201142-2	SPRING	AMP	0.05	11	0.55
MPX	SA	201143-5	COAXICON PIN	AMP	2.70	11	29.70
MPX	SA	202394-2	HOOD	AMP	1.04	1	1.04
MPX	SA	202422-1	POWER PINS	AMP	0.50	4	2.00
MPX	SA	328666	FERRULE	AMP	0.08	11	0.88
SS	SA	54220I009	F.P.SILK SCREEN	NYES	100.00	1	100.00
MS	SA	54220M004	FRONT PANEL	HAYSTACK	100.00	1	100.00
MS	SA	54220M005	PC BOARD SUPPORT	HAYSTACK	100.00	1	100.00
MS	SA	54220M011	REAR PANEL	HAYSTACK	100.00	1	100.00
MS	SA	54220M012	CENTER PLATE	HAYSTACK	100.00	1	100.00
U04	SA	AD9685BD	9685	ANALOG DEV	11.30	27	305.10
PC	SA	AER\SAMP	PC BOARD	PACLAB	40.00	9	360.00
PC	SA	AER\SCLK	PC BOARD	PACLAB	40.00	1	40.00
MS	SA	C53306M013-2UA	FRONT PANEL	PREC.MACHINE	20.00	1	20.00
MS	SA	C53306M014-2UA	PERFORATED COVER	PREC.MACHINE	10.00	2	20.00
MS	SA	C53306M015-2UA	MODULEREAR PANEL	PREC.MACHINE	20.00	1	20.00
MS	SA	C53306M016	BAR SUPPORT	PREC.MACHINE	10.00	4	40.00
MS	SA	C53306M017	SIDE PLATE	PREC.MACHINE	10.00	2	20.00
U02	SA	MC10101L	10101	MOTOROLA	1.00	2	2.00
U01	SA	MC10116L	10116	MOTOROLA	1.14	1	1.14
U05	SA	MC10131L	10131	MOTOROLA	1.14	9	10.26
U03	SA	OP-27EN	OP-27	ANALOG DEV	7.15	1	7.15
R03	SA	RCR05G100J	10 OHMS 1/8W	AB	0.20	1	0.20
R05	SA	RCR05G121J	120 OHMS 1/8W	AB	0.20	4	0.80
R02	SA	RCR05G122J	1.2K OHMS 1/8W	AB	0.20	1	0.20
R04	SA	RCR05G331J	330 OHMS 1/8W	AB	0.20	93	18.60
R01	SA	RCR05G510J	51 OHMS 1/8W	AB	0.20	38	7.60
R06	SA	RCR05G820J	82 OHMS 1/8W	AB	0.20	4	0.80
R07	SA	RN55D1272F	12.7K OHM 1%	CORNING	0.10	2	0.20
WORK	SA	TECH	ASSEMBLY	HAYSTACK	10.00	20	200.00
*** Total ***							1650.07

ANALOG DEVICES

Ultra-Fast Comparators

AD9685/AD9687

FEATURES

2.2ns Propagation Delay – AD9685BD/BH
2.7ns Propagation Delay – AD9687BD
0.5ns Latch Set-Up Time
Pin-Compatible to Am685/687 but FASTER
+5V, −5.2V Supply Voltages

APPLICATIONS

Ultra-High-Speed A/D Converters
Ultra-High-Speed Line Receivers
Peak Detectors
Threshold Detectors

GENERAL DESCRIPTION

The AD9685BD/BH and AD9687BD are ultra-fast comparators manufactured with a high performance bipolar process which makes it possible to obtain incredibly short propagation delays and latch set-up times.

The AD9685BD/BH is a single comparator which is pin-compatible with the Am685, but has speed capabilities that far outstrip the earlier unit. The AD9687BD is pin-for-pin compatible with the Am687 and, like its predecessor, is a dual comparator; its speed capabilities are far superior to the Am687.

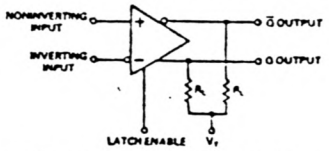
Both Analog Devices units have differential inputs and complementary outputs fully compatible with ECL logic levels. Their output current levels are capable of driving 50Ω terminated transmission lines, and their high resolution make them ideally suited for a variety of analog-to-digital signal processing applications.

AD9685BD/BH Single Comparator

A latch function allows the AD9685BD/BH to be operated in a sample-hold mode. When the Latch Enable (LE) is ECL HIGH, the comparator functions normally. When the Latch Enable is driven LOW, its outputs are locked in the logic state dictated by the input conditions at the time of the latch input transition. If the latch function is not used, the Latch Enable input should be connected to ground.

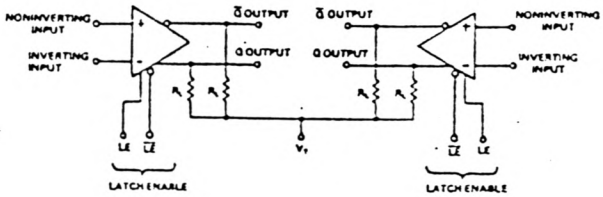
In addition to its speed advantages over the earlier Am685, the AD9685BD/BH also dissipates less power because it operates on a positive 5 volt supply instead of the 6 volts required by the AMD device.

AD9685BD/BH FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD Dual Comparator

The latch function of the AD9687BD provides an ability to operate the unit in either a track-hold or sample-hold mode. The latch function inputs are separated on the two comparators and are designed to be driven from the complementary outputs of a standard ECL logic gate. When LE is High and $\overline{LE}$ is LOW, the normal comparator function is in operation. When LE is forced LOW and $\overline{LE}$ is driven HIGH, the outputs of the comparator being exercised are locked in their existing logical states, as determined by the input conditions present at the time of arrival of the latch signal. If the latch function is not used on either one of the two comparators in the AD9687BD, the appropriate Latch Enable input should be connected to ground; the companion $\overline{\text{Latch Enable}}$ input can be left open.

The AD9687BD is basically two AD9685BD/BH units in a single package and operates in a similar fashion to a pair of the single comparators.

SPECIFICATIONS (typical @ +25°C with nominal supply voltages unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS	AD9685BD/BH	AD9687BD
Supply Voltages (V_{CC} and V_{EE})	±6V	•
Power Dissipation	336mW	500mW
Input Voltage	±5V	•
Differential Input Voltage	5.5V	•
Output Current	30mA	•
Operating Temperature Range	−30°C to +85°C	•
Storage Temperature Range	−55°C to +150°C	•
Lead Temperature (soldering, 10 seconds)	300°C	•

ELECTRICAL CHARACTERISTICS	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage[1]	V_{OS}	−5		+5	•		•	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$		20			•		µV/°C
Input Offset Current	I_{OS}			5			•	µA
Input Bias Current	I_B		10	20		•	•	µA
Input Voltage Range	V_{CM}	−2.5		+2.5	•		•	V
Common Mode Rejection Ratio	CMRR	80			•			dB
Input Resistance	R_{IN}	60			•			kΩ
Input Capacitance	C_{IN}		3			•		pF
Input/Output Logic Levels								
Output HIGH Voltage	V_{OH}	−0.96		−0.81	•		•	V
Output LOW Voltage	V_{OL}	−1.85		−1.65	•		•	V
Positive Supply Voltage	V_{CC}	+4.75	+5	+5.25	•	•	•	V
Negative Supply Voltage	V_{EE}	−4.95	−5.2	−5.45	•	•	•	V
Positive Supply Current	I_{CC}		19	23		30		mA
Negative Supply Current	I_{EE}		23	34		34		mA
Supply Voltage Rejection Ratio	S_{VRR}		60			•		dB
Power Dissipation	P_{DISS}		210	300		430		mW
SWITCHING CHARACTERISTICS								
Propagation Delays[2]								
Input to Output HIGH	t_{pd+}		2.2	3		2.7	4	ns
Input to Output LOW	t_{pd-}		2.2	3		2.7	4	ns
Latch Enable to Output HIGH	$t_{pd+}(E)$		2.5	3		2.7	4	ns
Latch Enable to Output LOW	$t_{pd-}(E)$		2.5	3		2.7	4	ns
Latch Enable								
Pulse Width	$t_{pw}(E)$	3	2		•	•		ns
Minimum Set-Up Time	t_s		0.5	1		•	•	ns
Minimum Hold Time	t_h			1			•	ns

NOTES
[1] R_S = 100 ohms
[2] Propagation delays measured with 100mV pulse, 5mV overdrive.
• Specifications same as AD9685BD/BH
Specifications subject to change without notice.

DEFINITION OF TERMS

V_{OS} — INPUT OFFSET VOLTAGE – The potential difference required between the input terminals to obtain zero potential difference between the outputs.

I_{OS} — INPUT OFFSET CURRENT – The difference between the currents into the inputs when there is zero potential difference between the outputs.

I_B — INPUT BIAS CURRENT – The average of the two input currents. This is a chip design trade-off parameter. Internally, it is desirable to have high values of I_B for circuit performance requirements; externally, it is desirable to have I_B as low as possible.

V_{CM} — INPUT VOLTAGE RANGE – The range of input voltages for which offset and propagation delay specifications are valid.

CMRR — COMMON MODE REJECTION RATIO – The ratio of input voltage range to the peak-to-peak change in input offset voltage over that range.

R_{IN} — INPUT RESISTANCE – The resistance looking into either terminal with the other grounded.

C_{IN} — INPUT CAPACITANCE – The capacitance looking into either input pin with the other grounded.

V_{OH} — OUTPUT HIGH VOLTAGE – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} — OUTPUT LOW VOLTAGE – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I_{CC} — POSITIVE SUPPLY CURRENT – The current required from the positive supply to operate the comparator.

I_{EE} — NEGATIVE SUPPLY CURRENT – The current required from the negative supply to operate the comparator.

S_{VRR} — SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

P_{DISS} — POWER DISSIPATION – The power dissipated by the comparator with both outputs terminated in 50 ohms to −2V.

t_{pd+} — INPUT TO OUTPUT HIGH DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} — INPUT TO OUTPUT LOW DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+}(E)$ — LATCH ENABLE TO OUTPUT HIGH DELAY – The propagation delay measured from the 50% point of the Latch Enable (LE) signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-}(E)$ — LATCH ENABLE TO OUTPUT LOW DELAY – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

$t_{pw}(E)$ — MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time the Latch Enable signal must be HIGH to acquire and hold an input signal.

t_s — MINIMUM SET-UP TIME – The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h — MINIMUM HOLD TIME – The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

OTHER SYMBOLS

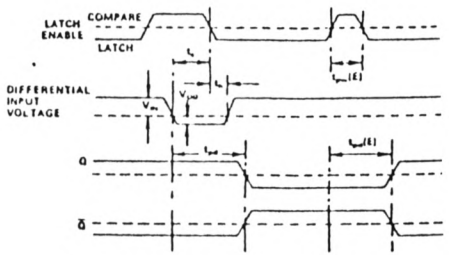
T_C	Case Temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{IN}	Input pulse amplitude
V_{CC}	Positive supply voltage	V_{OD}	Input overdrive
V_{EE}	Negative supply voltage	f	Frequency

TIMING DIAGRAM

The Timing Diagram illustrates a series of events in the AD9685BD/BH; the terms and their relationships are also valid for the AD9687BD. The relationships which are shown should not be interpreted as "typical", since several parameters have multiple values; and the worst case conditions are shown in the Timing Diagram.

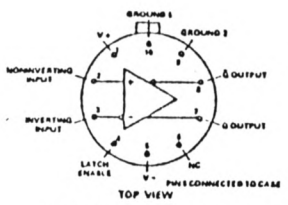
The top line of the diagram shows two Latch Enable (LE) pulses; each is high for "compare" and low for "latch". The first pulse illustrates the compare function in which part of the input action takes place during the "compare" mode. The second one illustrates a compare function interval during which there is no change in input.

The leading edge of the input signal, shown here as a large amplitude, small overdrive pulse, switches the comparator after a time interval t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch trailing (falling) edge and, to be acquired, must be maintained for a time t_h after that edge. After t_h, the output no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of tpw(E) is required the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.



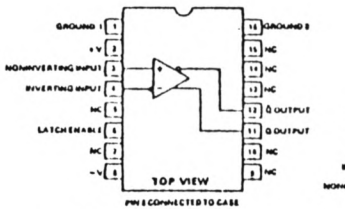
PIN CONFIGURATIONS

TO-100



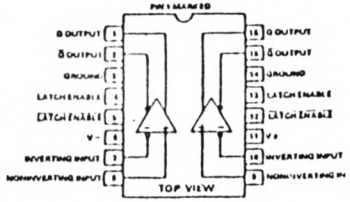
AD9685BH Pin Configuration
Package Option[1] — TO-100

DIP



AD9685BD Pin Configuration
Package Option[1] — Q16C

DIP



AD9687BD Pin Configuration
Package Option[1] — D16A

NOTE
[1] See Section 19 for package outline information.