VLBA Technical Report No. 40

VLBA Output Rate Synthesizer Module L123

Alan E.E. Rogers

October 1988

VLBA OUTPUT RATE SYNTHESIZER - MODULE L123

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Specifications:

Output Frequency	189 MHz, 190.072 MHz and these divided by 2,4,8,16,32
Auxilliary output	at freq above divided by 21
Input Reference Frequency	5 MHz

General Description:

This module derives the frequency needed to take the data out of the formatter. Thus the required frequency is somewhat higher than the data rate on each track by an amount needed to add the extra "overhead" bits. In the case of a Mark III format the overhead is an added parity bit every 8 data bits. For example when MK III data is recorded at 8 Mbits/sec per track 9 MHz is needed to clock the data out of the formatter and 9x21=189 MHz is needed for the bit synchronizer reference in the recorder. If the proposed VLBA non-data-replacement format is used the overhead is increased so that 190.072 is needed for bit synchronizer reference.

Theory of Operation:

A crystal oscillator is divided to 1 kHz and phase locked to a 1 kHz reference derived from 5 MHz. The loop filter is designed using the same general principles as used in the baseband converter synthesizer.

Circuit Details:

The MC14152 PPL frequency synthesizer chip is the heart of the circuit. Either a Vectron 189 MHZ VCXO (for MKIII) or 190.512 VCXO (for VLBA) is selected by a diode switch. The oscillator signal is then divided by 21 before passing to the PPL SYN which operates with a divide by 32/33 swallow counter external to the 14152. The 5 MHz reference is divided to 8 kHz and is divided further to 1 kHz in the 14152. The OP-27EN provides the loop filter/amplifier. Division by factors of 2 is provided in a separate submodule.

Front Panel Monitors:

The front panel BNCs provide buffered outputs of both the high frequency and the frequency divided by 21.

I/O Connections:

Pin #	Function
1	Ground
2	+5v (50 ma)
3	5 MHz Input + 13 dB Nominal
4	Synthesizer output
5	divide by 21 output
6	NC
7	NC
8	NC
9	NC
10	NC

11	NC
12	NC
13	NC
14	NC
15	+15v (200 ma)
16	VLBA/MK III cntr.
17	Control 1
18	Control 2
19	Control 3
20	NC

Test Procedures:

Check the output on a scope for frequency and phase stability. Check the divide by 21 output.

Replacement Instructions

Try to isolate problem. The divider submodule can be independently tested. Use "solder wick" to remove defective component.

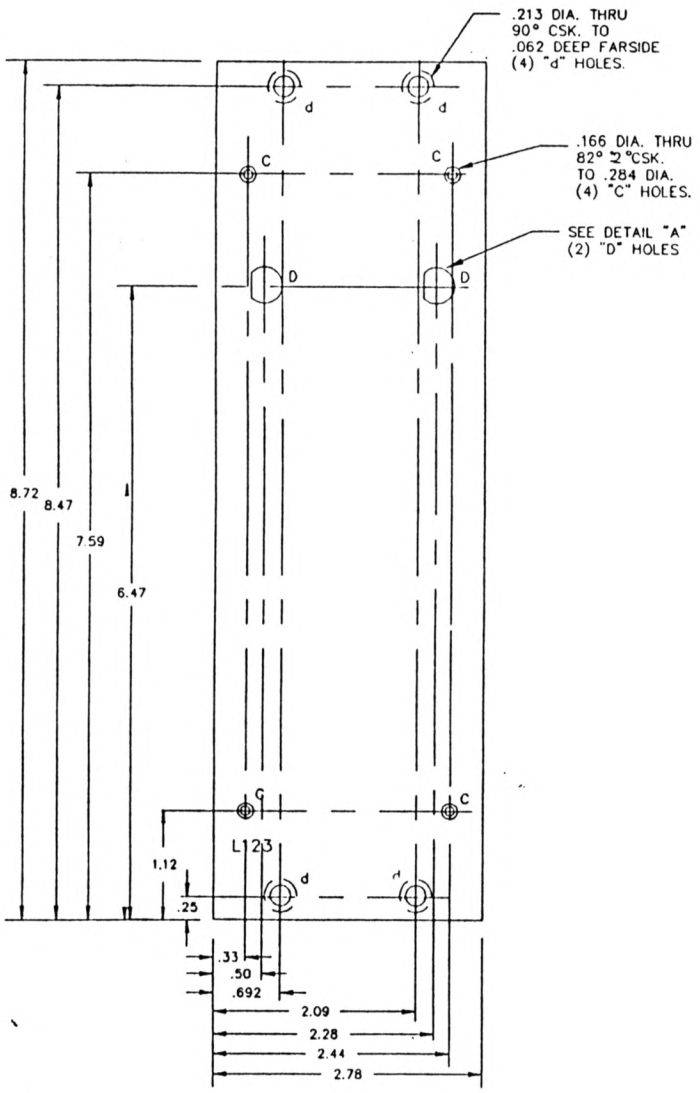
Parts List:

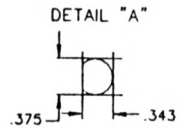
Data Sheets:

Vectron VCXO

MC145152P1
MC12019P
MC12015P

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION





CUT-OUT FOR
KINGS-153 BNC
CONNECTOR

C-5423UM001

NOTES

MATERIAL

.125 THICK ALUM. 6061-T6
REMOVE ALL BURRS AND
SHARP EDGES.

FINISH AND/OR HEAT TREATMENT

YELLOW CHROMATE
CONVERSION ALL OVER

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS
   PER MIL-STD-10
4. REMOVE BURRS AND BREAK
   SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY
   BEFORE PLATING OR CONV-
   [redacted] COATING

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

DRAWN FOR	A.E.ROGERS	1/88
DRAWN BY	A.P.HEBERT	1/88
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH [redacted]		

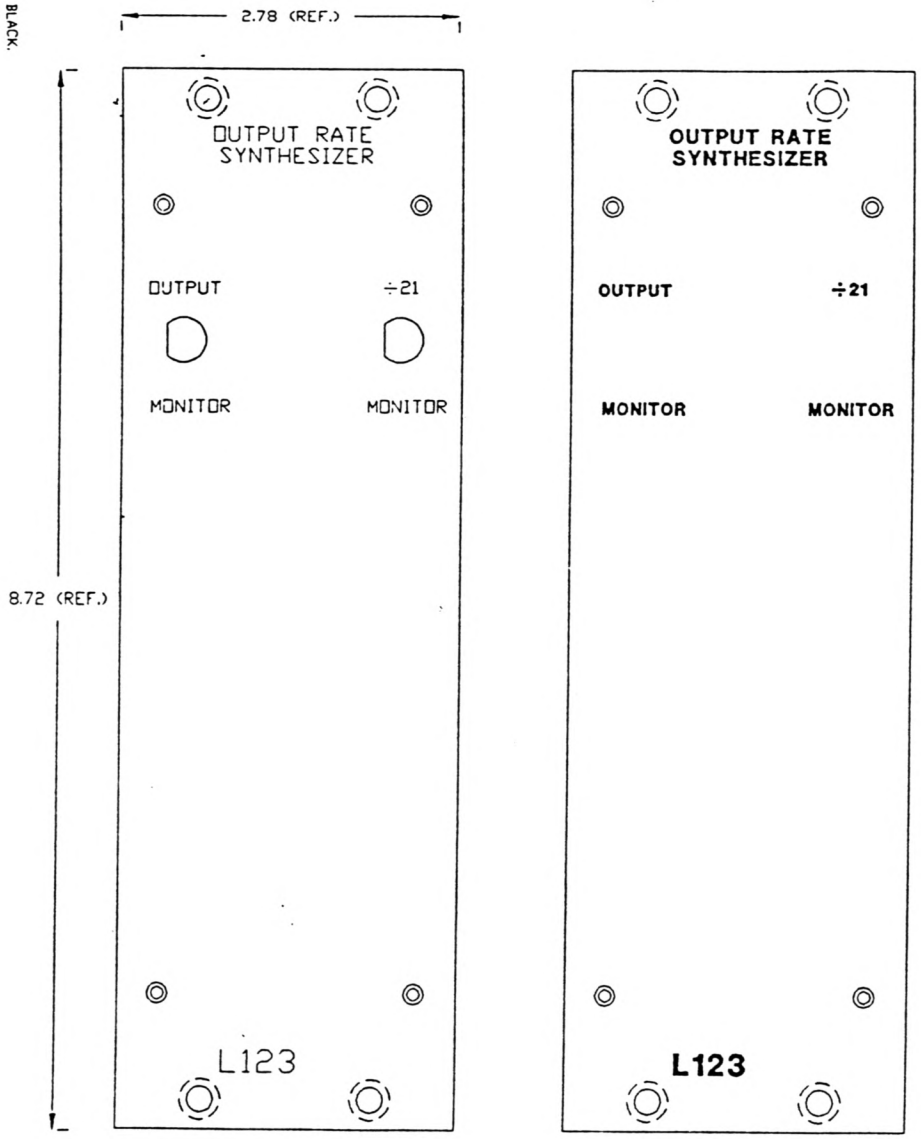
NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
OUTPUT RATE SYNTHESIZER
FRONT PANEL

[redacted] C [redacted] 230 [redacted]

AER\OUTPUT | DWG SIZE | DWG NO | REV.

NOTES:
1. SILK SCREEN CHARACTERS AND LINES BLACK.
2. PAINT HEWLETT PACKARD, MINT GRAY, P/N 6010-0577, FRONT AND EDGES ONLY, PER NRAO SPEC. NO. A1303N1.



SILK SCREENED PANEL

ARTWORK

ELECTRONICS NOTES:
UNLESS OTHERWISE NOTED
RESISTORS:
INDUCTORS:
CAPACITORS:

USED ON

SCALE: 2/1

CLASSIFICATION:

DRAWN FOR: A.E. ROGERS
DRAWN BY:
CHECKED BY:
ENGINEER:
APPROVED BY:
PROJECT:

DATE: 1/88 1/88

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

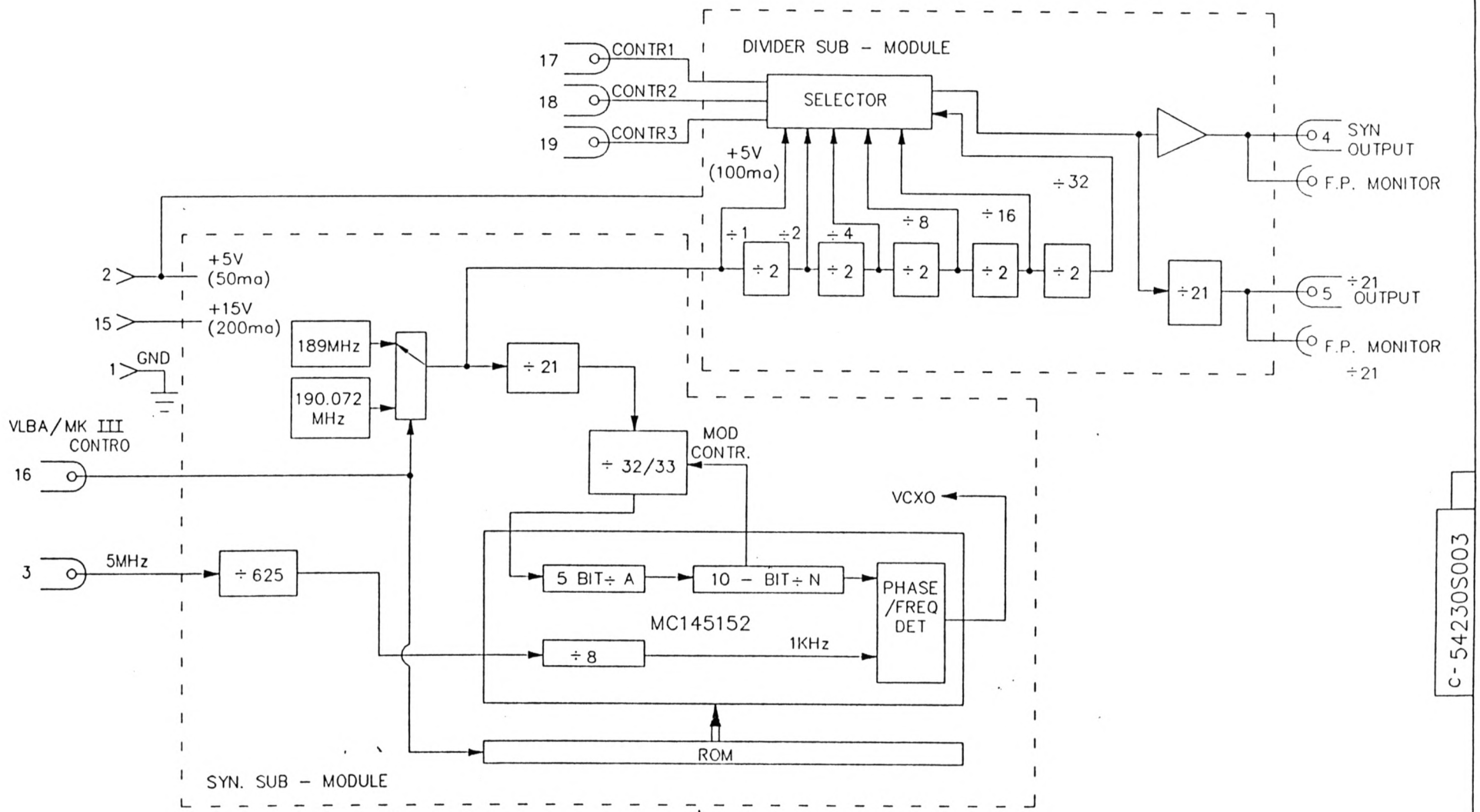
SILK SCREENING ARTWORK FOR
OUTPUT RATE SYNTHESIZER

542301002

CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	DCN & DESCRIPTION

542301002

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

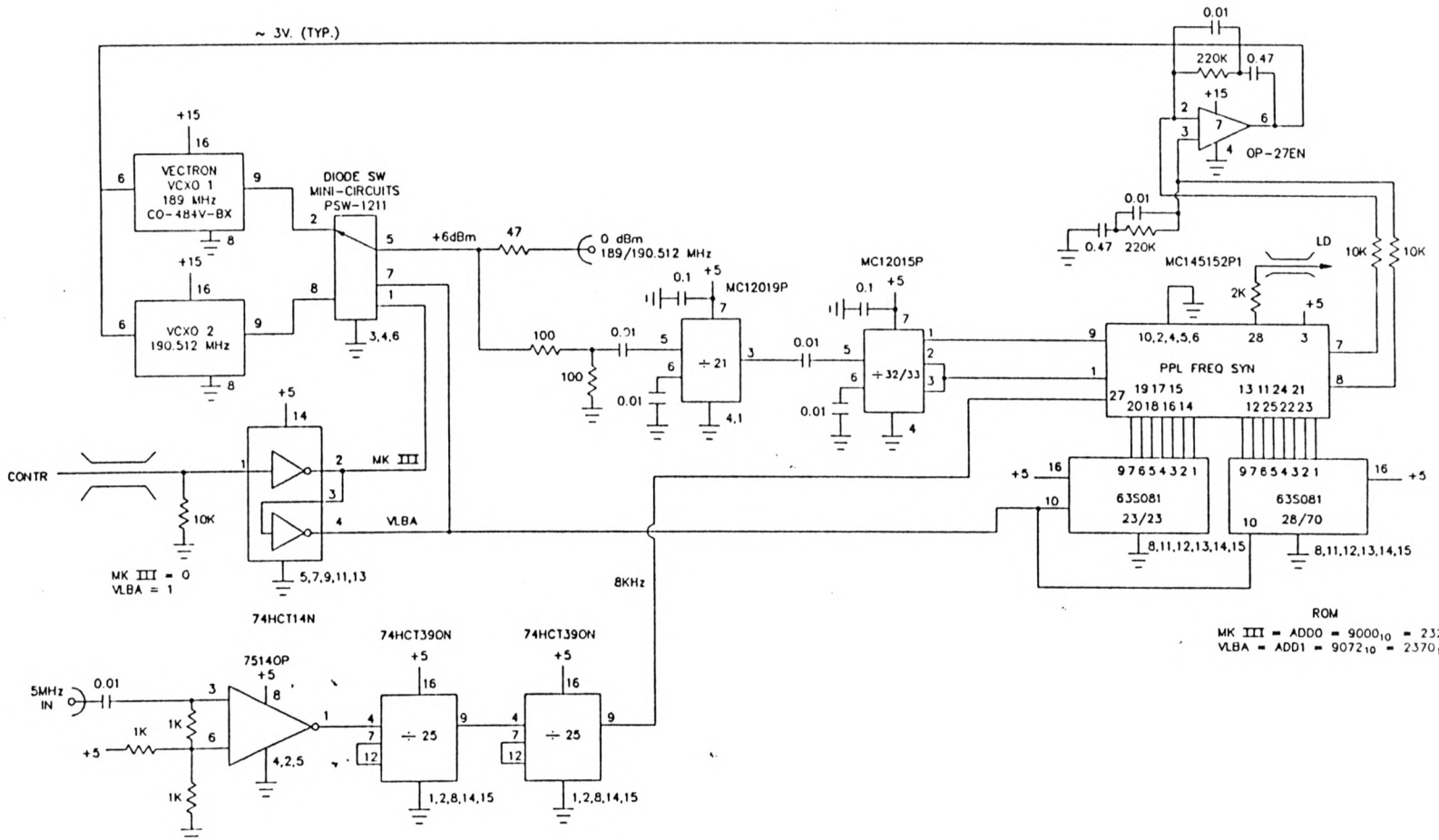


C-54230S003

NOTES:

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 1/88	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.P.HEBERT	1/88	OUTPUT RATE SYNTHESIZER BLOCK DIAGRAM 2 WIDE MODULE
		CHECKED BY:		
	SCALE NONE	OVAL PROJECT ENGIN		[redacted] C 54230S003

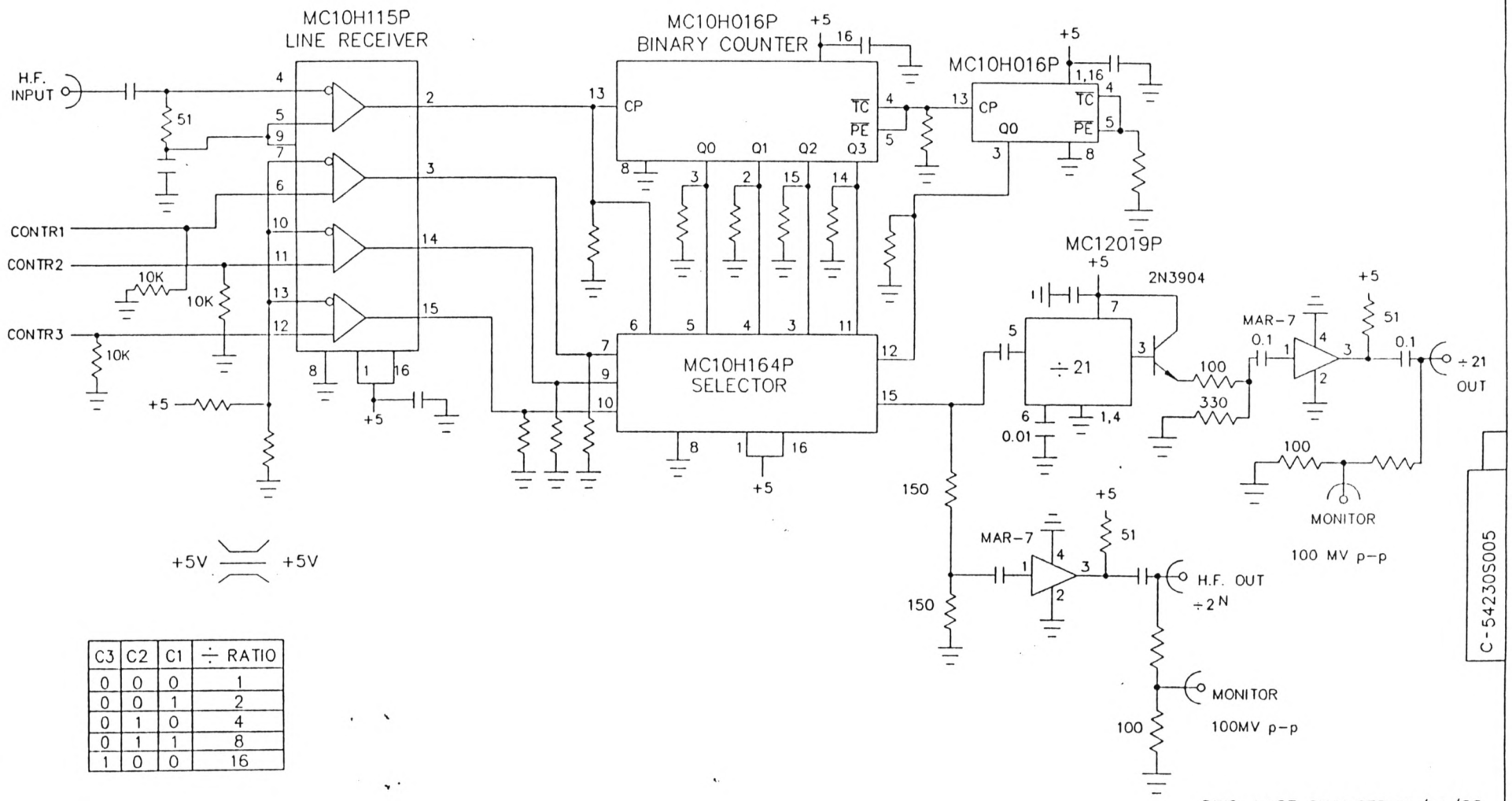
CHANGE LETTER	DWN BY:	CHK'D BY:	APP'D BY:	DATE:	D.C.N. & DESCRIPTION



D -542305004

ELECTRONICS NOTES: UNLESS OTHERWISE NOTED:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 1/88	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD,MASSACHUSETTS
RESISTORS:		DRAWN BY: A.P.HEBERT	1/88	
INDUCTORS:	SCALE: NONE	APPROVALS: CHECKED BY:		OUTPUT RATE SYNTHESIZER
CAPACITORS:	CLASSIFICATION:	ENGINEER:		
		PROJECT:		AER\OUTSYNTH D 542305004

CHANGE LETTER	DWN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



C3	C2	C1	÷ RATIO
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16

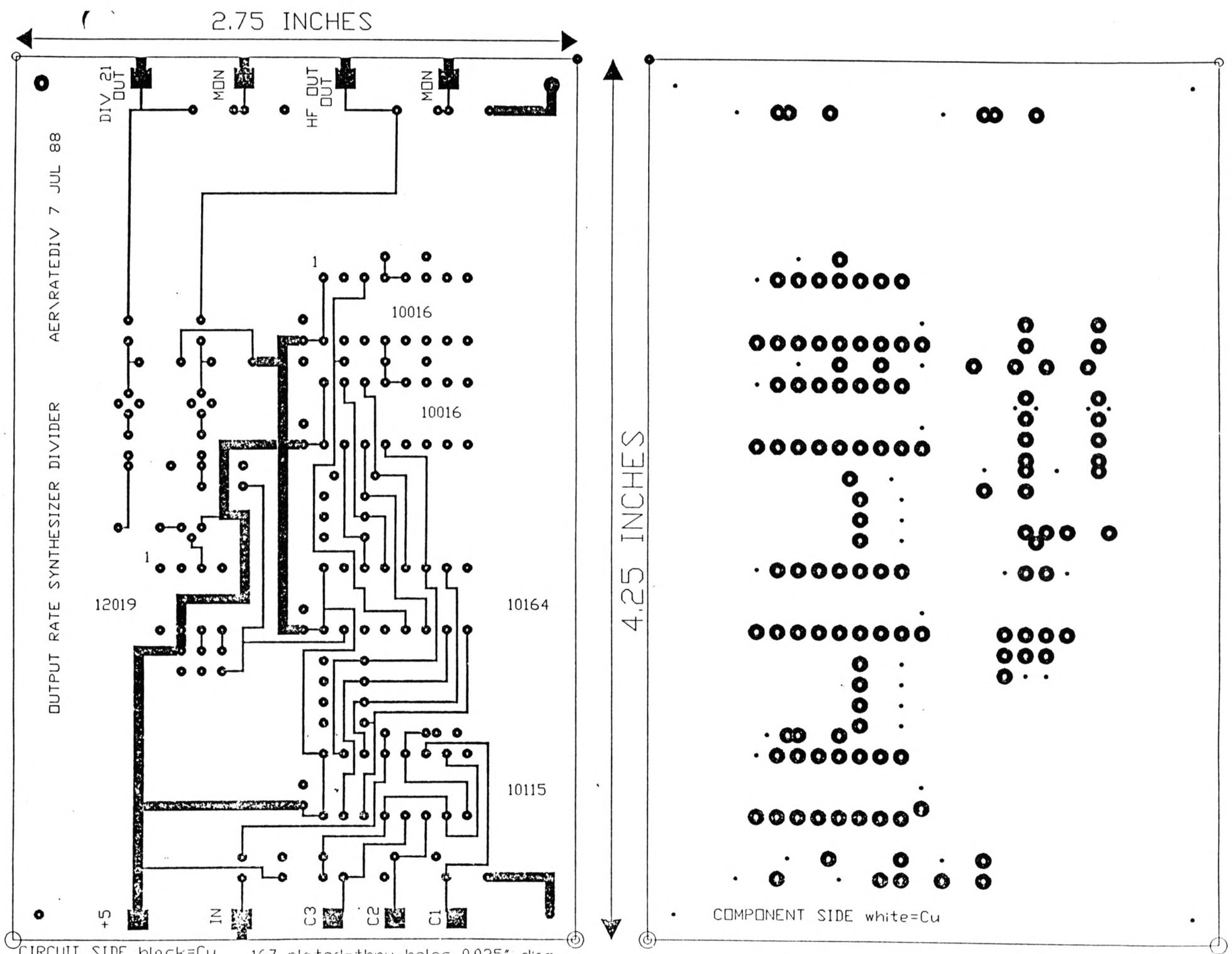
DWG. LAST CHANGED 11/14/88

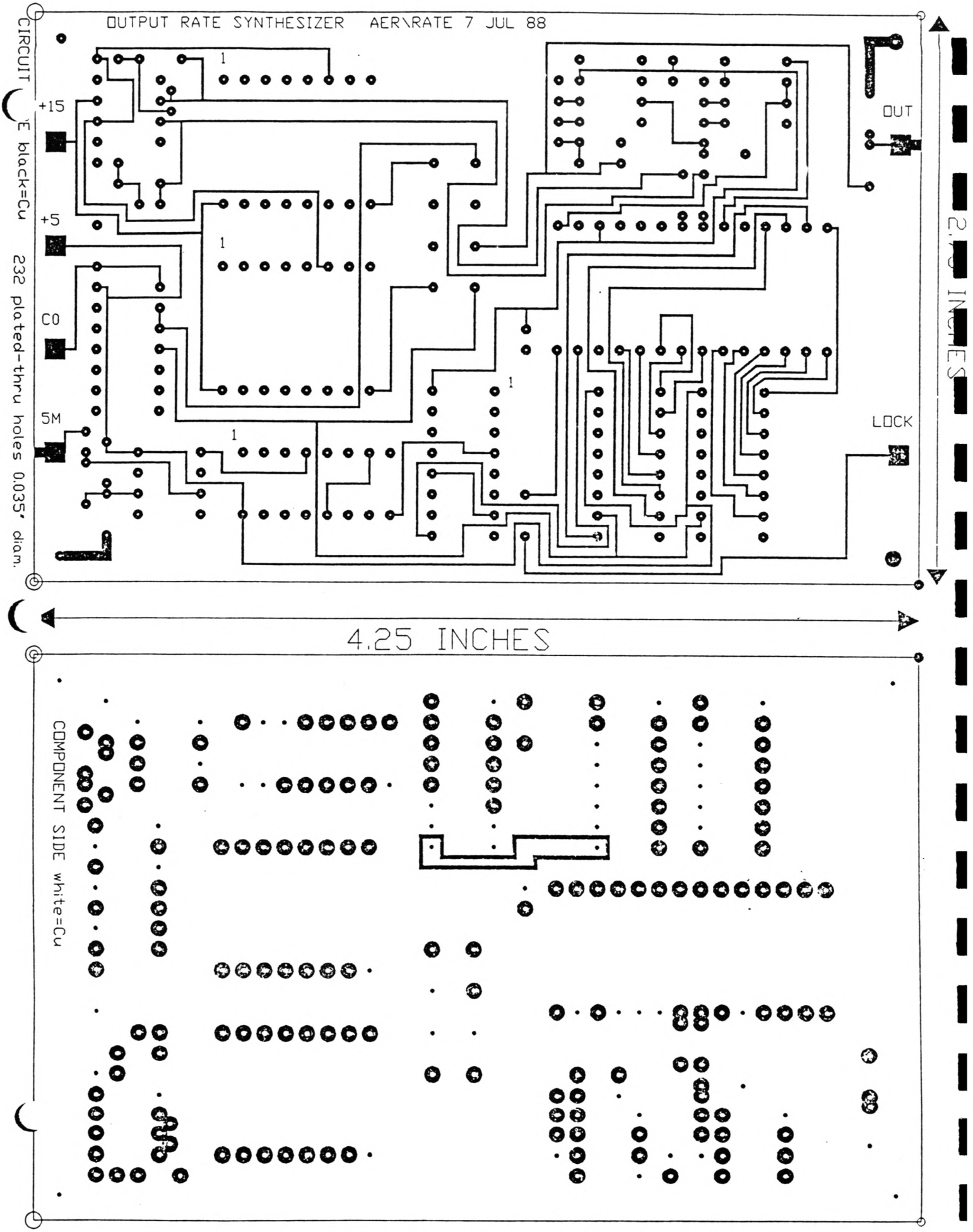
C-54230S005

NOTES:

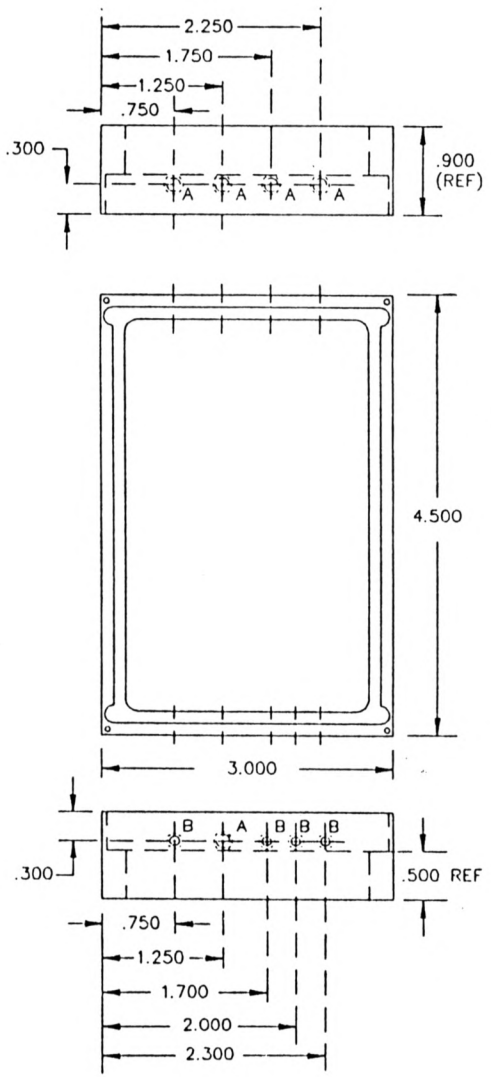
1. All resistors are 330 1/8W except when otherwise noted.
2. All capacitors are 0.01uF except when otherwise noted.

ELECTRONIC NOTES: UNLESS OTHERWISE NOTED: RESISTORS: CAPACITORS: INDUCTORS:	USED ON	DRAWN FOR: A.E.ROGERS	DATE: 1/88	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
		DRAWN BY: A.P.HEBERT	1/88	OUTPUT RATE SYNTHESIZER DIVIDER SUB - MODULE
		CHECKED BY:		
	SCALE NONE	PROJ ENGR		AERO DIV C 54230S005


2.75 INCHES
4.25 INCHES
DIV 21 OUT
MON
HF OUT OUT
MON
OUTPUT RATE SYNTHESIZER DIVIDER
AER\RATEDIV 7 JUL 88
1
10016
10016
1
12019
10164
10115
+5
IN
C3
C2
C1
CIRCUIT SIDE black=Cu
167 plated-thru holes 0.035" diam.
COMPONENT SIDE white=Cu


OUTPUT RATE SYNTHESIZER AER\RATE 7 JUL 88
CIRCUIT E black=Cu 232 plated-thru holes 0.035" diam.
+15
+5
CO
5M
OUT
LOCK
1
2.75 INCHES
4.25 INCHES
COMPONENT SIDE white=Cu

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. #10-32 TAPPED THRU (5) "A" HOLES.
2. #8-32 TAPPED THRU (4) "B" HOLES.

C-54230M008

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL XX ± .01
   DECIMAL XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX.
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY BEFORE PLATING OR CONVERSION COATING.

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE FULL

CLASSIFICATION

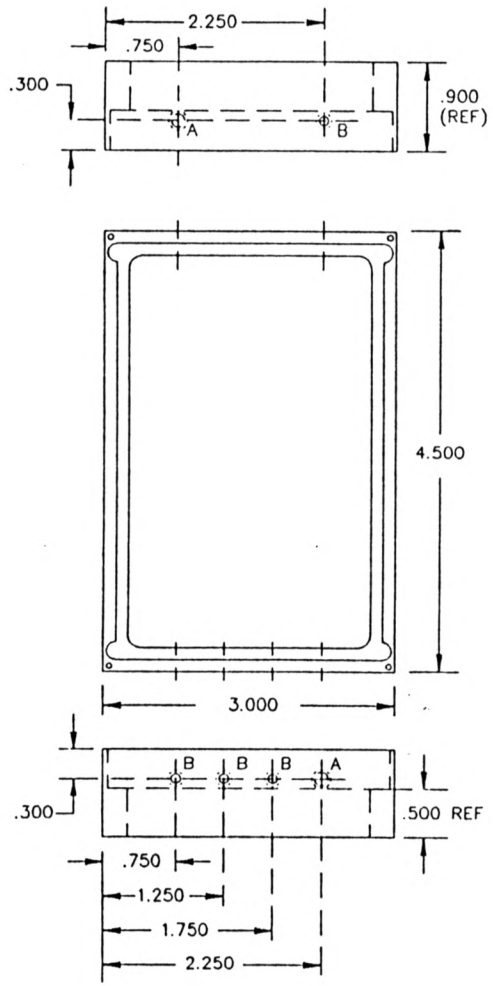
DRAWN FOR	A.E.ROGERS	DATE 3/88
DRAWN BY	A.P.HEBERT	3/88
CHECKED BY		
APPROVALS: PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
THERMAL		
MECH. ANALYSIS		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
OUTPUT RATE SYNTHESIZER DIVIDER

OUTDRILL	C	54230M008	
	DWG. SIZE	DWG. NO	REV.

CHANGE LETTER	D'WN BY	CHK'D BY	APP'D BY	DATE	D.C.N. & DESCRIPTION



1. #10-32 TAPPED THRU (2) "A" HOLES.
2. #3-32 TAPPED THRU (4) "B" HOLES.

C-54230M009

NOTES

MATERIAL

FINISH AND/OR HEAT TREATMENT

SHOP NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES
2. TOLERANCE ON DIMENSIONS
   FRACTIONAL ± 1/64
   DECIMAL .XX ± .01
   DECIMAL .XXX ± .005
   ANGULAR ± 0°30'
3. SURFACE ROUGHNESS PER MIL-STD-10
4. REMOVE BURRS AND BREAK SHARP EDGES 1/64 MAX
5. SCREW THREADS PER MIL-STD-9
6. ALL DIMENSIONS TO APPLY

USED ON

NEXT ASSEMBLY

WEIGHT

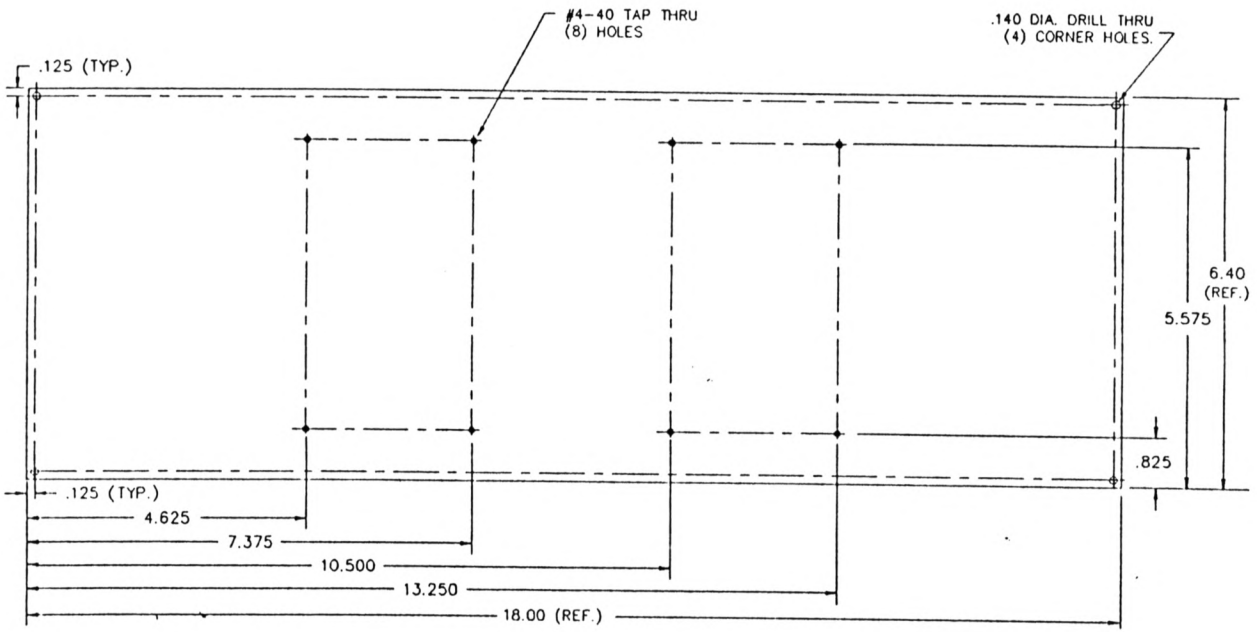
SCALE FULL

APPROVALS		
DRAWN FOR	A.E.ROGERS	3/88
DRAWN BY	A.P.HEBERT	3/88
CHECKED BY		
PROJECT		
ENGINEER		
MATL. & PROCESS		
STRUCTURES		
[redacted]		

NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS

DRILLING PLAN FOR
OUTPUT RATE SYNTHESIZER

[redacted] RATE/DR | C | 54230M009



NOTES:

MATERIAL: .125 ALUM. 6061-T6			A.E.ROGERS	12-86	NORTHEAST RADIO OBSERVATORY CORPORATION HAYSTACK OBSERVATORY WESTFORD, MASSACHUSETTS
FINISH AND/OR HEAT TREATMENT: CLEAR ALODINE			C.KOSTKA	12-86	DRILLING PLAN FOR MOUNTING PLATE OUTPUT RATE SYNTHESIZER
					AER\SYNPLT | D | 54230M010

D- 54230M010

PARTS LIST FROM DBASE FILE:PARTS.DBF

REF	SUBMOD	PART	DESC	MFR	COST	QTY	TOTAL COST
MP	RATE-A	1105-7521-003	SMC CABLE PLUG	AEP	2.49	7	17.43
MP	RATE-A	200458-1	BLOCK	AMP	3.00	1	3.00
MP	RATE-A	200833-4	GUIDE PINS	AMP	0.36	2	0.72
MP	RATE-A	200835-4	GUIDE SOCKETS	AMP	0.48	2	0.96
MP	RATE-A	201142-2	SPRING	AMP	0.05	10	0.50
MP	RATE-A	201143-5	COAXICON PIN	AMP	2.70	3	8.10
MP	RATE-A	202394-2	HOOD	AMP	1.04	1	1.04
MP	RATE-A	202422-1	POWER PINS	AMP	0.50	4	2.00
MP	RATE-A	328666	FERRULE	AMP	0.08	3	0.24
SS	RATE-A	54230I002	F.P.SILK SCREEN	NYES	100.00	1	100.00
MS	RATE-A	54230M001	FRONT PANEL	HAYSTACK	100.00	1	100.00
MS	RATE-A	54230M009	BOX DRILLING	HAYSTACK	20.00	1	20.00
MS	RATE-A	C53306M013-2UA	FRONT PANEL	PREC.MACHINE	20.00	1	20.00
MS	RATE-A	C53306M014-2UA	PERFORATED COVER	PREC.MACHINE	20.00	2	40.00
MS	RATE-A	C53306M015-2UA	MODULEREAR PANEL	PREC.MACHINE	20.00	1	20.00
MS	RATE-A	C53306M016	BAR SUPPORT	PREC.MACHINE	10.00	2	20.00
MS	RATE-A	C53306M017	SIDE PLATE	PREC.MACHINE	10.00	2	20.00
MS	RATE-A	HAY45030	BOX WITH COVERS	PREC.MACHINE	45.00	1	45.00
MP	RATE-DIV	1019-1511-000	SMC BULKHEAD	AEP	1.77	5	8.85
MP	RATE-DIV	1250-003	FEED THRU	ERIE	1.53	5	7.65
Q	RATE-DIV	2N3904	2N3904		1.00	1	1.00
MS	RATE-DIV	54230M008	BOX DRILLING	HAYSTACK	20.00	1	20.00
MS	RATE-DIV	HAY45030	BOX WITH COVERS	PREC.MACHINE	45.00	1	45.00
U	RATE-DIV	MAR-7	AMP	MINICIRCUITS	5.00	2	10.00
U	RATE-DIV	MC10H016P	10016	MOTOROLA	1.00	3	3.00
U	RATE-DIV	MC10H115P	MC10115	MOTOROLA	1.00	1	1.00
U	RATE-DIV	MC12019P	12019	MOTOROLA	10.00	1	10.00
MP	RATE-SYN	1019-1511-000	SMC BULKHEAD	AEP	1.77	4	7.08
MP	RATE-SYN	1250-003	FEED THRU	ERIE	1.53	2	3.06
U	RATE-SYN	63S081	PAL		1.00	2	2.00
U	RATE-SYN	74HCT14N	7414		1.00	1	1.00
U	RATE-SYN	74HCT390N	74390		1.00	2	2.00
U	RATE-SYN	75140P	75140		1.00	1	1.00
MP	RATE-SYN	CO-484V-BX	190.512 MHZ VCXO	VECTRON	100.00	1	100.00
MP	RATE-SYN	CO-484V-BX	189 MHZ VCXO	VECTRON	10.00	1	10.00
U	RATE-SYN	MC12015P	MC12015	MOTOROLA	1.00	1	1.00
U	RATE-SYN	MC12019P	MC12019	MOTOROLA	1.00	1	1.00
U	RATE-SYN	MC145152P1	PPL FREQ SYN	MOTOROLA	10.00	1	10.00
U	RATE-SYN	OP-27EN	OP-27	ANALOG DEV	10.00	1	10.00
MP	RATE-SYN	PSW-1211	DIODE SWITCH	MINICIRCUITS	24.00	1	24.00
*** Total ***							697.63

MOTOROLA

MC145152-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

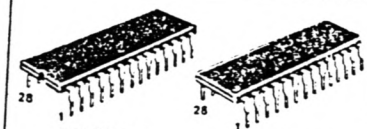
PARALLEL INPUT PLL
FREQUENCY SYNTHESIZER

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

The MC145152-1 is programmed by sixteen parallel inputs. The device features consist of a reference oscillator, selectable-reference divider, two output phase dectector, 10-bit programmable divide-by-N counter and 6-bit programmable ÷ A counter. When combined with a loop filter and VCO, the MC145152-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145152-1.

The MC145152-1 offers improved performance over the MC145152. Modulus Control output drive has been increased and the ac characteristics have been improved. Input current requirements have also been changed.

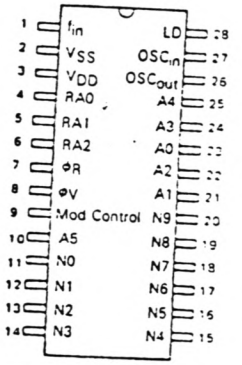
- General Purpose Applications:
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values — 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



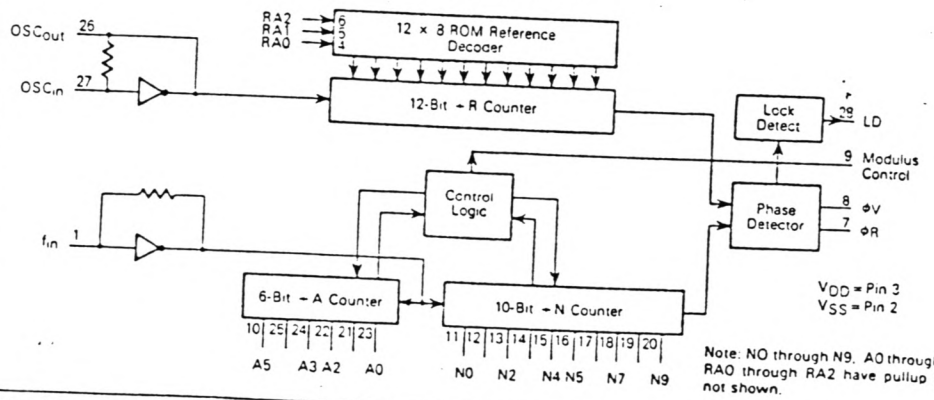
MC145152L1
CERAMIC PACKAGE
CASE 733

MC145152P1
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



BLOCK DIAGRAM



Note: N0 through N9, A0 through A5 and RA0 through RA2 have pullup resistors not shown.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature (8 Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
† Power Dissipation Temperature Derating
Plastic "P" Package: − 12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	− 40°C Min	− 40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level V_{in} = 0 V or V_{DD} I_{out} = 0 μA	V_{OL}	3 5 9	– – –	0.05 0.05 0.05	– – –	0.001 0.001 0.001	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
1 Level	V_{OH}	3 5 9	2.95 4.95 8.95	– – –	2.95 4.95 8.95	2.999 4.999 8.999	– – –	2.95 4.95 8.95	– – –	
Input Voltage 0 Level V_{out} = 0.5 V or V_{DD} − 0.5 V (All Outputs Except OSC_{out})	V_{IL}	3 5 9	– – –	0.9 1.5 2.7	– – –	1.35 2.25 4.05	0.9 1.5 2.7	– – –	0.9 1.5 2.7	V
1 Level	V_{IH}	3 5 9	2.1 3.5 6.3	– – –	2.1 3.5 6.3	1.65 2.75 4.95	– – –	2.1 3.5 6.3	– – –	
Output Current – Modulus Control V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	− 0.60 − 0.90 − 1.50	– – –	− 0.50 − 0.75 − 1.25	− 1.6 − 2.0 − 3.2	– – –	− 0.30 − 0.50 − 0.80	– – –	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	1.50 1.90 3.80	– – –	1.10 1.70 3.30	5.0 6.0 10.0	– – –	0.66 1.08 2.10	– – –	
Output Current – Other Outputs V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	− 0.44 − 0.64 − 1.30	– – –	− 0.35 − 0.51 − 1.00	− 1.0 − 1.2 − 2.0	– – –	− 0.22 − 0.36 − 0.70	– – –	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	0.44 0.64 1.30	– – –	0.36 0.51 1.00	1.0 1.2 2.0	– – –	0.22 0.36 0.70	– – –	
Input Current – I_{in}, OSC_{in}	I_{in}	9	–	± 50	–	± 10	± 25	–	± 22	μA
Input Current – Other Inputs (with Pullups)	I_{IH}	9	–	0.3	–	0.00001	0.1	–	1.0	μA
	I_{IL}	9	–	− 400	–	− 90	− 200	–	− 170	
Input Capacitance	C_{in}	–	–	10	–	5	10	–	10	pF
Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 μA	I_{DD}	3 5 9	– – –	800 1200 1600	– – –	200 300 400	800 1200 1600	– – –	1600 2400 3200	μA

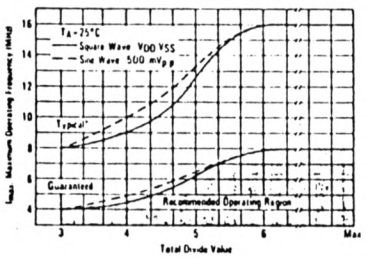
MC145152-1

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

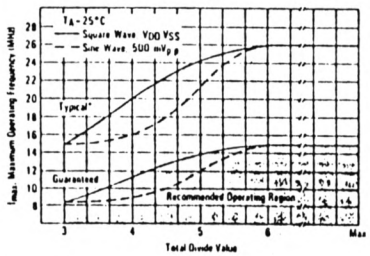
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 1 and 5)	t_{TLH}	3 5 9	– – –	50 30 20	115 60 40	ns
Output Fall Time, Modulus Control (Figures 1 and 5)	t_{THL}	3 5 9	– – –	25 17 15	60 34 30	ns
Output Rise and Fall Time, LD, ϕV, ϕR (Figures 1 and 5)	t_{TLH}, t_{THL}	3 5 9	– – –	60 40 30	140 80 60	ns
Propagation Delay Time f_{in} to Modulus Control (Figures 2 and 5)	t_{PLH}, t_{PHL}	3 5 9	– – –	55 40 25	125 80 50	ns
Output Pulse Width ϕR, ϕV with f_R in Phase With f_V (Figures 3 and 5)	$t_{W(e)}$	3 5 9	25 20 10	100 60 40	175 100 70	ns
Input Rise and Fall Times OSC_{in}, f_{in} (Figure 4)	t_r, t_f	3 5 9	– – –	20 5 2	5 2 0.5	μs

GRAPH 1 – OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

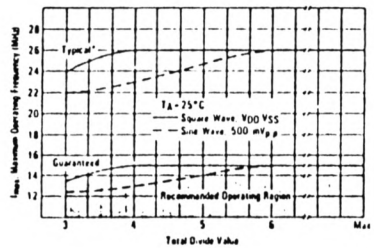
GRAPH 1A – V_{DD} = 3 V



GRAPH 1B – V_{DD} = 5 V

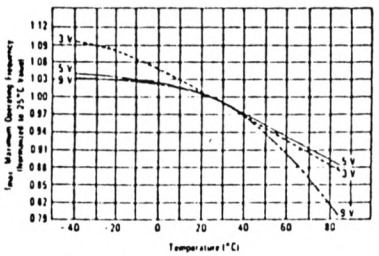


GRAPH 1C – V_{DD} = 9 V

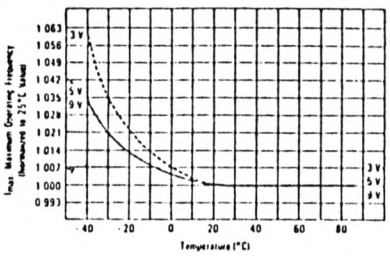


GRAPH 2 – OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A – TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B – TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance

PIN DESCRIPTIONS

f_{in} (Pin 1) – Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual modulus prescaler and is AC coupled into Pin 1. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

V_{SS} (Pin 2) – Circuit Ground.

V_{DD} (Pin 3) – Positive power supply.

RA0, RA1, RA2 (Pins 4, 5, and 6) – These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

ϕR, ϕV (Pins 7 and 8) – These phase detector outputs can be combined externally for a loop error signal.

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency of f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

MODULUS CONTROL (Pin 9) – Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter.

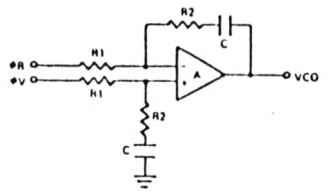
N INPUTS (Pins 11 through 20) – The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant digit and N9 is the most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

A INPUTS (Pins 23, 21, 22, 24, 25, 10) – The A inputs define the number of clock cycles of f_{in} that require a logic zero on the modulus control output. See page 8 for explanation of dual modulus prescaling. The A inputs all have internal pullup resistors that ensure that inputs left open will remain at a logic one.

OSC_{out}, OSC_{in} (Pins 26 and 27) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

LD (Pin 28) – Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

PHASE LOCKED LOOP – LOW PASS FILTER DESIGN



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NCR1}}$$

$$\zeta = \frac{\omega_N R2C}{2}$$

Assuming gain A is very large, then

$$F(s) = \frac{R2CS + 1}{R1CS}$$

NOTE: Sometimes R1 is split into two series resistors each R1 ÷ 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕV and ϕR. The value for C_C should be such that the corner frequency of the network does not significantly effect ω_N.

DEFINITIONS: N = Total Division Ratio in feedback loop

$$K_\phi = V_{DD}/2\pi$$

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N = (2\pi/10)\ f_r$ (at phase detector input)

$\zeta = 1$

SWITCHING WAVEFORMS

FIGURE 1

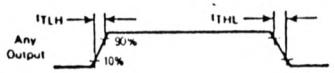


FIGURE 2

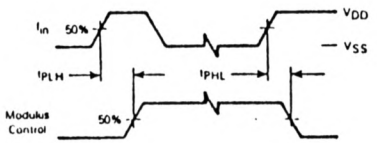
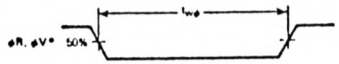


FIGURE 3



*f_V in phase with f_R

FIGURE 4

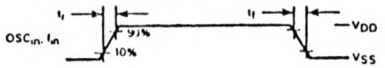


FIGURE 5 – TEST CIRCUIT

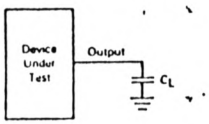
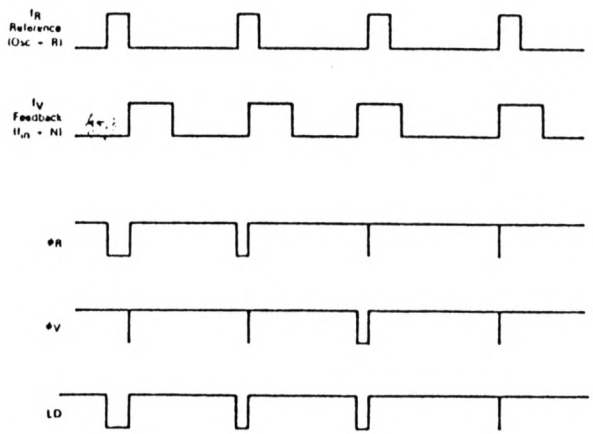


FIGURE 6
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is approximately equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)* New York, Wiley Interscience, 1979
Manassewitsch, Vadim, *Frequency Synthesizers Theory and Design (second edition)* New York, Wiley Interscience, 1980
Blanchard, Alain, *Phase-Locked Loops Application to Coherent Receiver Design* New York, Wiley Interscience, 1976
Egan, William F., *Frequency Synthesis by Phase Lock* New York, Wiley Interscience, 1981
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design* Englewood Cliffs, NJ, Prentice Hall, 1983
Berlin, Howard M., *Design of Phase Locked Loop Circuits, with Experiments* Indianapolis, Howard W. Sams and Co., 1978
Kinley, Harold, *The PLL Synthesizer Cookbook* Blue Ridge Summit, PA, Tab Books, 1980

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low frequency programmable counters to be used as high frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145152-1 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/ ÷ 4 to ÷ 64/ ÷ 65 can be controlled by the MC145152-1.

Several dual modulus prescaler approaches suitable for use with the MC145152-1 are given in Figure 7. The approaches range from the low cost ÷ 15/ ÷ 16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145152-1 and dual modulus prescaling are shown in Figures 8 and 9 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145152-1

The system total divide value (N_{Total}) will be dictated by the application i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N*P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{Total} values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the divide N counter. N is then incremented to N + 1 and the ÷ A is sequenced from zero through P – 1 again.

There are minimum and maximum values that can be achieved for N_{Total}. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint N ≥ A always applies. If $A_{max} = P - 1$ then $N_{min} \geq P - 1$. Then $N_{total-min} = (P - 1)\,P + A$ or $(P - 1)\,P$ since A is free to assume the value of zero.

$$N_{total-max} = N_{max} * P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of Pin 1 of the MC145152-1.

B. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the MC145152-1.

A sometimes useful simplification in the MC145152-1 programming code can be achieved by choosing the values for P of 8, 16, 32 or 64. For these cases, the desired value for N_{Total} will result when N_{Total} in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

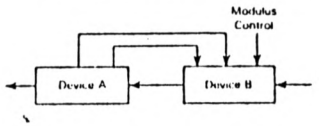
A. Assume the ÷ A counter contains "b" bits where $2^b = P$.
B. Always program all higher order ÷ A counter bits above "b" to zero.
C. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10 + b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_{Total}, now results when the value of N_{Total} in binary is used to program the "New" 10 + b bit counter.

FIGURE 7 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145152-1

MC12009	÷ 5/ ÷ 6	440 MHz Min
MC12011	÷ 8/ ÷ 9	500 MHz Min
MC12013	÷ 10/ ÷ 11	500 MHz Min
MC12015	÷ 32/ ÷ 33	225 MHz Min
MC12016	÷ 40/ ÷ 41	225 MHz Min
MC12017	÷ 64/ ÷ 65	225 MHz Min
*MC12018	÷ 128/ ÷ 129	520 MHz Min
MC3393	÷ 15/ ÷ 16	140 MHz Typ

*Proposed introduction

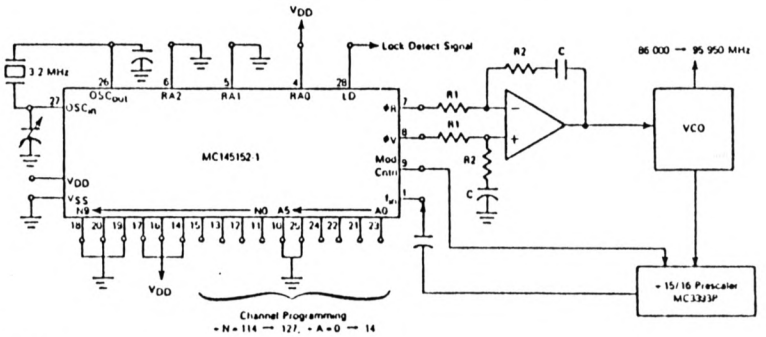
By using two devices, several dual modulus values are achievable.



Device A \ Device B	MC12009	MC12011	MC12013
MC10131*	÷ 20/ ÷ 21	÷ 32/ ÷ 33	÷ 40/ ÷ 41
MC10138	÷ 50/ ÷ 51	÷ 80/ ÷ 81	÷ 100/ ÷ 101
MC10154	÷ 40/ ÷ 41 or ÷ 80/ ÷ 81	÷ 64/ ÷ 65 or ÷ 128/ ÷ 129	÷ 80/ ÷ 81

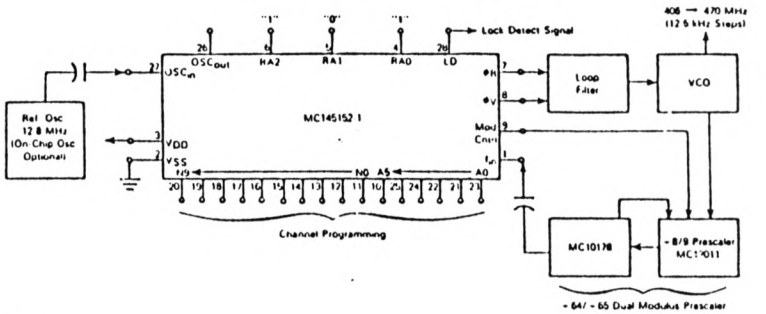
NOTE: MC12009, MC12011 and MC12013 are pin equivalent.
MC12015, MC12016 and MC12017 are pin equivalent.

FIGURE 8 — AIRCRAFT NAV RECEIVER SYNTHESIZER DEMONSTRATES A LOW COST DUAL MODULUS SYSTEM EMPLOYING THE MC145152-1



NOTES:
1. f_R = 50 kHz, ÷ R = 64; 22.0 MHz low side injection, N_{TOTAL} = 1720 → 1919.
2. Using 22.0 MHz for the receiver I.F. demonstrates how the choice of I.F. value can sometimes reduce the number of ÷ N bits that must be programmed. Using the more common 21.4 MHz I.F. would require six rather than four ÷ N programming inputs.

FIGURE 9 — SYNTHESIZER FOR LAND MOBILE RADIO UHF BAND COVERAGE DEMONSTRATES USE OF THE MC145152-1 IN SYSTEMS OPERATING TO SEVERAL HUNDRED MHz



NOTES:
1. $N_{TOTAL} = N*64 + A = 32480$ to 37600, N = 507 to 587, A = 0 to 63.
2. f_R = 12.5 kHz, ÷ R = 1024 (code 101).
3. The prescaling approach can be chosen for the application to enhance economy e.g., single chip MC3393P to approximately 100 MHz.
   MC12011 or MC12013 with dual flip flop to approximately 250 MHz.
   MC12011 or MC12013 with MC10178 to over 500 MHz.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For V_{DD} = 5 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_s, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

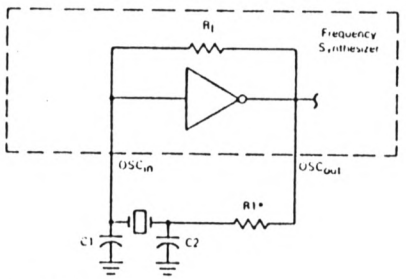
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

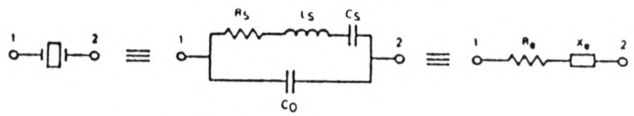
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



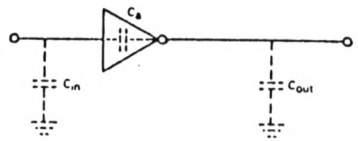
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES OF THE AMPLIFIER



MOTOROLA

MC12015
MC12016
MC12017

LOW-POWER TWO-MODULUS PRESCALER

The MC12015, MC12016 and MC12017 are two-modulus prescalers which will divide by 32 and 33, 40 and 41, and 64 and 65 respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc ±10% at pin 7 or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to pin 8.

- 225 MHz Toggle Frequency
- Low-Power — 7.5 mA Max at 6.8 V
- Control Input and Output are Compatible with Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

MECL PLL COMPONENTS

LOW-POWER
TWO—MODULUS
PRESCALER

P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-02

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

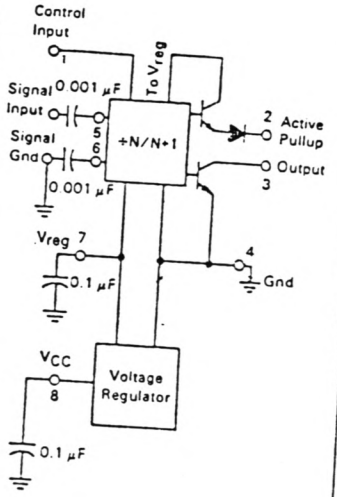
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	225	—	—	MHz
	f_{min}	—	—	35	MHz
Supply Current	I_{CC}	—	6.0	7.8	mA
Control Input High (÷32, 40 or 64)		2.0	—	—	V
Control Input Low (÷33, 41 or 65)		—	—	0.8	V
Output Voltage High* (I_{source} = 50 μA)	V_{OH}	2.5	—	—	V
Output Voltage Low* (I_{sink} = 2 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity 35 MHz	V_{in}	400	—	800	mVPP
50–225 MHz		200	—	800	
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} −70	ns

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

*Pin 2 connected to Pin 3

PRESCALER BLOCK DIAGRAM



1. Vreg @ pin 7 is not guaranteed to be between 4.5 and 5.5 V when Vcc is being applied to pin 8.
2. Pin 7 is not to be used as a source of regulated output voltage.

MOTOROLA

MC12019

LOW-POWER TWO-MODULUS PRESCALER

The MC12019 is a divide by 20 and 21 two-modulus prescaler. It will divide by 20 when the modulus control input is high and by 21 when the modulus control input is low.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 5.5 V
- Control Input Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Outputs

MECL PLL COMPONENTS

LOW-POWER
TWO—MODULUS
PRESCALER
÷20/21

P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-02

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 7	V_{CC}	8.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = -40° to +85° C)

Characteristic	Symbol	-40°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
Toggle Frequency (Sine wave input)	f_{max} f_{min}	225 —	— 35	225 —	— 35	225 —	— 35	MHz MHz
Supply Current	I_{CC}	—	7.5	—	7.5	—	7.5	mA
Control Input High (÷20)		2.0	—	2.0	—	2.0	—	V
Control Input Low (÷20)		—	0.8	—	0.8	—	0.8	V
Output Voltage Swing	V_{out}	—	600	—	600	—	600	mV_{pp}
Input Voltage Sensitivity 35 MHz 50–225 MHz	V_{in}	 400 200	 800 800	 400 200	 800 800	 400 200	 800 800	
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	t_{out}-70	—	t_{out}-70	—	t_{out}-70	ns

Notes:
1. t_{PLL} = the time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

PRESCALER BLOCK DIAGRAM