VLBA Technical Report No. 42
THE VLBA CORRELATOR SYSTEM OVERVIEW

EXCLUDING APPENDICES C, D and F

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TABLE OF CONTENTS

TABLE OF FIGURES

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1. INTRODUCTION AND SPECIFICATIONS

1.1 INTRODUCTION

The Very Long Baseline Array (VLBA) correlator is a highly specialized computer which was designed for the purpose of processing data, collected on magnetic tape, by the ten stations in the VLBA. The design allows for data from ten additional stations to be processed for a total of twenty stations. The conceptual design of the correlator can be traced to September 29, 1983, the date of the first memo written for the VLBA Correlator Memo Series. Construction began in Charlottesville, VA in 1988, and the correlator was moved to the Array Operations Center in Socorro, NM and put into service in 1992. The first scientific results were obtained from the correlator on October 21, 1993. Between 1993 and 1997, an upgrade was implemented to support Orbiting Very Long Baseline Interferometry (OVLBI), which includes an orbiting station as one of the twenty, on board a satellite. First fringes for the VLBA correlator in an OVLBI experiment were detected on June 27, 1997.

This manual is intended to provide scientists, operators, programmers, engineers, technicians, and others with a general yet comprehensive description of the VLBA Correlator System. Specifications, modes and basic hardware and firmware operation will be covered, primarily at the block diagram level. The correlator system is considered to be all components between the output of the Playback Drives and the VME computer system, including the applicable interface cards in the VME computer system. Those requiring a more detailed description of the system should refer to the series of technical reports on the VLBA correlator (Technical Reports No. 43 through 46). Any acronyms which are not defined where first used, can be found in Appendix E.

1.2 SPECIFICATIONS

Inputs.....Supports a maximum of 24 VLBA PBDs, 6 into each of 4 racks; 20 of 24 PBDs can be selected for input to FFT engines, 8 IF channels per station

Formats.....VLBA formatted data, and Mark III Mode B unrestricted, Mark III Modes A & C, with some restrictions, and a subset of Mark IV

Pulsar.....Arbitrary Gating Profile, 1024 points/period Pulse Phase Resolution, 16 uS minimum Pulse Timing Resolution

Tracking, Delay...Delay change rate +/- 1000 samp/sec (for 0.1% decorrelation limit), Delay resolution 1/128 bit (FSTC), Delay model update period 4 ms. for the integer portion and 16 uS for FSTC portion, Delay switching range 6000 samples, number of Delay models 4

Tracking, Fringe..Fringe rate range -128 to +128 kHz (+/- full

bandwidth), Fringe phase resolution 8 bits, Fringe acceleration range +/- 3400 Hz/s (for 0.1% decorrelation limit), Fringe model update rate 32 MHz, Fringe tracking error < 0.5 deg. times speedup factor, Fringe models per channel 4

Timing.....Sampling rate 32, 16, 8, 4, 2 Msamp/sec, Speedup factor at full speed playback 1, 2, 4 for record rates of 8, 4, and 2 MHz -- results in playback at constant rate of 8 MHz

FFT.....160 FFT engines, FFT sizes 64, 128, 256, 512, 1024, & 2048 points/channel, 2048 point FFT in 16 uS, FFT precision expressed in complex floating-point arithmetic 7 bit real, 7 bit imag. with common 4 bit neg. exp, also expressed as (7,7,4), Polarization mode is capable of 256 point FFTs and smaller (128 spectral channels) in 20 Station mode, 2K FFTs are limited to 2 IF channels, 1K FFTs are limited to 4 IF channels.

Quantization....Supports 2 bit 4 level, and 1 bit 2 level, the 2 bit quantization employs a +/- 200mv. threshold

Integration.....Short term on 131.072 ms fixed cycle with 15,15,6 precision, long term is variable up to 2.5 hrs. (430,080 complex terms), results of long term integration are in 32 bit IEEE floating-point format

Filtering.....Post Accumulation Finite Impulse Response (FIR) programmable filter stage provides an alternative to boxcar averaging of archive data, data taps provided 8, 16, 32, and 64 resulting in decimation rates of 1, 2, 4, and 8, respectively

Archive.....Specified max archive rate 0.5 Mbytes/sec to DAT, (current rate is 2 Mbytes/sec) distributed on various media in FITS tape format

Hardware.....Motorola 68000 uP and Intel 87C51 microcontrollers with associated RAM and EPROM ICs, AMD 29C327 Floating-point Math chips, Xilinx Programmable Gate Arrays, PAL and GAL Programmable Logic Devices, implementation of VLBA1 (semi-custom) in the LSI Logic ASIC device, and misc. TTL, ECL, and CMOS logic families

Design Software.ORCAD 386+ (elec. dwgs.), AutoCAD (mech. dwgs.) ABEL (some PALASM) PAL source equations, Xilinx, C, 2500AD cross asm. for 8751 and 68K uP. File Express, Lotus 123, WordPerfect, MS Word

Communications..Ethernet, SCSI bus, RS-232, HCB (internal bus)

Computers.....Sun 4 workstation w/UNIX OS, Motorola MVME167 w/68040 and Wind River VxWorks OS

Power.....D.C power capacity of system supplies: 1500W (8),

1250W (4), 475W (1), misc. 25W, total 17.5 kW; actual power consumption is approximately 70% of capacity, input power (AC) is approximately 15 kW, power supplies provide +5V, -5V, +15V, -15V,

2. GENERAL SYSTEM ARCHITECTURE

The large size and complexity of the correlator prohibits the presentation of the entire system in a single diagram. A top level view of the system is shown below in Figure 1 VLBA Correlator Overview, which includes the connections from the 24 individual tape play back drives (PBDs) and play back interfaces (PBIs), into the 20 FFT engines and on to the 20x20 cross-multiplier array. Figure 1 shows one of eight correlator channels. The output of the multiplier array enters the remaining blocks, beginning with the Long Term Accumulator (LTA), into the Finite Impulse Response Filter (FIR), and on to archive and distribution. The LTA and FIR are generally referred to as the back end of the correlator. Also shown inside the dotted lines of this diagram is a simplistic view of some of the functional software blocks that control their associated hardware elements. These software blocks are shown strictly for reference and will not be treated further in this document.

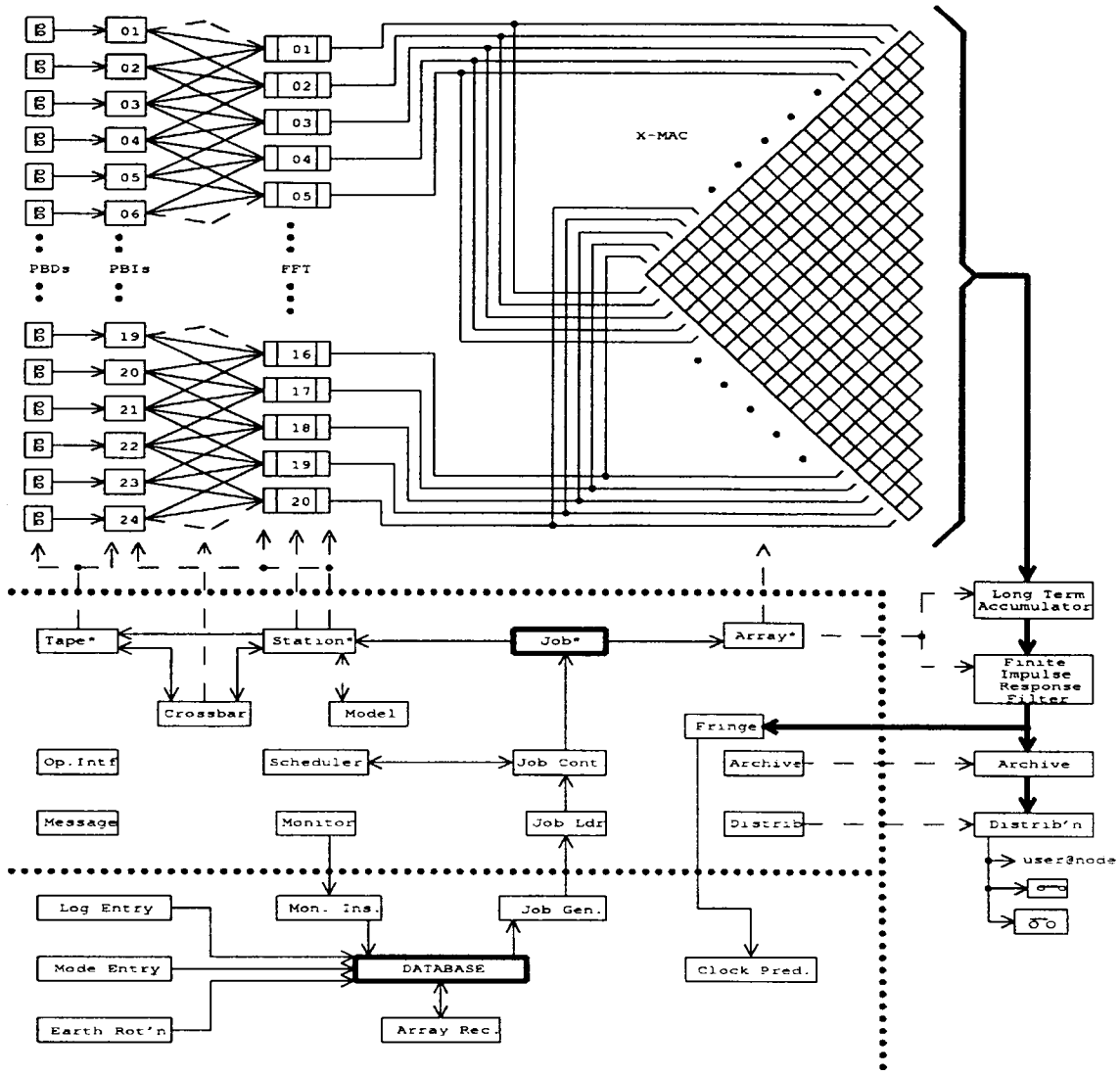


Figure 1 VLBA Correlator Overview

2.1 SYSTEM DATA PATH

The VLBA correlator has the capacity to process the data tapes from twenty stations (usually numbered Station 0-19) selected from twenty-four available playback drives (usually numbered PBD 1-24). The overall data path is illustrated in Figure 2. There is a crossbar switch between the deformatters and the FFT cards that selects which of the 24 deformatter outputs will be switched in to the 20 FFT channels.

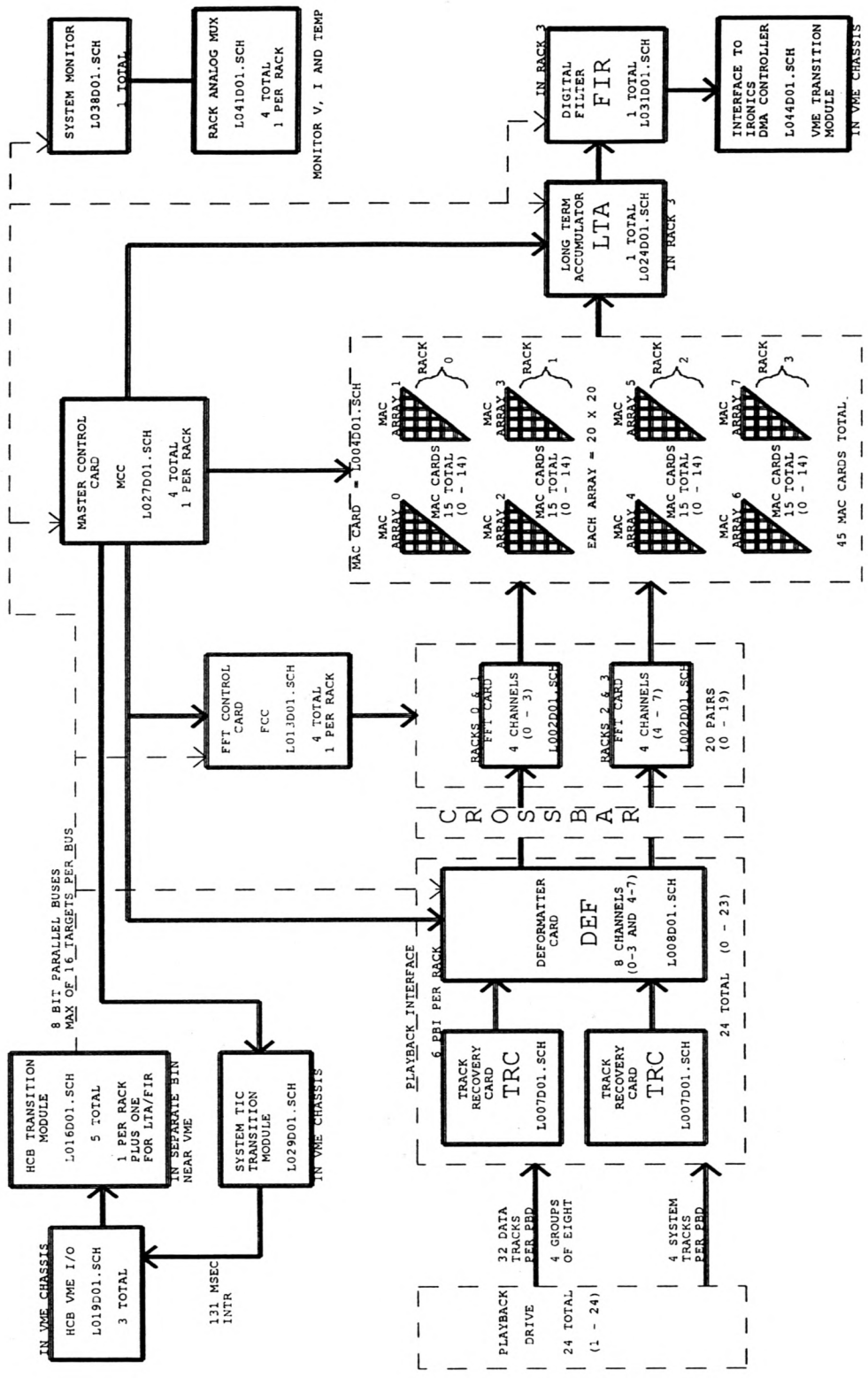


Figure 2 Overall Data Path

Each of these drives can supply 32 tracks at up to 8 Mbits/sec per track. Occasionally, an observation may start on one tape and terminate on a second tape for a particular station. The four idle drives can be preloaded with tapes containing the second portion of an observation. When the first part runs out, the second part can be switched in from a different drive via a crossbar switch while the experiment is being processed. The drives can be assigned to correlator inputs in a variety of ways. For example, a single experiment incorporating the ten VLBA stations and ten additional stations could be processed in a single experiment with twenty stations, or two independent ten station experiments could be processed simultaneously. These are but two examples; other input configurations are also supported. Depending upon the bandwidth and formatter mode used to record an experiment, the data from a single sampler may have been demultiplexed over several tape tracks or data from several samplers may have been multiplexed into a single tape track. During playback, these recording modes will require that the corresponding mux/demux operation be performed in the correlator in order to reconstruct the original data streams.

During playback, data from the drives must remain synchronized together. This is accomplished by initially finding the starting data frame on each tape, and starting all of the playback drives in unison. This starting frame will contain a time reference based on the Modified Julian Date (MJD) which is identical to the time reference in the starting frames of the other tapes. Synchronization is maintained by varying the tape speed under servo control while monitoring the time markers retrieved from each frame of each tape.

In most cases, tapes have been recorded to conform to one of several recording formats. An early format that is supported is Mark III (A & C), and a later one is the VLBA Longitudinal Track Format. Mark IV is coming into some use and a subset of this format is also supported, at up to 8 Mbits/sec. More discussion on these formats can be found in subsequent sections dealing with the PBI. The header fields are removed from the data frames and the original raw data streams are reconstructed in the PBI. The data then enters the FFT (Fast Fourier Transform) engines where spectral channels are developed. After the FFT is performed, multiplications are performed on baseline pairs in the Multiply/Accumulate (MAC) cards. Here, the results are accumulated on a short-term basis, with fixed integration intervals of 131 ms. The order in which these two steps are performed, FFT first and cross multiplication second, define the VLBA correlator as an FX type processor. In contrast, the VLA correlator multiplies first and performs FFT second, defining it as an XF type. Results from the short-term integrations are routed to a Long Term Accumulator (LTA) where additional integration, with a range of integration times, is performed. From the LTA, the data passes through a Finite Impulse Response filter stage (FIR), which may be used to further smooth the data before writing to tape.

In addition to tape synchronization, several other artifacts and structures within the data must be considered during processing. Software algorithms known as models are applied to the data to make necessary corrections and adjustments to remove these effects. There are three models: the delay model which is applied to reconstruct wave front timing, the fringe model which is used to remove Doppler effects, and the pulsar model which corrects for the wave dispersion inherent in pulsar observations.

Judgements of data quality are made starting with parity and CRCC. These errors, as well as momentary losses in frame synchronization or

discontinuities in the time stamp from frame to frame, may identify blocks of data that are not of sufficient integrity to process. Such blocks, when identified, will be prevented from contributing to the accumulated results.

The correlated results of an experiment are written to a Digital Audio Tape (DAT) and made available to the observer on a variety of media.

2.2 SYSTEM CONTROL FUNCTIONS

Top level control of the correlator is implemented in a SUN workstation, identified as `reber'. This workstation is the file server and provides a user interface through the workstation windowing system, to the real time system. An older workstation, identified as CCC (Correlator Control Computer), was the original control computer. CCC is now used as a multiple window terminal for the engineering staff to operate the correlator, primarily for diagnostics, through communications with reber and the Motorola VME system.

Within the correlator are over one hundred microprocessors, numerous control sequencers, and Xilinx FPGAs. All of these devices require volatile memories to be loaded for initial operation as well as system reconfigurations. The programmable nature of these hardware elements requires a considerable amount of data to be downloaded to the correlator cards, not only to initialize the system from a power up, but also to carry out the necessary reconfigurations and mode changes needed to playback the experiments. The workstation is not suitable to perform tasks at this level; therefore, they are done in a real time system.

A Motorola VME real time system containing the MVME167 processor and the VxWorks operating system is used to directly interface to the hardware. The VME system can be accessed through a local console (presently an IBM PC) or by remote login. The VME system is used to run the user interface 'rscreens' and to execute instructions from the VxWorks prompt. Communications between the workstation and the VME system are over an Ethernet connection. The MVME 167 processor communicates with the correlator cards over the Hardware Communications Bus (HCB). This is a custom hardware interface that allows the HCB controller in the VME chassis to send commands to the targets on the HCB and passes data bidirectionally according to a defined set of message protocols. Job control scripts are read by the real time system and configuration changes such as PBD assignments, playback modes, FFT size, and integration times are then made via HCB commands. The VME system is also equipped with several Small Computer System Interface (SCSI) busses. These are primarily used to write the correlator output data to hard drives and ultimately cassette tape.

All of the microprocessors in the system are directly accessible through serial ports. These port connections provide entry points for the engineering staff to monitor local status and execute commands at the card level. This serial port network is accessed with four terminals (presently IBM PC clones with VT100 emulators), one for each of the four racks. With each terminal, there is a four-way switch box to select one of four serial cables to the rack. The four cables can be plugged into a distribution board that selects a microprocessor to talk to. A three-way switch box within the rack further selects the desired PBI.

The system clock is derived from a master 32 MHz sine wave oscillator and distributed to all four correlator racks and to a test rack in the lab. Each of the correlator racks has three amplifier/divider modules, one for each bin. Since the lab test rack has only two bins, it also has only two clock/divider modules. These amplifier/divider modules each provide up to ten clock outputs which are transmitted across the bin backplanes and are received by a small differential driver circuit that can serve two module slots. The driver circuits are located as close to the module slots as possible.

In order to prevent damage to the system components, a system monitor module looks for faults or out of range values, with respect to voltages, currents, and temperatures. If one of these parameters is out of range, the system monitor will initiate a system shutdown and can then provide a snapshot of these values at the time the shutdown was initiated to assist in locating the problem. A terminal normally remains connected to the system monitor to make the status of these parameters available at a glance.

2.3 POWER REQUIREMENTS

The power supplies in the system have the combined capacity to deliver approximately 17,500 watts of DC power to the correlator components. The actual DC power consumption is roughly 70% of this capacity, 12,250 watts. The main voltage busses are the +5V, which is used by all of the TTL devices throughout the system, and the -5.2V, which is used by the ECL components. There is a +15V, which is used by the clock amplifiers. The devices used for RS232 signaling are capable of internally generating the +/-12V signal levels to meet the requirements for RS232.

3. CORRELATOR HARDWARE

The modules that collectively make up the correlator are packaged in a set of five racks. The front of this rack set is shown in Figure 3.

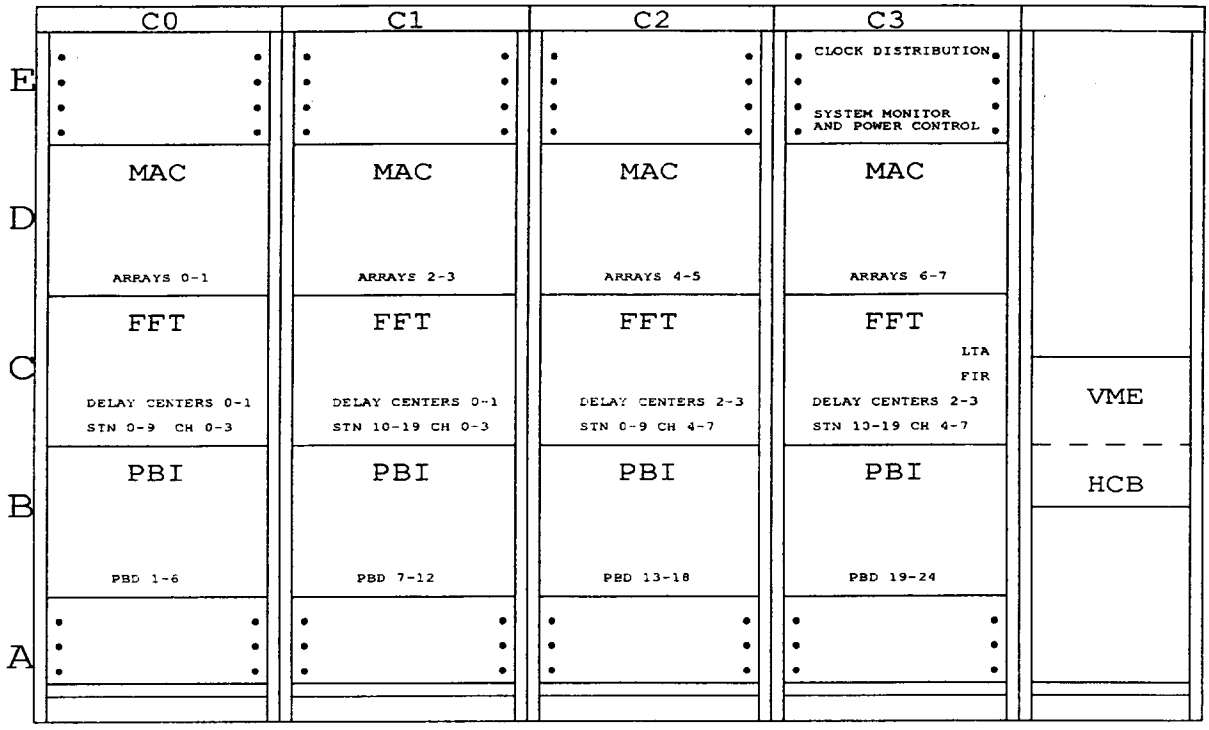


Figure 3 Correlator Racks Front View

The racks labeled C0-C3 all basically perform the same functions. The only exception is that rack C3 has additional modules which monitor system vitals, provide a back end interface, and supply master timing to the other three racks. The rack on the right end of Figure 3 contains the VME Real Time System (RTS), HCB controllers, hard disks, and tape drives. Semiconductor technology used in the correlator includes standard TTL and ECL logic devices; microprocessors, microcontrollers and associated RAM and EPROM memories; PALs, GALs and Xilinx FPGAs; ASICS, and a few arithmetic devices. In the discussion of correlator hardware, an overview of the rack architecture is first presented. The overview is followed by a closer look at the major blocks in the PBI, FFT and MAC bins, and concludes with a look at the back-end and VME functions. Many of the examples in this section will be limited to a single track or data path to simplify discussion of data flow through the system. After the system architecture is presented, topics that relate to the system as a whole can be treated. Some of these system level topics include timing and control, models, and the use of weights and validities for error handling.

3.1 OVERVIEW OF SYSTEM RACKS

Each C rack is divided into three bins, with the name of each bin reflecting the functions and modules associated with it; PBI, FFT, and MAC. Data flow within the rack is from bottom to top. The main modules accessible from the front of the racks and the associated bins are as follows below in Table 1:

Table 1 Module Types and Spares

BIN	MODULE	NUMBER OF CARDS	SPARES
PBI	Track Recovery Cards (TRC)	12/bin 48/system	7
PBI	Deformatter Cards (DEF)	6/bin 24/system	3
FFT	Fast Fourier Transform (FFT)	10/bin 40/system	5
FFT	FFT Control Cards (FCC)	1/bin 4/system	2
MAC	Multiply/Accumulate Card (MAC)	15/bin 60/system	8
MAC	Master Control Card (MCC)	1/bin 4/system	1
FFT	Long Term Accumulator (LTA)	1/bin 1/system *	1
FFT	Finite Impulse Response (FIR)	1/bin 1/system *	1

* NOTE: LTA and FIR are in Rack 3 only

Figure 2 provides a view of the major blocks in the system, with respect to the data path. In the back of each C rack, below the PBI bin, is a connector panel for the input connections from the PBDs. The PBI bin in each rack contains six PBIs, which are each cabled to a PBD. Each of the PBIs have 2 TRCs and one DEF. Thirty-two tracks of formatted data and four system tracks from each of the twenty-four PBDs are sent to the correlator at a 9 MHz rate. Each of the data tracks is accompanied by a 9 MHz data clock. These thirty-six tracks and clocks are transmitted to the PBI across four twisted pair, shielded ribbon cables. Each cable is twenty pairs wide. There is one each for odd track and even track data, and odd track and even track clocks. There is also a test path for the clock, data and control signaling for the loopback test mentioned in Appendix A.10. Each data and clock cable group terminates on the input panel and is redistributed to the backplane through an input harness to the TRCs such that each of the TRCs in the PBI receives a group of eighteen datas and clocks containing a mixture of odd and even tracks. There is also a cable (using 9 pin D connectors) between the PBI and the MVME 117 module in the PBD, which provides the path for servo control of the PBD using an RS-232 communications interface.

The 9 MHz data recording rate is used in a formatting mode generally identified as non-data replacement. In this mode, the sampled data is taken into the formatter at a rate of 8 MHz and clocked into a FIFO. Data is read out of this FIFO at the 9 MHz rate. The faster read rate allows for spaces to be opened up where header information and parity bits can then be inserted. Use of this mode prevents the data loss characteristic of the data replacement mode, which allows header information to overwrite astronomical data samples.

The PBI removes all formatting from the data streams and restores the data to its original state, at the 8 MHz rate, prior to being formatted for recording. The original digitized samples of the baseband signal could be either one-bit two-level, representing sign only, or two-bit four-level containing both sign and magnitude information. A pair of TRCs, each supporting eighteen tracks, both work into a single Deformatter. These three boards constitute a single PBI and are shown inside the dashed line on the block diagram of Figure 2. All the headers, track multiplexing, bit modulation, NRZI encoding, parity, and barrel rolling which was imposed in the formatter is removed (additional information on the formatter, can be found in VLBA Tech Report #15 on The VLBA Receiving and Recording System).

With as many as twenty PBDs playing out data from a single experiment, it is a non-trivial task to keep all of the drives synchronized. Data frames with identical time signatures in the headers must be found on every drive. This is done during initialization of the experiment on a tape pre-pass, with the starting time signature provided by the observe file. The RTS computer in the VME chassis contains a serial interface that supervises the MCB that all of the PBDs are connected to. Using the MCB, the RTS can read the tape frame headers directly with the PBD mini-decoders and extract the time code from the frame. Once the starting frames are located with the matching time signatures, the drives are started in unison and matching times must be maintained throughout the experiment. This synchronization is maintained by the play back interface circuitry, which is discussed in more detail in subsequent sections. While the tapes are turning, sync may be lost due to passing over a splice, a dirty head, or excessive errors. Any loss of sync results in the need to resync the tape with the rest of the experiment. This is accomplished by speeding up or slowing down the PBDs under servo control as necessary, to re-slave the drives to the same time.

As the array tracks the source through the sky, the time that the wave front arrives at one antenna relative to the others will constantly vary. Delays are applied to the data at playback in order to precisely synchronize the wave fronts as seen by each of the antennas. The delay model provides the delay values in two parts, an integer part and a fractional part. The integer delays, with a resolution of one Nyquist sample bit, are applied in the PBI. Phase rotation at the output of the FFT is used to correct for fractional bit delays. This is referred to as Fractional Sample Time Correction. The resolution of the FSTC is 1/128 of a Nyquist sample bit.

The TRCs receive data frames from the tape at a rate of 2.5 ms. Each frame contains header fields, longitudinal parity, bit modulation, track multiplexing and is subject to barrel rolling. The header fields, bit modulation, and longitudinal parity are removed and decoded in the TRCs. The data extracted from the formatted frames is delivered to the Deformatter in a 4 ms. cycle where the barrel rolling is removed and the channels are reconstructed from any track multiplexing that had been imposed. Details regarding the structure of the many formats and multiplexing modes that are used will be deferred to the discussion of the PBI.

Up to eight channels are output from each Deformatter into the FFT pipelines. The data in these channels is a function of which front ends were selected for the observation, which polarization (RCP & LCP) and portions of the IFs were selected in the BBCs, and what FFT size is selected in the correlator. A variety of recording modes, sampling rates, quantization levels, bandwidths and spectral resolution is supported by the VLBA. All of these variables will determine the internal configurations of the correlator required to process the data. Table 2 below summarizes the record rates and multiplexed modes of operation. Table 3 then summarizes the basic modes in the deformatter. More detail in this area can be found in VLBA Technical Report #43 which covers operation of the PBI.

Table 2 Record Rates

SAMPLE RATE MHz	BAND WIDTH MHz	OVS FACT	RECORD RATE 1-4	1-2	1-1	2-1	4-1 ←-(B-T)
32	16	1	8MB/s				
32	8	2	8MB/s				
32	4	4	8MB/s				
32	2	8	8MB/s				
32	1	16	8MB/s				
16	8	1	4MB/s	8MB/s			
16	4	2	4MB/s	8MB/s			
16	2	4	4MB/s	8MB/s			
16	1	8	4MB/s	8MB/s			
16	0.5	16	4MB/s	8MB/s			
8	4	1	2MB/s	4MB/s	8MB/s		
8	2	2	2MB/s	4MB/s	8MB/s		
8	1	4	2MB/s	4MB/s	8MB/s		
8	0.5	8	2MB/s	4MB/s	8MB/s		
8	0.25	16	2MB/s	4MB/s	8MB/s		
4	2	1		2MB/s	4MB/s	8MB/s	
4	1	2		2MB/s	4MB/s	8MB/s	
4	0.5	4		2MB/s	4MB/s	8MB/s	
4	0.25	8		2MB/s	4MB/s	8MB/s	
4	0.125	16		2MB/s	4MB/s	8MB/s	
2	1	1			2MB/s	4MB/s	8MB/s
2	0.5	2			2MB/s	4MB/s	8MB/s
2	0.25	4			2MB/s	4MB/s	8MB/s
2	0.125	8			2MB/s	4MB/s	8MB/s
2	0.0625	16			2MB/s	4MB/s	8MB/s
1	0.5	1				2MB/s	4MB/s
1	0.25	2				2MB/s	4MB/s
1	0.125	4				2MB/s	4MB/s
1	0.0625	8				2MB/s	4MB/s
0.5	0.25	1					2MB/s
0.5	0.125	2					2MB/s
0.5	0.0625	4					2MB/s

Table 3 Mode Table

	FFT SIZE	A 1 BITSTREAM TO 4 TRACKS	B 1 BITSTREAM TO 2 TRACKS	C 1 BITSTREAM TO 1 TRACK	D 2 BITSTREAMS TO 1 TRACK	E 4 BITSTREAMS TO 1 TRACK
1	512 or Smaller	n1-4e DEFCTL.MCS BSP-2.MCS Data Valid Delay = 04 Barrel Roll Delay = Pipeline Delay = ff c7 0	n1-2e DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff e3 1	n1-1e DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 2	n2-1e DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f2 3	n4-1e DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f0 4
2	OVERSAMPLED 512 or Smaller	v1-4e w1-4e x1-4e y1-4e DEFCTL.MCS BSP-1 BSP-6 BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff c7 5	v1-2e w1-2e x1-2e y1-2e DEFCTL.MCS BSP-6 BSP-3.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff e5 6	v1-1e DEFCTL.MCS BSP-6.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f6 7	v2-1e DEFCTL.MCS BSP-6.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff fb 8	v4-1e DEFCTL.MCS BSP-6.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f6 9
3	1K	n1-4f DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff c7 10	n1-2f DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff e3 11	n1-2f DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 12	n2-1f DEFCTL.MCS BSP-6.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 13	n4-1f DEFCTL.MCS BSP-6.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 14
4	OVERSAMPLED 1K	v1-4f w1-4f x1-4f y1-4f DEFCTL.MCS BSP-9 BSP-7 BSP-3.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff ef 15	v1-2f w1-2f x1-2f y1-2f DEFCTL.MCS BSP-7 BSP-4.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff fb 16	v1-1f DEFCTL.MCS BSP-7.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 17	v2-1f DEFCTL.MCS BSP-7.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f9 18	v4-1f DEFCTL.MCS BSP-7.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff fd 19
5	2k	n1-4g DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff cb 20	n1-2g DEFCTL.MCS BSP-2.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff fb 21	n1-1g DEFCTL.MCS BSP-7.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f3 22	n2-1g DEFCTL.MCS BSP-7.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 23	n4-1g DEFCTL.MCS BSP-7.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f7 24
6	OVERSAMPLED 2K	v1-4g w1-4g x1-4g y1-4g DEFCTL.MCS BSP-0 BSP-8 BSP-4.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f7 25	v1-2g w1-2g x1-2g y1-2g DEFCTL.MCS BSP-8 BSP-5.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f3 26	v1-1g DEFCTL.MCS BSP-8.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f1 27	v2-1g DEFCTL.MCS BSP-8.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f0 28	v4-1g DEFCTL.MCS BSP-8.MCS Data Valid Delay = Barrel Roll Delay = Pipeline Delay = ff f0 29

Between the PBI and the FFT bins, there is a logical element referred to as the crossbar switch. The purpose of this switch is to get the data from the PBIs into the FFT pipelines, the station delays from the FCCs back to the PBIs, and also to route statistics on data quality (validities) from the deformatters to the integrators on the MCCs. The full layout of this switching network is represented on the drawings labeled CROSSBAR, PBI-FFT: CHANS 0-3 (V0701.BLK), and CHANS 4-7 (V0702.BLK). Only the drawing for Channels 0-3 is shown in Figure 4 below. (The paths between the deformatters and the MCCs is not shown in Figure 4).

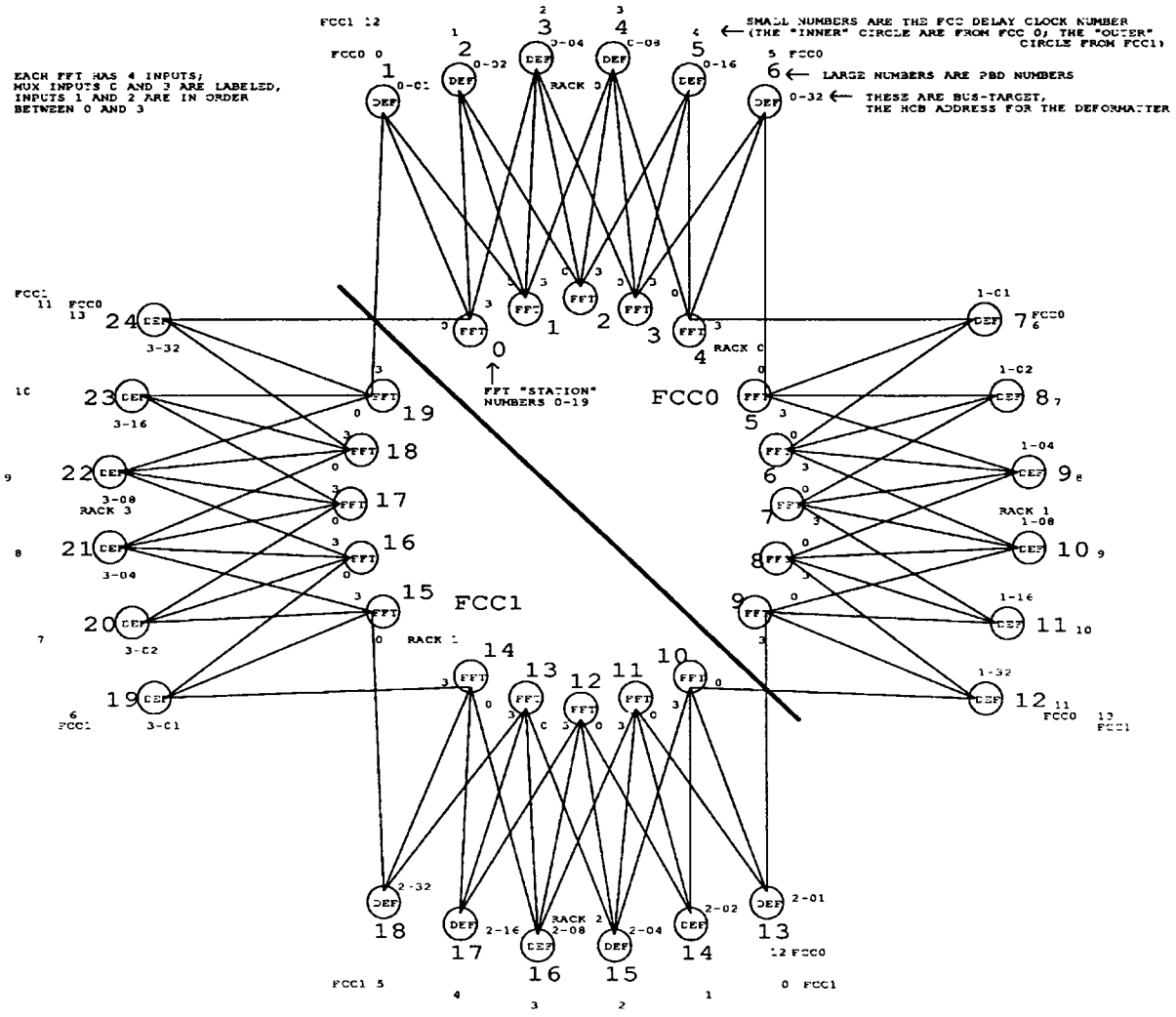


Figure 4 Channel 0-3 Crossbar

The data streams are reconstructed in the PBI into the same eight IF channels they were originally assigned to in BBCs. These eight channels come from each Deformatter as one or two bit samples that drive the inputs to 8 FFT channels which are distributed across 2 FFT cards with 4 channels each. These samples now have a correction applied for fringe rotation and result in an 18 bit complex floating-point representation to satisfy the inputs to the 160 FFT pipelines (8 per station, 20 stations). The FFT pipelines are implemented in ASICs, which are driven by a 32 MHz clock and operate on a 16 us. cycle. The ASIC was designed to operate in two modes, both FFT and Multiply/Accumulate. This IC then, is used in both the FFT pipelines and the multiplier arrays. Once in the FFT pipeline, the data is transformed from the time domain to the frequency domain. The total bandwidth can be transformed by the FFT engines with sizes ranging from 64 to 2048 time ordered points resulting in 32 to 1024 spectral channels. Some other functions performed in the FFT bin include the application of the fractional delay (FSTC), fringe rotation, and windowing.

The FFT size is specified by the observer. For FFT sizes of 512 points and less, the 8 IF channels are routed through the FFT cards and

subsequently into the 8 multiplier arrays with a mapping relationship of one to one. For FFT sizes greater than 512 points, the one to one mapping relationship is not maintained because a single IF channel must be processed in parallel FFT pipelines. The switching of data between the FFT pipelines arises from the fact that the ASIC memory is 512 words deep and larger FFTs must be distributed into RAM in adjacent ASIC pipelines.

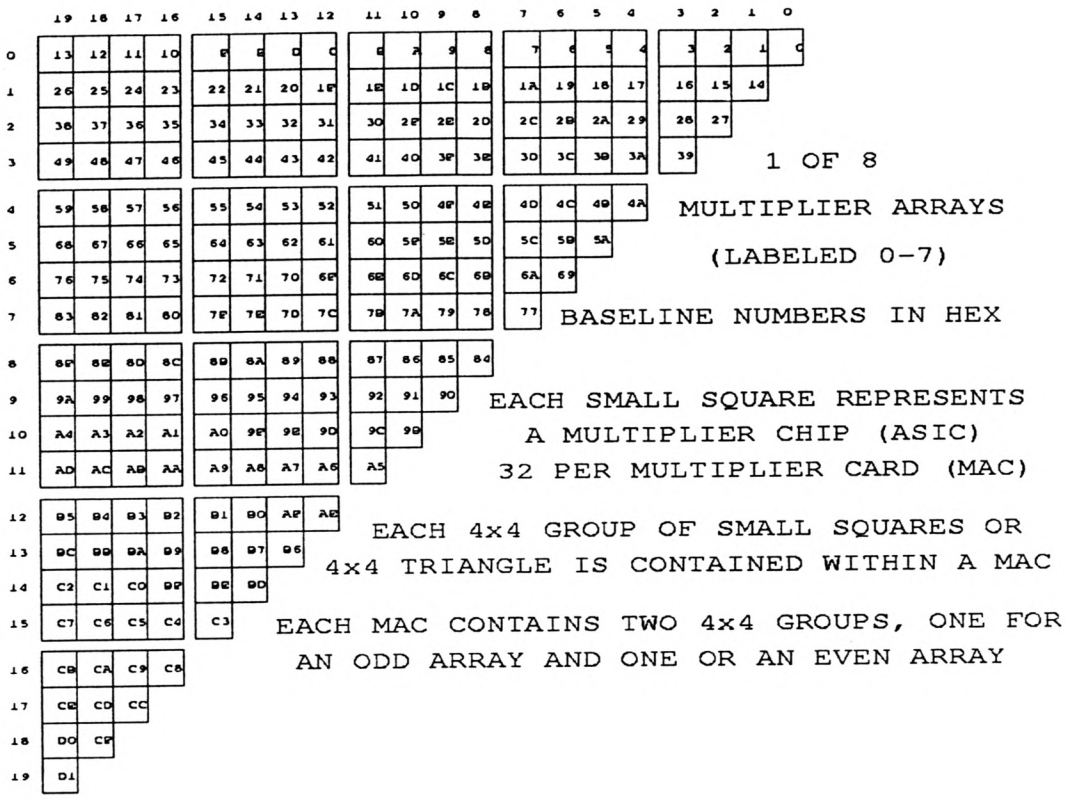


Figure 5 Triangular Multiplier Array

After the FFT is performed on the incoming data, eight IF channels per station, the FFT results remain in complex floating-point format. These results are subsequently used to drive the cross multiplier arrays (Refer again to Figure 2). The 18 bits of computational precision used to calculate the FFT starts out with 7 bit real and 7 bit imaginary mantissas expressed in sign-magnitude convention with a common 4 bit negative exponent for the real and imaginary parts (expressed in short hand notation as 7,7,4). After the calculation of the FFT is performed, this level of precision is not required. The FFT results presented to the cross multipliers are scaled back in precision to 4,4,4.

The cross multiplier system is comprised of eight triangular arrays (labeled 0-7), each configured as a 20 x 20 triangular half matrix, including the diagonal. A multiplier chip (ASIC) is located at each intersection to cover multiplications for 210 baselines. (For n = stations and b = baselines, the baseline formula is b = n(n-1)/2 = 190 baselines + 20 self products = 210.) Each multiplier card contains two 4 x 4 subsets of the larger 20 x 20 triangular arrays, with the two arrays labeled 0 and 1. The

spectral output of one FFT pipeline from each of the twenty stations will drive one row and one column of the triangular matrix.

Each station spectral point is multiplied as a complex conjugate pair with a precision of 4,4,4, by the same spectral point from every other station. The multiplications along the diagonal of the multiplier array are self products. A configuration known as MAC Polarization Mode places some requirements on the manner in which the multiplications of right(R) and left(L) polarized points are performed. In this mode, the eight triangular arrays are divided into four pairs. One member of each pair handles RR & RL and the other member handles LR & LL polarizations. Also in this mode, the rate of multiplications is double the rate of non-polarized modes.

After the multiplications are performed, the results are integrated at fixed intervals of 131.072 ms. each, with a precision of 15,15,6. These results are held in local RAM internal to the ASIC. The RAM is structured as a double buffer so that one buffer can be read while the other is being written.

The three basic timing cycles used in the correlator are the fringe/delay cycle of the PBI (4 ms.), the FFT cycle (16 us.), and the short term integration cycle (131 ms.). These cycles are illustrated in Figure 6.

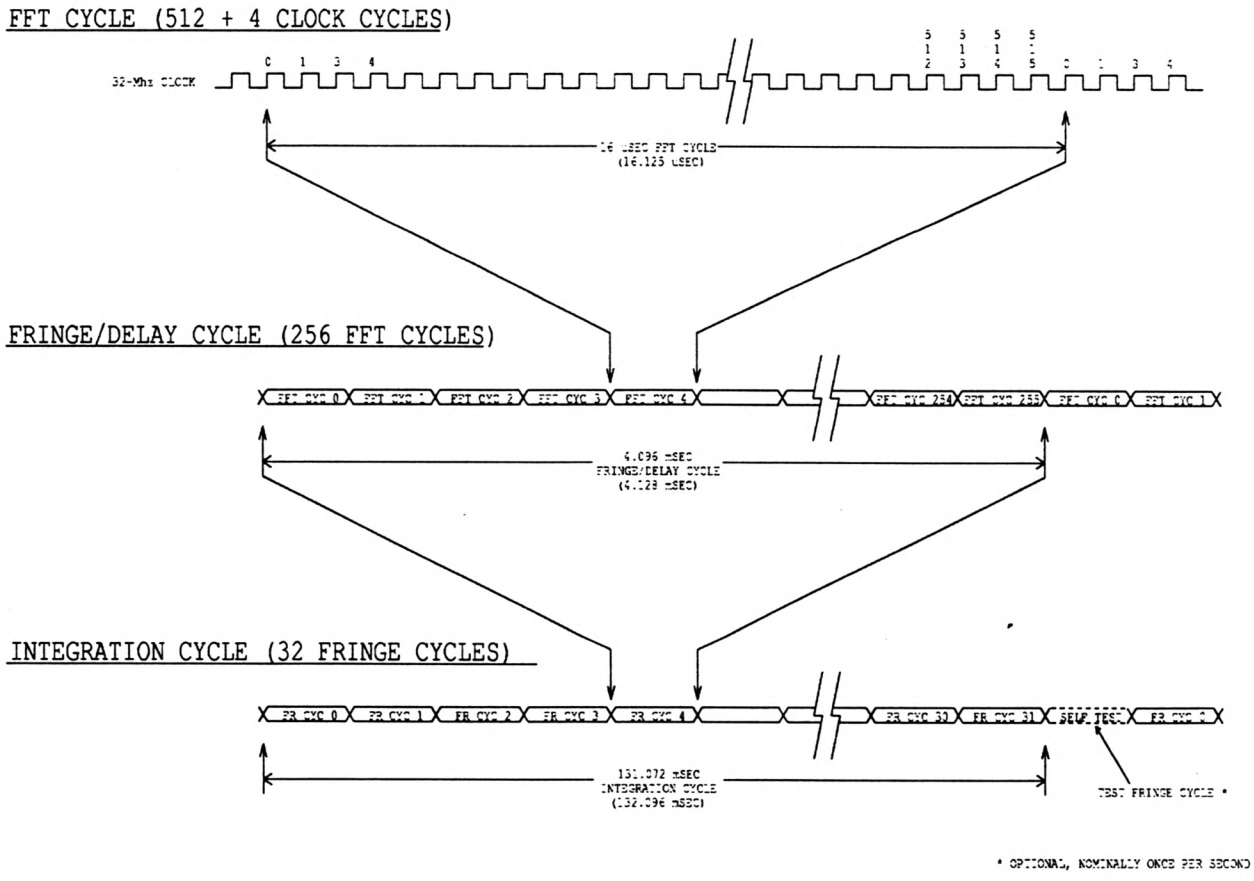


Figure 6 Master Timing

At the end of the 131 ms. cycle the short term integration RAM is read out and the intermediate results are further accumulated in the Long Term Accumulator (LTA). This module is located in the FFT bin of rack C3. The 15,15,6 results from all eight cross multiplier arrays are read into the LTA and promptly converted to IEEE 32 bit floating-point format. The conversion to IEEE format leads to a pair of 32 bit words per result, one for the imaginary part and one for the real. The integration after conversion to IEEE can now be handled by a pair of Am29C327 floating-point math chips, one to integrate the imaginary portion of the result and the other, the real part. The integration interval of this module is variable in increments of 131 ms. intervals up to 2.5 hours if desired. The LTA accumulates 2048 results from 210 baselines for a total of 430,080 complex terms in 32 bit IEEE floating-point format. The long term integrated results are held in a DRAM on the LTA and made available as requested by the Finite Impulse Response (FIR) filter.

Since the correlator produces a large amount of data at the output, it is somewhat desirable to reduce this flow. Data output is reduced either by extending the LTA time or by use of the FIR filter. Interference fringes that are produced in an interferometer from a single source are a function of $(\mathrm{Sin}x)/x$. Depending on the nature of the source, (i.e. a point source, extended source, or some combination of both), the fringes may have some drift, they may have a relatively high or low rate of turn, or there may be several interference fringes that need to be resolved simultaneously. Although the LTA offers further smoothing with longer integration over time, it is not always the ideal way to recover fringes, in some cases the integration process can even average out the fringes. In these cases, the filter may be used instead. In cases where the FIR filter is used, the LTA integration time is limited to a small number of the 131 ms. periods, either 1, 2, or 4.

The FIR Filter module is a multiple tap digital filter that can either operate in straight through mode or filter data from the LTA. The number of actual taps is fixed at 8, but a larger number of tap weights can be applied to these 8 and therefore expand the filter. Selectable tap weights are in multiples of 2 starting with 8, resulting in an 8, 16, 32, or 64 tap filter. Only eight tap weights can be applied for each 131 ms. period, so with the larger tap sizes selected, more 131 ms. tics are required to assign the weights to the filter and the data is reduced accordingly. Tap sizes of 16, 32, and 64 decimate the data by factors of 2, 4, and 8 respectively. The FIR module also serves as a buffer between the LTA and the VME system. The card in the VME system that reads the results from the FIR is a commercially available DMA controller made by Ironics.

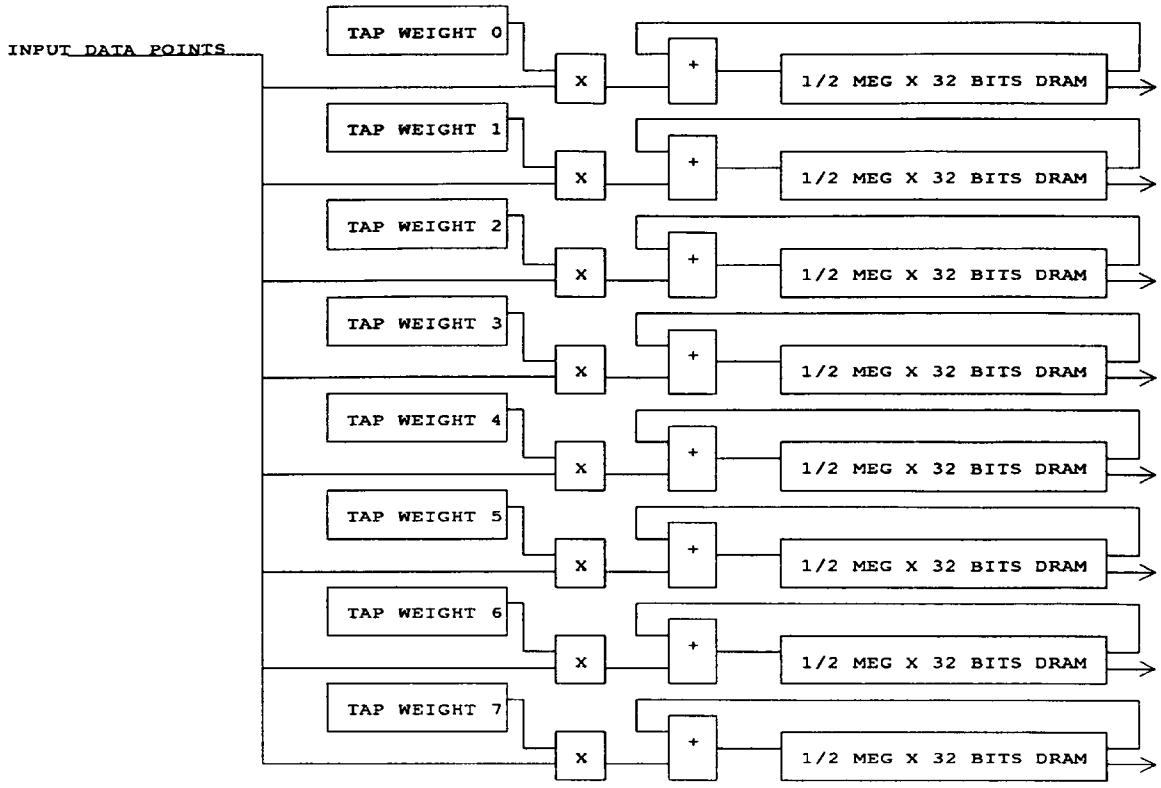


Figure 7 Fir

The real time system rack (rack RT) contains the VME computer. The first module used in this position was a Motorola MVME 147. This module has since been upgraded to an MVME 167, which runs the Wind River VxWorks OS in 68040 hardware architecture. One of the primary duties of this computer is to manage the communications traffic over the HCB. The HCB Controller Module in the VME chassis serves as the bridge between the VME data bus and the HCB interface used by the correlator modules. The three HCB control modules support two busses each, for a total of six. Four of the busses serve one each of the four C racks. Each of these busses has targets in the PBIs, MCCs, and FCCs. One of the remaining busses targets the LTA and FIR modules in rack 3 and the other is dedicated to transmitting the system tic (131 ms.) from the master MCC to the VME system. Commands can be issued from the VME to any of the individual modules that have an HCB interface. Modules with an HCB interface include the MCCs, FCCs, Deformatters, LTA, FIR, and indirectly, the TRCs. Communications over the HCB are issued in accordance with a set of protocols that define the function codes used to communicate with each module. Communications with the TRCs are indirect in that the messages are passed through a communications interface between the TRCs and the Deformatters. The protocol for the Deformatter contains a function code that identifies the TRC as the target for the message.

The 131 ms. short term integration cycle serves as a sort of epoch for hardware and software activity. In this capacity, the 131 ms. cycle is referred to as the system tic, or even more loosely referred to as the 'big tic'. As part of this master timing, the MCC in rack C3 serves the MCCs in the other three racks with the master reference for the 131 ms. cycle. The

other three MCCs receive an HCB function code upon initialization that instructs them to slave to the master timing. The VME also receives a system tic from the master MCC in rack C3 over the dedicated HCB called the system tic bus. This timing tic is the main reference that is used by the system to coordinate events between the VME system and the correlator hardware.

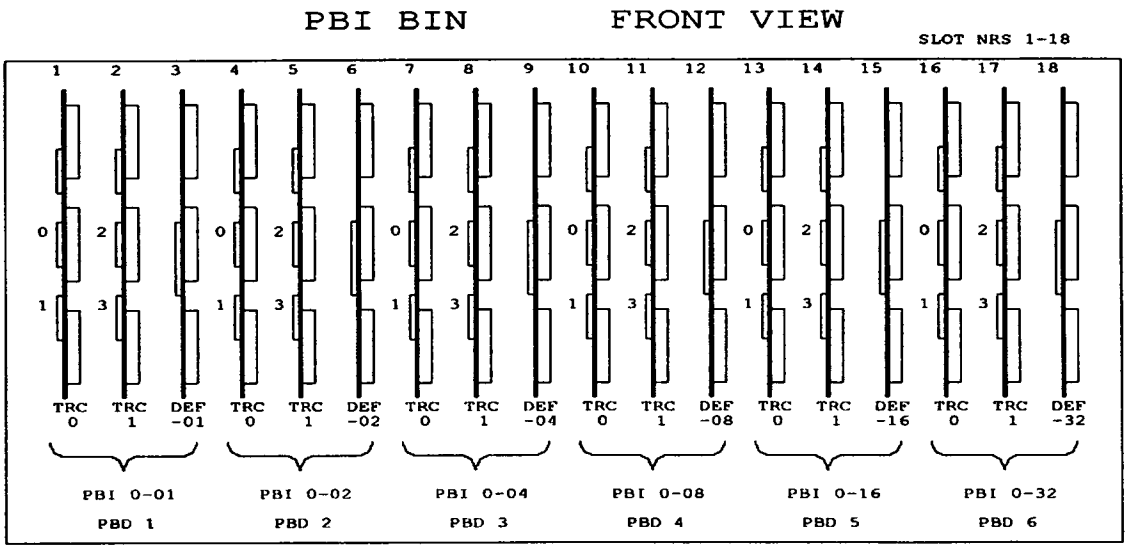
An interface to the MCB is used for direct communication to the PBDs. This is the standard communications interface used throughout the VLBA electronics (See the VLBA Technical Report #12 on the standard interface).

The Ironics interface is a DMA controller that has access to the 68040 bus in the MVME 167 module to transfer the output of the FIR module into the MVME 167 RAM space. Once in RAM, bus control is returned to the 68040 and the RAM contents are written to hard disk. The VME supports several SCSI bus interfaces that connect to hard disks and DAT drives which archive the data output from the correlator. After storage on disk, the transfer to DAT tapes is a low priority task performed by the operations staff at their convenience.

3.2 THE PLAYBACK INTERFACE

3.2.1 Track Recovery

The PBI for each drive consists of two Track Recovery Cards (TRCs), one labeled 0 and the other labeled 1, and one Deformatter card (DEF). The PBD supports 36 tracks of data, 18 tracks go to TRC0 and the other 18 go to TRC1. The card arrangement can be seen in Figure 8.



1) PBI = PLAYBACK INTERFACE; EACH PBI CONSISTS OF TWO TRC (TRACK RECOVERY CARD) AND ONE DEF (DEFORMATTER)

2) PBI NOMENCLATURES SHOWN ARE FOR RACK 0. REPLACE THE 0- BY 1-, 2- OR 3- FOR THE OTHER RACKS. (e.g. PBI 1-02) ADD (RACK# TIMES 6) TO THE PBD NUMBERS.

3) THE -01, -02 etc. NOMENCLATURE IS THE HCB TARGET MASK ID BIT (1, 2, 4, 8, 16 OR 32) USED TO ADDRESS THE DEFORMATTER IN EACH PBI.

4) TRC 0 HANDLES DELAY CENTERS 0 AND 1. TRC 1 HANDLES DELAY CENTERS 2 AND 3.

5) THE FRONT EDGE TEST CONNECTOR FOR EACH DELAY CENTER ON THE TRCs ARE INDICATED BY 0, 1, 2 AND 3 NEXT TO THE CONNECTOR.

Figure 8 PBI Bin

The footprint of a data bit on the tape is extremely small, on the order of a wavelength of light. Very small offsets in the exact position of each head will cause skews of up to several hundred bits in the playback data streams relative to one another. In addition, a small individual component of wow and flutter may exist in each track. For these reasons, each active track signal has an individual clock derived from the transitions in the data stream. This clock is derived just prior to the transmission of the data from the playback drive to the correlator. Both the data and clock signals are transmitted to the correlator at differential ECL logic levels. The playback data rate is always approximately 9 MHz, which results in a data rate of approximately 8 MHz after the framing overhead is removed. (The data rate would be exactly 8 MHz except there exists a 512/516 FFT cycle factor and a contribution of the station Doppler component).

Currently, there are three recording formats supported in the correlator. The VLBA format, which has record time frame rates of 2.5, 5.0, and 10 ms., the Mark III modes A, B & C (with some restrictions on modes A & C), also with frame rates of 2.5, 5.0, and 10 ms., and subsets of Mark IV having frame rates down to 2.5 ms. The frame data rate that is played back into the PBI is always at the rate of 2.5 ms. per frame, regardless of the original recorded rate. The VLBA format is detailed in VLBA Specification A56000N003 (this may be easier to locate in Appendix V of VLBA Technical Report No. 43, that describes the PBI) the Mark III format is referenced in VLBA Acquisition Memo #91 (NEROC Haystack Observatory Drawing #6056), and

the Mark IV format is described in memo #205.6 of the Mark IV memo series (NEROC Haystack Observatory).

The track inputs to a single TRC are divided into two groups of nine. Each track is processed by the Data Playback Chip (DPC), an XC-3030 Xilinx FPGA. This chip, paired with a 64K x 4 track buffer RAM, are all that is required to perform the track recovery function on one track. Each group of nine DPCs is under the supervision of an 87C51 microprocessor. Each microprocessor sets the delay for one phase center, which satisfies the correlator specifications of four delay phase centers per station. By providing multiple delay centers for each station, several areas within an extended source can be correlated. Without this feature, a source must be treated as a point.

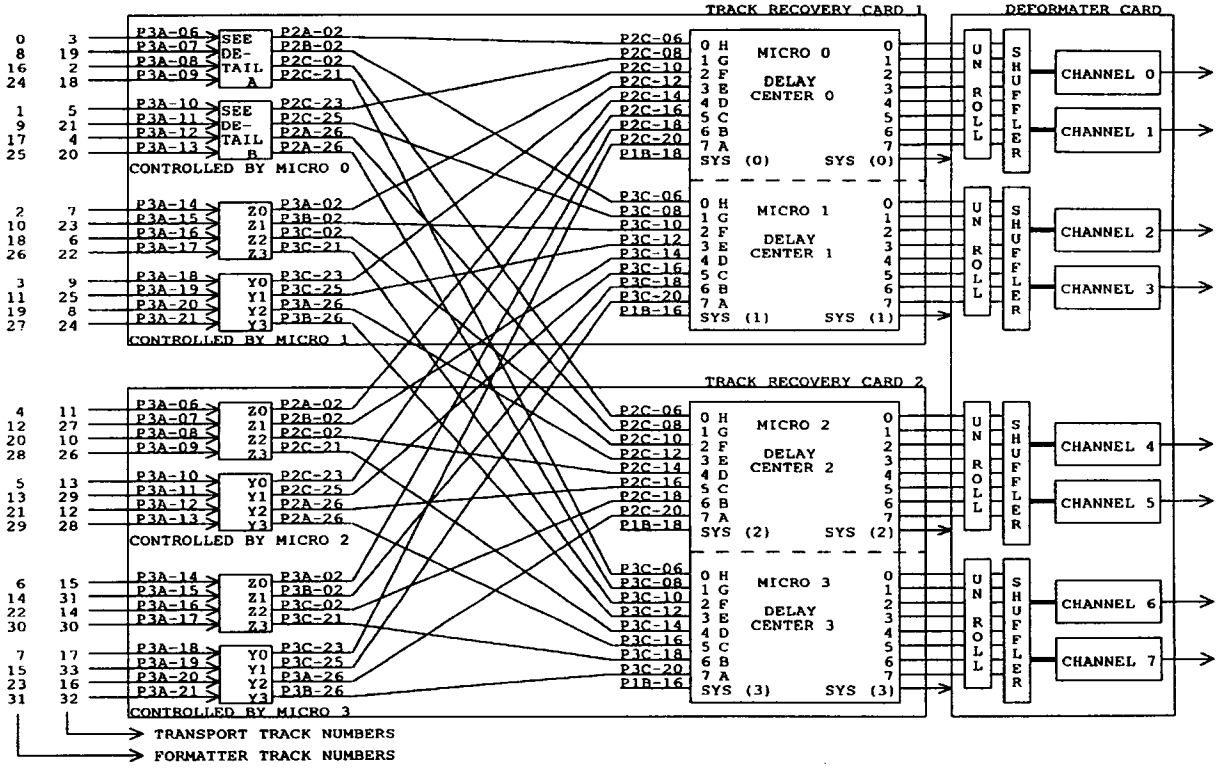


Figure 9 TRC Data Path

The track mix stage of the TRC can be seen in Figure 9 above. The input multiplexers are under control of the microprocessors, which receive instructions via the HCB. As an example, wide band observations may require a sampling rate of 32 Msamp/sec. The maximum track data recording rate is 8 Msamp/sec. If two bit sampling were implemented in this observation, the data would be multiplexed across eight tracks. During track recovery, these eight tracks must be brought together through the track mix stage into a single delay center. Although not currently in use, there are cases where fewer than four or eight channels could be processed, allowing the exact same tracks to be routed through the track mix stage to more than one TRC delay center. In these cases, the information contained in one channel would be processed by more than one FFT engine (using overlap) and a slight increase in channel sensitivity would be realized.

Once the track mix is established, the raw track data and its associated clock are input to the DPC. Some of the information recovered by the DPC chipset is illustrated in Figure 10 below. This discussion will use examples based on the VLBA format and will not always be true for Mark III or Mark IV.

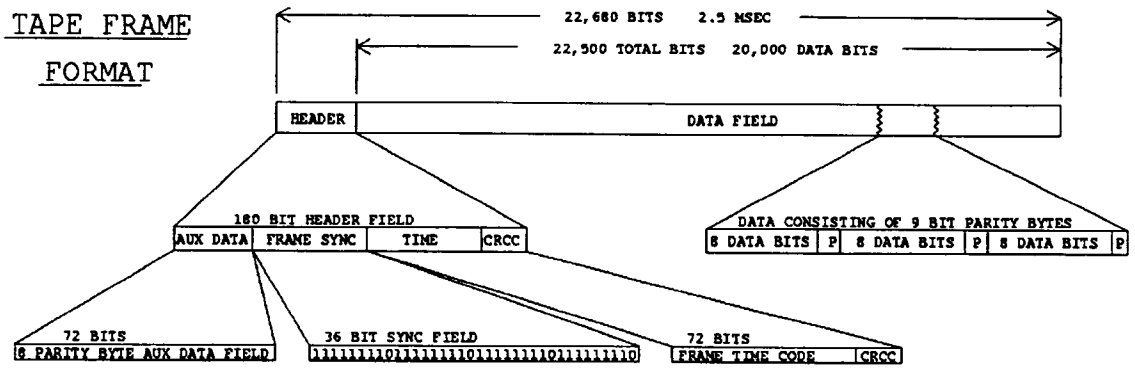


Figure 10 VLBA Tape Frame Format

The serial data stream is input to the DPC and continuously monitored by the internal sync detector for the presence of the sync word. There are two modes of detection, wide band and narrow band. In wide band mode, the detector is enabled during the entire frame. This leads to a potential problem of spurious sync detection from similar patterns that may be present in the data stream. Narrow band mode restricts the search for the sync word to a 180 bit window where the header is expected to be found. Normally, the TRC is in narrow band mode. Wide band mode is used only if necessary to establish sync. Sync detection is the corrective mechanism used to recover from slips in the clock and the potential loss of data frames. When the sync word is detected, several counters are initialized including a frame counter and two RAM address counters. The position of the next sync word can be precisely determined from the state of these counters. The DPCs for a group of eight tracks in a delay center all output a sync detect pulse onto a common bus to interrupt the microprocessor. As long as sync is detected by a single DPC, the sync interrupt line to the microprocessor will be driven. If the sync word is detected at an unexpected position or if sync detection is missed, there exists a strong possibility that some data frames may be flagged as invalid. A watchdog circuit is available to monitor sync detection and provide a microprocessor interrupt in the event sync is missed. A missing sync from one or several DPCs would not be noticed at this point, as it only takes one to successfully drive the interrupt line. Sync detection on a per track basis is done after the headers are read out of the RAM buffer associated with the DPC.

Inside the DPC, the parity on the data fields is calculated immediately and internal error counters are updated as required. Parity is odd throughout the frame with the exception of the sync field, which uses even parity. The parity bits in the data field are stripped out, and the rest of the data stream is converted to parallel and written to RAM. The

parity bits for the header fields are stored in the RAM buffer with the headers and are evaluated later. This buffer is central to many of the responsibilities of the TRC. The buffer primarily serves as a large sample reservoir to allow a relaxed servo positioning of the PBD by the Deformatter. Some of the buffer capacity is also used to absorb the wow and flutter of the track signal, eliminate the head skew, and for application of the delay model as directed by the Deformatter.

Separate pointers are maintained for the locations of the header bytes and the data bytes stored in the buffer RAM. When the RAM is read out, the pointer to the header identifies the exact locations and allows the header to be completely removed from the data. The data stream at this point may still exhibit some level of channel multiplexing and barrel rolling, which will be untangled in the Deformatter.

The 87C51 maintains a clock which is called "filtered time". The reference used to set the filtered time clock is taken from the time field in a known good header. A specified number of consecutive headers, typically 12 to 16, must be error free before filtered time is set and declared good. The filtered time is then checked against the track time in every header. Once filtered time is set, it can help to salvage a frame of data if the time becomes corrupted and then recovers in subsequent frames.

A CRCC result of 16 bits is calculated on the time code and checked against the result sent by the formatter. Longitudinal parity is calculated and checked against the parity sent with each byte in the frame. Data fields, as well as header fields, are accompanied by a parity bit. Some level of time stamp disturbances, sync errors, and parity errors can be tolerated. If errors become excessive, however, data will be lost. The evaluation and tabulation of various detected errors is collectively referred to as data statistics.

Ultimately, the PBIs must deliver station samples to the FFTs that are precisely timed with respect to the station delay model. The samples must be coincident with the specific clock transition that will be used to correlate samples from the other stations that reflect the same time epoch.

In order to achieve this goal, the PBD must be precisely controlled. The large sample reservoir in the TRC allows the job of servo control by the Deformatter to be smoothly executed. As the time codes in the data frames are extracted and evaluated, the TRC microprocessor uses the model delay provided by the Deformatter to establish the proper read address for retrieval of the data samples from the buffer. By continually monitoring the current RAM read and RAM write addresses, the TRC microprocessor can determine how full the buffer is. Ideally, the buffer is maintained at about half full. The half-full condition provides the optimum control point in the buffer to either speed up or slow down the drive, thus keeping the data flow through the buffer comfortably away from the boundaries.

In addition to the track recovery chipset, there are two additional Xilinx FPGAs on each TRC that provide control functions, One is the header control chip and the other is the delay control chip. Each of the two microprocessors on the TRC works together with a pair of these control chips.

3.2.2 Deformatting

Each Deformatter card receives thirty-six tracks of data, with headers removed, from the pair of TRCs local to the particular PBI. Four of these thirty-six tracks are considered system tracks and could serve one of two purposes. The first would be in the event of a recording system failure in a data path, either due to a defective head or other reason, any one of the thirty-two data tracks can be reassigned to one of the four system tracks to prevent data loss. During playback at the correlator, the system track data can then be substituted back into the appropriate Deformatter channel for processing. If a substitution was made during recording, the correlator control computer must be given the track assignment information to pass along to the PBI. The second use intended for the system tracks is to carry cross track parity. The logic to implement the cross track parity is in place, but is not currently made use of in either the Mark III/IV or VLBA formats.

System track assignments, mentioned above, are only useful to prevent data loss in the event that a defective path is known to exist. A feature known as "barrel rolling" can be employed to guard against excessive loss of data in the event a path becomes defective and is not noticed. This recording technique does not prevent data loss but can reduce the effect by spreading the impact of a bad path over all of the channels instead of causing a single channel to be 100% bad. The barrel rolling logic is in the formatter and can be thought of as a large rotary switch with thirty-two inputs and thirty-two outputs. The bit streams from the samplers are on the input side of the switch and the output side is directed to the thirty-two tape tracks (the four system tracks are not included in this rolling scheme). Most of the frame header is not affected by the barrel rolling action, except for a few fields, which roll with the frame and identify the source of the data (from which BBC/Sampler) for the particular frame being rolled. At the end of every 2.5 ms. frame, the switch rotates one position and shifts all of the track assignments by one position. If we were to look at one bit stream, the first frame would be on the first track, the second frame on the second track, etc. For a complete roll cycle in this case, the switch would take thirty-two frames to return to its original position. Actually the roll group does not include all thirty-two tracks, but occurs as two groups of sixteen tracks or four groups of eight. The switch also actually has an apparent backward motion from the case described above. The first frame in a roll group of 16 tracks appears on track 16; the second frame appears on track 15; the third frame on track 14; etc. The effects of the barrel rolling are removed by PALs in the Deformatter.

Depending on what parameters were used during recording with respect to bandwidth and sample rate, the recorded bit streams may have been multiplexed or demultiplexed onto the recorder tracks. Any mux/demux operation that was initially employed during recording must be removed. The restoration of the channel data from the tape tracks is done by a Xilinx FPGA, which is called the bit shuffler. This single stage of logic is reprogrammed as necessary to accommodate all of the mux/demux modes that are supported. If tracks were multiplexed for recording, the track decoding is done in the delay/demux PALs in conjunction with the bit shufflers.

The stages discussed in this section are shown in Figure 11 Deformatter Data Path.

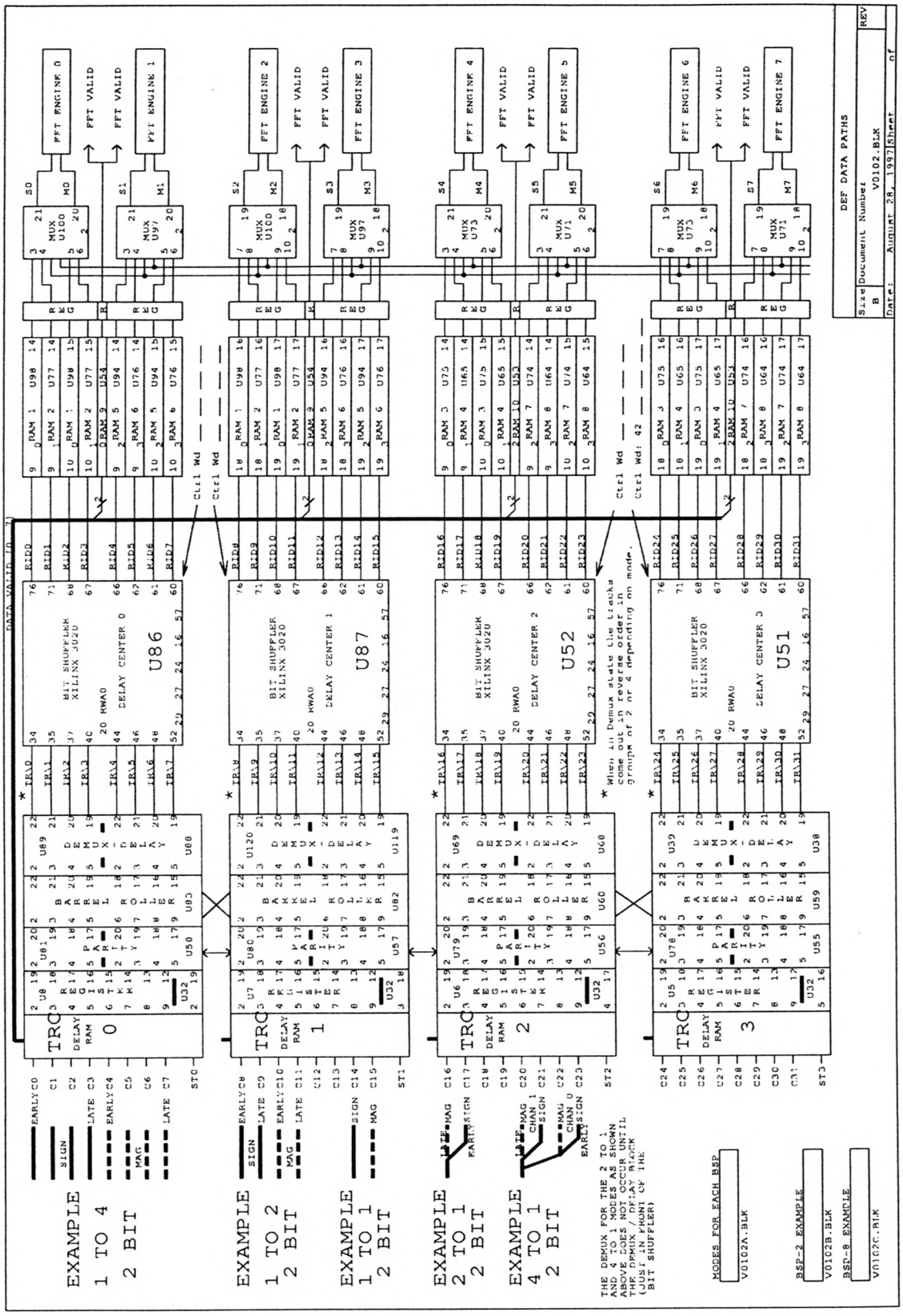


Figure 11 Deformatter Data Path

Through no small miracle then, the data is back to the original state as it appeared from the BBCs after sampling. An additional chore which is performed in the bit shufflers is to sort the samples from the IF channels and route them to the appropriate FFT pipeline based on the selected FFT size. The final stage of the Deformatter card is a combination of RAM and muxes. Since the data at the output of the Xilinx ICs is 16 MHz, a pair of RAMs and a mux are used as a final stage to reconstruct the data into 32 MHz streams prior to routing into the FFT pipelines.

3.3 THE FFT SYSTEM

A view of the FFT bin can be seen in Figure 12 FFT Bin. The FFT bin in each rack contains one FFT Control Card (FCC) and 10 FFT cards. The C3 rack FFT bin also contains the LTA and FIR cards.

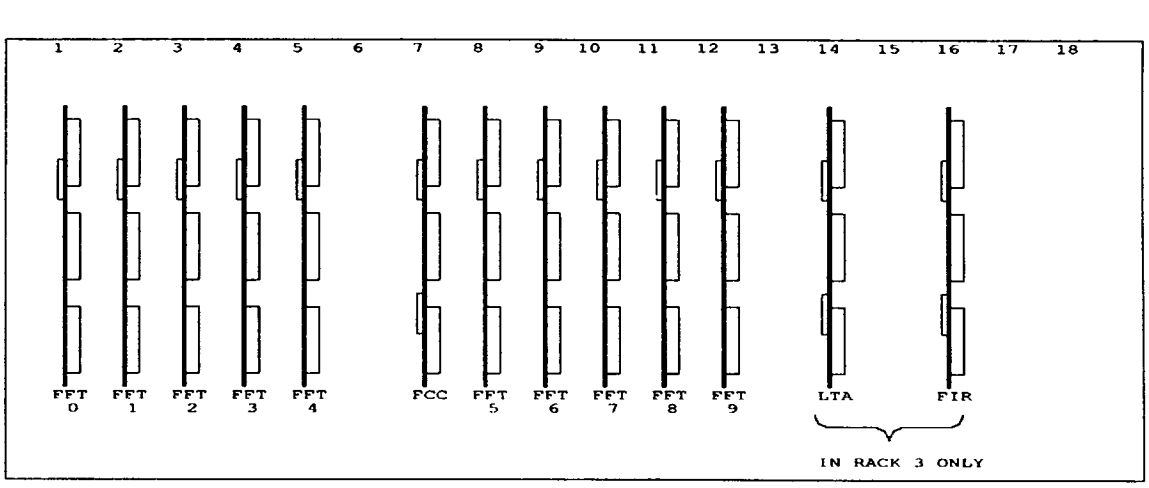


Figure 12 FFT Bin

3.3.1 The FFT Control Card

The FFT Control Card provides timing and control for the ten FFT cards in the bin, relays trig tables to the FFT cards, implements pulsar gating, model generation, and HCB communications. An 87C51 microcontroller is central to the FCC architecture, and is accompanied by a floating-point math chip and Xilinx FPGA, which are instrumental in the model generation.

3.3.2 The FFT Card

Each FFT card provides 4 FFT pipelines for a total of 40 on the ten cards within the bin. The FFT computation most closely resembles a Cooley-Tukey, Decimation in Time (DIT) algorithm, computed in place, using the scrambled input and natural order output data architecture. The following discussion and associated diagrams are a very limited explanation of this technique. A 512 point FFT is used as an example, but to gain an understanding of other FFT sizes, the FFT system manual (VLBA Report #44), butterfly listings, ASIC address tables, and a good Digital Signal Processing textbook should be consulted.

In Figure 13 ASIC Butterfly Stages, the bits from the deformatter are labeled T_0 to T_{511}, and come into the FFT card in serial streams. These time ordered sample bits from the deformatter are used as a portion of the address for the Fringe Rotator ROM. The remainder of the address comes from the NCO which is driven by the fringe model. The ROM contains, in a lookup table, all possible values that the one or two bit samples could take on, coupled with all possible rotations applied. This composite address of the data sample and NCO bits select the appropriate value in ROM that represents a fringe rotated sample which is then output from the ROM as a 7,7,2 number. The ASIC requires a 7,7,4 number input, so two of the exponent bits are grounded at the input to the Stage 0 ASIC. This is not detailed on the diagram but is pointed out to avoid any confusion in the numerical precision change from 7,7,2 to 7,7,4.

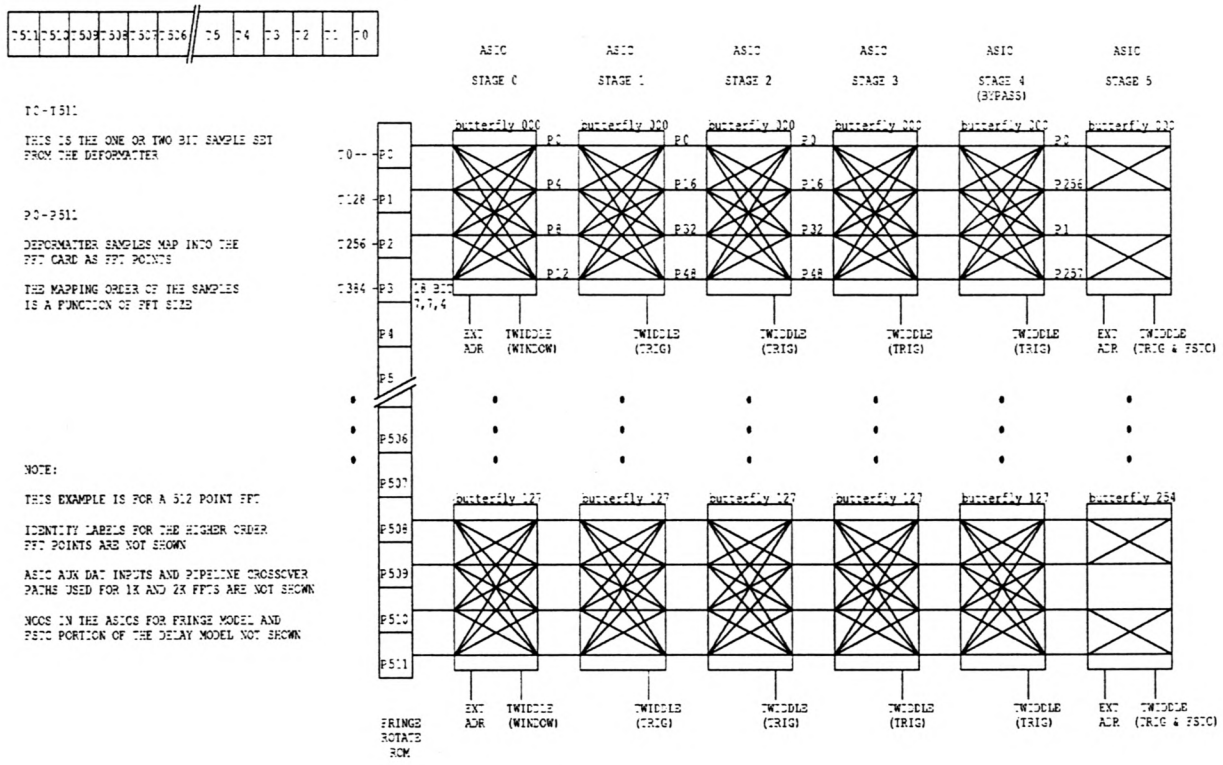


Figure 13 ASIC Butterfly Stages

At this point a few terms should be defined. The ASIC performs the FFT algorithm in butterfly operations. In Figure 13 above, these stages are

shown as crisscrossed paths through the ASIC with 4 outputs developed from 4 inputs. This particular size is called a radix 4 butterfly. The only other size butterfly used in the ASIC is a radix 2, and the radix 2 is the one used in the stage 5 ASIC, (if the selected FFT size requires it). The mathematical operation performed through the radix 4 and radix 2 stages is described in Figure 14 Butterfly Operations. The ASIC stages cascade in a multiplicative fashion to develop further resolution in the final FFT from left to right. One radix 4 develops a 4 point FFT (in subsets of the final 512 FFT product), stage 1 develops 4x4 for 16 points, stage 2 develops 4x4x4, etc. Depending on the FFT size required, some of the stages may be in a bypass mode where they simply copy equivalent results from input to output so as not to affect the results. The stage 5 radix 2 is used as required for the selected FFT size and the FSTC portion of the delay model is applied in the Radix 2 of stage 5. For example, the 512 point FFT uses 4x4x4x4x2.

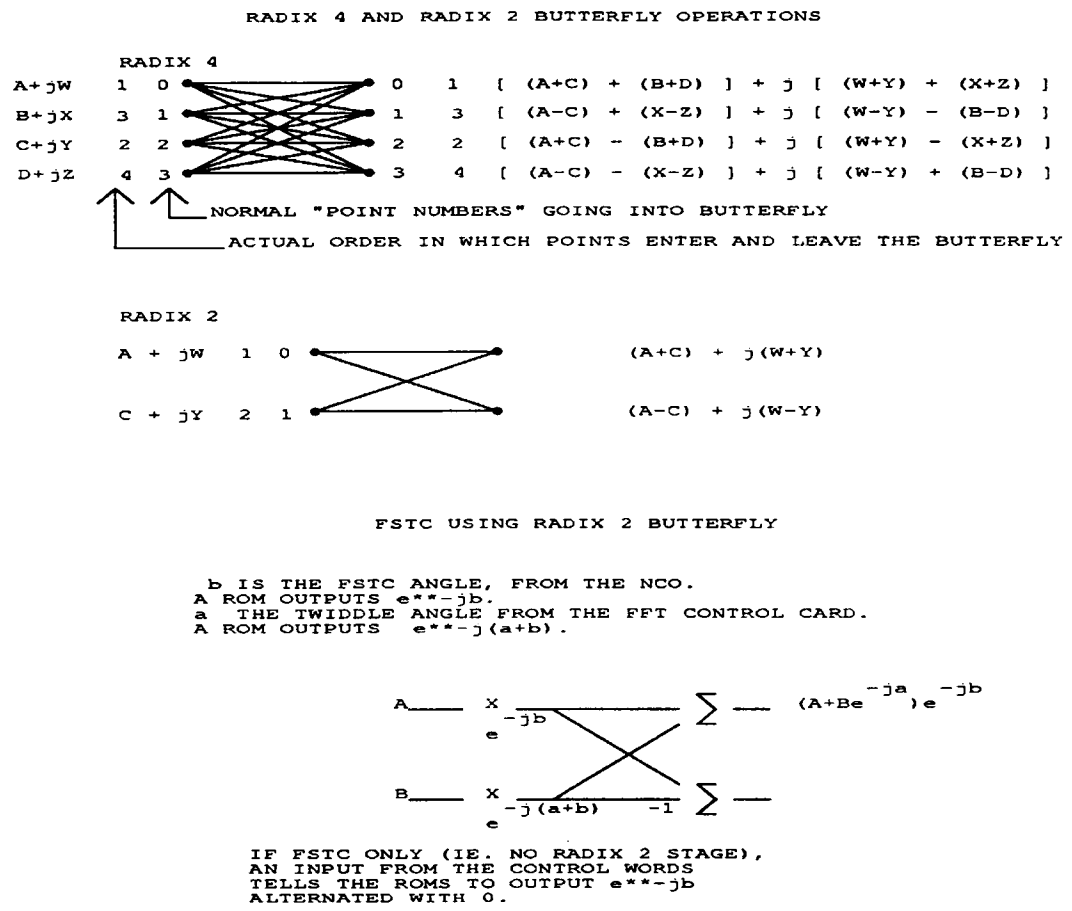


Figure 14 Butterfly Operations

The FFT requires a specific ordering of samples at the stage 0 input to accomplish the FFT and the ordering is a function of the FFT size. This is sometimes referred to as scrambling or shuffling the bits. The 7,7,2 number from the Fringe Rotator ROM is written into the ASIC as 7,7,4. The RAM in the ASIC has the ability to be addressed from either an external source or an internal generator. In order to scramble the data at the input to Stage 0, the external address is used to direct the butterfly input to

the appropriate sample in the ASIC RAM. Subsequent ASIC stages are addressed from the internal address generator, to satisfy the requirements of the FFT algorithm, and the final result from stage 5 is taken out with the external address to properly order the FFT point results.

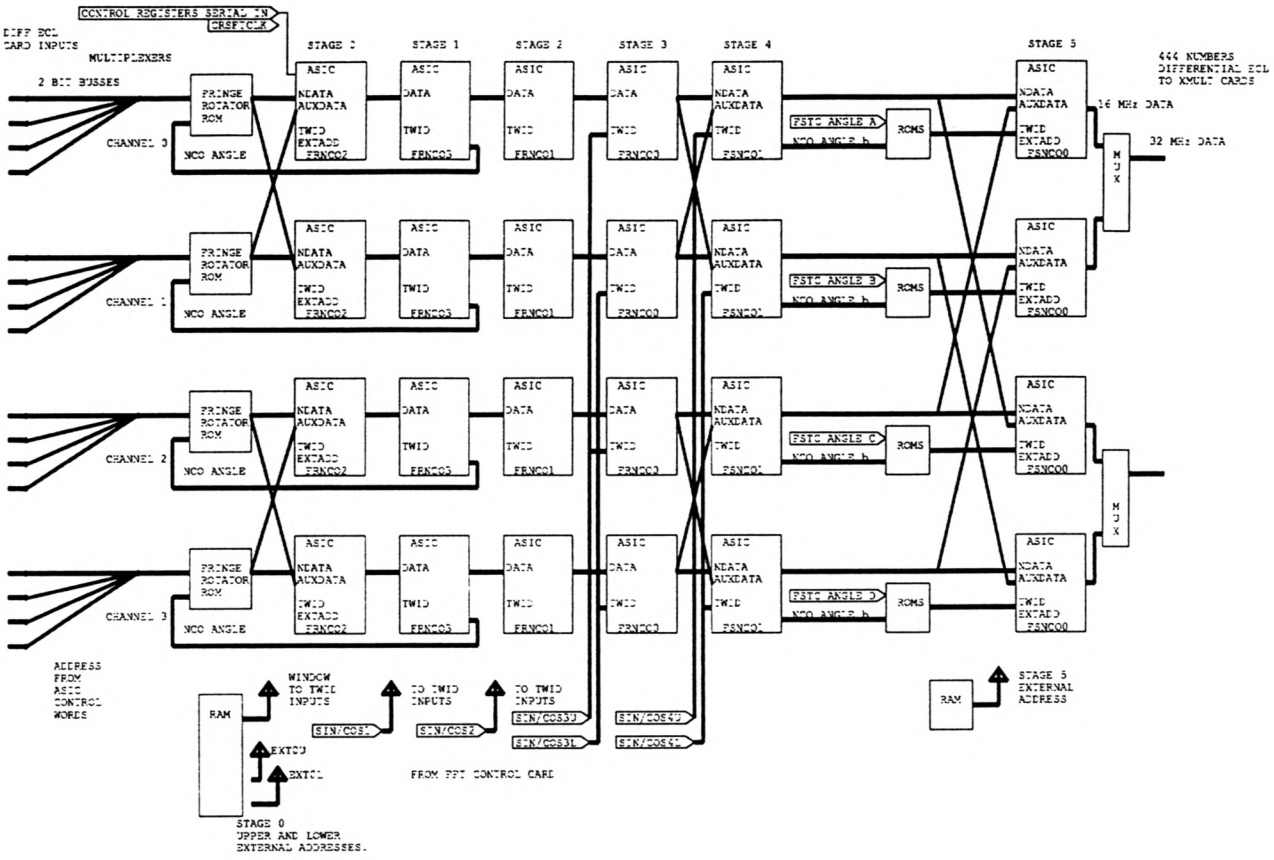


Figure 15 FFT Card Simplified Block Diagram

Calculation of the FFT requires a trigonometric term in each of the ASIC stages (except stage 0). The trigonometric terms are called twiddle factors. These terms are downloaded from the VME RTS and sent to the FCC cards via the HCB and loaded into the trig tables in RAM. From the trig tables, values are retrieved and sent from the FCC to the FFT ASICs on dedicated parallel lines under control of the FFT cycle sequencer on the FCC. The RAM configuration used for the FFT mode in the ASIC is set up as two banks, with each bank 18 bits wide x 512 deep, which is why the 512 point is the natural size performed and why it was picked for the example here. (This is in contrast to the RAM configuration of the ASIC in MAC mode which is 36 bits wide x 256 deep by two banks). Smaller FFTs put more of the stages in bypass mode and larger sizes require that the multiple FFT pipelines are ganged together to make a larger effective RAM to take in and process a sample set larger than 512 points. With a 512 point FFT, each of the 4 pipelines can handle a deformatter channel. With a 1K FFT, two pipelines are combined to process one deformatter channel so the FFT card can handle two deformatter channels for a 1K FFT. For a 2K FFT, it takes all

4 pipelines to process a single deformatter channel. These configurations for 1K and 2K are more complex than 512 points and details are left for the FFT Manual (VLBA Report #44). The block diagram of Figure 15 shows the paths crossing between pipelines into the aux data inputs that are used for 1K and 2K FFTs. The number of samples clocked into the ASIC RAM is equal to the FFT size. The earliest sample at t_0 occupies the top position in the RAM and the last sample occupies the last position filled in RAM depending on FFT size. The remaining bits must be reordered for presentation to the first FFT stage but are not shown for all 512 samples. Since stage 0 does not require a trigonometric twiddle factor, the twiddle input is used to apply a window function which is a sort of template imposed on the data for smoothing.

Each ASIC has a 10 bit NCO which is used to apply the models. NCOs in ASIC stages 0-3 are combined into a 40 bit NCO which is used in the fringe rotation (FRNCO1-3). Stages 4 and 5 are combined into a 20 bit NCO (FSNO0-1) for use in Fractional Sample Time Corrections (FSTC). The FSTC is combined with the stage 5 trig value and applied in stage 5.

3.4 THE MULTIPLIER , LONG TERM ACCUMULATOR, AND FIR FILTER

3.4.1 The Multiplier System

The front of the MAC Bin is shown in Figure 16 below.

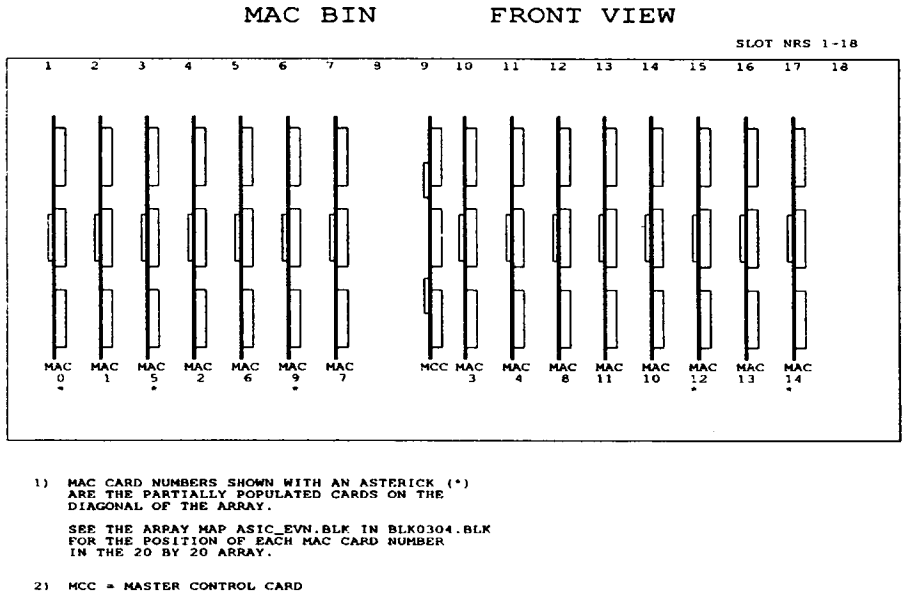


Figure 16 MAC Bin

Up to this point, data through the correlator is still station based. Data from the FFTs that drive the multiplier array form baselines. As mentioned previously, there are eight triangular multiplier arrays, each of which form 190 baselines and 20 self-products along the diagonal. Spectral points coming into the rows and columns of the multiplier array are in 4,4,4 format.

3.4.2 The Long Term Accumulator (LTA)

The LTA integrates results in DRAM. The assignment of 'stations' within the correlator FFT system is a function of where the station tapes are loaded and how many subarrays (up to 8) have been established in the correlator. Station assignments and the number of spectral points being processed also affects how the LTA RAM will be loaded. Since these parameters are subject to change, a translation table which identifies the location of the data in LTA RAM is generated and maintained in the VME system. Results are stored in the LTA with respect to subarray, baseline, and spectral result. The address portion of the LTA/FIR interface contains 20 bits, with 8 bits used to identify the baseline (0-255), 11 bits used to identify the spectral result, and one bit to select one of two banks. Since there are only 210 baselines, some remaining RAM locations are used to hold validity information and some are not currently used. In the earlier discussion of the FFT system, it was pointed out that a 512 point FFT is the largest size that can be processed through all 4 channels of the FFT card without sharing of adjacent FFT pipelines. For 1K FFTs, two pipelines are used and the card can process one channel and for 2K FFTs all four pipelines are used to process a single channel per FFT card. The DRAM on the LTA can store the results of 2K FFTs from 2 channels, 1K FFTs from 4 channels, or 512K FTS from all 8 channels. FFT sizes smaller than 512 do not fully utilize the DRAM capacity. Some combination of these storage schemes may be found if subarrays are assigned with different FFT sizes. Data is taken out of the DRAM and sent to the FIR filter card based on processing needs in the VME system.

3.4.3 The Finite Impulse Response (FIR) Filter and Ironics Interface

Requests for data come from the MVME167 which provides the Ironics interface with address information based on the translation table originally used to store it in the LTA. The requests are made for a particular spectral point of the baseline to be processed. The FIR receives the request from the Ironics card and retrieves results from the LTA with reference to the baseline and number of spectral points. In straight through mode, the data follows the same path as if the filter were active, but filter parameters are set such that the data is unaffected.

3.5 SYSTEM TIMING AND CONTROL

The correlator is driven by a 32 MHz sine wave oscillator master clock, which is in rack C3. Distribution of the clock to the bins in the racks is over RG-188 coax. Figure 17 Clock Distribution, illustrates the connections.

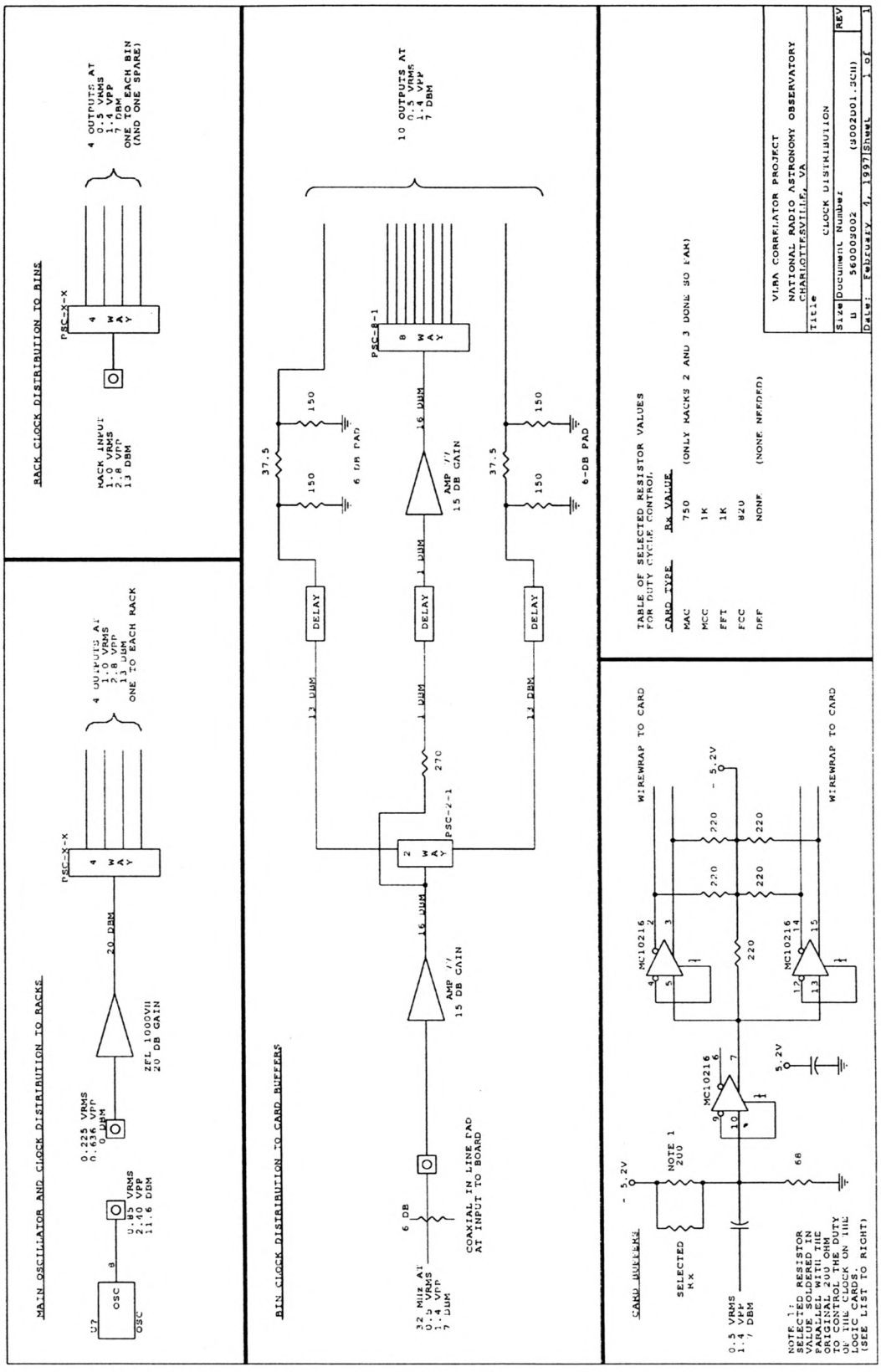


Figure 17 Clock Distribution

The oscillator output is amplified and routed to a four-way splitter. Each output of the splitter serves one of the four C racks. The clock is again subjected to a four-way splitter once it enters a C rack. Three of the splitter outputs are used, one for each of the bins in the rack. The fourth splitter output is simply terminated, except this output in the C3 rack is routed into the lab to provide a clock for the test rack. The three splitter outputs are routed to each of the three bins in the C rack. At this point, the clock enters a two-stage amplifier at each bin. After the first amplifier stage, the clock is again divided and each of these three paths is subjected to a delay stage. This delay element can be selected from a range of fixed values to adjust the clock timing for best data capture at points throughout the racks. Further programmable delays are also obtained on the MCC. Two of these delayed clocks exit the Clock Amp board as "right clock" and "left clock". The third path goes into the second amplifier stage to drive an eight-way splitter. These eight clocks exit the board as "common clocks". The right, left, and common clocks are routed across the backplane via wire wrapped coax. Any unused clocks are locally terminated on the Clock Amp board. Each of these coax lines is sent to an ECL line receiver on a small PCB that serves two card slots. The clock for each slot is transmitted over a relatively short twisted pair line to the backplane.

There are three major timing cycles used to manage the flow of data through the correlator. These are the FFT cycle, the fringe/delay cycle, and the integration cycle. The general relationship between these cycles was introduced earlier in Figure 6 Master Timing. Most of these cycles and their associated control lines are generated in programmable data sequencer stages, which offer a great deal of design flexibility. Examples of these can be found on the MCC, FCC, LTA, and Deformatter modules. These sequencers are built from either RAM or PROM ICs and are usually driven by cyclical counters. Each bit position of the data output at the memory chip is the source of a clock or other periodic data pattern. The depth of the sequencer memory is determined by the longest required bit repetition period.

The FFT cycle is the shortest in the system, repeating at 16 us. intervals. This cycle is of fixed length independent of the number of FFT points processed, 64 to 2048. The cycle time of 16 us. is required to process 512 FFT points with a 32 MHz clock. Processing of FFT sizes greater than 512 is distributed across parallel pipelines in order to fit into the 16 us. cycle.

The fringe/delay cycle in the PBI and FFT runs at a 4 ms. rate. Data comes off the tape packaged in frames conforming to one of the supported formats as mentioned earlier, either Mark III/IV or VLBA and could have a frame rate of 2.5, 5.0, or 10 ms. Regardless of the recorded frame rate, playback will always be at a 2.5 ms. rate to satisfy the timing needs of the correlator. After the frame headers are stripped out, the resulting raw data streams are subsequently handled in the 4 ms. cycle. During the 4 ms. cycle, the Deformatter calculates delay values on a linear slope and receives new model parameters at the 4 ms. cycle boundaries.

The integration cycle is the longest, with a 131 ms. repetition rate. This is also loosely referred to as the "Big Tic", and is primarily the rate at which data is taken out of the multipliers. The boundaries of this cycle are an important reference throughout the system.

3.5.1 The 131 ms. Integration Cycle

The ASICs in the MAC card provide an area in RAM for the short term accumulation of the multiplication results. This storage area must be periodically read out to make room for new results to accumulate. This readout occurs at a repetition rate of 131 ms. and is defined as the integration cycle. Since this is the longest cycle in the correlator, the FFT cycles (at a repetition rate of 16 us.) and Deformatter cycles (recurring at a 4 ms. rate) must ultimately be synchronized to this slower integration tic.

The source of this master timing is the MCC in rack 3. When the system is initialized, the MCC in rack 3 receives an HCB command that designates it to be 'master'. The MCCs in the other three racks are then slaved to the control of the master. Distribution of the integration cycle tics throughout the system and the timing relationships are illustrated in Figure 18 131 ms. Cycle Timing.

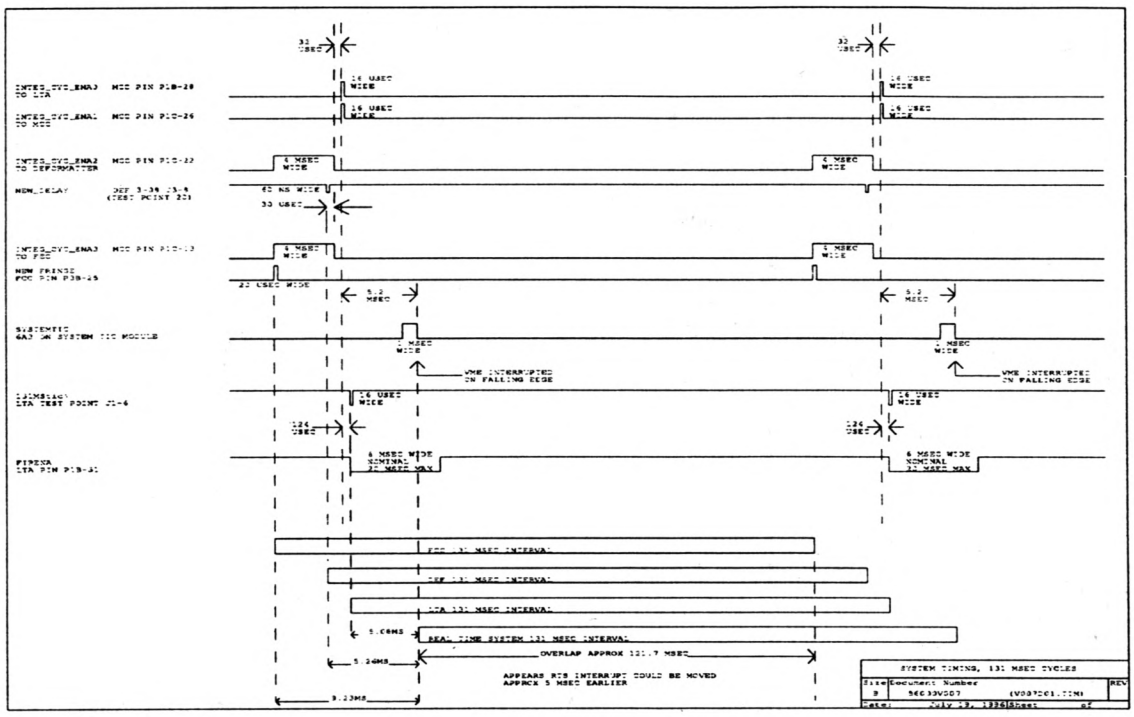


Figure 18 131 ms. Cycle Timing

Each of the MCCs is responsible for providing the tic to the FCC and six Deformatters associated with its rack. The master MCC in rack 3 must also supply a tic for the LTA and the VME system. The sequencers in the master MCC are free running, driven only from the 32 MHz system clock. The sequencers on the slave MCCs in the other three racks are under control of the master through the INTEG_CYC_ENA input to the board. Since the FIR receives input from the LTA, the LTA is responsible for generating an interrupt to initiate data transfers from the LTA to the FIR.

3.5.2 Frame Rate and the Deformatter Timing Cycle

The 87C51 microprocessors on the TRCs, which supervise the recovery of data from the PBDs, operate from a 16 MHz clock. Data boundaries that are of a primary concern to the TRCs occur with the detection of sync in the track frames. The frame headers and data are written into a track buffer RAM, on the TRCs, where the samples are kept track of with respect to sync detection and frame time. Data samples are extracted from this RAM by use of a pointer that skips over the headers. The integer portion of the delay model is applied in the timing of this track buffer RAM read operation and the data next goes into a circular buffer on the deformatter card. The headers remaining in the track buffer are written into 87C51 memory.

The delay interrupt operates on a 4 ms. cycle and has control of the data flow from the track buffer RAM into the deformatter circular buffer. Every 4 ms. the delay model polynomial is evaluated and a linear correction is applied throughout the 4 ms. interval. The data in the circular buffers needs to have barrel rolling removed and any multiplexing mode from Table 3 that was imposed must now be demultiplexed. In addition to these features, the FFT size that will be used will determine how the bits need to be ordered by the bit shufflers to go into the FFT pipelines.

3.5.3 The FFT Cycle

Data samples are clocked into the RAM buffers of the ASICS at the system clock rate of 32 MHz. These buffers are configured as a doubly buffered array of two banks of RAM, 512 x 18 each. The FFT cycle consists of 516 periods of the 32 MHz clock and is the shortest cycle in the system. 512 of these clock periods are used to load samples into one of the ASIC RAM buffers and the remaining 4 periods are used to switch to the other bank. One bank can be written as the other is being read. The buffering capacity in the delay system RAMS provides for delivery of the samples to the FFT engines so that no data is lost during the bank switching interval.

The fractional part of the delay model is applied on the FFT card during the FFT cycle. NCOs in the ASICs apply these corrections at the rate of 62.5 ns.

3.6 THE HARDWARE CONTROL BUS

3.6.1 Introduction

The VLBA Correlator Hardware Control Bus (HCB) Sub-System provides the communication path between the VME Real Time System (RTS) and the correlator hardware. A single HCB is an 8 bit bi-directional data bus with associated handshake control lines that communicates with up to 16 different targets (microprocessors in the correlator). The HCB hardware consists of three major blocks

1) HCB VME I/O controller cards
2) HCB Transition Modules
3) HCB Target Interfaces (in correlator racks)

as seen in Figure 19:

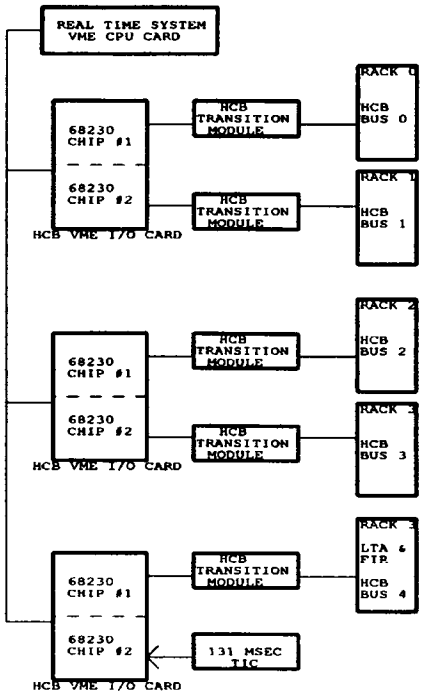


Figure 19 HCB Block Diagram

3.6.2 HCB Block Diagram Description

There are three I/O controller cards in the correlator VME chassis. One controller interfaces to two Transition Modules each of which support one of the 8 bit buses as shown in Figure 19.

The HCB VME I/O cards provide an interface from the VME backplane to the HCB Transition Module chassis, mounted behind and below the VME chassis. There are 8 bi-directional data lines and 8 control lines between each Motorola 68230 Parallel Interface Chip on the I/O cards and the corresponding transition module.

Each HCB Transition Module has both a transmit and a receive FIFO for buffering transfers to and from targets. The VME CPU uses programmed I/O to transfer data to and from the FIFOs.

There are 43 signals between each transition module and the corresponding correlator rack (targets), as follows:

Global Signals to all Targets

Nr	Description	Signal name
8	bi-directional data lines	HCB[0..7]
2	mode control lines	MODE[1..0]
1	strobe line	STROBE

Dedicated Signals, One Pair to Each Target

Nr	Description	Signal name
16	select lines	SELECT[0..15]
16	acknowledge lines	ACK[0..15]

All signals between a transition module and a correlator rack are differential RS-485 signals, resulting in 86 signal wires, distributed over two 50 pair twisted cables.

The data lines have 100 ohm line-to-line terminations at each end of the cable. The STROBE and MODE lines have terminations at the far end of the run which float low if there is no driver. The SELECT lines have a termination at the target that floats low if there is no driver. The ACK lines have a termination at the transition module that floats high if there is no driver.

Each target implements a HCB Target Interface. This consists of RS-485 transceivers, a PAL and a 8 bit bi-directional bus register. NRAO drawing number L018D01.SCH represents a generic version of a target interface. The AMD 2950 bus register was originally selected for use in the interface. The AMD chip was later found to be going out of production, so a pin compatible replacement header was fabricated, as represented in NRAO drawing number L034D01.SCH. See Appendix for all HCB schematic drawings.

3.6.3 Target Selection

For transfers to targets, one or more targets may be selected at the same time (this allows broadcasting). Targets are addressed using a 16 bit number (called the target mask or target number). This number is equal to the sum of the binary weights of the select numbers targeted. The maximum number of targets on any bus is presently nine (on Bus 3). The target mask for each bus and select are tabulated below, along with the target name:

BUS 0

SELECT NR :	7	6	5	4	3	2	1	0
TARGET MASK:	128	64	32	16	8	4	2	1
TARGET NAME:	MCC	FCC	PBI 6	PBI 5	PBI 4	PBI 3	PBI 2	PBI 1

BUS 1

SELECT NR :	7	6	5	4	3	2	1	0
TARGET MASK:	128	64	32	16	8	4	2	1
TARGET NAME:	MCC	FCC	PBI 12	PBI 11	PBI 10	PBI 9	PBI 8	PBI 7

BUS 2

SELECT NR :	7	6	5	4	3	2	1	0
TARGET MASK:	128	64	32	16	8	4	2	1
TARGET NAME:	MCC	FCC	PBI 18	PBI 17	PBI 16	PBI 15	PBI 14	PBI 13

BUS 3

SELECT NR :	8	7	6	5	4	3	2	1	0
TARGET MASK:	256	128	64	32	16	8	4	2	1
TARGET NAME:	MON	MCC	FCC	PBI 24	PBI 23	PBI 22	PBI 21	PBI 20	PBI 19

BUS 4

SELECT NR :							1	0
TARGET MASK:							2	1
TARGET NAME:							FIR	LTA

3.6.4 The 131 msec Tic Bus

As seen in Figure 19, there is a path through one of the HCB VME I/O Controller cards for the correlator system 131 msec tic. This provides a periodic interrupt to the VME CPU from the correlator. Switches on the front panel of the HCB VME I/O Controller select normal HCB operation, or TIC operation for each bus handled by the controller. This "TIC BUS" is identified as BUS 5 in the HCB sub-system. L029D01.SCH is the schematic of the TIC Transition Module that replaces the HCB Transition Module on Bus 5.

3.6.5 Low Level vxWorks Functions and Target Selection

The lowest level vxWorks based correlator HCB functions were written to take both a bus number and target mask as parameters. For example, hcbRstTarget(0,1) will reset the first PBI in rack 0 and hcbRstTarget(3,63) will reset all PBI in rack 3. Likewise, hcbRstTarget(0,65535) will reset all possible targets in rack 0. The monitor routines built into each microprocessor use the bus and target number as a prompt for the RS-232 terminal display, except for the LTA, FIR and System Monitor, where there is only one of each card in the system. The prompts for all other cards are initialized with the following functions:

```
hcbDefId (bus, target)          Deformatter and TRC
hcbFccPrompt (bus, target)      FFT Control Card
hcbMccPrompt (bus, target)      Master Control Card
```

The identity of any microprocessor connected to a terminal can be seen from the prompt, after the correlator racks have been initialized, in terms of the bus and target mask:

```
Def1-08>   is the prompt from the Deformatter in rack 1
           target mask 8.
```

3.6.6 High level vxWorks Functions and Playback Interface Selection

Higher level vxWorks functions address the Playback Interface (PBI)targets in terms of a unit number, using the numbers 0-23. This set of numbers is offset by one from the Playback Drive (PBD)numbers associated with each PBI. For purposes of inventory maintenance, the PBI are labeled the same as the PBD. Unfortunately this results in three different reference numbers for each PBI in the system, as tabulated below:

PBI Bus-Target#	PBI Inventory #	PBI Software #	PBI Bus-Target #	PBI Inventory #	PBI Software #
0-01	1	0	1-01	7	6
0-02	2	1	1-02	8	7
0-04	3	2	1-04	9	8
0-08	4	3	1-08	10	9
0-16	5	4	1-16	11	10
0-32	6	5	1-32	12	11

PBI Bus-Target#	PBI Inventory #	PBI Software #	PBI Bus-Target #	PBI Inventory #	PBI Software #
2-01	13	12	3-01	19	18
2-02	14	13	3-02	20	19
2-04	15	14	3-04	21	20
2-08	16	15	3-08	22	21
2-16	17	16	3-16	23	22
2-32	18	17	3-32	24	23

3.6.7 Data Transfers

The HCB does not allow a target to request a transfer. All transfers are initiated by the VME CPU. The HCB is block oriented and single tasking. Once a transfer has been initiated, the bus is not available for other transfers until the transfer in process has completed. The transfer rate is limited by the HCB handshakes to a maximum of approximately 100 Kbyte/sec. The actual transfer rate is controlled by the target. The highest typical rate is something over 50 Kbyte/sec. Transfer rates for specific types of transfers are listed in the documents that define the protocols for each target. These documents are all maintained in the same directories as the assembly language source code for each target microprocessor, and are listed below:

Target	HCB Protocol File Name
Master Control Card	D025MCC.HCB
FFT Control Card	D026FCC.HCB
Deformatter Card	D027DEF.HCB
Track Recovery Card	D028TRC.HCB
Long Term Accumulator	D024LTA.HCB
Filter (FIR)	D023FIR.HCB
System Monitor (MON)	D033MON.HCB

The Track Recovery Card is not a physical target on the HCB. Transfers to and from the TRC are passed through the Deformatter.

3.6.8 Bus Mode

The two bit mode control lines define the current state of the bus as follows:

Mode
---
0 first byte written to target, generates interrupt
  to the selected target(s)
1 subsequent bytes transferred to target
2 bytes transferred from target to VME (if requested)
3 reset selected target(s)

The sum of the total number of bytes transferred to the target plus any bytes returned from the target must be a minimum of two. As a result of this requirement, any defined function that needs only a single byte transferred to the target, and no bytes returned, will transfer the specified byte plus one dummy byte. The target will accept and discard the dummy byte. The state of the bus will always start at mode 0 for the first byte, automatically advance to mode 1 for one or more bytes, and then advance to mode 2 for zero or more bytes.

The first byte of each transfer is always a defined function code that the target interprets in order to determine what further action to take.

The reset operation (mode 3) causes a reset pulse to be applied to the target microprocessor. At rack download time, a reset to all targets is necessary prior to any data transfers.

3.6.9 HCB VME I/O Controller Module

Refer to the HCB VME I/O Controller Card schematics, L019D01.SCH - L019D10.SCH for the following sheet references. Sheet 1 provides entry points to all other HCB related schematics. The logic represented on this schematic is wired on a Bicc-Vero Model VME-6159 prototyping module. A copy of the users manual for this module is provided in Appendix C.

The I/O Controller Cards are mapped in VME short I/O address space. Sheet 6 of the drawing shows the defined addresses for up to a total of four cards. Only three cards are presently used in the correlator. Sheet 5 shows jumper settings for mapping the different cards.

The Bicc-Vero card normally provides a fixed delay DTACK generator. This provision is not used. A replacement DTACK generator is shown on sheet 1, at IC locations 10C, 10D and 10E. This replacement generator allows the DTACK from the Motorola 68230 Parallel Interface Chips to be used for accesses to those chips, and a fixed delay DTACK to be used for all other accesses to the card. The DIP switches at location 10D are set to select a DTACK range of 435 to 497 nsec.

Sheets 2 and 3 show the Motorola 68230 I/O chips. These chips each handle one Hardware Control Bus. A copy of the data sheet for this chip is provided in Appendix D.

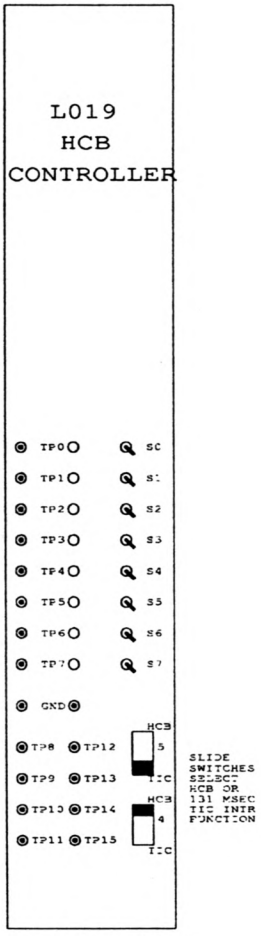
The 68230 chips interface between the VME bus accesses and the HCB Transition Module resources. Port A of the chips provides a three bit address, BUSA[0..2], that selects different resources on the transition module. Port B provides the 8 bit bi-directional bus. The timer function in the 68230 counts down the handshakes on the bus (applied to Port C, bit 2), in order to produce a VME interrupt at the end of the transfer, via Port C, bit 3.

IC 11D, seen on Sheet 1, is a multiplexer that selects between the 68230 interrupt (for normal HCB applications) and the 131 msec tic (at bus 5) used to provide the periodic system interrupt to the VME CPU.

The P2 connector (see Sheet 1) connects the 8 data bus lines and 8 handshake and control lines (all single ended) to the transition modules. Sheet 8 defines the details for fabricating the cable that connects to the P2 connector.

The PAL at location 11A (Sheet 1) provides several functions, defined in the representative schematic shown on Sheet 9. The SEL\0 and SEL\1 output select lines go to the two 68230 chip select inputs. SEL\2 is used to select the front panel input and output test points, shown on sheet 4. Data written to the front panel is latched in the register at location 11F. For each write to this register, the three LS bits of the data are presented to the decoder at location 11E, producing pulsed test points. Data read from the front panel (using SEL\2) provides the state of the eight toggle

switches, by way of the buffer at location 10F. The data written to location 11F can be seen on the eight front panel LEDs, and observed with a scope on the test points labeled 0-7. The associated pulsed test points can be observed on a scope at the test points labeled 8-15. The wiring of the front panel is shown on sheet 10. Figure 20 shows the panel layout.



FRONT PANEL

Figure 20 HCB VME I/O Controller Front Panel

3.6.10 HCB Transition Module

Refer to the HCB Transition Module schematics, L016D01.SCH - L016D06.SCH, for the following sheet references. Sheet 1 shows the I/O connector from the HCB VME I/O Controller Card in the upper left corner (J1/11C). I/O cables to the Correlator rack are shown in the lower right (J2/11A and J3/10A).

The transition module is constructed on an 11 row "Shalloway" wirewrap card, that has a Plexiglas connector plate mounted at the top. This plate mounts the J1, J2 and J3 3M style connectors. For purposes of the wirewrap program, these connectors are "mapped" to standard IC locations at 11C, 11A and 10A. The IC location pin numbers are shown outside the connector symbols and the 3M connector pin numbers are shown inside the symbols.

Sheet 2 contains the Transmit and Receive FIFO chips. The Cypress CY7C429-65 FIFOs are 2K deep, limiting transfers to a maximum of 2048 bytes (including the function code). Transfer size could be increased by replacing the FIFOs with larger capacity chips. Some protocols are customized for the 2K size, so it would require programming changes at both the target and in the VME software to take advantage of larger FIFOs.

Selection of resources on the transition module is controlled by the decoder at location 11B, seen at the upper left on sheet 1. Most of these resources are located on sheet 2. The transmit FIFO is at location 9E. The receive FIFO is at location 10E. The two registers at locations 8F and 7F provide the 16 select lines to targets. The register at location 6E sets the mode of the bus, and selects the source of data for reads from the transition module back into the VME (by way of the decoder at location 5F on sheet 1).

The register at location 5E, seen on sheet 2, controls bus operations. The signal TXFIFORST\ resets the transmit FIFO when low. TXSTBRST\ holds the oneshots at location 3E (sheet 1) reset when low. When this control line transitions to a logic 1, this initiates the transfer of data from the transmit FIFO to a target. NOTRDFIFO selects between reading data from the receive FIFO or from the other three sources (the two ACKNOWLEDGE registers, 8G and 7G, and the STATUS register at location 6F). NOTRDFIFO is set to logic 1 when the receive FIFO is not being read. The BUSEN signal is set to logic 1 to enable the RS-485 bi-directional bus drivers.

The general sequence of steps required to control a HCB transfer are:

1) Release TXFIFORST\
2) Write data to the transmit FIFO
3) Release TXSTBRST to initiate the transfer to the target

Releasing TXSTBRST\ will shoot the 3E one shot pair. 3E pin 12 will enable the FIFO data onto the bus for approximately 1 usec. 3E pin 13 will generate a strobe to clock the data into the target (on the trailing edge), allowing approximately 0.8 usec from the time data is enabled onto the bus. The trailing edge of 3E pin 12 will clock a logic 1 into 1B pin 6 (FORCEMODE1), which will change the bus mode from 0 to 1.

As long as the transmit FIFO is not empty, the handshake will proceed at a pace determined by the target. When the last byte is clocked out of the FIFO, 4C pin 5 will go low, and the final ACK returned from the target will clock TXENA into 1B pin 9, taking 1B pin 8 high. This changes the bus mode from 1 to 2, and releases the reset on the receive FIFO. If there is data to be returned from the target, the transfer will continue until the last byte has been received.

At this time, the counter in the 68230 chip (on the I/O controller) will generate an interrupt and the VME software will then set up to read the data from the receive FIFO.

If no data was to be returned, the transfer complete interrupt would be the final step (no data would be read from the receive FIFO).

The PALs at locations 1A, 2A and 3A control the ACKNOWLEDGE handshake from the target(s). If more than one target is selected (broadcast), then

all of the selected targets must produce an ACK before the composite ACK at 3A pin 22 will assert.

3.6.11 HCB Target Interface

Refer to drawing L018D01.SCH for the following description. This drawing presents the generic logic that is implemented on the TRC, DEF, MCC, FCC, LTA, FIR and MON cards. The 2950 register chip is implemented in some cases in the form of the replacement header seen in drawing L034D01.SCH. In other cases, the same logic is present, but standard DIP ICs are used discretely in place of the header. The header is only used where a PC card layout was completed prior to learning that the 2950 chip would not be available.

The 16L8 PAL seen in L018D01.SCH decodes the SELECT, MODE and STROBE inputs in order to process transfers to and from the target. The drawing represents the initial plans for implementing the target interfaces. If any conflict is found between the statements on this drawing and the actual ABEL files for the PAL at each target, the equations in the ABEL files are to be considered the true definitions.

3.6.12 HCB Trouble Shooting

Most transfers to a HCB target include a checksum or some other confidence check. A watchdog timer is also used, so that if a transfer exceeds a specified amount of time before completing, an interrupt is generated. This watchdog is a vxWorks based function.

It is intended that any error conditions result in a report to the log file indicating the bus, target number and function code involved. With this information, the target causing the problem can usually be identified.

One situation that can be difficult to diagnose is the case where one of the Playback Interfaces in a rack causes a transfer to hang in broadcast mode, resulting in the watchdog barking. During rack download, broadcast mode is used when downloading the six PBI in each rack. The target number for these transfers is thus equal to 63 (1 + 2 + 4 + 8 + 16 + 32), and there is no way to tell which of the six PBI is causing the transfer hang.

When this condition occurs, the BUS TIMEOUT messages and other resulting error messages fill the console and seem to go on forever. The procedure to follow in this case is to first press the hardware reset button and reboot. The normal reboot procedure currently is similar to the following:

```
v47c->  cd "code"
v47c->  < load.cmd
v47c->  go
```

In the above sequence of commands, the "go" command causes the racks to be downloaded, resulting in the massive error reporting due to the attempt to download the PBI in a rack, where one is causing a bus timeout. In order to determine which PBI is causing a problem, we need to skip the go command, and manually initialize the HCB in each rack, and then attempt to

do simple memory transfers to each PBI target in the rack that has the problem as follows:

```
v47c-> cd "code"
v47c-> < load.cmd
v47c-> hcbInit(5);   /*  bus 5 MUST be the first one initialized */
v47c-> hcbInit(4); hcbInit(3); hcbInit(2);
v47c-> hcbInit(1); hcbInit(0);
v47c-> hcbRstTarget(4,65535); hcbRstTarget(3,65535);
v47c-> hcbRstTarget(2,65535); hcbRstTarget(1,65535);
v47c-> hcbRstTarget(0,65535);
```

In the above sequence of commands, we replace the "go" command with sets of commands to initialize the HCB in each rack. Note that bus number 5 is the 131 msec tic bus and must be initialized first. This is because there are only two VME interrupts used in the HCB, so more than one HCB interrupts at the same level. Since the 131 msec tic runs continuously, it will cause interrupts as soon as any HCB is initialized that uses the same level as the tic, but no interrupt handler will be in place to handle the tic interrupt unless bus number 5 has been initialized. Following the hcbInit() commands, the hcbRstTarget commands will reset all targets on each of the buses. At this point, we can now attempt to do simple reads and writes of ram memory space at various targets, in an attempt to determine where the problem is. Several memory test commands are in the hcb/hcbMemTest.c software module:

```
/*****************************************************************/
int hcbReadMem(startadr,nrbytes,busnr,targetnr,mode,micro)
unsigned int startadr,nrbytes,busnr,targetnr;
unsigned int mode;  /* DIRECT (0) or VIADFM (1) */
unsigned int micro; /* if mode==VIADFM then this specifies 0,1,2 or 3 */
{

}

/*****************************************************************/
/*
      Fill a block of memory with a constant value, or an incrementing value
      incr = 0 means constant value; non-zero means increment value by this
      amount
*/

int hcbFillMem(startadr,totalbytes,value,incr,busnr,targetnr,mode,micro)
unsigned int startadr,totalbytes,value,incr,busnr,targetnr;
unsigned int mode;  /* DIRECT (0) or VIADFM (1) */
unsigned int micro; /* if mode==VIADFM then this specifies 0,1,2 or 3 */
{

}

/*****************************************************************/
```

If the target number specifies one of the Deformatters (1,2,4,8,16 or 32), then the transfer may be to either the Deformatter itself or to one of the four TRC microprocessors handled by the Deformatter. If the mode parameter is zero, then the transfer is to the Deformatter. If the mode parameter is one, then the transfer is to one of the four TRC microprocessors.

An example of a simple memory read from a Deformatter would be:

```
hcbReadMem(0x4000,32,0,1,0,0)
```

which when invoked at the vxWorks command line could be shortened to:

```
hcbReadMem 0x4000,32,0,1
```

since trailing parameters are passed as zeroes.

The above command would read the 32 bytes starting at location 0x4000 in Deformatter memory, from the first Deformatter in rack 0.

An example of writing an incrementing sequence of bytes to a Deformatter would be:

```
hcbFillMem(0x4000,32,0,1,3,32,0,0)
```

This command should write the byte values 0 through 31 in the 32 locations starting at location 0x4000 in the last Deformatter in Rack 3.

In the process of determining which PBI in a rack is causing a bus hang, first try the above read command. If that transfer does not hang, then try the write, followed by another read to verify that the memory contents were indeed written to.

If all six Deformatters in the rack pass the above test, then try reading and writing each of the four TRC microprocessors at each PBI by using the mode and micro parameters in the commands. (When mode = 1, then the micro parameter value of 0, 1, 2 or 3 is used to target one of the TRC microprocessors.) A reasonable start address for the TRC memory is 0x2000.

The following is a list of reasonable start addresses for each target in the correlator, where reasonable means there should be some RAM mapped at this address:

TRC	DEF	MCC	FCC	LTA	FIR	MON
0x2000	0x4000	0x1000	0x1000	0x1000	0x2000	0x2000

The simple reads and writes of target memory space are useful for verifying that a target is basically alive and able to communicate. They are particularly useful for determining which PBI is causing a bus hang during rack download.

3.7 MODELS

3.7.1 General

The correlator uses three tracking models to process data from the interferometer stations. These three are the fringe model, the delay model,

and the pulsar model. The structure of the model hierarchy can be seen on the Figure 21 VLBA Station Electronics block diagram.

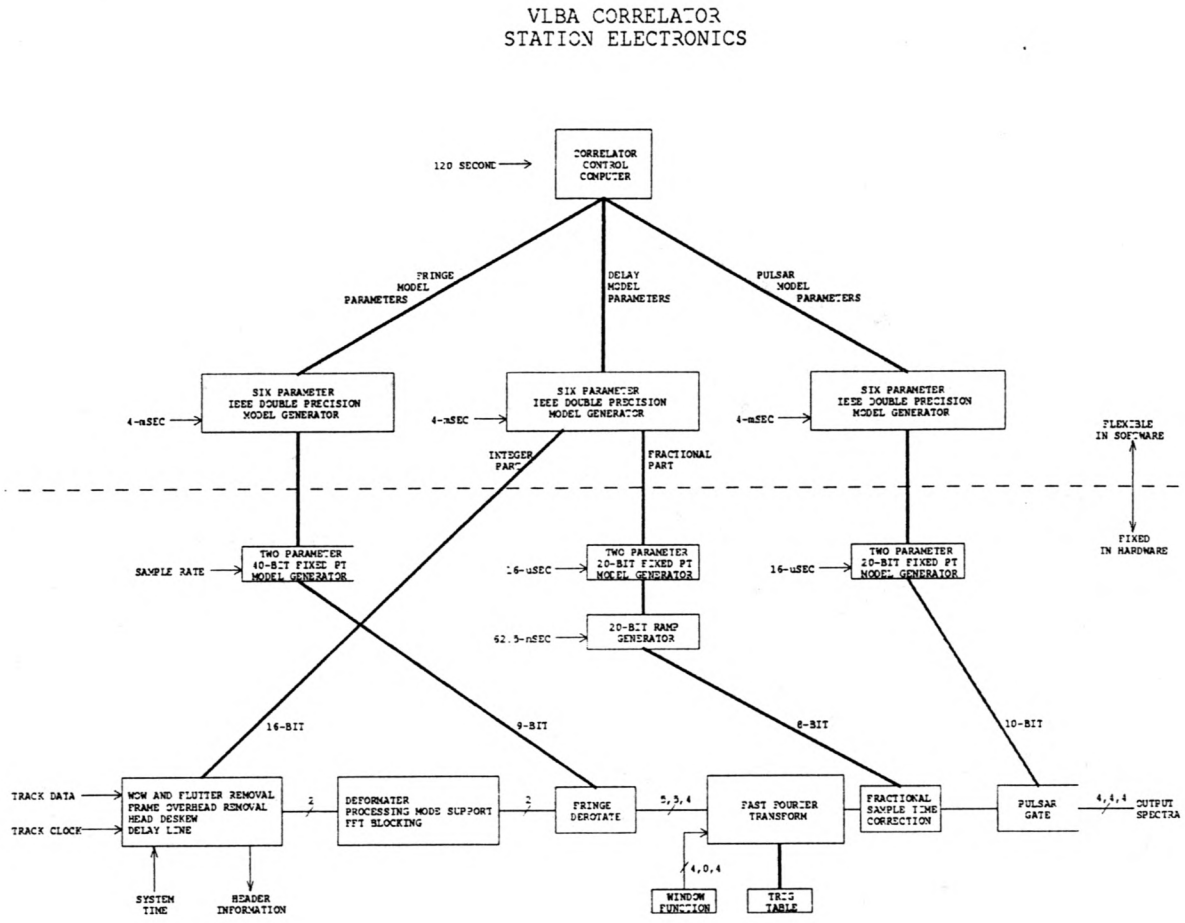


Figure 21 VLBA Station Electronics

The three model generators are somewhat similar and each is implemented partly in software and partly in hardware. Computation of the parameters for use in these models is conducted on three levels. The top level is in the VME system using CALC, where the tracking functions are analyzed every 120 seconds and a set of coefficients are produced for use in the second level. Each of these coefficients is in IEEE double precision floating-point representation and thus, 64 bits wide. A diagram of the second level of the model, which contains a floating-point processor stage on the FCC card, is illustrated in Figure 22 FCC Model Generator.

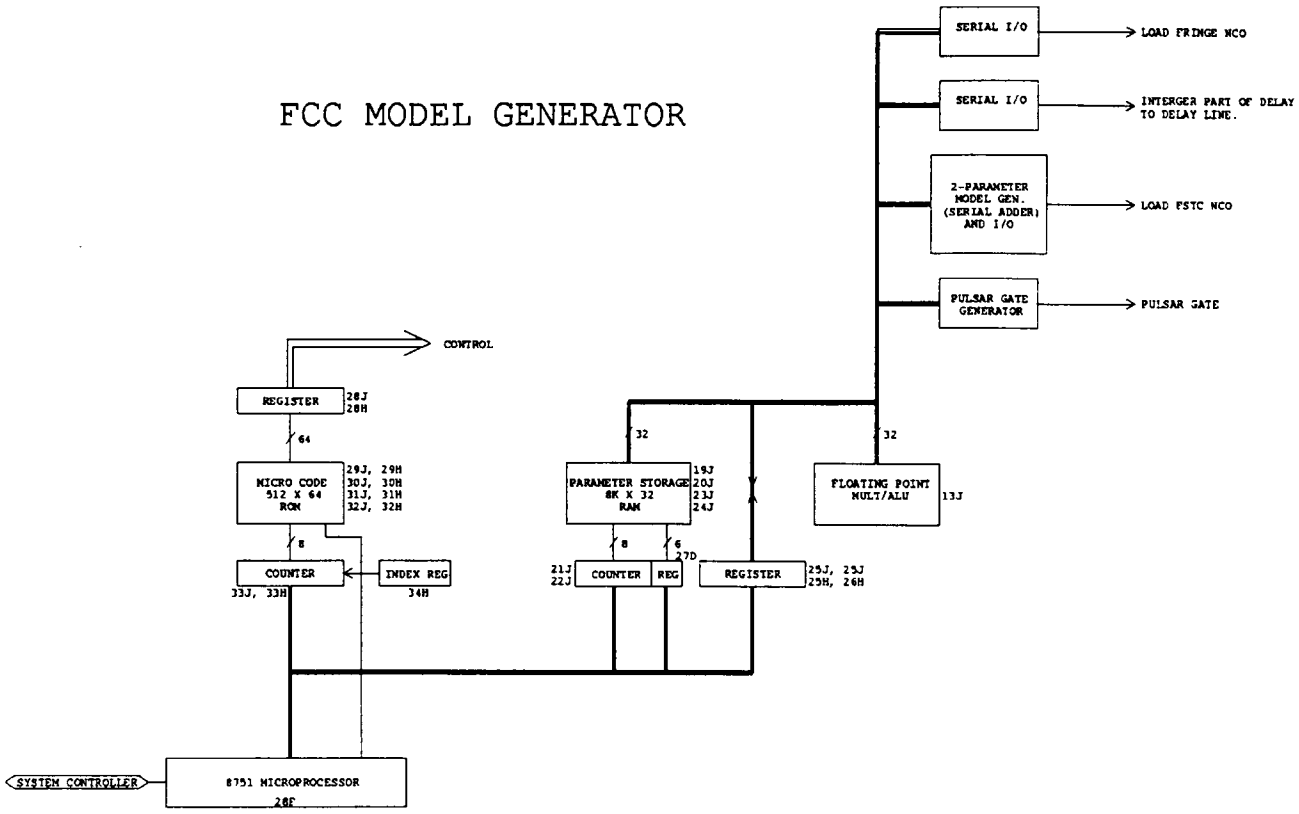


Figure 22 FCC Model Generator

Four outputs from the models are shown instead of three because the delay model is applied in two places. At this second level, an AMD 29C327 floating-point numeric processor on each FFT control card receives the coefficient values. The floating-point processor assigns the set of coefficients to a multi-term polynomial. The polynomial, generated from a Taylor series expansion, is stored in the floating-point processor memory. Each of these three models requires evaluation of two polynomials. The first polynomial contains six terms and represents the initial value of the correction (either delay, fringe phase, or pulsar phase). The second polynomial is the derivative, or time rate of change of the first polynomial. The second polynomial then, contains five terms. Model coefficients are calculated in the VME system and provided to the floating-point processors every 120 seconds, the length of the model update period. The polynomials are evaluated every 4 ms. The first polynomial represents the initial value of either a fringe phase, delay value, or a pulsar phase, as a function of time (t). Results of the polynomial evaluation with coefficients (A) of the variable (t) would then be of the general form:

$$result = A_0 + A_1 t + A_2 t^2 + A_3 t^3 + A_4 t^4 + A_5 t^5$$

Evaluation of the time rate of change of the first polynomial, or derivative, with coefficients (R) of the variable (t) would be of the following form:

$$Rate = R_0 + R_1 t + R_2 t^2 + R_3 t^3 + R_4 t^4$$

Evaluation of these two polynomials every 4 ms., results in a pair of IEEE double precision numbers representing the current correction result and the rate of change that will be applied to the data at the third and final level of the model. These two values are used by the hardware at the third level of the model to generate a linear correction ramp during this 4 ms. period between polynomial evaluations. This third and final level is slightly different for each of the models and is discussed in the following sections on each particular model.

3.7.2 The Fringe Model

This model is used to remove the Doppler shift in the data that was introduced largely due to the rotation of the earth. During the observation, each station is either moving toward the source, or moving away from the source. If the station is moving toward the source, the received wave is compressed and the apparent frequency is slightly increased. If moving away from the source, the wave is observed to expand slightly and the apparent frequency is decreased. The result of this apparent motion of the stations with respect to the source shows up as a slight frequency error. In order to maintain fringes, this effect must be removed.

The two polynomial results discussed in the General section above are each 64 bits wide. The format is converted from IEEE floating-point to a fixed-point format and only 40 bits of each are retained. The first result represents the initial fringe phase of the correction. After conversion to fixed-point, the 24 uppermost bits represent the integer portion and are discarded leaving 40 bits of fractional component. The second number is the rate at which the fringe phase needs to change. After conversion to fixed-point, the decimal point precedes the msb with all 64 bits as fractional component. The 24 lsbs are discarded. The floating-point chip produces results from the polynomial evaluations every 4 ms. based on the parameters sent during the 120 second model update cycle. Every 4 ms., the 40 bits of phase and 40 bits of rate results are sent to a Numerically Controlled Oscillator (NCO) on the FFT cards. The NCO uses the initial phase and the rate of change to produce a linear ramp, which will drive a fringe derotator in the FFT pipelines for the 4 ms. cycle until a new set of results is available. The updates to the fringe derotator are applied with each tic of the 32 MHz clock.

3.7.3 The Delay Model

With the extremely long baselines encountered in the VLBA, there are features inherently present in the data, related to wave front delay, which must be removed by the correlator. A wave front from the astronomical source will arrive at two antennas at different times. In order to process the data from the array, which has received a wave front at a different time at each station, a delay must be introduced for every station such that the electrical signals will all line up with the station that occupies the

position at the farthest point from the source. These delays must continuously be updated since as the array tracked the source through the sky, the relative position of each antenna was changing with respect to the source. The antenna that occupies the farthest position from the source is also subject to change during the course of the observation.

The delay model updates, under control of the VME system, occur on the 120 second model update cycle. During each cycle update, the set of coefficients is sent to the floating-point processor on the FCC in each of the four racks. In addition, due to bus limitations, a time reference is sent to each Deformatter over the HCB. Between the 120 second model updates, the floating-point chip must use these coefficients to evaluate the delay polynomials, which occurs on the FCC every 4 ms. The delay and rate results are applied to the data at two different points in the system, the PBI and the FFT. The delay and rate polynomial evaluations each result in a 64 bit IEEE floating-point number. The rate result is converted to fixed-point with 32 bits of integer component, and 32 bits of fractional component. Of the integer part, 16 lsbs are retained and sent to the PBI and applied in the delay centers of the TRCs. The integer delay is typically integral multiples of the sampling clock period. Of the 32 bits in the fractional component, the 20 msbs are retained and applied in the FFT cards, along with the 20 msbs of the rate results, after the FFT has been performed. This 20 bit delay and rate pair are then used on the FFT card by a NCO to generate a correction ramp, with updates at the FFT cycle rate of 16 us. Typically, this part of the delay will be some fraction of the period of the sampling clock, commonly known as Fractional Sample Time Correction (FSTC).

Delay parameters are transmitted to the PBIs by two different paths. The time reference, mentioned above, uses the first path, which is from the VME system over the HCB to the Deformatters. The second path is used by the integer delay. This delay is limited to 16 bits at this point in the correlator because the serial data path between the model generator and the Deformatter card can only handle 16 bit numbers. The larger, cumulative delays are sent from the VME over the HCB during the 120 ms. model update. The integer delays are sent to the PBIs from the floating-point processors every 4 ms.

A note concerning OVLBI: Observations incorporating an orbiting station require larger delays to be updated faster than the correlator was originally able to accommodate. Refitting of the correlator to process data from the OVLBI experiments included changes to the FSTC, enabling some level of integer delays to be applied in the FSTC.

3.7.4 The Pulsar Model

The observations of a pulsar require that the correlator be gated on and off, at the rate of the emissions received from the pulsar. These emissions are comprised of a mixture of frequencies. Since the velocity of propagation is a function of frequency due to normal wave dispersion, when the pulsar "turns on", the higher frequencies arrive first. Likewise, when the pulsar "turns off", the higher frequencies disappear first while the lowest frequencies are still being received. In order to capture the entire signal with a minimum of noise in any spectral bin, the correlator must be

gated on at the arrival of the earliest and highest frequencies and allowed to remain gated until all of the lower frequency energy disappears. At the beginning of the correlator "on" time, the highest spectral channels contain useful data immediately, while the lowest channels have not yet seen the arrival of the slower frequencies. On the other hand, when the correlator gates "off", the lowest channels contain valid data while the higher frequencies have since disappeared. In order to correct for this situation, a model must be tracked which can accurately predict when the spectral channels will contain valid data. The model then exercises control over the pulsar gate. A block diagram of the hardware elements that accomplish the gating is shown in Figure 23 Pulsar Gate Generator.

PULSAR GATE GENERATOR BLOCK DIAGRAM

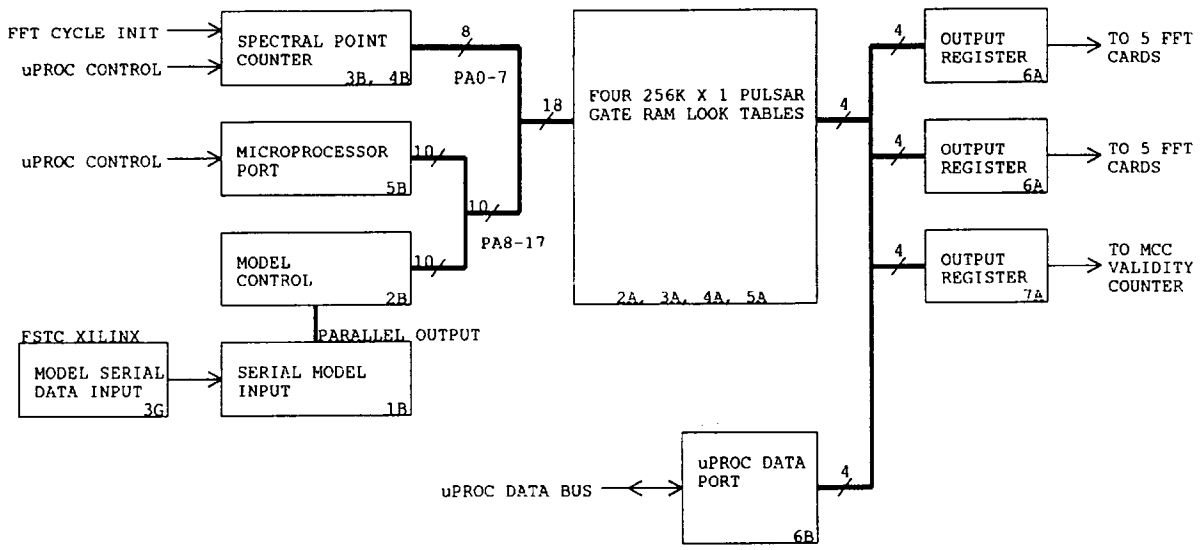


Figure 23 Pulsar Gate Generator

The pulsar model is similar to the delay and fringe models with respect to the use of the two polynomials and the evaluations at the 4 ms. rate. The program used to calculate the coefficients for the terms of the pulsar polynomial is called TEMPO. This model incorporates a mask that prevents accumulation of samples into the spectral channels during the times it is known the channels could not contain pulsar data. The correction polynomial is called the pulsar phase and is paired with a second polynomial that represents the rate of change of the initial phase. As with the other two models, the 64 bit floating-point results are converted to fixed-point. The pulsar phase result is fixed at 32 bits of integer, which are discarded, and 32 bits in the fractional component, with 20 of the msbs in the fractional portion retained. Of the 64 bits representing the rate, only 20 of the msbs are retained. These two 20 bit numbers representing the pulsar phase and rate are used by the FCC to generate a 10 bit field to correct pulsar phase on a 16 us. cycle.

3.8 ERROR CHECKING, VALIDITIES, AND WEIGHTS

The correlator must make judgements on data quality at several points throughout the system. This process begins as soon as the headers are removed from the data stream, on the TRC. An error free time stamp in the header is crucial to successfully processing the frame. A Cyclical Redundancy Check (CRC) is performed on the time field when it is inserted into the frame in the formatter. The result of the CRC calculation is an eight bit field, which is inserted into the data stream as a field in the header. When the time field is recovered in the TRC, another CRC is performed and checked against the one sent with the frame. If the CRC bytes do not match exactly, then the time field is assumed to have been corrupted. This may lead to declaring the frame invalid depending on successful recovery of subsequent time frames, sync integrity, and header errors.

The next level of error checking is parity. Each byte in the data frame, including the bytes in the header, was appended with a parity bit in the formatter. Parity is calculated in the DPC on the TRC for each byte in the data field before the data is stored in the TRC RAM. Any mismatches with the transmitted parity bit will increment a parity error counter in the DPC. Parity errors for the frame are tallied and if a predetermined threshold is exceeded, the entire frame is declared bad. A typical value for this threshold is 16 errors per frame; the limit on this counter is 253.

Sync detection problems can also lead to the declaration of invalid frames. Without the use of the sync watchdog and sync probation mode, any loss of sync or detection of sync in the wrong place would result in an invalid frame. The use of these features, however, provides a level of tolerance for sync errors before data is lost.

Errors in the headers are also used to make validity judgements. If a header is not perfect (perfect is defined as sync detected in the right place, with no CRC errors or header parity errors), then a header error counter will be incremented. An imperfect header alone is not sufficient cause to flag an entire frame as bad, but if bad headers are concurrent with other data quality problems a frame may be declared invalid.

Invalid frames ultimately cause the FFT results to be zeroed out to prevent errors from contributing to the accumulated results. The invalid judgements discussed so far are considered to be track based, and accumulated in a counter. Before any action is taken to zero the FFT results, the track based validities are translated frame by frame into channel based validities taken together with other considerations to make channel based validity judgements. Since in some modes, a single track may be assigned to more than one FFT channel, a track based invalid will be translated to each channel to which it is assigned.

After the data enters the Deformatter, mux/demux operations are performed, barrel rolling is removed, and other configurations of the data are done before the FFT is performed on a channel. If a barrel roll phase is missed or other errors are detected in these operations, the track invalidity is taken together with problems at this stage to make a judgement on channel validity. Judgements on channel based invalids are also kept in a counter and are based on frames.

As the FFT results are multiplied and accumulated in the short term and long term buffers, counters keep track of the number of valid FFT intervals that occur in the 131 ms. integration cycle. This judgement is referred to as a weight and is a value between zero and one that represents the percentage of the integration cycle that is expected to have been error free.

4. SYSTEM MAINTENENCE

4.1 GENERAL

Technical support of the correlator with respect to troubleshooting, feature enhancements, and other design changes is an ongoing process. Several fixtures in the lab, as well as the system diagnostics, are used for troubleshooting system modules and working out the details associated with engineering changes. During system development, a series of bench-top test fixtures was conceived and built. In 1996, the need for more complex and comprehensive lab simulation of system behavior was realized. The capacity to accurately replicate the signal path from the input at the PBI to the output of the FIR was not very practical by daisy chaining the test fixtures together. This drawback with the bench fixtures led to the construction of a test bed, which more closely resembles the signal path in the system.

4.2 LAB FIXTURES

The test environment in the lab, shown in Figure 24, has a VME computer system central to the environment that is very similar to the VME system in the correlator. Most of the fixtures have one or more RS232 interfaces for access to the microprocessors on the cards as well as the ones in the test fixtures. These interfaces are not shown in Figure 24. In order to operate the correlator, or any of the test fixtures, the VME system must first be downloaded with the correlator software, which resides on a networked disk drive. The software includes the HCB functions and protocols necessary to operate the correlator and the test environment. The initialization files for all of the local microprocessor RAMs, data sequencer files, and Xilinx PLD personalities are a part of this software. Operation of a lab fixture involves transmitting the RAM, sequencer, and Xilinx PLD files necessary for the particular subset of boards under test, from the VME memory to the boards. Each test fixture is set up to accommodate a different subset of correlator boards.

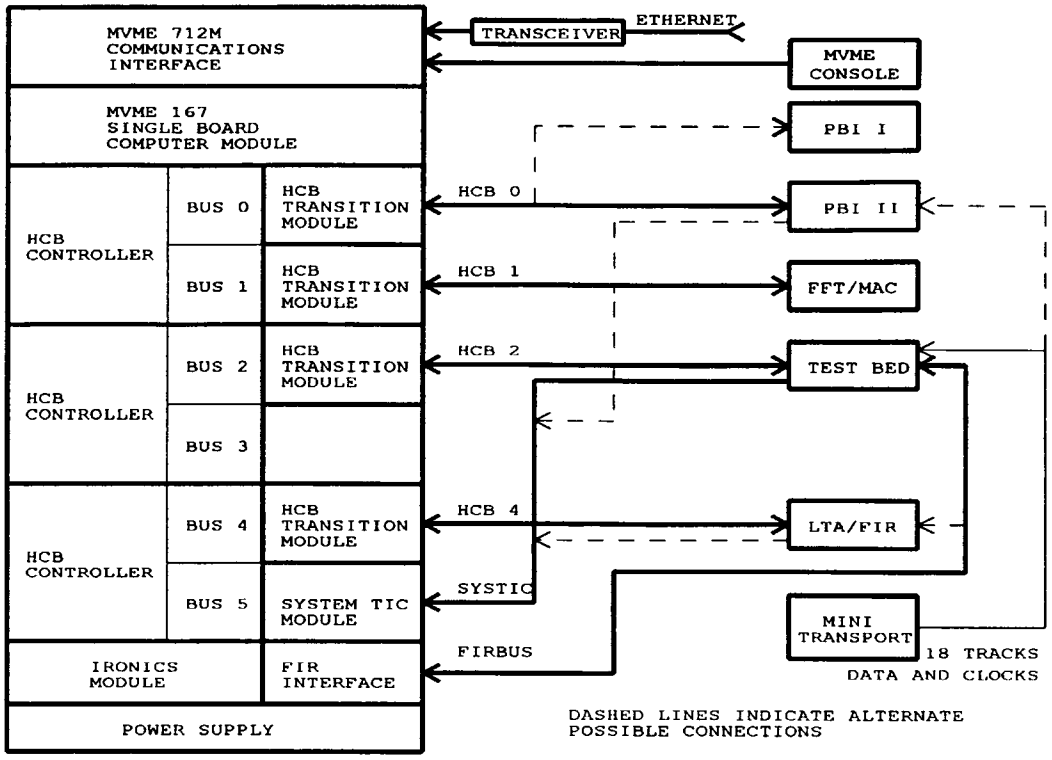


Figure 24 Test Environment

The VLBA Blue Books that describe the individual correlator modules also describe the use of the test fixtures, which includes the files needed and testing strategies.

4.2.1 Mini-Transport

The Mini-Transport is a portable bench unit that can simulate 18 of the 36 PBD tracks and serves as a data source for the PBI test fixtures. The data can come from one of several sources including a pseudo-random generator, a bank of user defined RAM, or a simulated spectral line.

4.2.2 PBI I

The PBI I fixture supports a Deformatter and a single TRC, has an internal data source, and a microprocessor card with a terminal interface. This fixture is most useful for troubleshooting TRCs. A small module, the Deformatter replacement card, can be used in place of the Deformatter allowing a TRC to be tested in a stand-alone mode independent of the VME. Since it is used in a stand-alone configuration, errors are reported via LEDs on the front panel. The front panel also has a bank of switches that are used to control bits in the internal data generator. There is also a substitute TRC card that can be used to test a DEF card by itself. With a DEF installed, an HCB connection to the VME can be made and the card can be downloaded using configuration files external to the test fixture. This

provides more flexibility and complexity to the tests that can be performed. The use of a single TRC, however, proved to be too much of a limitation for a fully comprehensive test of the DEF and PBI, which led to the construction of PBI II.

4.2.3 PBI II

The PBI II fixture will support two TRCs, a DEF, and a MCC. This constitutes a full playback interface, but it has no internal data source, and no local utilities or diagnostics available. A 32 MHz clock is provided by the test fixture and RS232 connections from a terminal may be switched via a level translation board to the TRC and DEF microprocessors. This fixture requires an HCB connection to the VME computer. Several utilities exist for exercising the boards in this test fixture from the VME computer via the HCB.

4.2.4 FFT/MAC

This fixture will support an FCC, an FFT card, and a MAC. There is an internal 87C51 in this fixture that is accessible to the HCB. When the fixture is downloaded, a data pattern is loaded into the data generator portion of memory within the fixture. A comparison snapshot is also loaded into memory in the fixture. As the test runs, the results from the FFT/MAC cards are compared to the reference snapshot. Front panel LEDs report the occurrence of errors and observing status. Detailed errors can be retrieved from the 87C51 in the fixture and reported to the VME terminal screen. Testing includes all of the spectral modes as well as MAC polar mode. Two internal clocks are provided, a 32 MHz fixed clock and a variable clock over the 19 to 40 MHz range. An external clock can also be used. A 25 pin 'D' connector on the back panel of the fixture provides access to the microprocessor on the FCC card or the microprocessor in the test fixture and a connection for the HCB is also provided. The substitute MAC card may be used for testing which allows better access to the FFT for probing and troubleshooting. The substitute FFT card may be used for MAC card testing independent of the FFT and FCC.

4.2.5 LTA/FIR

This fixture also has a fixed internal 32 MHz clock and a pair of connectors for the HCB, but no internal microprocessor card or built in test utilities. The microprocessors on each card are accessed through independent 9 pin 'D' connectors on the rear panel. In the system, the LTA would normally receive data from the MACs via the HCB. In the test fixture, simulated data is produced by a test mode in the input register on the LTA. The PALs on the LTA can be put into a mode to generate pseudo random data.

4.2.6 Test Bed

The test bed contains two correlator module bins. The lower bin supports two complete PBIs, consisting of four TRCs and two Deformatters.

The center bin supports two FFT cards, two MACs, an MCC, an FCC, an LTA, and an FIR. This card set is the minimum required to replicate the data path through the correlator for a single baseline. With this configuration the capacity for troubleshooting modules as well as further development is greatly enhanced over that offered with the bench fixtures. The 32 MHz clock to the test bed is taken from the correlator. All of the modules with a HCB are connected to a single bus that serves the entire rack.

4.2.7 VME System

The VME system in the lab is the real time system for the test environment. The MVME167 in the lab system, as well as the other modules, are spares for the system. The lab system has the capacity for six HCBs, one of which must be committed to the system tic (Bus 5).

APPENDIX A *systest & opsSystest*

A.1 INTRODUCTION

System test (systest) provides the primary means of determining the health of the VLBA Correlator. This document presents the interpretation of the results, to determine what is wrong with the VLBA Correlator. A companion document, hcbtest/opsSystest.txt is meant as an aid to the operators in interpreting opsSystest results. The operators would then be able to know which Tape Drives and FFT Engines to disable via the EQUIPSTAT screen. Troubleshooting tips for the system are presented, including the use of the monitor card.

A.2 INVOKING SYSTEST

In hcbtest/hcbSysTestFix.c, the functions dosystest and opsSystest are defined. opsSystest is periodically invoked by the operators. opsSystest calls dosystest three times, to test different configurations of the system. dosystest is defined:

```
int dosystest(autoflag,fftsize,btfact,ovsfact)
     int autoflag;
     /* 0= configure system, but do not start test of results */
     /* >0 = configure, start various tests based value of autoflag */
      1 = Snapshot test
      2 = Snapshot test using the LTA as the output device instead
            of the fir.
      3 = Compare test comparing 0 to 10, 1 to 11 etc.
      4 = Compare test comparing 0 to 19, 1 to 18 etc.
      5 = Compare test comparing ch0-3 to ch4-7
     int fftsize;              /* 0 defaults to 512  */
         /* or else actual fft size (64, 128, 256, 512, 1024, 2048) */
     char *bit_trk;  /* "1-4", "1-2", "1-1", "2-1" or "4-1"  */
      /* blank defaults to 1-4 */
     int ovsfact;               /* 0 defaults to 1 in hcbSysTest, else
                              have 1,2,4,8 or 16 */
```

A.3 VIEWING SYSTEST RESULTS

Systest results can be viewed real-time using the screens package. There are two screens available for use. The screen named ltasyserrs0 can be invoked to display the error map for any pair of channels. The screen named pbisysco can be invoked to display the servo status. ltasyserrs0 is in hcbtest/hcbLtaScrn0.c. pbisysco is in hcbtest/hcbPbiCOScrn.c. For normal use, four ltasyserrs0 screens are invoked and configured to display the eight channels. Also, one pbisysco screen is invoked for monitoring the servo status. From /home/azalea/corrlab/autoscreens.v47c, invoke the script files r0, r1, r2, r3, and r4 in five separate xterms. This will set up

displays of the error maps for Channels 0 and 1, 2 and 3, 4 and 5, 6 and 7, and the Servo Status, respectively. These script files utilize the -r command line switch to the rscreen command. This switch specifies a response file to be used in place of the key strokes. The response files configure each screen as required.

The script files contain the following:

```
r0:  rscreen -r quad0.rscreen v47c
r1:  rscreen -r quad1.rscreen v47c
r2:  rscreen -r quad2.rscreen v47c
r3:  rscreen -r quad3.rscreen v47c
r4:  rscreen -r pbisysco.rscreen v47c
```

The response files contain spaces and tabs and returns embedded so as to set up the desired screens. In case these files need to be re-constructed from scratch, the following section provides duplicates of the files, including the spaces and tabs. Copy and Paste operations may be used to copy these lines to new files (make sure the white space at the beginning and end of each line is picked up) except that the ^M shown in the lines is not a real <ret>. It will need to be replaced with a real Control-M in the actual response files. Each line is followed by a line that shows the hex bytes (as seen using the UNIX od utility). Note that tab is 09, space is 02 and ^M is 0d. The trailing tabs are used to position the cursor on specific screen "buttons".

```
quad0.rscreen:  (26 bytes)
 e^M ltasyserrs0^M      0^M         1^M
20 65 0d 20 6c 74 61 73 79 73 65 72 72 73 30 0d 20 09 30 0d 20 09 09
31 0d 09

quad1.rscreen:  (28 bytes)
 e^M ltasyserrs0^M      2^M         3^M
20 65 0d 20 6c 74 61 73 79 73 65 72 72 73 30 0d 20 09 32 0d 20 09 09
33 0d 09 09
09

quad2.rscreen:  (27 bytes)
 e^M ltasyserrs0^M      4^M         5^M
20 65 0d 20 6c 74 61 73 79 73 65 72 72 73 30 0d 20 09 34 0d 20 09 09
35 0d 09 09

quad3.rscreen:  (31 bytes)
 e^M ltasyserrs0^M      6^M         7^M
20 65 0d 20 6c 74 61 73 79 73 65 72 72 73 30 0d 20 09 36 0d 20 09 09
37 0d 09 09 09 09 09 09

pbisysco.rscreen:  (13 bytes)
e^M pbisysco^M
65 0d 20 70 62 69 73 79 73 63 6f 0d 0a
```

On ccc, the xterms can be set up by invoking /home/azalea/corrlab/ccc.init. This provides the R0, R1, R2, R3, and R4 titles in the xterm borders.

The setup script for the xterm windows contains:

```
ccc.init:
  xterm -T R0 -n R0 -sb &
  xterm -T R1 -n R1 -sb &
  xterm -T R2 -n R2 -sb &
  xterm -T R3 -n R3 -sb &
  xterm -T R4 -n R4 -sb &
  xterm -T PBD -n PBD -sb &
```

A.4 OPSSYSTEST

The most common way of invoking systest is to use the function opsSystest. opsSystest automatically sequences through

```
dosystest(1,0,"1-4",0); /* Snapshot test */
dosystest(3,256,"1-2",0); /* 256 max fft size for polar mode */
dosystest(4,512,"1-2",2);
```

opsSystest results are placed in the file /home/fxcorr/vwlog/ops.123. If ops.123 reports no errors, as indicated by a small file size, then the previous results are stored as ops.123.previous. The old ops.123.previous is stored as ops.123.oldest. Only storing ops.123.previous with no errors eliminates filling the previous and old versions with the multiple runs of opsSystest that occur when an error is discovered. The main thing of interest is when was the last run with no errors. This information defines the period when the VLBA Correlator was broken.

Below is a sample of an error free ops.123 file.

```
1997AUG27  7h49m54.63s
lta_current_config= 1, model nr=0, bit to trk=1-4, pgena=0
dosystest(1) (snapshot test), fftsize=512, oversamp=1, overlap=1
Validity errors for 18 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
MAC nonpolar data errors, chans 0-7 are:
     0       0       0       0       0       0       0       0
No data errors present.
-----------------------------------------------------------------
1997AUG27  7h53m34.90s
lta_current_config= 2, model nr=2, bit to trk=1-2, pgena=1
manyparms(3) compare test (0-9/10-19). fftsize=256, oversamp=1,
overlap=2
Validity errors for 7 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
MAC polar data errors, chans 0-7 are:
     0       0       0       0       0       0       0       0
No data errors present.
-----------------------------------------------------------------
1997AUG27  7h57m16.97s
lta_current_config= 3, model nr=3, bit to trk=1-2, pgena=0
manyparms(4) compare test (0-9/19-10). fftsize=512, oversamp=2,
overlap=2
Validity errors for 7 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
MAC nonpolar data errors, chans 0-7 are:
```

```
      0       0       0       0       0       0       0       0
No data errors present.
-----------------------------------------------------------------
```

A.5 EXPLANATION OF SYSTEST PARAMETERS

This section explains the parameters seen in the above opsSystest result.

lta_current_config reflects the state of the FFT Card input multiplexers. Each FFT Card has a four input multiplexer which choses the Deformatter (DEF) and associated Playback Drive (PBD). The tables below define, for each configuration, the DEF and PBD corresponding to the station (FFT card).

```
CONFIGURATION TABLE
lta_current_config= 0
      Station  0 source= DEF3-32 PBD=24
      Station  1 source= DEF0-01 PBD=01
      Station  2 source= DEF0-02 PBD=02
      Station  3 source= DEF0-04 PBD=03
      Station  4 source= DEF0-08 PBD=04
      Station  5 source= DEF0-32 PBD=06
      Station  6 source= DEF1-01 PBD=07
      Station  7 source= DEF1-02 PBD=08
      Station  8 source= DEF1-04 PBD=09
      Station  9 source= DEF1-08 PBD=10
      Station 10 source= DEF1-32 PBD=12
      Station 11 source= DEF2-01 PBD=13
      Station 12 source= DEF2-02 PBD=14
      Station 13 source= DEF2-04 PBD=15
      Station 14 source= DEF2-08 PBD=16
      Station 15 source= DEF2-32 PBD=18
      Station 16 source= DEF3-01 PBD=19
      Station 17 source= DEF3-02 PBD=20
      Station 18 source= DEF3-04 PBD=21
      Station 19 source= DEF3-08 PBD=22

lta_current_config= 1
      Station  0 source= DEF0-01 PBD=01
      Station  1 source= DEF0-02 PBD=02
      Station  2 source= DEF0-04 PBD=03
      Station  3 source= DEF0-08 PBD=04
      Station  4 source= DEF0-16 PBD=05
      Station  5 source= DEF1-01 PBD=07
      Station  6 source= DEF1-02 PBD=08
      Station  7 source= DEF1-04 PBD=09
      Station  8 source= DEF1-08 PBD=10
      Station  9 source= DEF1-16 PBD=11
      Station 10 source= DEF2-01 PBD=13
      Station 11 source= DEF2-02 PBD=14
      Station 12 source= DEF2-04 PBD=15
      Station 13 source= DEF2-08 PBD=16
      Station 14 source= DEF2-16 PBD=17
```

```
        Station 15 source= DEF3-01 PBD=19
        Station 16 source= DEF3-02 PBD=20
        Station 17 source= DEF3-04 PBD=21
        Station 18 source= DEF3-08 PBD=22
        Station 19 source= DEF3-16 PBD=23

    lta_current_config= 2
        Station  0 source= DEF0-02 PBD=02
        Station  1 source= DEF0-04 PBD=03
        Station  2 source= DEF0-08 PBD=04
        Station  3 source= DEF0-16 PBD=05
        Station  4 source= DEF0-32 PBD=06
        Station  5 source= DEF1-02 PBD=08
        Station  6 source= DEF1-04 PBD=09
        Station  7 source= DEF1-08 PBD=10
        Station  8 source= DEF1-16 PBD=11
        Station  9 source= DEF1-32 PBD=12
        Station 10 source= DEF2-02 PBD=14
        Station 11 source= DEF2-04 PBD=15
        Station 12 source= DEF2-08 PBD=16
        Station 13 source= DEF2-16 PBD=17
        Station 14 source= DEF2-32 PBD=18
        Station 15 source= DEF3-02 PBD=20
        Station 16 source= DEF3-04 PBD=21
        Station 17 source= DEF3-08 PBD=22
        Station 18 source= DEF3-16 PBD=23
        Station 19 source= DEF3-32 PBD=24

    lta_current_config= 3
        Station  0 source= DEF0-04 PBD=03
        Station  1 source= DEF0-08 PBD=04
        Station  2 source= DEF0-16 PBD=05
        Station  3 source= DEF0-32 PBD=06
        Station  4 source= DEF1-01 PBD=07
        Station  5 source= DEF1-04 PBD=09
        Station  6 source= DEF1-08 PBD=10
        Station  7 source= DEF1-16 PBD=11
        Station  8 source= DEF1-32 PBD=12
        Station  9 source= DEF2-01 PBD=13
        Station 10 source= DEF2-04 PBD=15
        Station 11 source= DEF2-08 PBD=16
        Station 12 source= DEF2-16 PBD=17
        Station 13 source= DEF2-32 PBD=18
        Station 14 source= DEF3-01 PBD=19
        Station 15 source= DEF3-04 PBD=21
        Station 16 source= DEF3-08 PBD=22
        Station 17 source= DEF3-16 PBD=23
        Station 18 source= DEF3-32 PBD=24
        Station 19 source= DEF0-01 PBD=01
```

Changing configuration can be accomplished manually by typing a new value into the CONFIG field of the R0 screen. This is useful for differentiating Playback Interface(PBI) and FFT related faults. PBI faults will shift with configuration, while FFT faults will remain unchanged.

In the opsSystest results, model nr refers to the active model used for FSTC/Fringe/Pulsar calculations in the FFT Control Card(FCC).

bit to track refers to the method of combining tracks used on the deformatter card.

pgena is a global variable that determines if the pulsar gate is enabled.

The next field tells the type of systest, as defined by the first argument of dosystest.

dosystest 1 is the snapshot test. This compares each baseline to a single, identical snapshot. Models are set to zero. The advantage is it detects any system wide changes and changes in an individual baseline. There are not the ambiguities present in the compare tests. The disadvantage is it is not flexible for testing different modes. Since the models are set to zero, most model related errors are not detected.

dosystest 3, dosystest 4 and dosystest 5 are the compare tests. They each compare one half of the VLBA Correlator to the other half. They differ in the way the correlator is split in half. Their advantage is they allow the correlator to be tested in any mode, without having new snapshots required. The models can change as a function of time. This was impossible with a snapshot test, since a constantly changing snapshot would be required. The compare tests' disadvantage is there are ambiguities, where we do not know which half of the correlator is bad.

dosystest 3 compares stations 0-9 to stations 10-19. dosystest 4 compares stations 0-9 to stations 19-10. These complement each other in that they can be used to resolve any compare test ambiguities. For example if dosystest 3 said station 1 or 11 was bad, and dosystest 4 said station 1 or 18 was bad, then we would know station 1 was the actual bad station. The command manyparms, allows switching between the two modes while dosystest 3 or 4 is running. Type manyparms 3 to put systest in the dosystest 3 compare mode. Type manyparms 4 to put systest in the dosystest 4 compare mode.

dosystest 5 compares channels 0-3 to channels 4-7.

The values reported in opsSystest: fftsize, oversamp, and overlap, specify the mode of the FFT card and deformatter.

Any validity errors are reported next. Validity errors can be viewed on a baseline basis by toggling the DVTOG field in screen R1.

The next line, of the opsSystest results, displays the MAC Polar or MAC Non-Polar errors. MAC polar mode is determined by the global variable glmacpolar. In MAC Polar mode, the MAC card cross multiplies the two polarizations obtained from adjacent pairs of FFT pipelines.

A.6 INTERPRETING SYSTEST RESULTS WHEN THERE ARE ERRORS

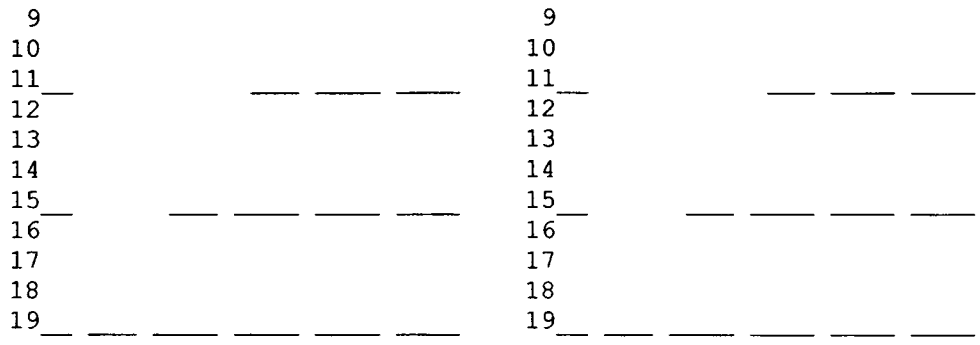
Below is an opsSystest result that contains errors. Interpretation of the results is provided after each of the three sections.

The display shows for each of eight channels, a graph of the baselines, with FFT engines 0 through 19 on the x and y axes. Errors are represented by a error count of 0 through hexadecimal F. Error counts greater than F are represented by F. The number of loops is also presented. "Hard" errors will have the number of loops equal to the number of errors. An intermittent error where a 1 is shown in the matrix out of 7 loops is not as serious.

Notice the row that was all 0's now shows the total number of errors present for each channel.

```
FIRST SECTION OPSSYSTEST RESULTS
1997AUG27 16h14m51.07s
lta_current_config= 1, model nr=0, bit to trk=1-4, pgena=0
dosystest(1) (snapshot test), fftsize=512, oversamp=1, overlap=1
Validity errors for 18 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
MAC nonpolar data errors, chans 0-7 are:
   367      26       0       0     510     510       0       0

          CHAN 0          18 LOOPS       CHAN 1   Config=1
    1111 1111 11                    1111 1111 11
    9876 5432 1098 7654 3210        9876 5432 1098 7654 3210
    ---- ---- ---- ---- ----        ---- ---- ---- ---- ----
 0             F                  0                       F
 1             F                  1
 2             F                  2
 3__           F          ___     3__                     ___
 4             F                  4
 5             F                  5
 6             F                  6
 7__           F     ___ ____     7__                ___ ____
 8             F                  8
 9             F                  9
10  FFFF FFFF FF                  10
11__           ___ ____ ____      11__          ___ ____ ____
12                                12
13                                13
14                                14
15__       ___ ____ ____ ____     15__      ___ ____ ____ ____
16                                16
17                                17
18                                18
19__ ___ ____ ____ ____ ____      19__ ___ ____ ____ ____ ____
          CHAN 4          18 LOOPS       CHAN 5   Config=1
    1111 1111 11                    1111 1111 11
    9876 5432 1098 7654 3210        9876 5432 1098 7654 3210
    ---- ---- ---- ---- ----        ---- ---- ---- ---- ----
 0  FFFF FFFF FFFF FFFF FFFF     0  FFFF FFFF FFFF FFFF FFFF
 1                                 1
 2                                 2
 3__                    ___       3__                     ___
 4                                 4
 5                                 5
 6                                 6
 7__               ___ ____       7__                ___ ____
 8                                 8
```



The channel 0 results show a single bad FFT pipeline for FFT 10. This could be due to a bad ASIC. Note F indicates a hard error where the error occurred at least 15 of the 18 loops. To determine which FFT card to replace, refer to the below chart.

	Rack0	Rack1	Rack2	Rack3
Ch 0-3	FFT0-9	FFT10-19		
Ch 4-7			FFT0-9	FFT10-19

Note: Each FFT card has four channels on it.

Running dosystest with an FFT size of 2048 can be useful in determining which of the six ASICs in an FFT pipeline is bad (dosystest 3, 2048 for example). Label the ASICs in a pipeline, 0 to 5 from left to right. If the same single pipeline is bad for the 2048 point FFT, as was bad for the 512 point FFT, then ASIC 5 is bad. If two pipelines are bad in the 2048 point FFT, then ASIC 4 is bad. The other bad pipeline would be:

Bad 512 point pipeline	Bad 2048 point pipelines
0	0 and 2
1	1 and 3
2	0 and 2
3	1 and 3

If all four pipelines are bad for a 2048 point FFT, where there was but a single bad pipeline for the 512 point FFT, then ASIC 0, 1, 2, or 3 is bad. The bad ASIC usually can be determined, or confirmed, by testing it in a MAC card. The above test could be performed in the FFT Test Fixture, or in the system.

ASIC failures in FFT cards should be rare, since the new batch of ASICs have been placed in the FFT cards. This is because it is easier to determine the bad ASIC in the MAC cards. There are a few FFT cards left with the old ASICs. Do not mix the old and new ASICs on a card. The date codes on the old ASICs have 90 or 91 as the year. The new ASICs have 95 as the year in the date code.

In the above opsSystest results, channel 1 shows a single bad baseline. This is probably a bad ASIC in a MAC card. The most common system failure is a failure of an ASIC in a MAC card. The MAC failure appears as a hard error on a single baseline. Sometimes a MAC ASIC will begin as an intermittent error, and later become a hard error.

To determine which ASIC on which MAC card to replace, refer to the drawing BSLNMAP.AR0 for channels 0, 2, 4, or 6. Refer to BSLNMAP.AR1 for

channels 1, 3, 5, or 7. (These drawings are sheets in VLBACORR.BLK) Circle the corresponding baseline on the appropriate map. The map tells you the MAC card number and the ASIC U number. MAC channels 0 and 1 are in rack 0. MAC channels 2 and 3 are in rack 1. MAC channels 4 and 5 are in rack 2. MAC channels 6 and 7 are in rack 3.

Channels 4 and 5 show identical FFT pipeline errors. On the FFT card, pairs of pipelines (0 and 1, or 2 and 3) are multiplexed together. The combined signals go via slip on cables to the MAC cards. The pair of bad pipelines could indicate a bad cable, a bad FFT card transmitter, or a bad MAC card receiver. Cables slipping off had been a chronic problem. The cables have been replaced with higher insertion force cables, which should help.

```
SECOND SECTION OPSSYSTEST RESULTS
Channel = 1,specpnt = 1,bl = 3,Real ref = 0.000090 38BD3000,error = -
0.000878 BA661A80
Channel = 1,specpnt = 1,bl = 3,Imag ref = 0.000803 3A529B80,error =
0.000803 3A529400
Channel = 1,specpnt = 3,bl = 3,Real ref = 0.000059 3876D000,error = -
0.000967 BA7D8200
Channel = 1,specpnt = 3,bl = 3,Imag ref = 0.000752 3A451E00,error =
0.000752 3A452580
Channel = 1,specpnt = 5,bl = 3,Real ref = -0.000217 B9636400,error = -
0.000967 BA7D7080

1997AUG27 16h18m32.18s
lta_current_config= 2, model nr=2, bit to trk=1-2, pgena=1
manyparms(3) compare test (0-9/10-19). fftsize=256, oversamp=1,
overlap=2
Validity errors for 7 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
Mac polar data errors, chans 0-7 are:
   273     196       0       0     259     259       0       0

           CHAN 0            7 LOOPS       CHAN 1   Config=2
    1111 1111 11                    1111 1111 11
    9876 5432 1098 7654 3210        9876 5432 1098 7654 3210
    ---- ---- ---- ---- ----        ---- ---- ---- ---- ----
 0  7777 7777 7777 7777 7777     0  7777 7777 7 77 7777 777
 1            7                  1
 2            7                  2
 3__          7         ___      3__                    ___
 4            7                  4
 5            7                  5
 6            7                  6
 7__          7    ___ ____      7__                ___ ____
 8            7                  8
 9            7                  9
10  7777 7777 77                 10  7777 7777 77
11__          ___ ____ ____      11__           ___ ____ ____
12                               12
13                               13
14                               14
15__      ___ ____ ____ ____     15__      ___ ____ ____ ____
16                               16
17                               17
```

```
18                                        18
19__ ___ ____ ____ ____ ____              19__ ___ ____ ____ ____ ____
          CHAN 4                 7 LOOPS          CHAN 5   Config=2
    1111 1111 11                              1111 1111 11
    9876 5432 1098 7654 3210                  9876 5432 1098 7654 3210
    ---- ---- ---- ---- ----                  ---- ---- ---- ---- ----
 0  7777 7777 7 77 7777 777                0  7777 7777 7 77 7777 777
 1             7                          1             7
 2             7                          2             7
 3__           7         ___              3__           7         ___
 4             7                          4             7
 5             7                          5             7
 6             7                          6             7
 7__           7    ___ ____              7__           7    ___ ____
 8             7                          8             7
 9             7                          9             7
10  7777 7777 77                          10  7777 7777 77
11__          ___ ____ ____               11__          ___ ____ ____
12                                        12
13                                        13
14                                        14
15__      ___ ____ ____ ____              15__      ___ ____ ____ ____
16                                        16
17                                        17
18                                        18
19__ ___ ____ ____ ____ ____              19__ ___ ____ ____ ____ ____
```

Here, we see the pattern which the same faults cause with dosystest 3. MAC Polar mode is also turned on.

The initial printed errors are due to the bad MAC ASIC in channel 1. The baseline referred to by bl (baseline) = 3, can be seen by referring to the chart BSLNMAP.DEC. This baseline corresponds to the bad ASIC previously identified. The specific spectral points failing in the ASIC can be seen.

The pattern for the bad FFT ASIC in channel 0, FFT 10 has spread out. Both FFT 10 and FFT 0 are shown, due to the ambiguities of the compare test. Also the pattern has partially spilled over to channel 1, due to MAC Polar being turned on. This is due to the MAC card multiplying the two pipelines together to get cross polarizations. This pattern has obscured the bad MAC ASIC.

The bad cable problem of Channel 4 and 5, FFT 0, has also grown due to the ambiguities of the compare test.

Sometimes errors will show up in compare test that don't show up in the snapshot test, since more of the system is activated.

Note the 7's in the error display corresponds to the indicated 7 loops. This indicates hard errors.

```
THIRD SECTION OPSSYSTEST RESULTS
Channel = 1,specpnt = 0,bl = 3,Real ref = 0.000079 38A55400,error = -
0.000196 B94DF600
Channel = 1,specpnt = 0,bl = 3,Imag ref = 0.000406 39D50A00,error =
0.000406 39D50400
```

```
Channel = 1,specpnt = 1,bl = 3,Real ref = 0.000276 3990CD00,error = -
0.000305 B99FC400
Channel = 1,specpnt = 1,bl = 3,Imag ref = 0.000625 3A23F100,error =
0.000625 3A23F700

1997AUG27 16h22m12.78s
lta_current_config= 3, model nr=3, bit to trk=1-2, pgena=0
manyparms(4) compare test (0-9/19-10). fftsize=512, oversamp=2,
overlap=2
Validity errors for 7 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
Mac nonpolar data errors, chans 0-7 are:
   273       7       0       0     259     259       0       0

           CHAN 0            7 LOOPS       CHAN 1   Config=3
    1111 1111 11                    1111 1111 11
    9876 5432 1098 7654 3210        9876 5432 1098 7654 3210
    ---- ---- ---- ---- ----        ---- ---- ---- ---- ----
 0             77                 0                       7
 1             77                 1
 2             77                 2
 3__           77         ___     3__                     ___
 4             77                 4
 5             77                 5
 6             77                 6
 7__           77    ___ ____     7__               ___ ____
 8             77                 8
 9  7777 7777 777                 9
10  7777 7777 77                 10
11__           ___ ____ ____      11__           ___ ____ ____
12                                12
13                                13
14                                14
15__       ___ ____ ____ ____     15__       ___ ____ ____ ____
16                                16
17                                17
18                                18
19__ ___ ____ ____ ____ ____      19__ ___ ____ ____ ____ ____
           CHAN 4            7 LOOPS       CHAN 5   Config=3
    1111 1111 11                    1111 1111 11
    9876 5432 1098 7654 3210        9876 5432 1098 7654 3210
    ---- ---- ---- ---- ----        ---- ---- ---- ---- ----
 0   777 7777 7777 7777 777      0   777 7777 7777 7777 777
 1  7                            1  7
 2  7                            2  7
 3__7                    ___     3__7                    ___
 4  7                            4  7
 5  7                            5  7
 6  7                            6  7
 7__7               ___ ____     7__7               ___ ____
 8  7                            8  7
 9  7                            9  7
10  7                           10  7
11__7           ___ ____ ____   11__7           ___ ____ ____
12  7                           12  7
13  7                           13  7
14  7                           14  7
```

```
15__7     ___ ____ ____ ____     15__7     ___ ____ ____ ____
16  7                            16  7
17  7                            17  7
18  7                            18  7
19__7___ ____ ____ ____ ____     19__7___ ____ ____ ____ ____
```

Here, in the third part of opsSystest, we are doing dosystest 4, with MAC Polar mode turned off. Recall dosystest4 compares 0-9 to 19-10.

The Channel 0, FFT 10 error shows up as a bad pipeline in 9 and 10. Recall dosystest 3 in the previous section showed bad pipelines in 0 and 10. Since 10 is the common element, it would probably be the actual bad pipeline, as confirmed by the first section.

The Channel 4 & 5 Cable problem now shows up in stations 0 and 19. dosystest 3 had the errors in 0 and 10. 0 is the common element, which corresponds to dosystest 1.

Notice the configuration was 1, 2, and 3 for the 1st, 2nd, and 3rd sections. Since none of the errors shifted pipelines, the errors were not PBI related.

A.7 OPSSYSTEST ERRORS DUE TO PBI FAULTS

In the above example the errors were all FFT or MAC related. The errors in the three parts of opsSystest all pointed to the same stations.

If an error is due to the PBI, the errors will appear to change stations between parts of the test. This is due to the multiplexers at the input to the FFT card being in a different position, for each part of the opsSystest.

The table, shown below, defines which FFT Engines would appear bad, in the three parts of opsSystest, if the PBI were bad for that row. This table is derived from the configuration tables earlier in this document.

	Bad FFT Engines		
opsSystest Section	First	Second	Third
PBI=01	0	-	19
PBI=02	1	0	-
PBI=03	2	1	0
PBI=04	3	2	1
PBI=05	4	3	2
PBI=06	-	4	3
PBI=07	5	-	4
PBI=08	6	5	-
PBI=09	7	6	5
PBI=10	8	7	6
PBI=11	9	8	7
PBI=12	-	9	8
PBI=13	10	-	9
PBI=14	11	10	-

PBI=15	12	11	10
PBI=16	13	12	11
PBI=17	14	13	12
PBI=18	-	14	13
PBI=19	15	-	14
PBI=20	16	15	-
PBI=21	17	16	15
PBI=22	18	17	16
PBI=23	19	18	17
PBI=24	-	19	18

A.8 EXAMPLES OF PLAYBACK INTERFACE (PBI) FAULTS

Refer to the above chart. If PBI 3 were bad, the first third of opsSystest would show errors for station 2. The second third would show errors for station 1. The third third would show errors for station 0.

If PBI 1 were bad, the first third of opsSystest would show errors for station 0. The second third would not show any errors, as indicated by the -. The third third would show errors for station 19. Since there are 20 stations, and 24 PBIs, each configuration has four PBIs which are not used.

Below is a sample ops.123 result. PBI faults typically occur to channels 0-3, channels 4-7, or channels 0-7. We would expect the channels to be consistent for all three sections of opsSystest. PBI faults look similar to FFT faults in that they affect entire pipelines. We still get the compare ambiguity for the second and third parts of the test. Below, the first part is error free and the second part has errors showing for 4 and 14. Looking at the above table, we see this can correspond to PBI 6 for - 4, or to PBI 18, for - 14. The third part of the test has errors for the same four channels in 3 and 16. In the above table, - 4 3 corresponds to PBI 6 bad. There is no entry for - 4 16, - 14 3, or - 14 16. Thus, PBI 6 is unambiguously bad. The operator action would be to flag Tape Drive 6 bad in the EQUIPSTAT screen, and to continue operation.

```
1997SEP04 14h14m55.33s
lta_current_config= 1, model nr=0, bit to trk=1-4, pgena=0
dosystest(1) (snapshot test), fftsize=512, oversamp=1, overlap=1
Validity errors for 18 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
Mac nonpolar data errors, chans 0-7 are:
     0       0       0       0       0       0       0       0
No data errors present.
------------------------------------------------------------------------
1997SEP04 14h18m37.57s
lta_current_config= 2, model nr=2, bit to trk=1-2, pgena=1
manyparms(3) compare test (0-9/10-19). fftsize=256, oversamp=1,
overlap=2
Validity errors for 7 loops, chans 0-7 are:
     0       0       0       0       0       0       0       0
Mac polar data errors, chans 0-7 are:
     0       0       0       0     273     273     273     273
```

A.9 OPSSYSTEST ADVANCED FEATURES

Typing linger during a portion of opsSystest, will cause the test to stay in that portion. That is useful for testing cables or checking low duty cycle errors. Also while the test is running, manyparms 3 or 4 can be used to switch type of compare test. The configuration could also be changed while the test is running. Changing configuration can be accomplished manually by typing a new value into the CONFIG field of the R0 screen. Typing resumesystest restarts the normal test sequence.

Typing killsystest will abort the test in the middle. There is some delay until it actually aborts.

If opsSystest is called with an argument of 0, the test will proceed through all three sections automatically. This is the way it is normally called by the operations staff. An argument value of 0 is the default if nothing is entered.

If opsSystest is called with an argument of 1, 2, or 3, the test will come up in the first, second, or third section, in linger mode.

For dosystest 1, if a new snapshot is desired, first invoke dosystest 1. While the test is synchronized and running invoke the function:

```
firsnap(bsln,subarray,filename)
```

Use a bsln of 0, and a subarray of 0. Currently, the filenames used are "firsystestref.56" for MAC nonpolar, and "firsystestrefpolar.56" for MAC polar.

A.10 TROUBLESHOOTING TIPS

Intermittent errors one FFT cycle wide can be due to fstc problems. Set zerodlys=1 can be used to turn off the fractional sample time correction (fstc). Setting zerofr=1 can be used to zero the fringe rotator. These changes occur next time the active model changes. systest automatically rotates through the four model banks, 0 through 3, changing about every 5 minutes.

FSTC errors were eliminated by modifying the FFT Cards to buffer the FSSRCLK. This involved adding a piggyback chip. Racks 0 and 1 only have an added FSTC buffer board, buffering the FSTC data and clocks. Since this did not prove effective, it was never done to Racks 2 and 3.

A useful technique is to compare FFT card outputs using an oscilloscope set to add two signals with one inverted. A good signal to use is Pin 25 on the logic analyzer port of an FFT card. This provides DT.T0, the lsb of the multiplexed output of pipelines 0 and 1. For dosystest(1), the snapshot test, any card can be compared to any other. For the dosystest(3) compare test, card x is compared to card x+10, where x<10. For dosystest(4), card x is compared to card 19-x. For dosystest(3) or dosystest(4), compare within the same grouping of four channels. For dosystest(5), compare card x of channels 0-3, to card x of channels 4-7.

The scope display gives a feel if the errors are an occasional bit wrong. Errors that are a whole FFT cycle of 16 usec bad, are probably due to FSTC problems. Errors 4 ms. wide could be due to Fringe Rotator problems. The PBI could also cause errors 4 ms. or 16 usec wide. Or, maybe, the pattern will show a total wipeout. The oscilloscope could also show if the output of one FFT card is zero. The pulsar gate should show the data zeroed when the gate is enabled and in effect. Validities also can zero the data. The validities and pulsar gate signals going into the FFT cards can be probed on the backplane.

The FFT Card logic analyzer port also provides the lsb of each fstc and fringe rotator number controlled oscillator (nco). Doing similar oscilloscope compare tests with these can pinpoint fstc or fringe rotator problems.

If an entire screen (R0, R1, R2, or R3) is bad, suspect a problem with the FCC or MCC. Sometimes, an MCC will get in a bad state. Rebooting and reloading the software might cure the MCC. If that doesn't work, try cycling power on the rack, then commanding: ldracks racknr,1,63.

A four by four square of baseline errors indicates a bad MAC card. This would be a triangle, for a partially populated MAC card on the self product diagonal. A bad row or column in a MAC card would show up as a row or column of four baseline errors. Each MAC card has two channels worth of baselines, referred to as array 0 and 1.

Note fully populated MAC cards can be temporarily substituted for partially populated cards.

Screen R4 shows the status of the PBI servos. For the systest functions, the test frames produced in the MCCs provide simulated tape data frames, under control of phase locked loops local to the test frame generator on each MCC. These test frames are routed into the TRCs. Test software in the VME system uses the calculated offset values produced by the deformatters, which are normally needed for servo control to the tape drives. These values are used in the VME to correct the MCC test frame rates, under control of the phase locked loop. The bar graphs should be going up and down, without hitting the limits.

If a single ASIC shows up in a self product, in a compare test, this could be due to a validity problem, instead of a bad MAC ASIC. Suspect this if changing the ASIC does not fix the problem. Refer to the four data invalid signals going to the four FFT pipelines on the FFT card. These zero the FFT card output. The errors only show up in self products since zero times a non-zero, erroneous output still gives zero out. But the non-zero self product gives a different answer. The validity problem can be verified by doing the scope add/invert difference and seeing the errors corresponding to the validity signals. Also, the validity checking can be turned on and off, on a FFT card basis, to see the effect go away. To turn off validity checking, set the global variable gldatavalid=0. Then use dofftctrl(bus,card) to selectively turn off validity checking. For example, if we are doing dosystest 3, and we see self product 0, channel 3 bad. If we set gldatavalid=0, then dofftctrl 0,0 , we should see all 4 channels bl 0 go bad. Then if we do dofftctrl 2,0, to turn off the checking for card 10, we should see all errors go away. This assumes the error is due to invalid not being correctly applied on the FFT card. The Invalid signal comes from

the MCC, where each rack supplies two channels. An FFT to MAC cable not being seated properly has caused similar problems.

MAC polar mode can be turned on by setting the global glmacpolar=1, then starting dosystest 1,3,4,or 5. dosystest 1 uses a separate snapshot. During dosystest 3, 4, or 5, MAC polar mode can be toggled while the test is running by using the functions macpolar() and macnonpolar(). Similarly, dosystest 3 or 4 can be toggled real-time by using the function manyparms(3) or manyparms(4). These changes produce momentary glitches in the data, which can then be cleared, using the CLEAR field in screen R3. There have been ASICs that only fail in MAC polar mode.

Note during MAC polar mode, a FFT pipeline failure might be reported for 2 adjacent pipelines, since the pipelines are distributed to the MAC chips of two arrays. This shows up as errors in two adjacent channels (0 and 1, 2 and 3, 4 and 5, or 6 and 7) in systest.

When a cross product MAC chip fails, the spectral points affected are reported, in dosystest 3 or 4.
Example:

```
Channel = 1,specpnt = 1,bl = 3,Real ref = 0.000090 38BD3000,
      error = -0.000878 BA661A80

Channel = 1,specpnt = 1,bl = 3,Imag ref = 0.000803 3A529B80,
      error = 0.000803 3A529400
```

The global macverbose counts how many spectral point errors are reported. The limit can be reinitialized by setting macverbose=0. A baseline can be specified to be not reported, if there is a second baseline of interest, being overwhelmed by error reports from the first baseline. To blank the uninteresting baseline set glblankbl=baseline number.

The function dsplylta_tofile (0,4) can be used to write the systest results to the file dsplylta.map.config.x, where x=0,1,2, or 3 for the corresponding configuration.

Errors in single or multiple FFT pipelines in an FFT card could be caused by a bad control word load to the FFT card. dofftctrl(bus,card) reloads default FFT card control word for a 512 point FFT. Bus is the rack number (0-3). Card is 0 to 9. dofftctrl can be used during a systest. It may cause momentary errors, which can be cleared using the clear field in screen R3. The system does not check the control words being shifted out of the FFT card. However, the FFT Test Fixture does check the control words being shifted out.

Similarly, there could be bad RAM contents in the FFT card. dofftram(bus,card) reloads default FFT card RAM contents and control words.

An error in all 8 channels of the same station is probably due to the deformatter card. This can be verified by seeing if the errors move with configuration. The deformatter could affect only 4 channels which would look similar to FFT card errors. However the deformatter errors would move with configuration.

The cables from the tape drives to the VLBA Correlator can be checked by setting kill_loopback=0, and then running the normal dosystest functions.

If there are errors, try calling clrLBErrors a few times to see if they go away. If they go away, don't worry about them. Errors can be localized to specific tracks by viewing the deformatter microprocessor HD screens.

A total wipeout is hard errors in all baselines. A total wipeout of the dosystest 1 snapshot test, but not for the compare tests, indicates something in the entire system has changed to make the snapshot no longer valid.

If there is a total wipeout in the compare tests as well as the snapshot test, first try rebooting and see if that fixes things. Next, determine if the LTA/FIR combination is good. This can be ascertained by executing, hcbTestLtaFir 15, for a 15 baseline check. hcbTestLtaFir can also be used in the LTA test fixture, or testbed, if <ldlf.cmd is executed first.

dosystest(2) can be used to see if the path is good through the LTA. Run dosystest(1) first to set things up correctly.

Test C, from the FIR console, can be used to see if the data is getting into the FIR. Test C prints whatever LTA baseline is in FIR microprocessor location 7000. To invoke Test C, first modify location 7000 with the command:

M7000 baseline

Baseline is the desired LTA baseline. Next invoke Test C, with the command TC. The baselines will print out on the FIR console. Keep in mind that the FIR baselines do necessarily not correspond to the LTA baselines.

A stand alone test of the FIR can be performed by doing <ldlf.cmd, then firRun(0,3) on the RTS. The output should read:

```
Baselines 0-2, 4 results each
    1.550000e+02  43  1B  00  00          1.550000e+03  44  C1  C0  00
    1.630000e+02  43  23  00  00          1.630000e+03  44  CB  C0  00
    1.710000e+02  43  2B  00  00          1.710000e+03  44  D5  C0  00
    1.790000e+02  43  33  00  00          1.790000e+03  44  DF  C0  00
    1.560000e+02  43  1C  00  00          1.560000e+03  44  C3  00  00
    1.640000e+02  43  24  00  00          1.640000e+03  44  CD  00  00
    1.720000e+02  43  2C  00  00          1.720000e+03  44  D7  00  00
    1.800000e+02  43  34  00  00          1.800000e+03  44  E1  00  00
    1.570000e+02  43  1D  00  00          1.570000e+03  44  C4  40  00
    1.650000e+02  43  25  00  00          1.650000e+03  44  CE  40  00
    1.730000e+02  43  2D  00  00          1.730000e+03  44  D8  40  00
    1.810000e+02  43  35  00  00          1.810000e+03  44  E2  40  00
```

A.11 MONITOR CARD TIPS

Detailed monitor card documentation can be found in vlbsoft/monasm/mon.doc.

The terminal for the monitor card provides useful information. Typing TS brings up a display of the rack voltages, currents, and temperatures. A

voltage that is lower or higher than nominal can be adjusted on the individual power supply. Voltages that jump around excessively could indicate excessive ripple in the power supply. This can be verified by looking at the power supply output, at the power supply, with an oscilloscope. The cure is to swap out the power supply, and replace its filter capacitors. There are spare filter capacitors in the cabinet.

High temperatures can mean that one of the Contempo units in back of the correlator is not turned on. After a power glitch, usually only one of the two will come back online. High temperatures could also indicate one or both of the chillers downstairs are down. The monitor card will shut off the correlator at 28 degrees C.

The monitor card will power down the correlator if voltages or temperatures are out of range. If the monitor card powers down the correlator, the TS screen will freeze at the values at power down.

The automatic power down ability of the monitor card microprocessor can be inhibited on a rack by rack basis. The lower, right hand push button switch, on the Rack 3 front panel, labeled (RACK) DISABLE, is the automatic power down disable switch. To use this function, push a rack 0, 1, 2, or 3 switch and then press the disable switch (the rack select switch must be pushed first, if it is not, the rack displayed on the front panel LEDs when the disable switch is pressed will also have its automatic power down function disabled). After the procedure above, the rack selected is excluded from the dangerous limit scan and an out of limit measurement in this rack will not cause the system to power down. Any combination of racks can be excluded from the automatic power down ability of the microprocessor.

One use of the automatic power down inhibit feature above is to change a card. If a bad card is discovered during operation, the card may be changed without powering down the entire system. The rack that the bad card is in can be excluded from the automatic power down scan as above, the rack in question can then be powered down (using the AC breakers in the back of the rack) and the card changed with power to the one rack off. After the card change, the rack can be brought back on line with the AC breaker.

Execute ldracks(racknr, number of racks, 63) for all DEFs. This reloads the repowered rack.

In order to restore normal operation, i.e. the automatic power down function enabled for all racks, press the upper right hand ENABLE switch. This switch enables all racks for automatic power down. Systest will also enable automatic power down for all racks.

The red AIRFLOW and WATCHDOG LED's on the front panel are hardware driven. Their lighting can indicate the shutting down of the correlator. The AIRFLOW light indicates a lack of airflow from the Contempos. The airflow pressure sensor is in Rack 3. The WATCHDOG LED lights if the Monitor Card Microprocessor goes brain dead.

APPENDIX B *Documentation Conventions*

The file naming convention is as follows:

txxxfyy.ext

t= drawing type identifier (per VLBA memo #364), coded as follows:

- A= assembly
- B= bill of materials
- D= documents or data (firmware)
- F= fixtures, jigs or templates
- I= silkscreen
- K= block diagram
- L= logic
- M= mechanical
- N= specification
- P= printed circuit, mechanical
- Q= printed circuit, artwork
- S= schematic
- V= logic timing diagram
- W= wiring list or diagram
- Z= sketch

xxx= a 3 digit number obtained from the master drawing log book

f= a single letter identifying the file type, coded as follows:

- A= AutoCAD
- D= ORCAD ("Draft")
- G= Generic Cad
- L= Lotus (spreadsheet)
- T= Text (plain text editor file)
- W= Word Perfect document
- X= Xilinx

yy= a 2 digit sequential number, starts at 01 for the first related file, an increments for additional related files

ext= user defined, typically is .sch, .txt, .abl etc.

e.g. l024d01.sch is a logic, drawing number 024, ORCAD, sheet 1
l024d02.sch is the second sheet of the same drawing

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APPENDIX C *VME 6159 Wire Wrap Prototyping Module*

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APPENDIX D *MC68230 Parallel Interface/Timer IC*

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APPENDIX E *Acronyms*

ASIC	Application Specific Integrated Circuit
BBC	Base Band Converter
BCD	Binary Coded Decimal
CAD	Computer Aided Drafting
CCC	Correlator Control Computer
CLB	Configurable Logic Block
CLCC	Ceramic Leadless Chip Carrier
CPU	Central Processing Unit
CRC	Cyclic Redundancy Code
CRCC	Cyclic Redundancy Code Character
DAT	Digital Audio Tape
DIP	Dual In line Package
DIT	Decimation in Time
DMA	Direct Memory Access
DPC	Data Playback Chip
ECL	Emitter Coupled Logic
EPROM	Erasable Programmable Read Only Memory
FCC	FFT Control Card
FIR	Finite Impulse Response
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSTC	Fractional Sample Time Correction
FX	FFT, Cross Multiplication
GAL	Generic Array Logic
HCB	Hardware Communications Bus, Hardware Control Bus
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
IF	Intermediate Frequency
IOB	Input Output Block
JEDEC	Joint Electronic Device Engineering Council
LCA	Logic Cell Array
LCP	Left Circular Polarization
LSB	Least Significant Bit
LSI	Large Scale Integration
LTA	Long Term Accumulator
MAC	Multiplier Accumulator Card
MCB	Monitor & Control Bus
MCC	MAC Control Card
MJD	Modified Julian Date
MSB	Most Significant Bit
MVME	Motorola Versa Module Eurocard
NCO	Numerically Controlled Oscillator
NWO	New World Order
OVLBI	Orbiting Very Long Baseline Interferometry
PAL	Programmable Array Logic
PBD	Play Back Drive
PBI	Play Back Interface
PGA	Programmable Gate Array or Pin Grid Array
PLCC	Plastic Leadless Chip Carrier
PLD	Programmable Logic Device
PROM	Programmable Read Only Memory
RAM	Random Access Memory

RCP	Right Circular Polarization
RF	Radio Frequency
ROM	Read Only Memory
RTS	Real Time System
SCCS	Source Code Control System
SCSI	Small Computer System Interface
SIP	Single In line Package
TRC	Track Recovery Card
TTL	Transistor Transistor Logic
VLA	Very Large Array
VLBI	Very Long Baseline Interferometry
VLBA	Very Long Baseline Array
VLSI	Very Large Scale Integration
VME	Versa Module Eurocard
VSOP	VLBI Space Observatory Program

APPENDIX F *HCB Schematic Drawings*