US/GR BK/VLBA/

VLBA Technical Report No. 43

THE VLBA CORRELATOR

PLAYBACK INTERFACE SUB-SYSTEM

VOLUME 2 of 2

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PLAYBACK INTERFACE SUB-SYSTEM

VOLUME 2 of 2

Chuck Broadwell

Ray Escoffier

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January 1, 1998

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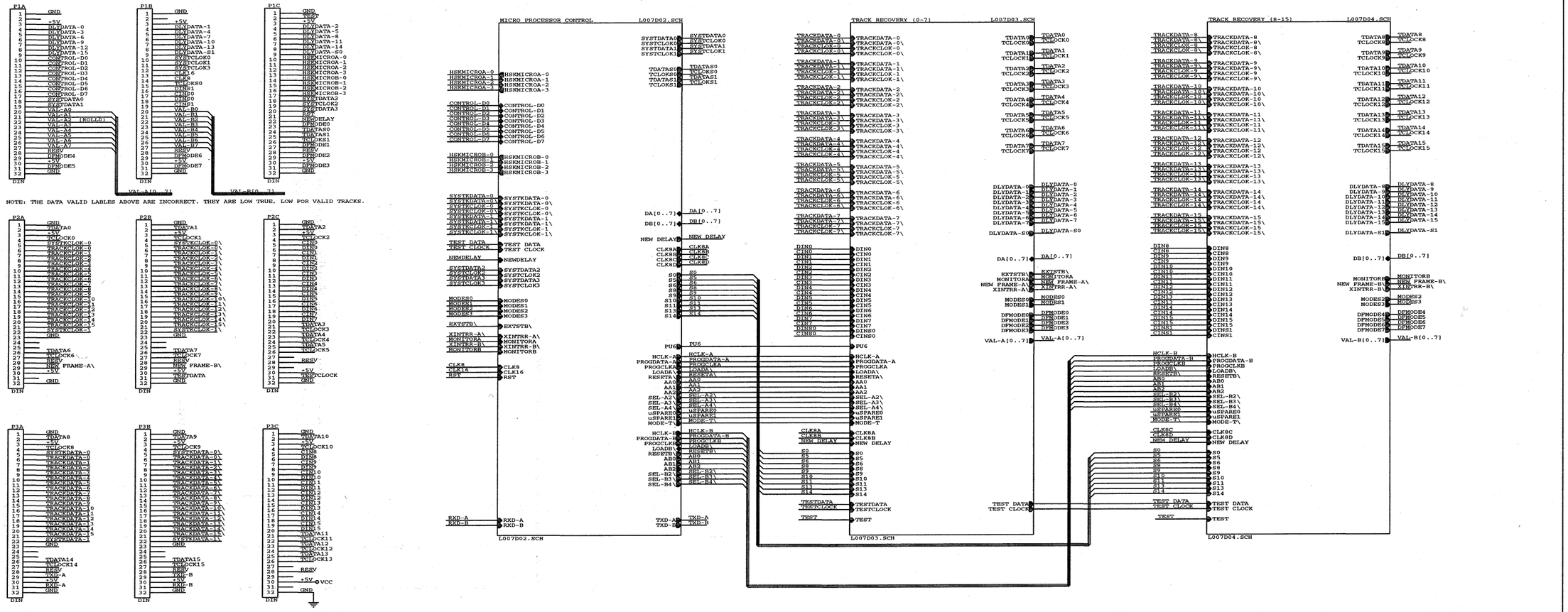
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Volume 2 Section 1

Track Recovery Card Drawings

Drawing Number and/or Filename	Title	Nr of Sheets
56000L007 (L007D01.SCH - L007D04.SCH)	Track Recovery Card Schematics	4
56000Z007 (Z007D01.LAY - Z007D02.LAY)	Track Recovery Card IC Layout	2
(PAL_U29.SCH)	Track Mix, Inputs 12-15	1
(PAL_U33.SCH)	Track Mix, Inputs 4-7	1
(PAL_U35.SCH)	Track Mix, Inputs 0-3 and 8-11	1
(PAL_U36.SCH)	Track Mix, System Tracks	1
56000K008 (K008D01.BLK - K008D10.BLK)	(This is the DPC Xilinx) Track Recovery Xilinx Design	10
56000K009 (K009D01.BLK - K009D10.BLK)	Delay Control Xilinx Design	10
56000K010 (K010D01.BLK - K010D09.BLK)	Header Control Xilinx Design	9
(WRITE.DPC)	Write Operations Into Trk Buf	1



REV. A	8\22\90	ADD PIN/PAGE NUMBERS TO I/O CONNECTIONS CHANGE U72 AND U73 TO 8K X 8 ROMS CHANGE CHIP TYPES TO ALS
REV. B	7\06\92	INVERT NEW FRAME LABLE CHANGE 2950 PART NUMBER ADD PARITY TEST POINT NOTE CHANGE U66 TO 74HC541

VLBA CORRELATOR PROJECT

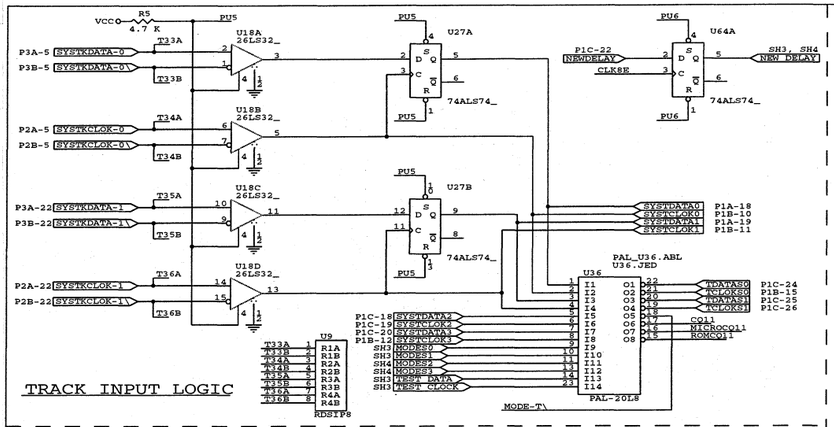
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA.

Title: TRACK RECOVERY CARD

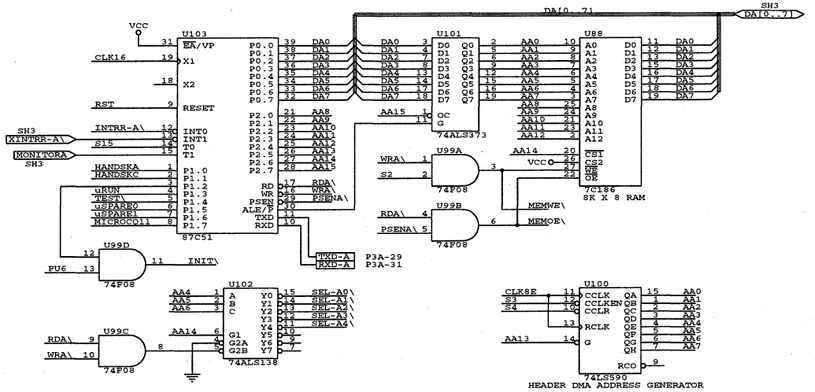
Size	Document Number	REV
D	56000L007 (L007D01.SCH)	B

Date: December 19, 1996 Sheet 1 of 4

TRACK INPUT LOGIC



MICROPROCESSOR A



NOTE: THE SIGNAL MICROCQ11 SELECTS BETWEEN TWO RANKS IN THE FRAME SEQUENCER ROM U72/U73. THE FUNCTION THUS PROVIDED IS TO SWITCH BETWEEN MKIII (MICROCQ11 LOW) AND VLBA (MICROCQ11 HIGH) TAPE FORMATS.

SELECT	FUNCTION
SEL-A0	READ 68000 I/O PORT
SEL-A1	WRITE TO 68000 PORT
SEL-A2	READ/WRITE TO DELAY CONTROL XILINX CHIP
SEL-A3	WRITE TO HEADER CONTROL XILINX CHIP
SEL-A4	WRITE TRACK ENABLE SIGNALS
SEL-A5	
SEL-A6	
SEL-A7	

SPARE SIGNAL UTILIZATION

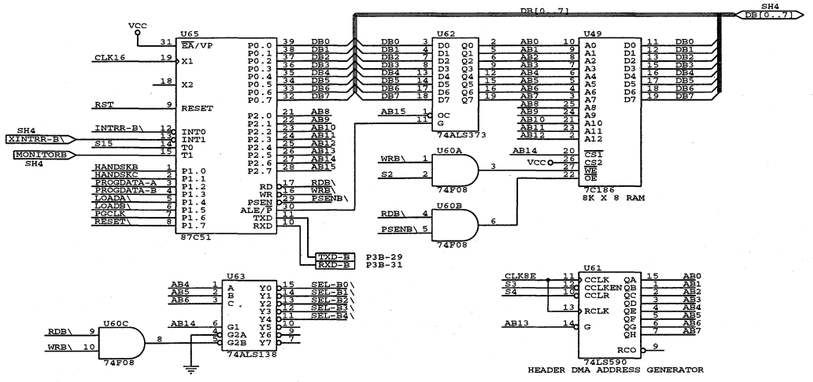
SIGNAL	FUNCTION
SPARE0	= 1, DEMOD ACTIVE
SPARE1	= 0, MKIII = 1, VLBA
MICROCQ11	= 0, MKIII = 1, VLBA

MONITOR CODE BITS

DATA BUS	FUNCTION
00	READ RECEIVE SYNC FLAG
04	READ SYNC ERROR FLAG
08	
0C	

AA15	AA14	AA13	FUNCTION
1	0	0	DMA CYCLE
0	0	1	uPROC EXTERNAL MEMORY CYCLE
0	1	1	uPROC I/O CYCLE

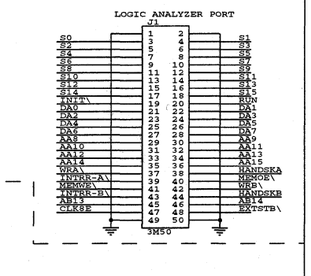
MICROPROCESSOR B



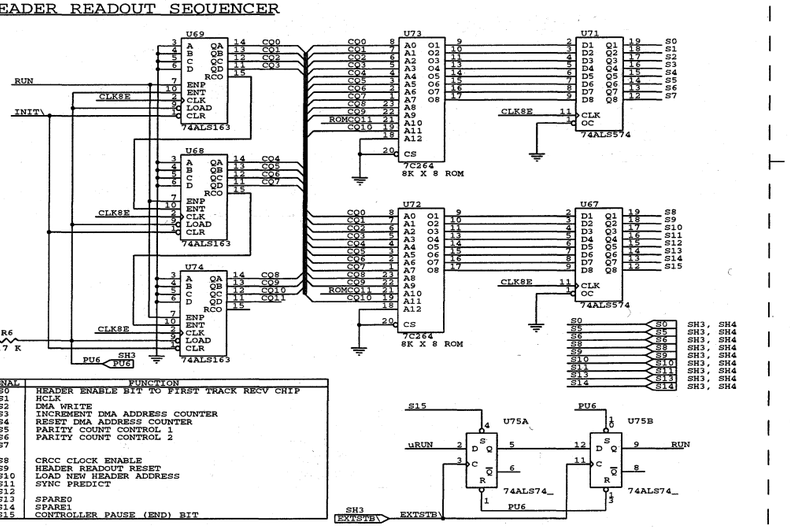
MEMORY MAP

MEMORY LOCATION	FUNCTION
0000 TO 0FFF	INTERNAL ROM MEMORY
2000 TO 3FFF	EXTERNAL RAM MEMORY
6000	READ 68000 I/O PORT
6010	WRITE TO 68000 I/O PORT
6020	WRITE INITIAL DELAY
6021	WRITE HEADER SKIP ADDRESS
6022	WRITE HEADER START ADDRESS
6023	WRITE TRACK MIX PROGRAM BITS
6024	READ MONITOR DATA
6025	RESET SYNC DETECT INTERRUPT
6026	RESET NEW FRAME INTERRUPT
6027	RESET NEW DELAY INTERRUPT
6030	WRITE HEADER START ADDR/CALCULATED NEXT SYNC ADDR
6031	WRITE DATA VALID FLAGS
6032	WRITE MONITOR CODE BITS
6033	WRITE SERVICE TRACK MIX BITS
6034	WRITE DELAY BITS
6040	STORE TRACK ENABLE SIGNALS

LOGIC ANALYZER PORT

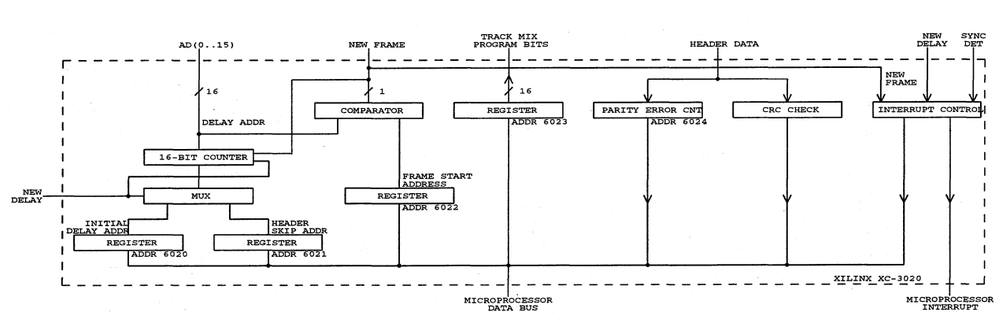


HEADER READOUT SEQUENCER

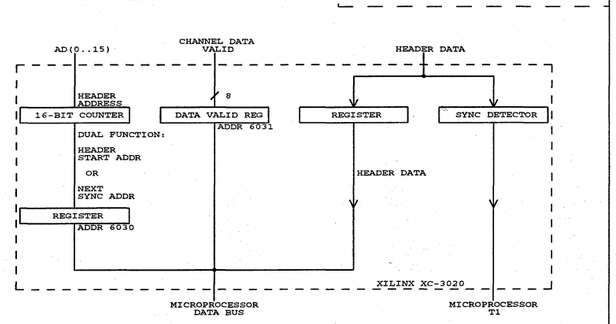


SIGNAL	FUNCTION
S0	HEADER ENABLE BIT TO FIRST TRACK RECV CHIP
S1	HCLK
S2	DMA WRITE
S3	INCREMENT DMA ADDRESS COUNTER
S4	RESET DMA ADDRESS COUNTER
S5	PARITY COUNT CONTROL 1
S6	PARITY COUNT CONTROL 2
S7	
S8	CRCC CLOCK ENABLE
S9	HEADER READOUT RESET
S10	LOAD NEW HEADER ADDRESS
S11	SYNC PREDICT
S12	
S13	SPARE0
S14	SPARE1
S15	CONTROLLER PAUSE (END) BIT

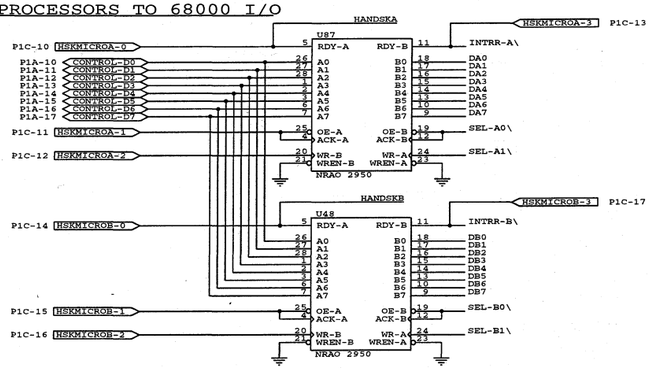
DELAY CONTROL LOGIC BLOCK DIAGRAM



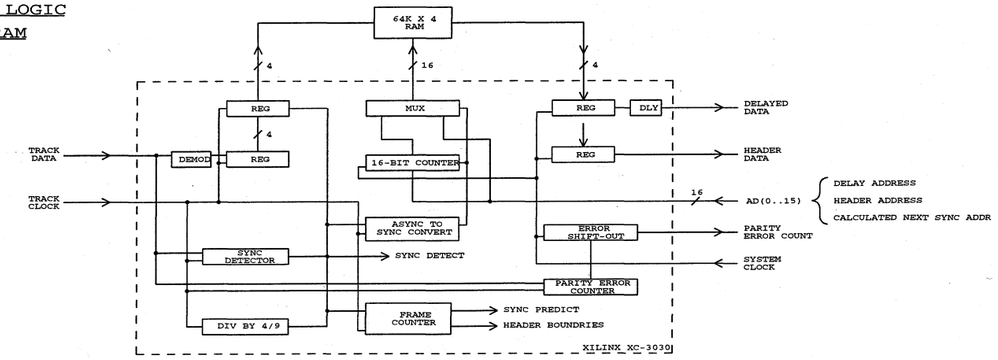
HEADER CONTROL LOGIC BLOCK DIAGRAM



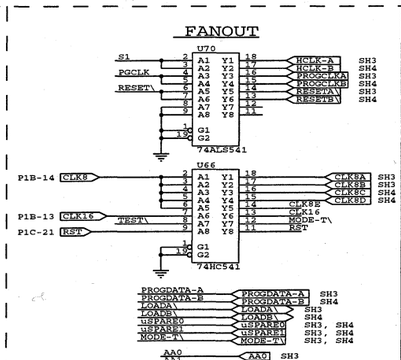
MICROPROCESSORS TO 68000 I/O



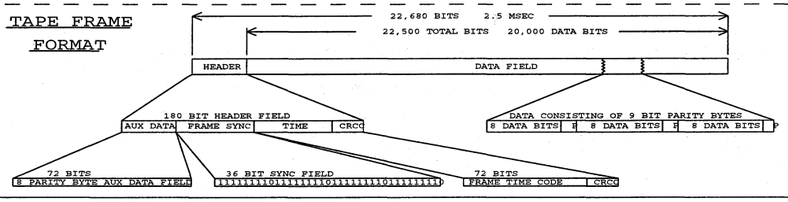
TRACK RECOVERY LOGIC BLOCK DIAGRAM



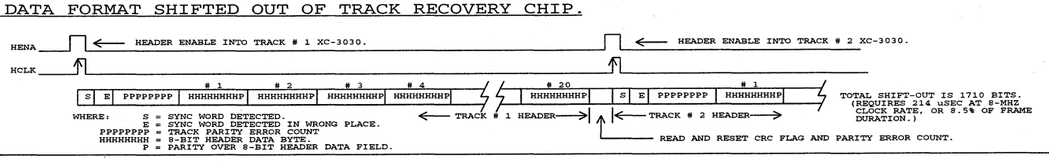
FANOUT



TAPE FRAME FORMAT



HEADER DATA FORMAT SHIFTED OUT OF TRACK RECOVERY CHIP.



WHERE: S = SYNC WORD DETECTED.
E = SYNC WORD DETECTED IN WRONG PLACE.
PPPPPPPP = TRACK PARITY ERROR COUNT
HHHHHHHH = 8-BIT HEADER DATA BYTE.
P = PARITY OVER 8-BIT HEADER DATA FIELD.

TOTAL SHIFT-OUT IS 1710 BITS. (REQUIRES 214 uSEC AT 8-MHZ CLOCK RATE, OR 8.5% OF FRAME DURATION.)

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
TRACK RECOVERY CARD (MICRO PROC CONTROL)

Size	Document Number	REV
D	56000L007 (L007D02.SCH)	B
Date: December 3, 1996	Sheet 2 of 4	

U34 = U35

PAL_U35.ABL
U35.JED

U32 = U33

PAL_U33.ABL
U33.JED

SPARE SIGNAL UTILIZATION

SIGNAL	FUNCTION
SPARE0	= 1, DEMOD ACTIVE
SPARE1	= 0, MKIII = 1, VLBA

NOTE: THE FOLLOWING PINS ON THE TRACK RECOVERY XILINX CHIP ARE TEST POINTS FOR INTERNAL SIGNALS:

P19	DEMOD DATA GENERATOR
P26	SYNCDET TEST POINT
P40	H/D TEST POINT
P49	SYNC PRED TEST POINT
P68	A15 TEST POINT
P28	9 TEST POINT
P14	UN-NRZed TRACK DATA
P38	PARITY ERROR TEST POINT
P50	TCLK TEST POINT

THE DELAY CONTROL XILINX CHIP HAS ONE TEST POINT:
P68 A15 TEST POINT

NOTE: THE SIGNAL PROGDATA IS USED AS A PROGRAM DATA LINE TO PROGRAM THE XILINX CHIP AT POWER-UP. DURING OPERATION, HOWEVER, THIS SIGNAL BECOMES THE SYNCMODE SIGNAL WHICH TELLS THE CHIP TO SEARCH FOR SYNC DURING THE HEADER ONLY OR ALL THE TIME.

LOGIC ANALYZER PORT

ADA0	1	2	ADA1
ADA2	3	4	ADA3
ADA4	5	6	ADA5
ADA6	7	8	ADA7
ADA8	9	10	ADA9
ADA10	11	12	ADA11
ADA12	13	14	ADA13
ADA14	15	16	ADA15
DLYA0	17	18	HCLK-A
DLYA1	19	20	HEADROUT-A
NEW_A	21	22	SPARE0
NEW DELAY	23	24	SPARE1
NEW FRAMEA	25	26	DIN0
HEADROUT-A	27	28	DIN1
XINTRR-A	29	30	DIN2
SYNCDET-A	31	32	DIN3
MONITORA	33	34	DIN4
DLYDATA-0	35	36	DIN5
DLYDATA-1	37	38	DIN6
DLYDATA-2	39	40	DIN7
DLYDATA-4	41	42	DIN8
DLYDATA-5	43	44	DIN9
DLYDATA-80	45	45	SIL0
CLKSA	47	48	SIL1
	49	50	

JM50

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY		
CHARLOTTESVILLE, VA		
Title	TRACK RECOVERY CARD (0-7)	
Size D	Document Number 560L007 (L007D03.SCH)	REV B
Date: December 3, 1996	Sheet 3 of 4	

U30 = U31 = U34 = U35

U28 = U29

SPARE SIGNAL UTILIZATION

SIGNAL	FUNCTION
SPARE0	= 1, DEMOD ACTIVE
SPARE1	= 0, MK4II = 1, VLBA

DELAY CONTROL

HEADER CONTROL

LOGIC ANALYZER PORT

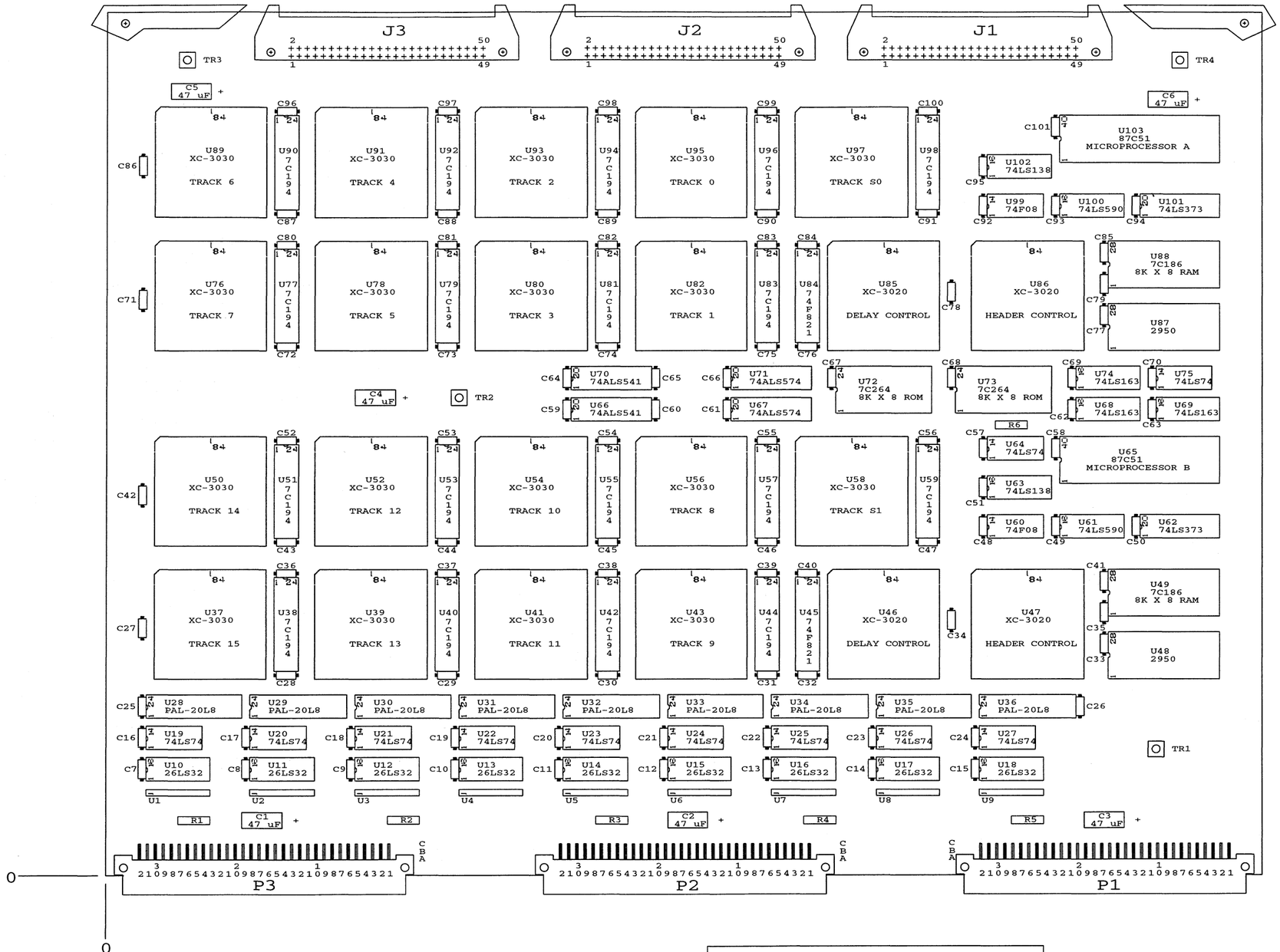
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: TRACK RECOVERY CARD (8-15)

Size	Document Number	REV
D	560001007 (L007D04.SCH)	B

Date: December 3, 1996 Sheet 4 of 4

VIEW IS FROM COMPONENT SIDE



THIS SYMBLE REPRESENTS MOUNTING PAD FOR KEYSTONE TURRET #1593-3 4 REQD. EACH CONNECTS TO GROUND.

DESCRETE RESISTORS:
DESCRETE CERAMIC CAPACITORS
(2 PIN DIPS):

PIN 1 ON RIGHT SIDE

PIN 1 AT TOP

POLORIZED (TATALUM) CAPACITORS - THE + SIGN ON THIS SKETCH INDICATES PIN 1 END OF CAPACITOR.

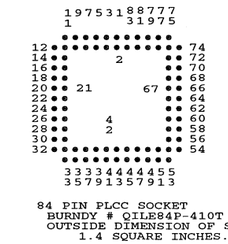
ALL ICs ARE SOCKETED.

ALL DIP ICs USE TEXAS INSTRUMENTS C93XX FAMILY

ALL PLCC ICs USE BURNDY QILE84P-410T OR EQUAL

74LS ICs MAY BE REPLACED WITH 74ALS CHIPS

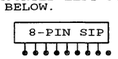
TOP VIEW OF HOLE PATTERN



84 PIN PLCC SOCKET
BURNDY # QILE84P-410T
OUTSIDE DIMENSION OF SOCKET:
1.4 SQUARE INCHES.

9U x 280 mm EUROCARD

NOTE: 8-PIN SIPS U1 THRU U9 HAVE 9-HOLE FOOTPRINTS PROVIDED FOR THEM ON THE CIRCUIT CARDS. THESE DEVICES MUST BE MOUNTED LEFT JUSTIFIED IN THE HOLE PATTERNS AS SEEN BELOW.



SEE NRAO DRAWING # 56000M003 FOR MECHANICAL DETAILS OF CARD.

THIS SKETCH DETAILS THE APPROXIMATE LOCATIONS OF ALL COMPONENTS.

ALL COMPONENTS WILL BE ON GRID UNLESS OTHERWISE NOTED.

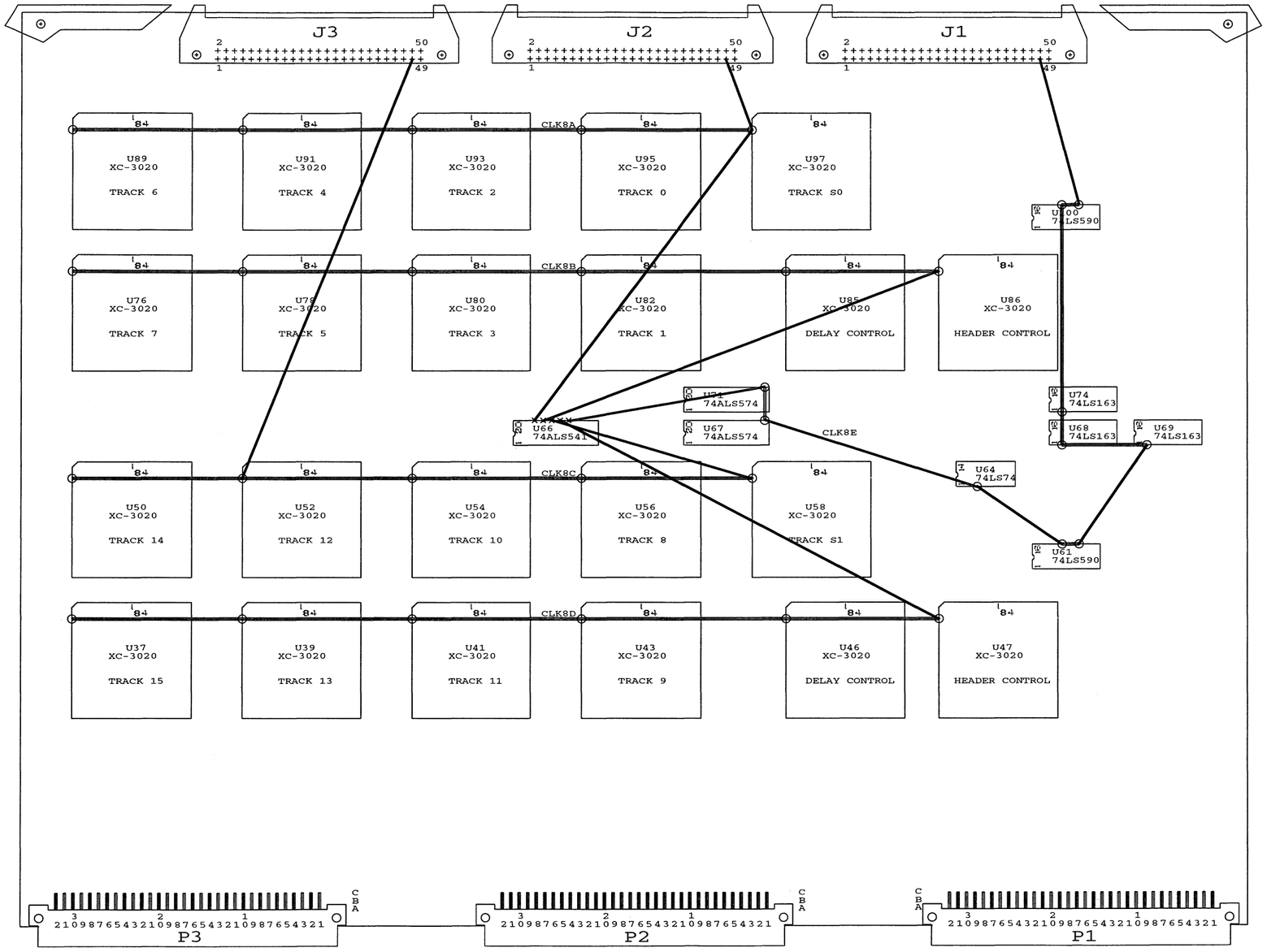
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: TRACK RECOVERY CARD IC LAYOUT

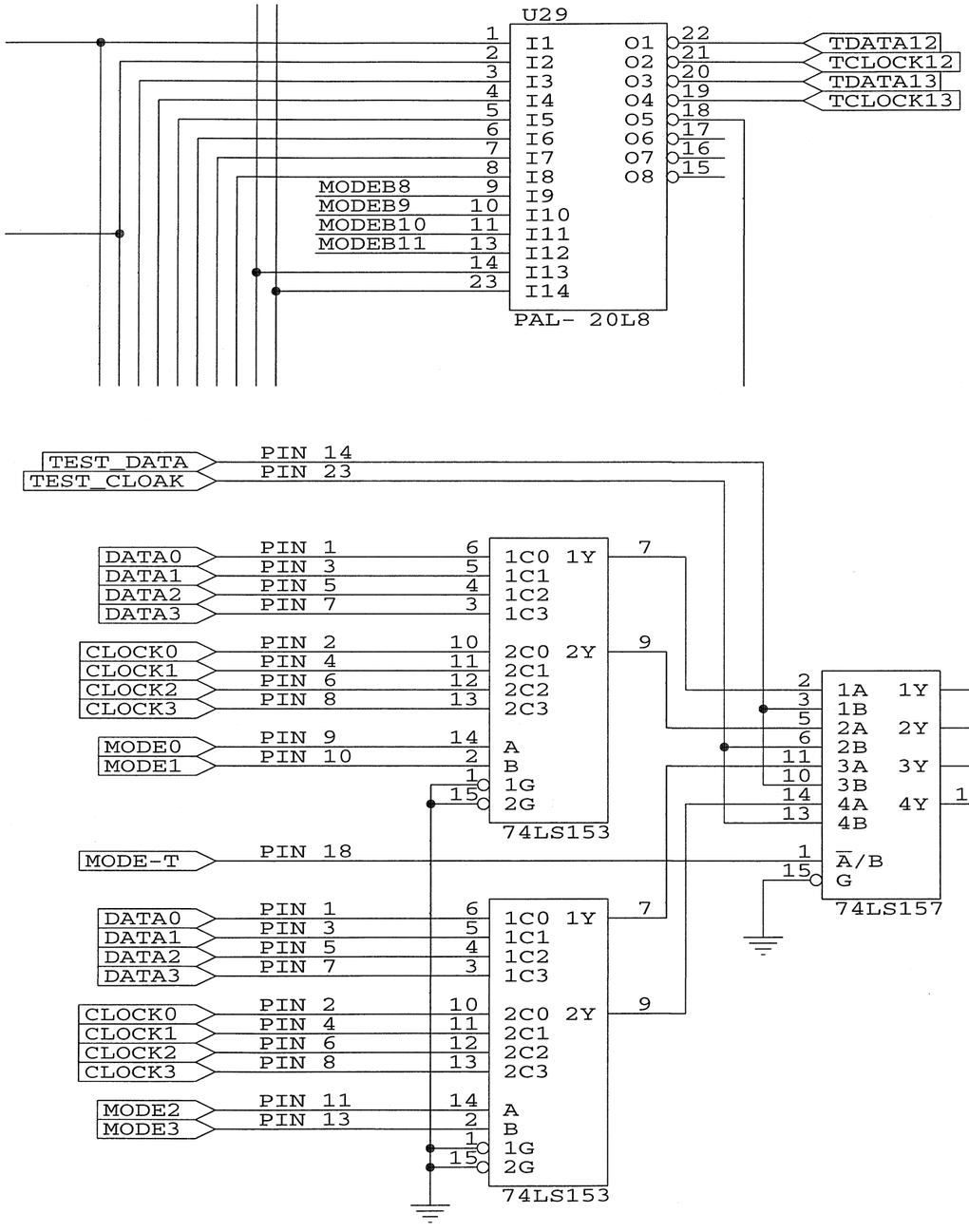
Size	Document Number	REV
C	56000Z007 (Z007D01.LAY)	C

Date: August 17, 1990 Sheet 1 of 2



VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title TRACK RECOVERY CARD IC LAYOUT		
Size C	Document Number 56000Z007 (Z007D02.LAY)	REV
Date: May 5, 1989	Sheet 2 of 2	

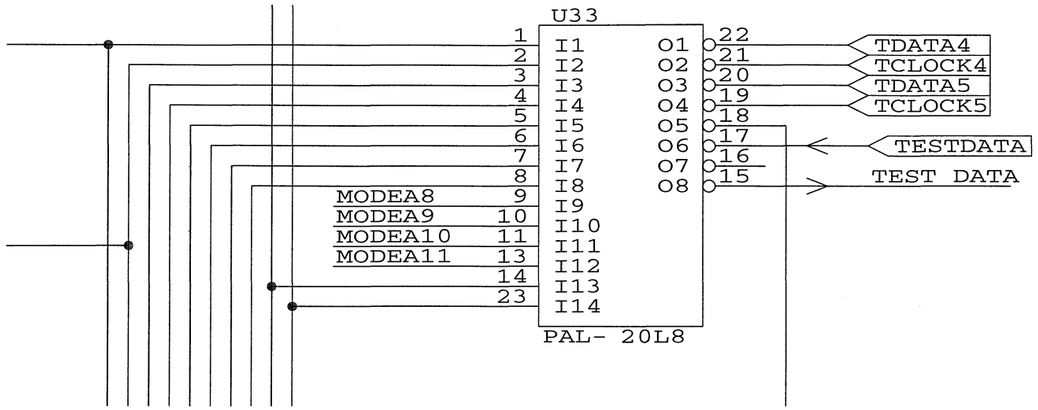
TRACK MIX PAL

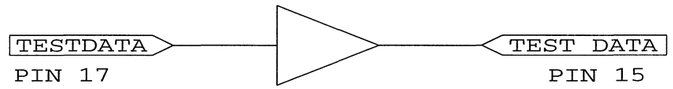


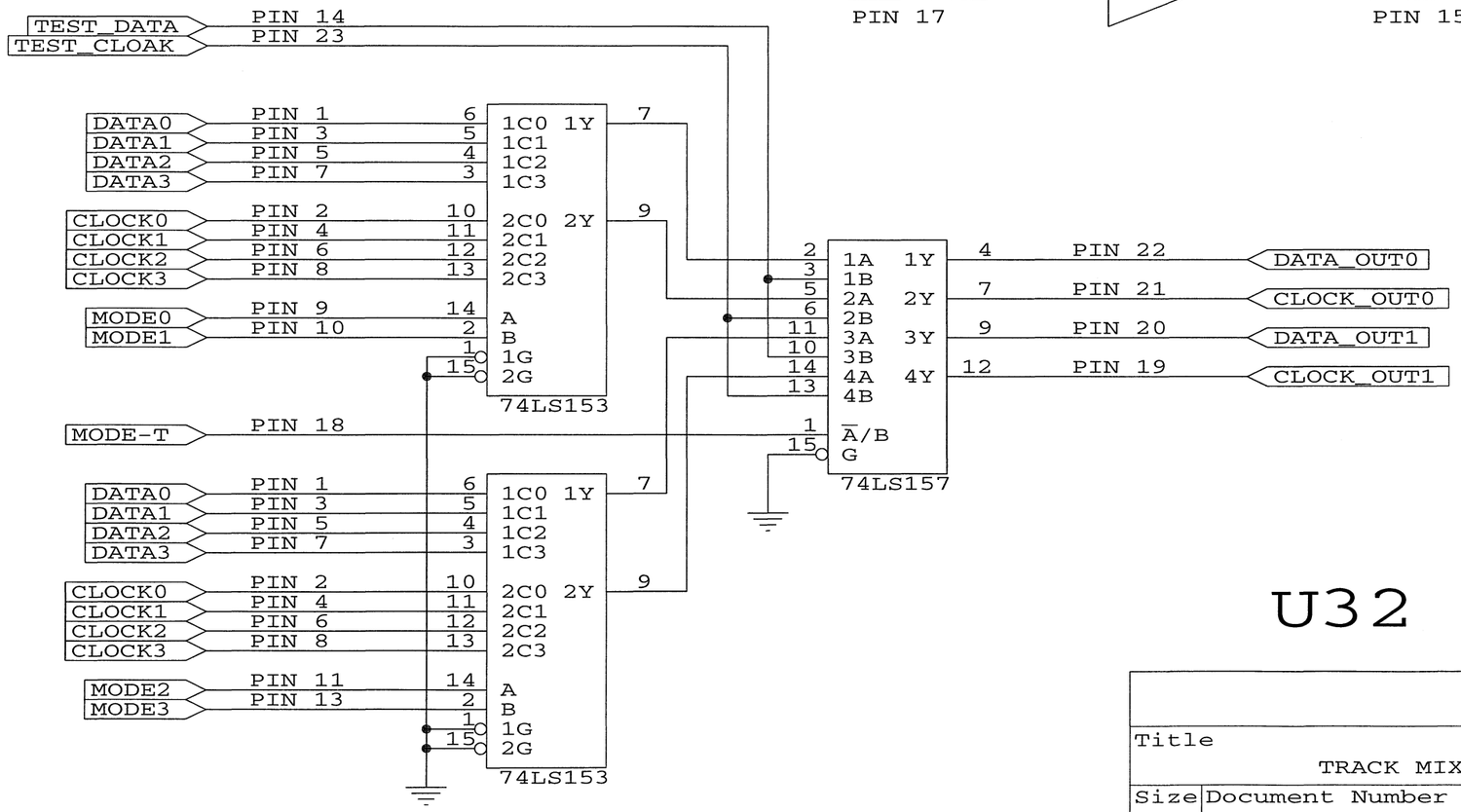
U28 = U29

Title: TRACK MIX, INPUTS 12-15		
Size: A	Document Number: PAL_U29.SCH	REV:
Date: December 3, 1996	Sheet 1 of 1	

TRACK MIX PAL



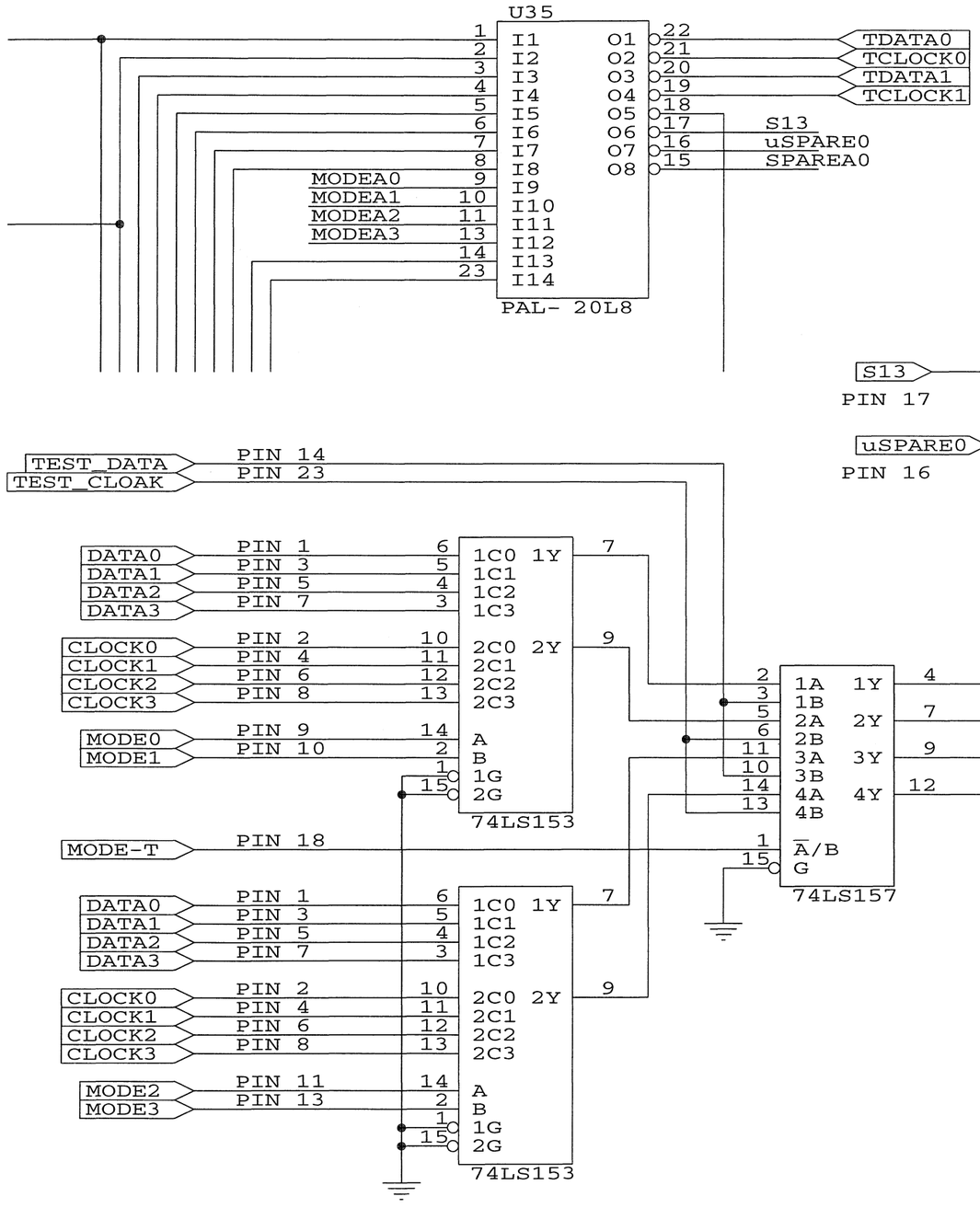




U32 = U33

Title: TRACK MIX, INPUTS 4-7		
Size: A	Document Number: PAL_U33.SCH	REV:
Date: December 5, 1996	Sheet 1 of 1	

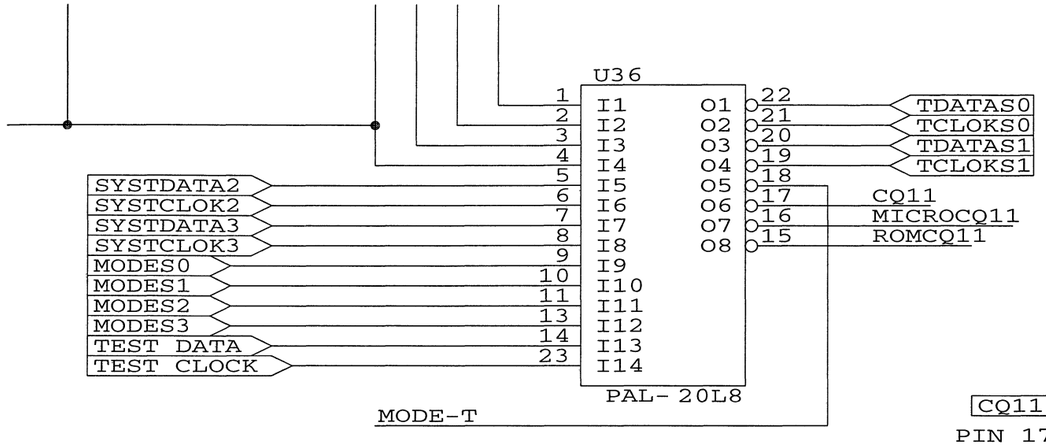
TRACK MIX PAL

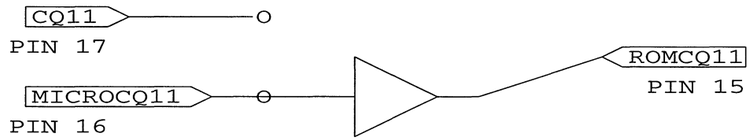


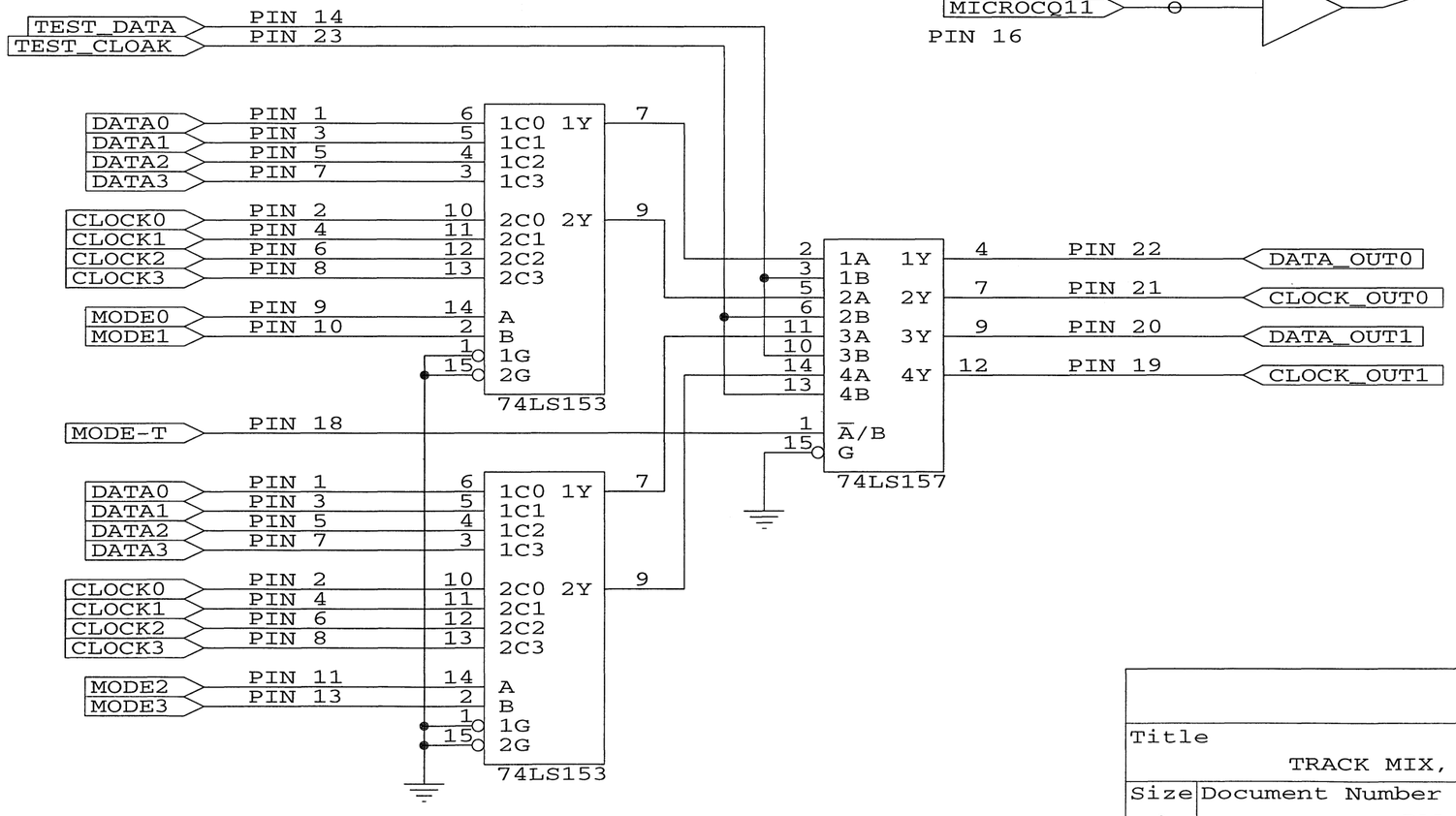
U30 = U31 = U34 = U35

Title: TRACK MIX, INPUTS 0-3 AND 8-11		
Size: A	Document Number: PAL_U35.SCH	REV:
Date: December 3, 1996	Sheet 1 of 1	

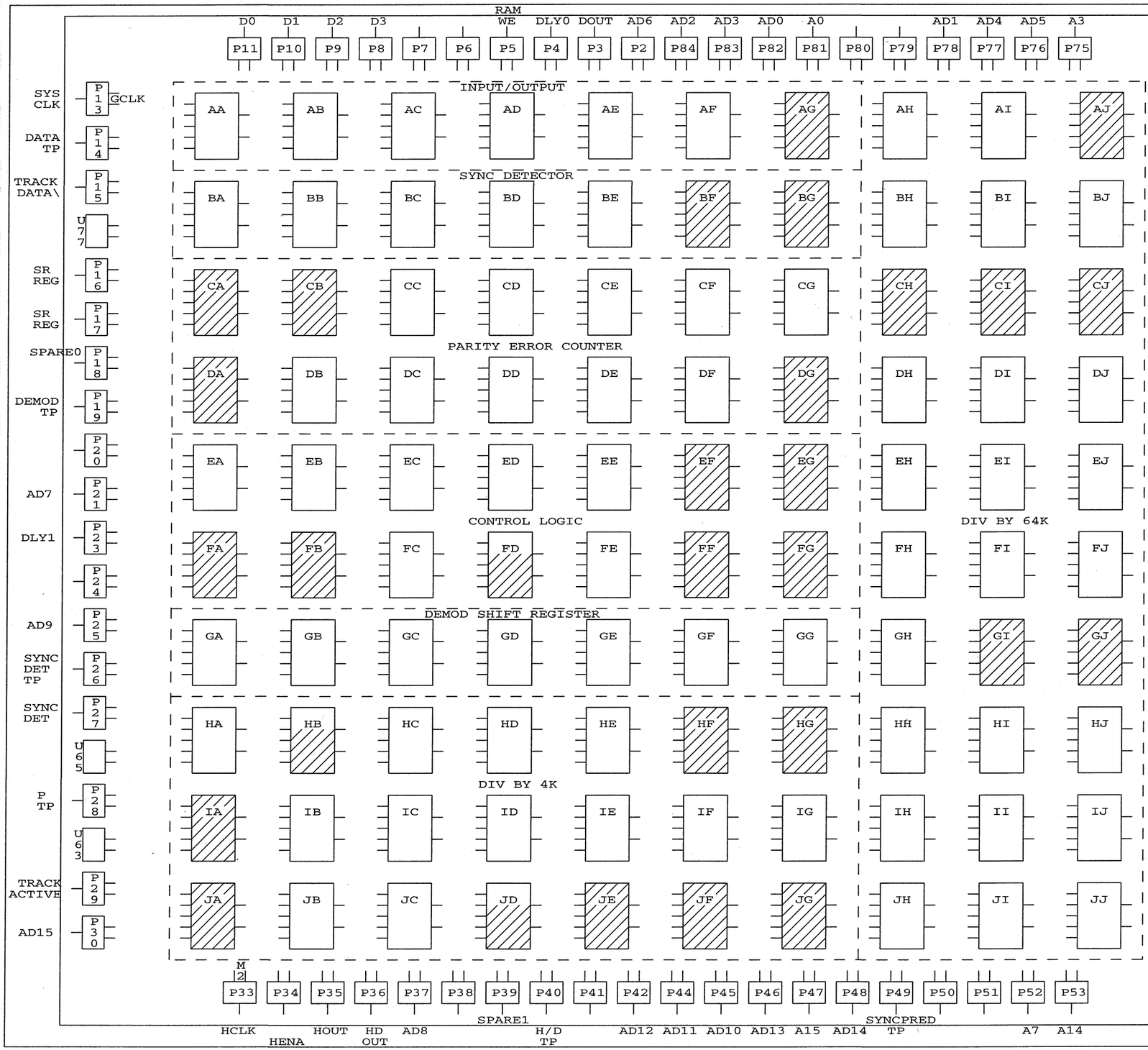
TRACK MIX PAL







Title: TRACK MIX, SYSTEM TRACKS		
Size: A	Document Number: PAL_U36.SCH	REV:
Date: December 3, 1996	Sheet 1 of 1	



INPUT & DEMOD
K008D02.BLK

OUTPUT
K008D03.BLK

TRK FRAME CNTR
K008D04.BLK

TRK CNTR TIMING
K008D05.BLK

SYNC DETECTOR
K008D06.BLK

PARITY ERR CNTR
K008D07.BLK

DIVIDE BY 64K SH1
K008D08.BLK

DIVIDE BY 64K SH2
K008D09.BLK

CONTROL LOGIC
K008D10.BLK

SPARE I/O PINS

P14	UN-NRZMed TRACK DATA
P18	SPARE0 (MODULATION ON)
P19	DEMOD PATTERN TP
P26	SYNCDET TEST POINT
P28	P TP
P39	SPARE1 (= VLBA/MKIII)
P40	H/D TEST POINT
P49	SYNC PRED TEST POINT
P68	A15 TEST POINT

DPC FLOOR PLAN

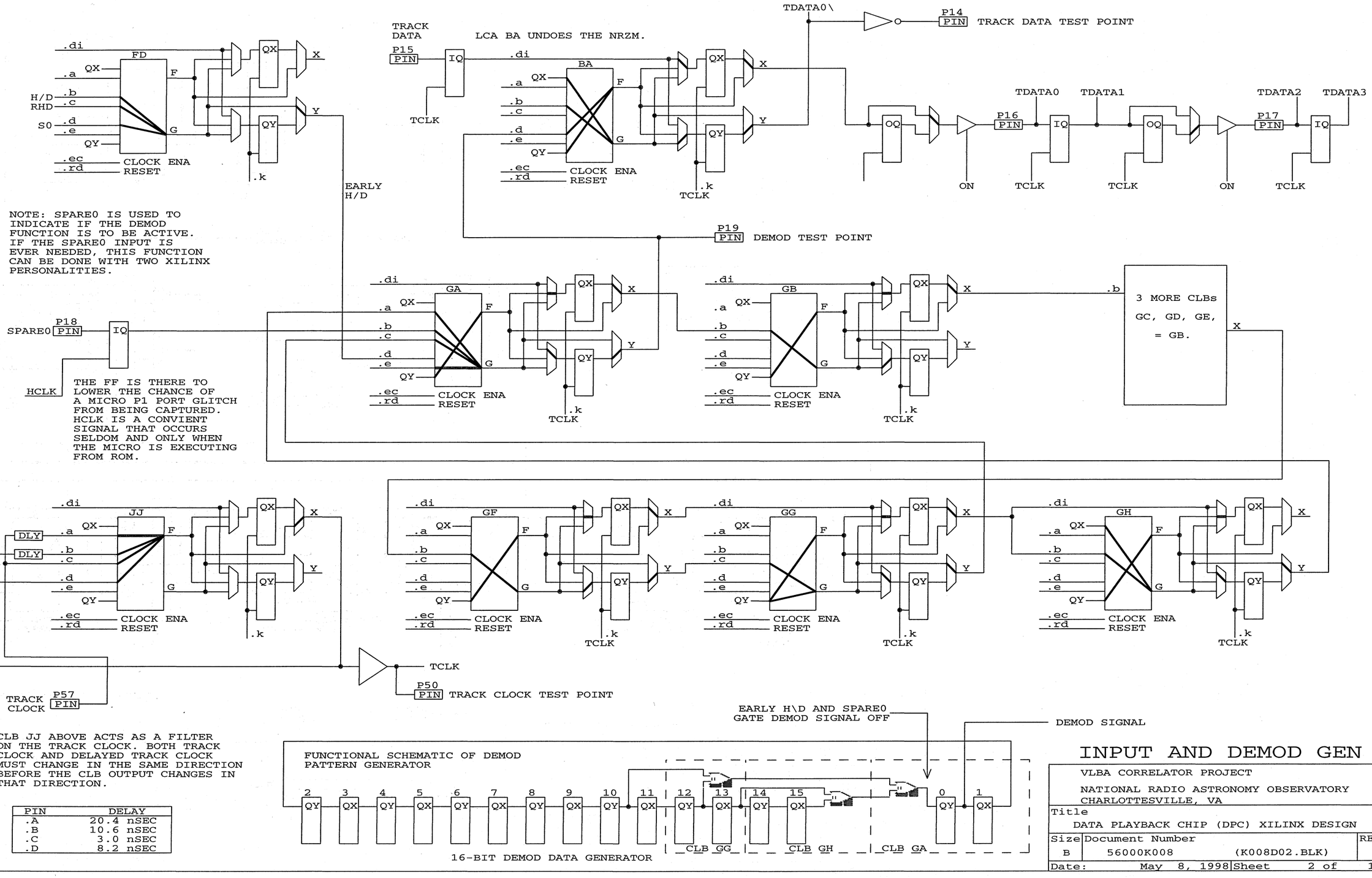
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DATA PLAYBACK CHIP (DPC) XILINX DESIGN

Size	Document Number	REV
B	56000K008 (K008D01.BLK)	

Date: May 8, 1998 Sheet 1 of 10



INPUT AND DEMOD GEN

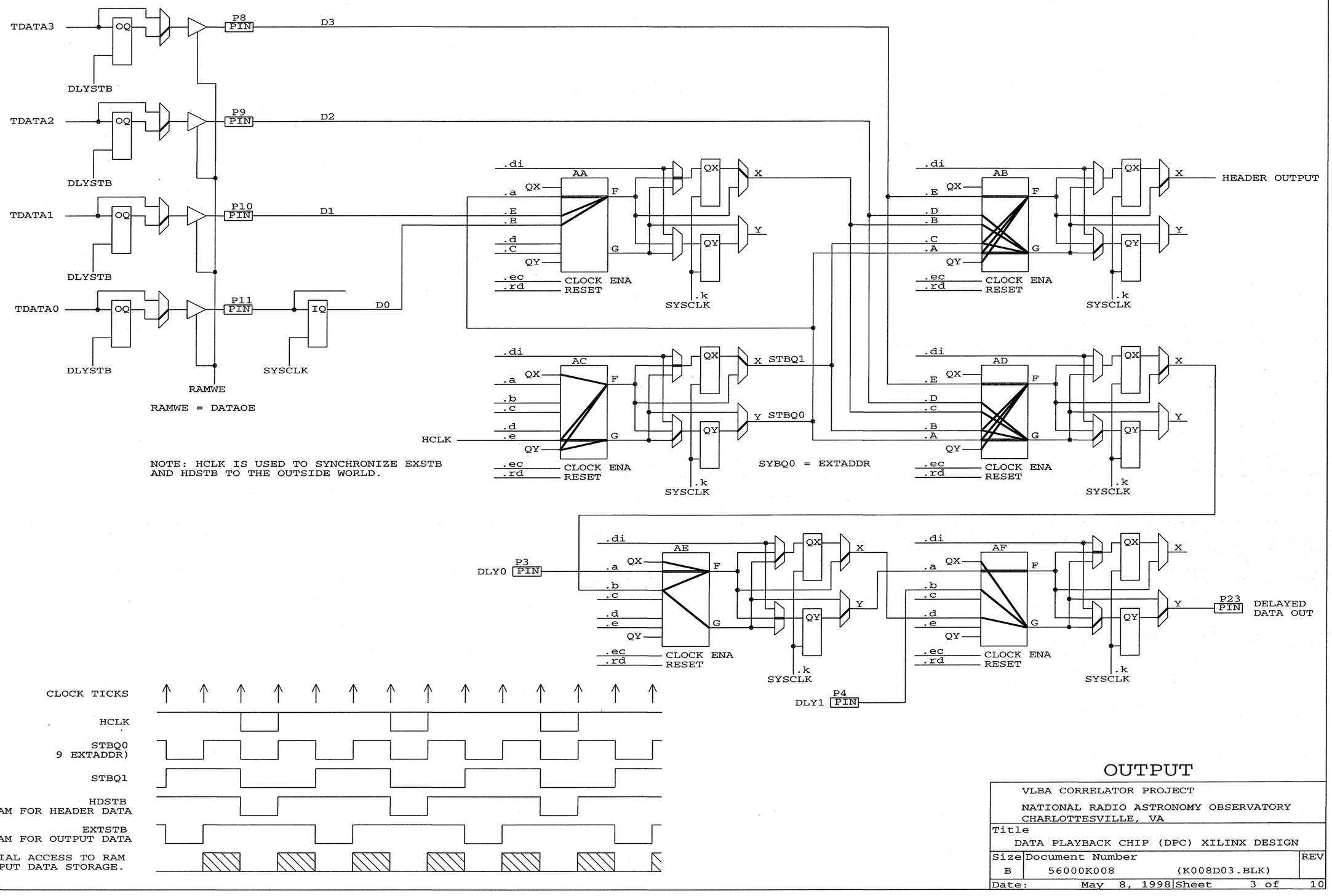
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DATA PLAYBACK CHIP (DPC) XILINX DESIGN

Size	Document Number	REV
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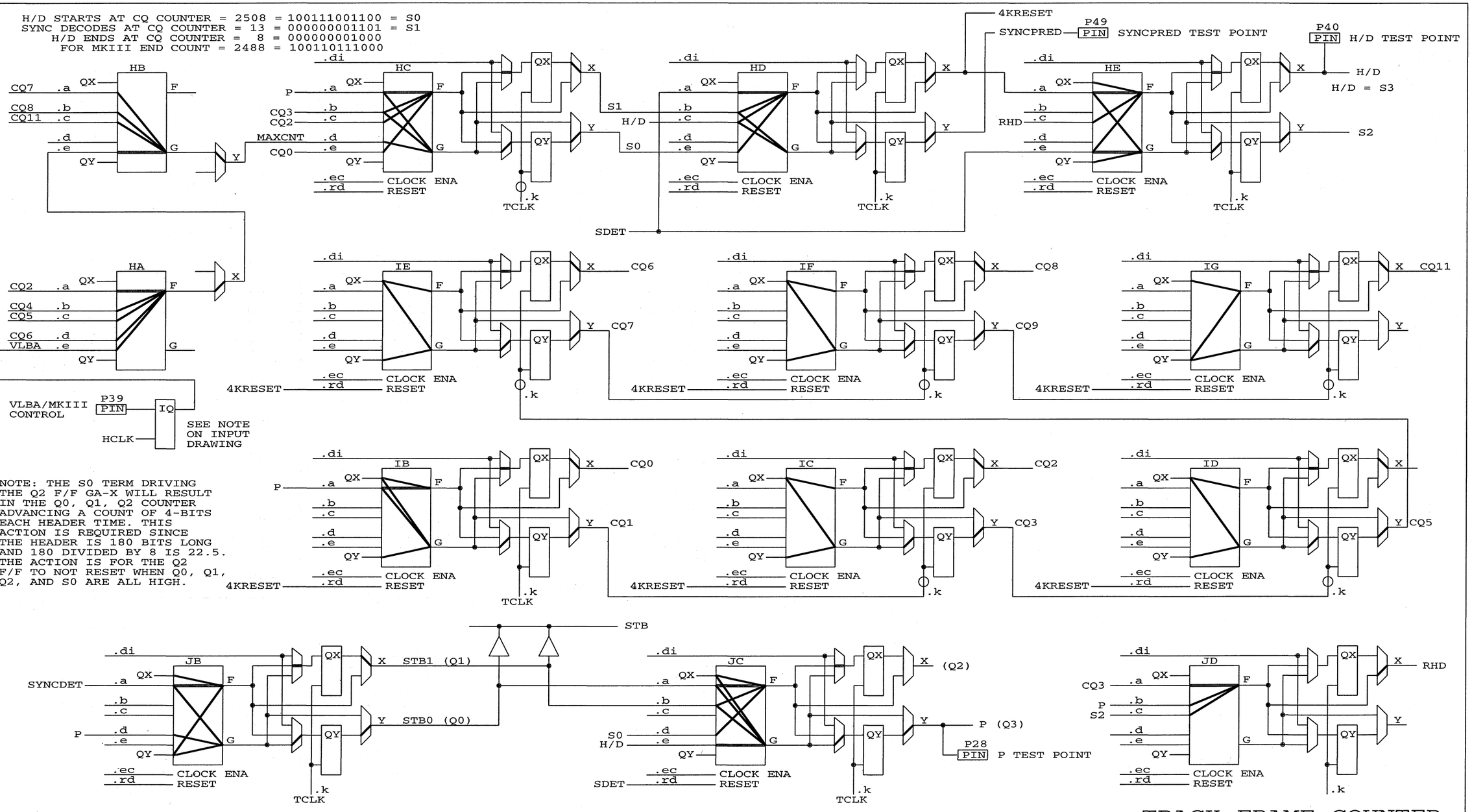
Date: May 8, 1998 Sheet 2 of 10



OUTPUT

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title DATA PLAYBACK CHIP (DPC) XILINX DESIGN		
Size B	Document Number 56000K008 (K008D03.BLK)	REV
Date: May 8, 1998	Sheet 3 of 10	

H/D STARTS AT CQ COUNTER = 2508 = 100111001100 = S0
SYNC DECODES AT CQ COUNTER = 13 = 000000001101 = S1
H/D ENDS AT CQ COUNTER = 8 = 000000001000
FOR MKIII END COUNT = 2488 = 100110111000



NOTE: THE S0 TERM DRIVING THE Q2 F/F GA-X WILL RESULT IN THE Q0, Q1, Q2 COUNTER ADVANCING A COUNT OF 4-BITS EACH HEADER TIME. THIS ACTION IS REQUIRED SINCE THE HEADER IS 180 BITS LONG AND 180 DIVIDED BY 8 IS 22.5. THE ACTION IS FOR THE Q2 F/F TO NOT RESET WHEN Q0, Q1, Q2, AND S0 ARE ALL HIGH.

S0	S1	FUNCTION
0	0	IDLE
1	0	MAXCOUNT
0	1	SYNCTIME
1	1	NOT USED

S2	H/D	TERMINAL COUNT OF 4K COUNTER
0	0	100111001100 (DATA PORTION OF FRAME)
1	1	000000001101 (HEADER UP TO SYNC WORD)
0	1	000000001000 (HEADER FOLLOWING SYNC WORD)

DATA PORTION OF FRAME (H/D = 0)

Q0	Q1	Q2	Q3	STB	P
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	1	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	1	0
0	0	0	1	0	1

HEADER PORTION OF FRAME (H/D = 1)

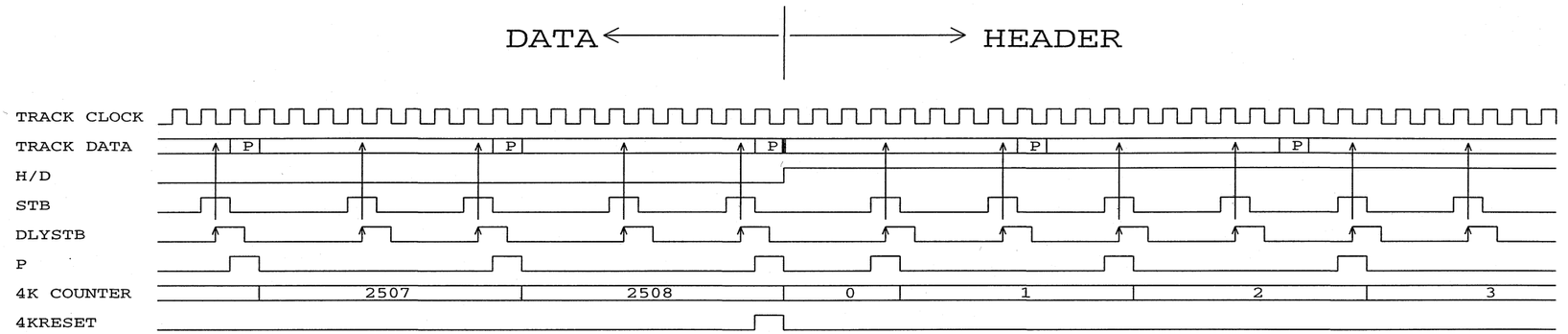
Q0	Q1	Q2	Q3	STB	P
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	1	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	1	1	1

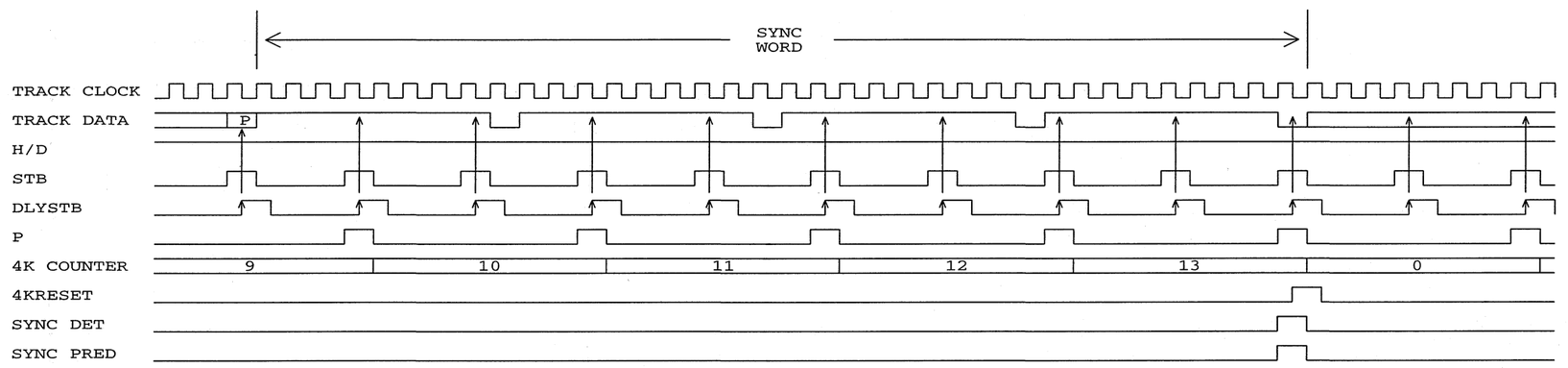
TRACK FRAME COUNTER

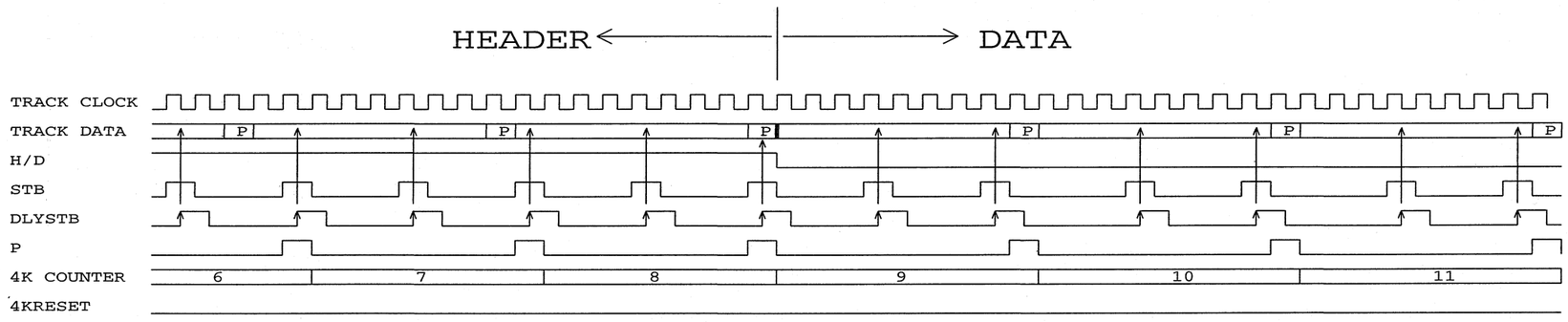
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DATA PLAYBACK CHIP (DPC) XILINX DESIGN

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TRACK COUNTER TIMING DIAGRAM

8	1000
2508	100111001100
13	1101

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

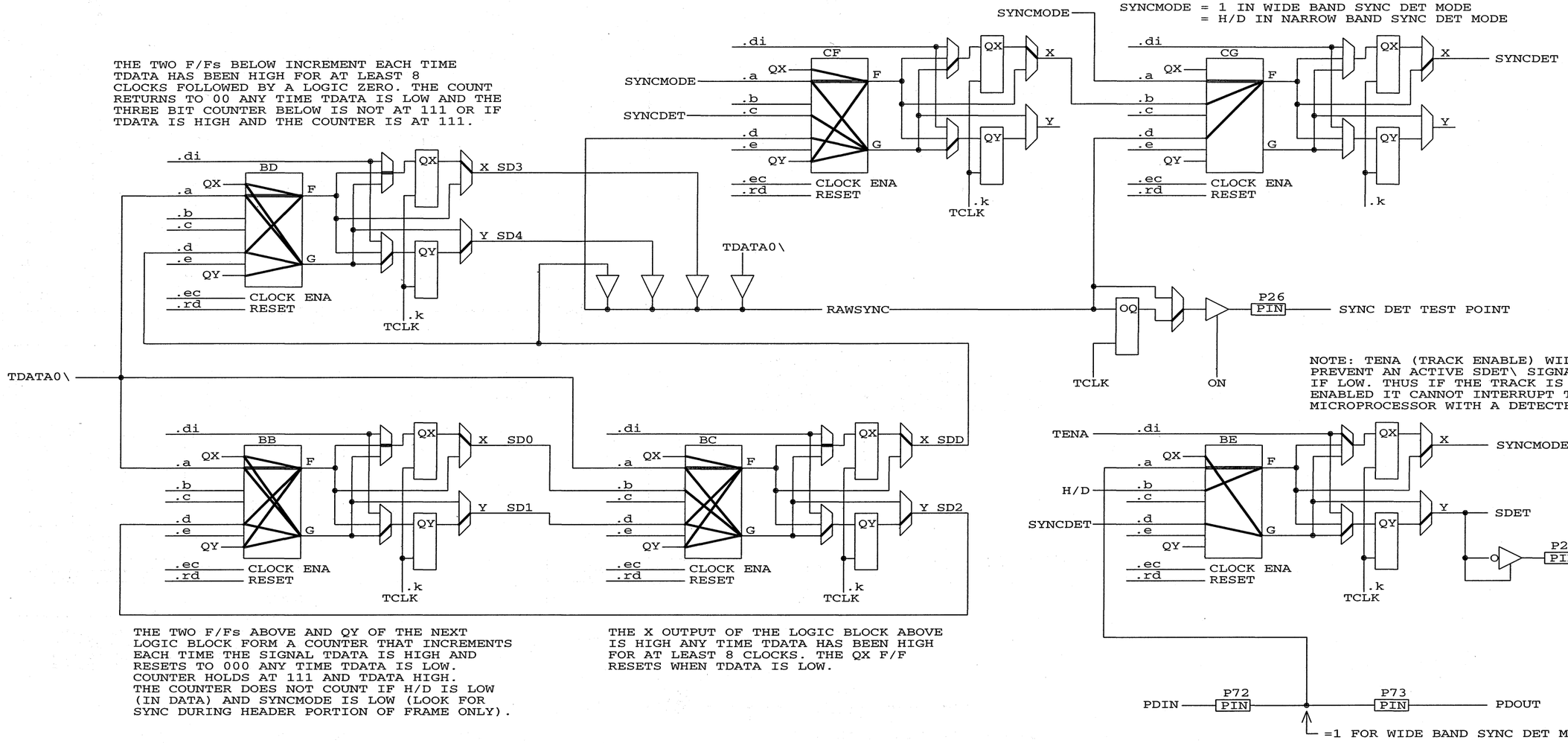
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THE TWO F/Fs BELOW INCREMENT EACH TIME TDATA HAS BEEN HIGH FOR AT LEAST 8 CLOCKS FOLLOWED BY A LOGIC ZERO. THE COUNT RETURNS TO 00 ANY TIME TDATA IS LOW AND THE THREE BIT COUNTER BELOW IS NOT AT 111 OR IF TDATA IS HIGH AND THE COUNTER IS AT 111.

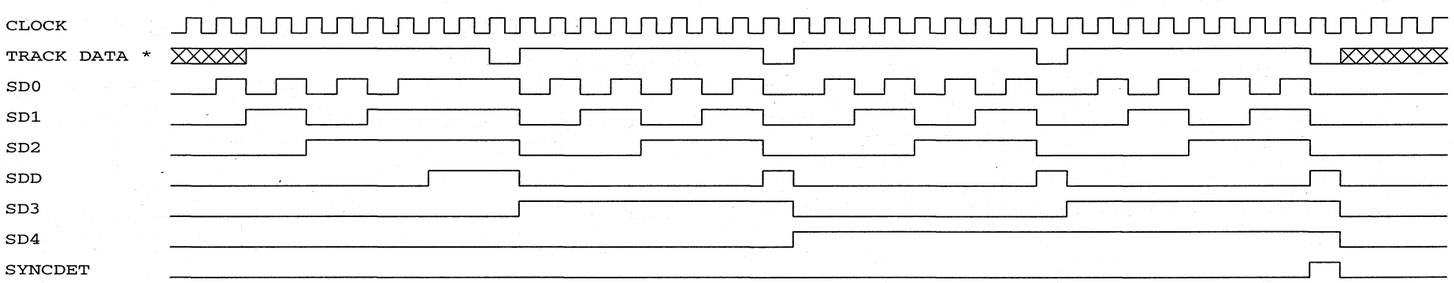
SYNCMODE = 1 IN WIDE BAND SYNC DET MODE
= H/D IN NARROW BAND SYNC DET MODE



NOTE: TENA (TRACK ENABLE) WILL PREVENT AN ACTIVE SDET\ SIGNAL IF LOW. THUS IF THE TRACK IS NOT ENABLED IT CANNOT INTERRUPT THE MICROPROCESSOR WITH A DETECTED SYNC.

THE TWO F/Fs ABOVE AND QY OF THE NEXT LOGIC BLOCK FORM A COUNTER THAT INCREMENTS EACH TIME THE SIGNAL TDATA IS HIGH AND RESETS TO 000 ANY TIME TDATA IS LOW. COUNTER HOLDS AT 111 AND TDATA HIGH. THE COUNTER DOES NOT COUNT IF H/D IS LOW (IN DATA) AND SYNCMODE IS LOW (LOOK FOR SYNC DURING HEADER PORTION OF FRAME ONLY).

THE X OUTPUT OF THE LOGIC BLOCK ABOVE IS HIGH ANY TIME TDATA HAS BEEN HIGH FOR AT LEAST 8 CLOCKS. THE QX F/F RESETS WHEN TDATA IS LOW.



THE TWO CLBs AT THE TOP OF THIS PAGE IMPLEMENT THE NARROW BAND SYNC DET MODE. IF SYNCMODE IS LOW WE ARE IN THE DATA PORTION OF THE FRAME AND SHOULD RECV NO SYNC. IF A SYNC IS DETECTED THIS FACT IS LATCHED IN THE QX FF OF BLOCK CF. WHEN THE H/D SIGNAL GOES HIGH THE FLAG IS TRANSFERED INTO FF QY. QY HOLDS THE INFO AND IF A SYNC DETECT IS SEEN IN THE DATA PORTION OF THE NEXT (BUT NO SYNC IS SEEN DURING THE HEADER BETWEEN) A SYNC DET IS GENERATED WHICH INITIALIZES THE DPC CHIP FRAME COUNTER. THUS IF THE DPC CHIP WAS OUT OF SYNC THIS ACTION WILL CORRECT THE SITUATION WITHOUT uPROC INTERVENTION.

* DATA IS ASSUMED TO HAVE TWO LOGIC ONE' THAT PRECEED THE SYNC CODE (BUT SHOWN AS CROSS HATCH).

NOTES:

1) SYNCMODE SIGNAL INDICATES IF SYNC IS TO BE SEARCHED FOR DURING THE HEADER ONLY OR ALL OF THE TIME. PIN 72 IS A DUAL FUNCTION PIN. DURING PROGRAM LOAD TIME IT IS THE PROGRAM DATA INPUT BUT DURING OPERATION, IT BECOMES THE SYNC MODE INPUT.

2) MARK III SYNC WORD IS 11111111011111111101111111101111111110

SYNC DETECTOR

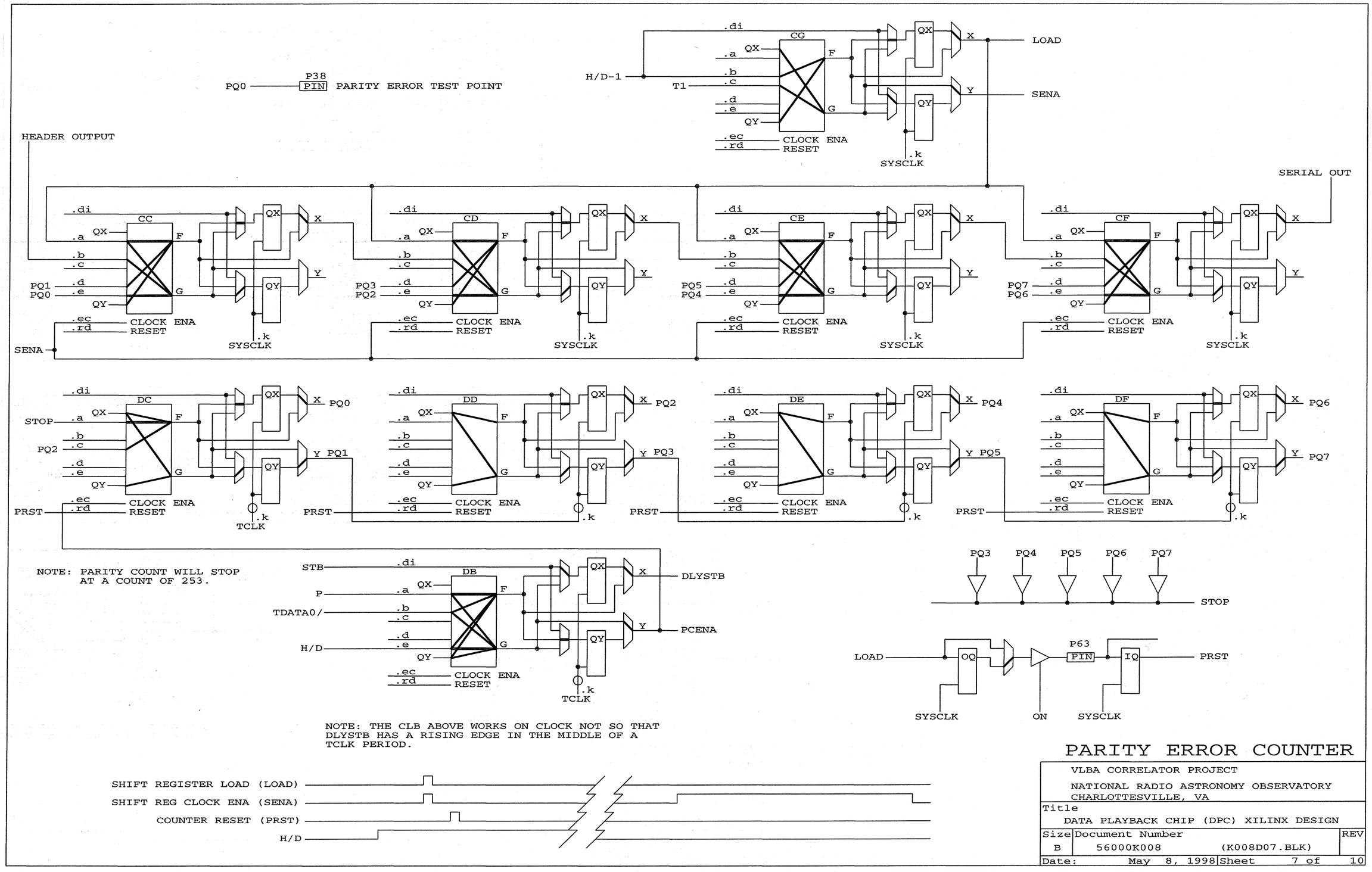
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DATA PLAYBACK CHIP (DPC) XILINX DESIGN

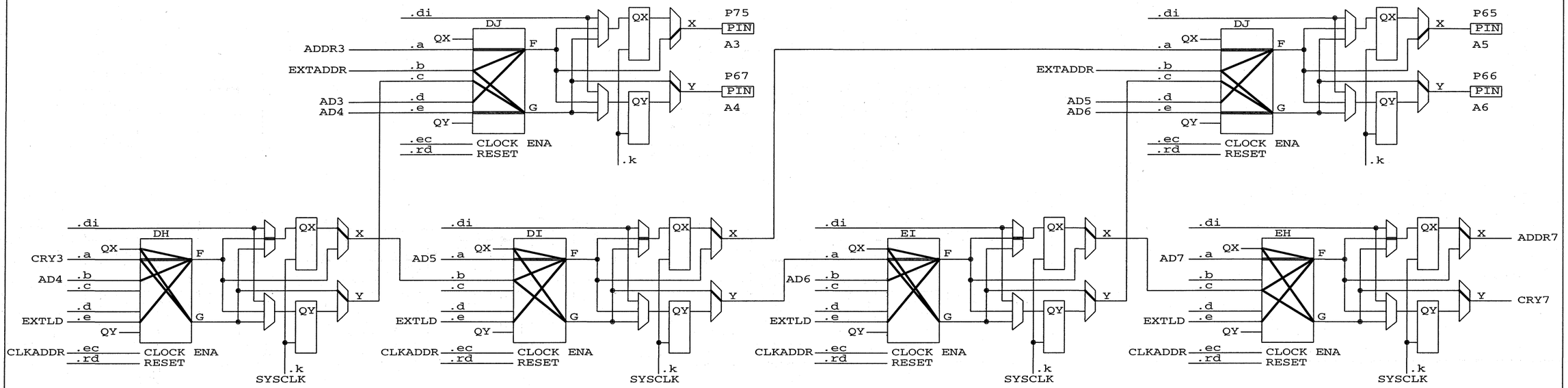
Size	Document Number	REV
B	56000K008 (K008D06.BLK)	

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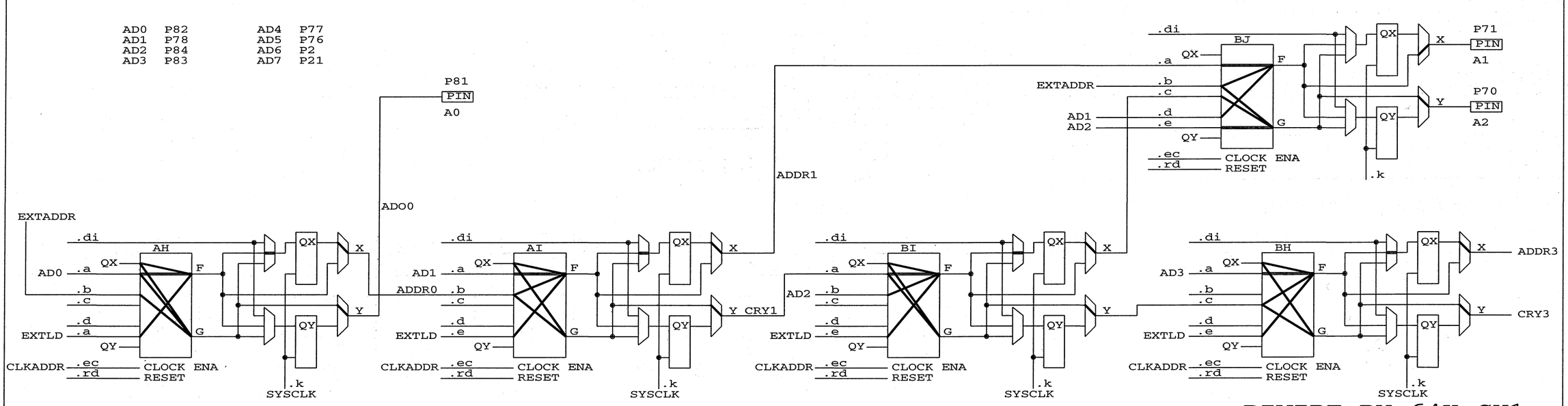


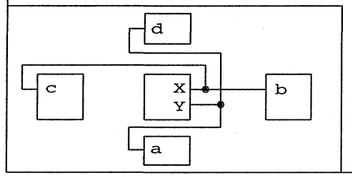
PARITY ERROR COUNTER

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title DATA PLAYBACK CHIP (DPC) XILINX DESIGN		
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AD0	P82	AD4	P77
AD1	P78	AD5	P76
AD2	P84	AD6	P2
AD3	P83	AD7	P21





NOTE: ALL RAM ADDRESS PINS A0 THRU A6 HAVE OUTPUT PIPELINE FLIP FLOPS.

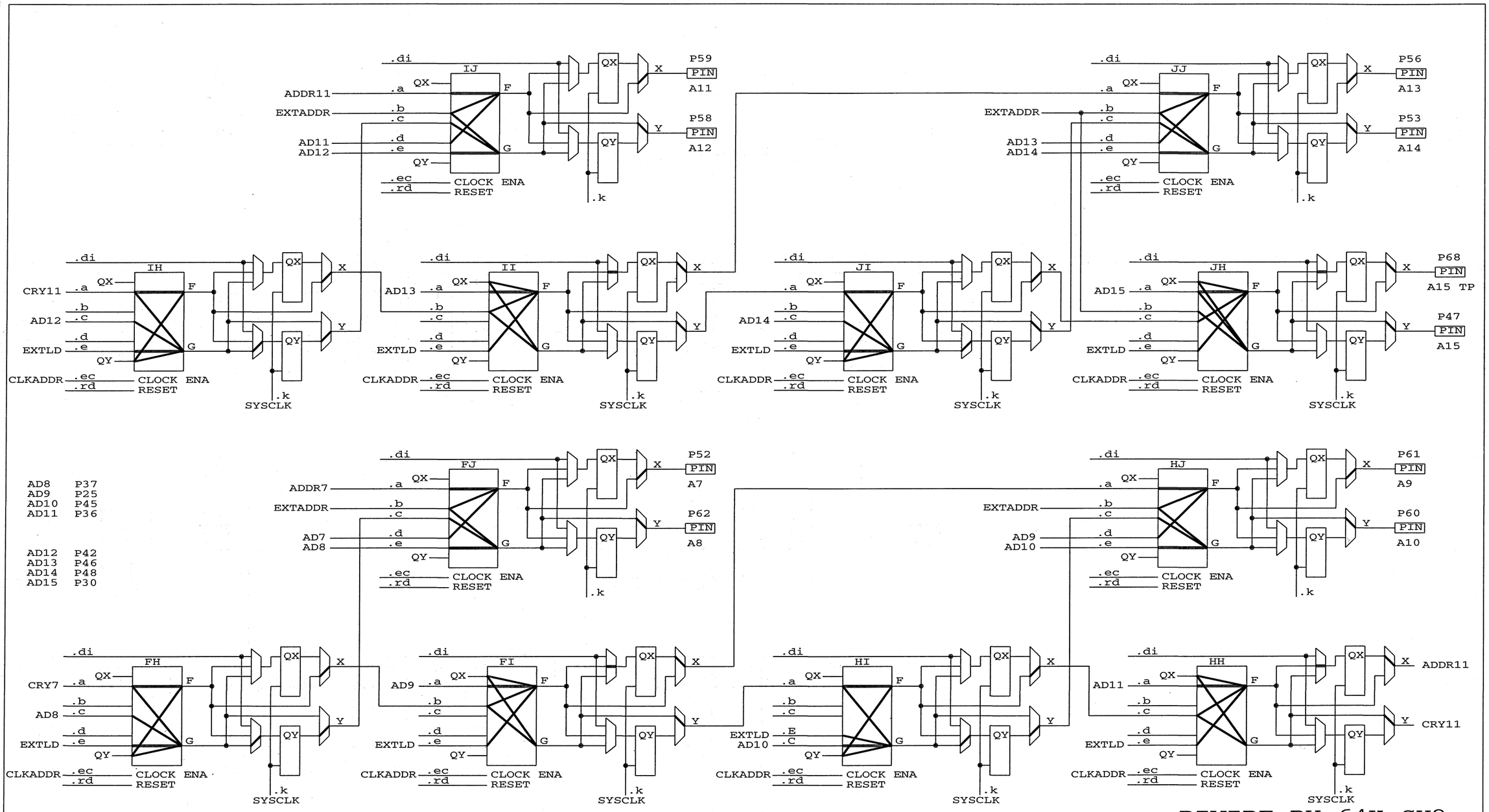
DIVIDE BY 64K SH1

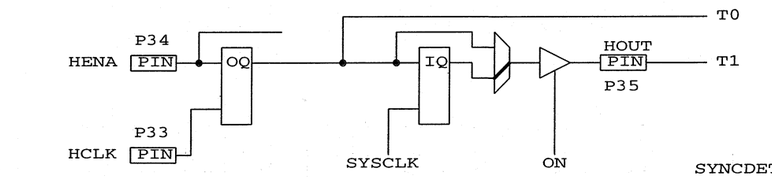
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DATA PLAYBACK CHIP (DPC) XILINX DESIGN

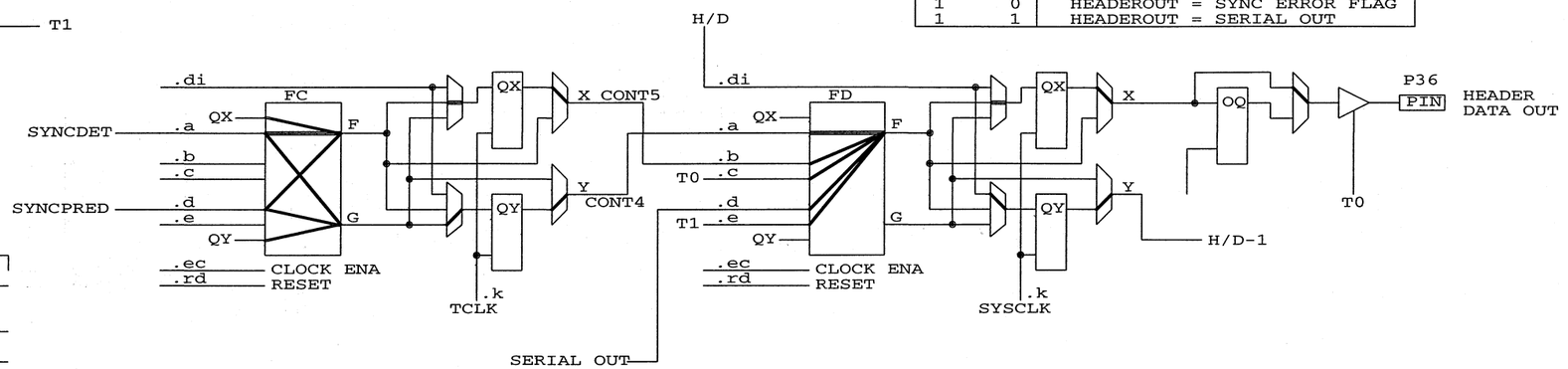
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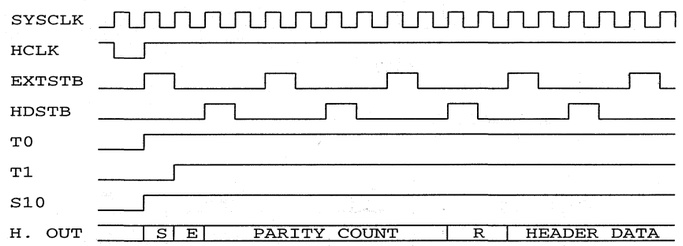

IJ
.di
ADDR11
EXTADDR
AD11
AD12
.a
.b
.c
.d
.e
QY
.ec
.rd
CLOCK ENA
RESET
.k
QX
F
G
X
Y
P59
PIN
A11
P58
PIN
A12
IH
CRY11
AD12
EXTLD
CLKADDR
SYSCLK
II
AD13
JI
AD14
JJ
AD13
AD14
P56
PIN
A13
P53
PIN
A14
JH
AD15
P68
PIN
A15 TP
P47
PIN
A15
FJ
ADDR7
AD7
AD8
P52
PIN
A7
P62
PIN
A8
FH
CRY7
AD8
FI
AD9
HI
EXTLD
AD10
HJ
AD9
AD10
P61
PIN
A9
P60
PIN
A10
HH
AD11
ADDR11
CRY11
AD8 P37
AD9 P25
AD10 P45
AD11 P36
AD12 P42
AD13 P46
AD14 P48
AD15 P30
d
c
X
Y
b
a
NOTE: ALL RAM ADDRESS PINS A7 THRU
A15 HAVE OUTPUT PIPELINE FLIP FLOPS.
DIVIDE BY 64K SH2
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
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DATA PLAYBACK CHIP (DPC) XILINX DESIGN
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SIGNAL CONT4 IS THE REC SYNC FLAG.
SIGNAL CONT5 IS THE SYNC ERROR FLAG.

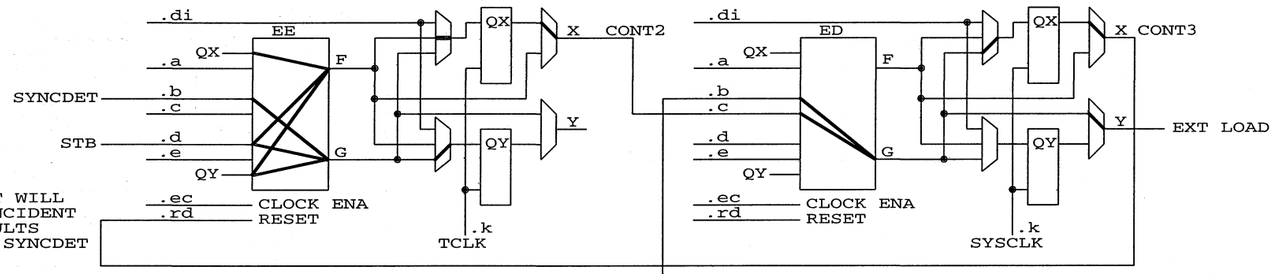
T0	T1	FUNCTION
0	0	HEADEROUT = REC SYNC FLAG
1	0	HEADEROUT = SYNC ERROR FLAG
1	1	HEADEROUT = SERIAL OUT

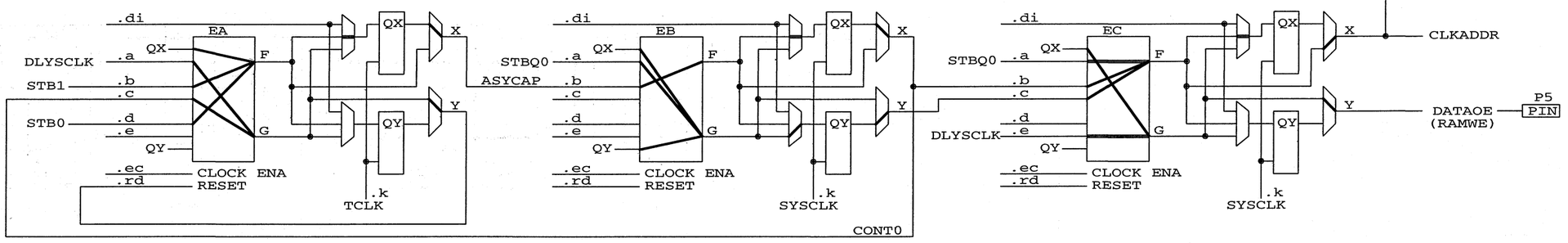




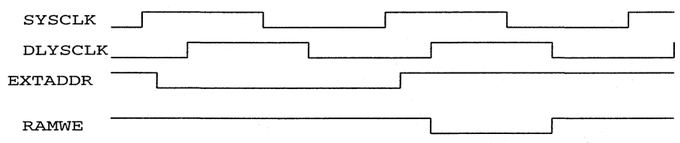
S = SYNC REC FLAG
E = SYNC OUT OF PLACE FLAG
R = RUBBISH

THE TWO LOGIC BLOCKS AT THE RIGHT WILL GENERATE THE EXT LOAD SIGNAL COINCIDENT WITH THE CLKADDR STROBE THAT RESULTS FROM THE FIRST STB FOLLOWING THE SYNCDET SIGNAL.





THE FIRST LOGIC BLOCK ABOVE WILL LATCH THE STB SIGNAL UNTIL IT IS CAPTURED BY THE SYSTEM CLOCK. THE SECOND LOGIC BLOCK DOES THE ASYNCHRONOUS CAPTURE OF STB BY SYSCLOCK AND RESETS THE LATCHED STB SIGNAL. THE F/F IN THE SECOND LOGIC BLOCK WILL HOLD THE CAPTURED STB SIGNAL FOR ONLY ONE CLOCK AFTER WHICH IT RESETS. THE LAST LOGIC BLOCK ABOVE USES THE CAPTURED STB SIGNAL TO GENERATE CLKADDR AND RAMWE. IF THE STBQ0 SIGNAL ALLOWS IMMEDIATE ACCESS TO THE RAM THESE SIGNALS APPEAR RIGHT AWAY. IF STBQ0 INDICATES THAT THE RAM IS BUSY, THE CAPTURED STB SIGNAL IS STORED AND SERVICED WHEN THE RAM IS AVAILABLE.



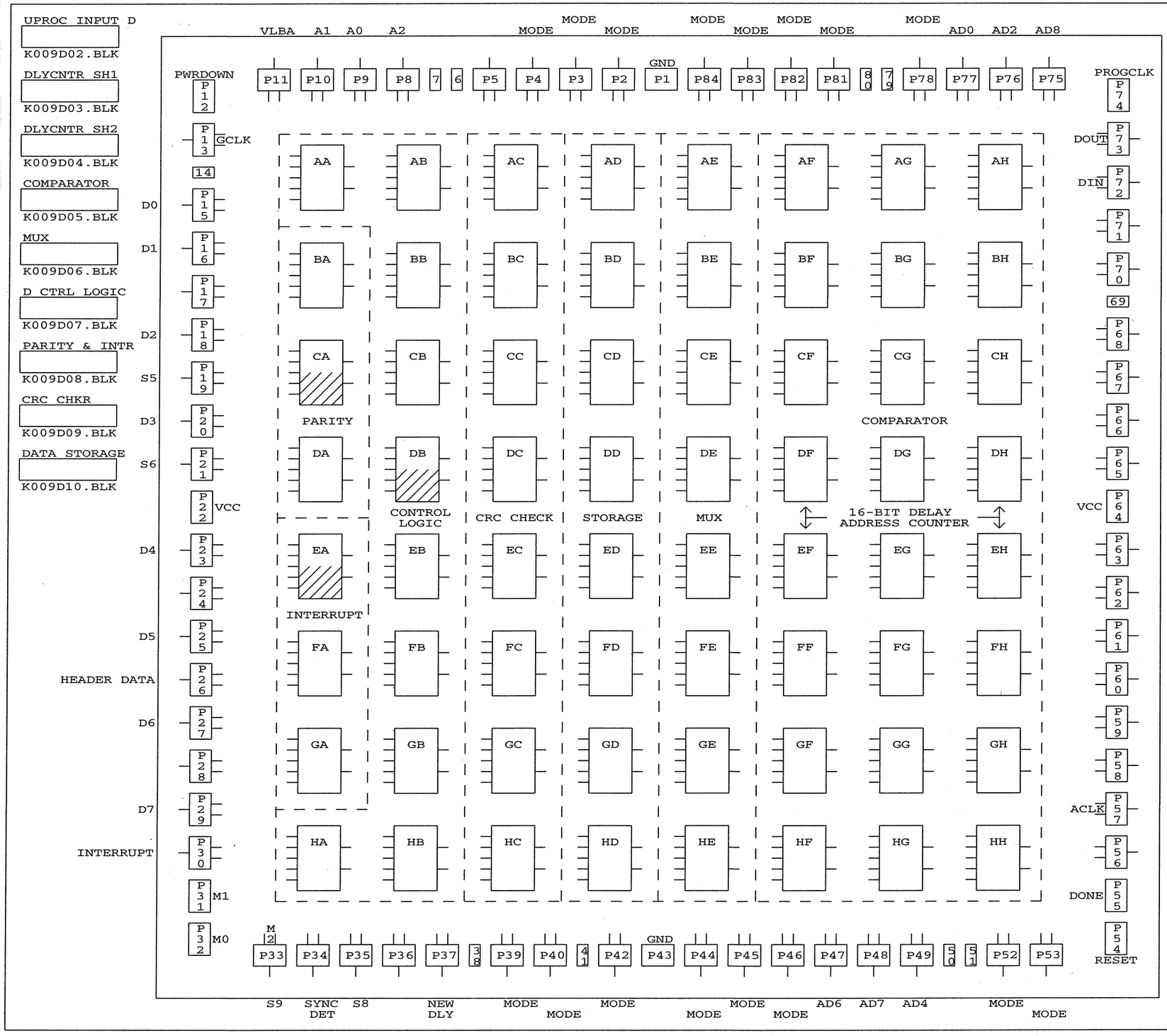
CONTROL LOGIC

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

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DATA PLAYBACK CHIP (DPC) XILINX DESIGN

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MICROPROCESSOR ADDRESSES

WRITE:

- INITIAL DELAY
- HEADER SKIP ADDRESS
- HEADER START ADDRESS
- TRACK MIX BITS
- RESET INTERRUPT BITS

READ:

- MONITOR DATA

MONITOR DATA

PARITY ERR	3 BITS
ECC	1 BIT
INTERRUPT	3 BITS

INTERRUPTS

- NEW FRAME
- NEW DELAY
- SYNC DETECT

SEQUENCER CONTROL BITS

PARITY CONTROL 0	S5
PARITY CONTROL 1	S6
CRCC ENABLE	S8
CRCC RESET	S9

SPARE I/O PINS

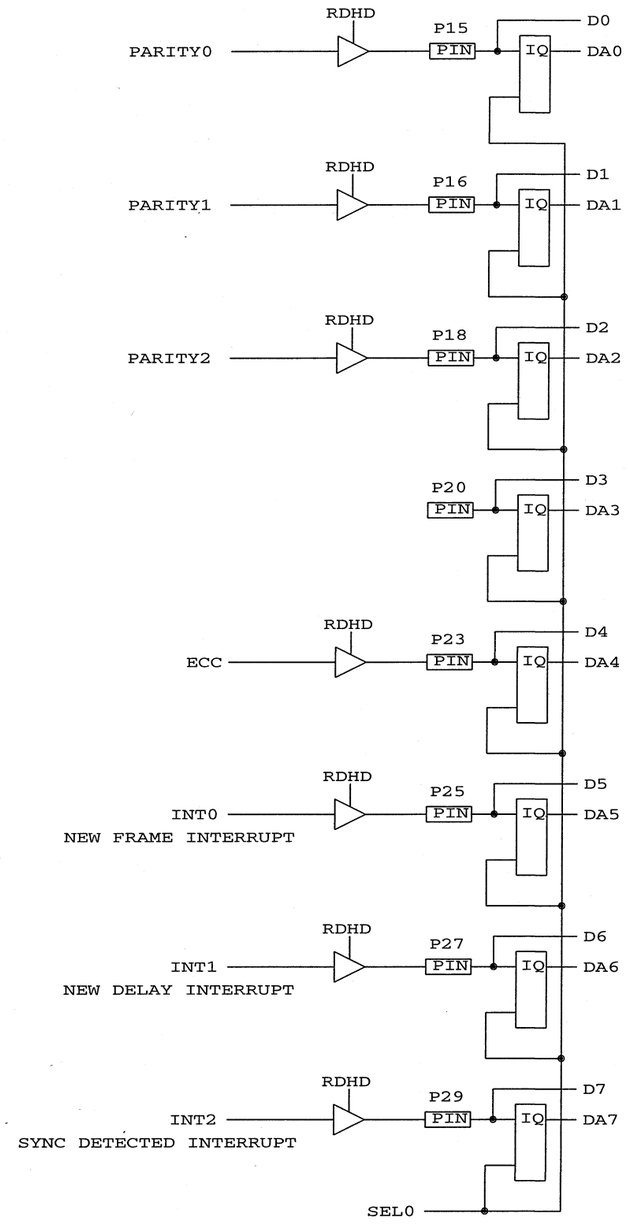
P68 A15 TEST POINT

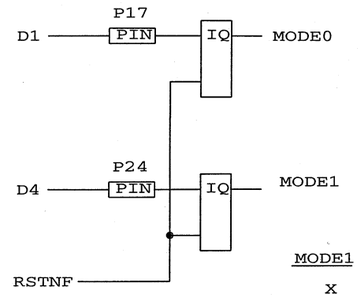
D FLOOR PLAN

VLBA CORRELATOR PROJECT

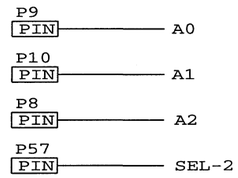
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MODE1	MODE0	
X	0	DISABLE COMPARATOR
X	1	ENABLE COMPARATOR
0	X	ENABLE NEW FRAME INTERRUPT
1	X	RESET NEW FRAME INTERRUPT



MICROPROCESSOR MEMORY MAP

A2	A1	A0	FUNCTION
0	0	0	WRITE INITIAL DELAY
0	0	1	WRITE HEADER SKIP ADDRESS
0	1	0	WRITE HEADER START ADDRESS
0	1	1	WRITE TRACK MIX PROGRAM BITS
1	0	0	READ MONITOR DATA
1	0	1	RESET SYNC DET INTERRUPT
1	1	0	RESET NEW FRAME INTERRUPT
1	1	1	RESET NEW DELAY INTERRUPT

DA(0..7) IS HALF OF THE INITIAL DELAY ADDRESS (THE SECOND HALF IS STORED IN THE MUX).

MICROPROCESSOR INPUT D

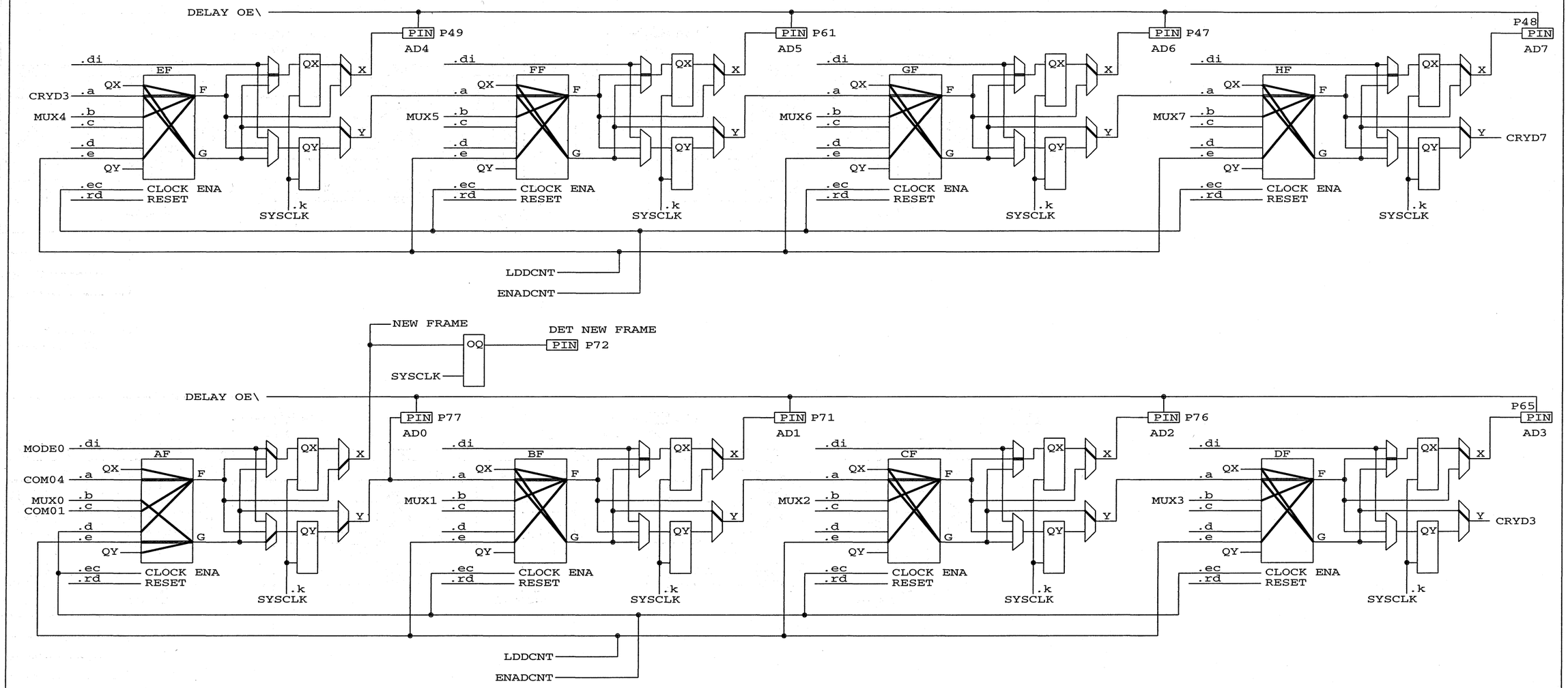
VLBA CORRELATOR PROJECT

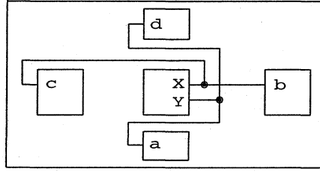
NATIONAL RADIO ASTRONOMY OBSERVATORY
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Title: DELAY CONTROL XILINX DESIGN

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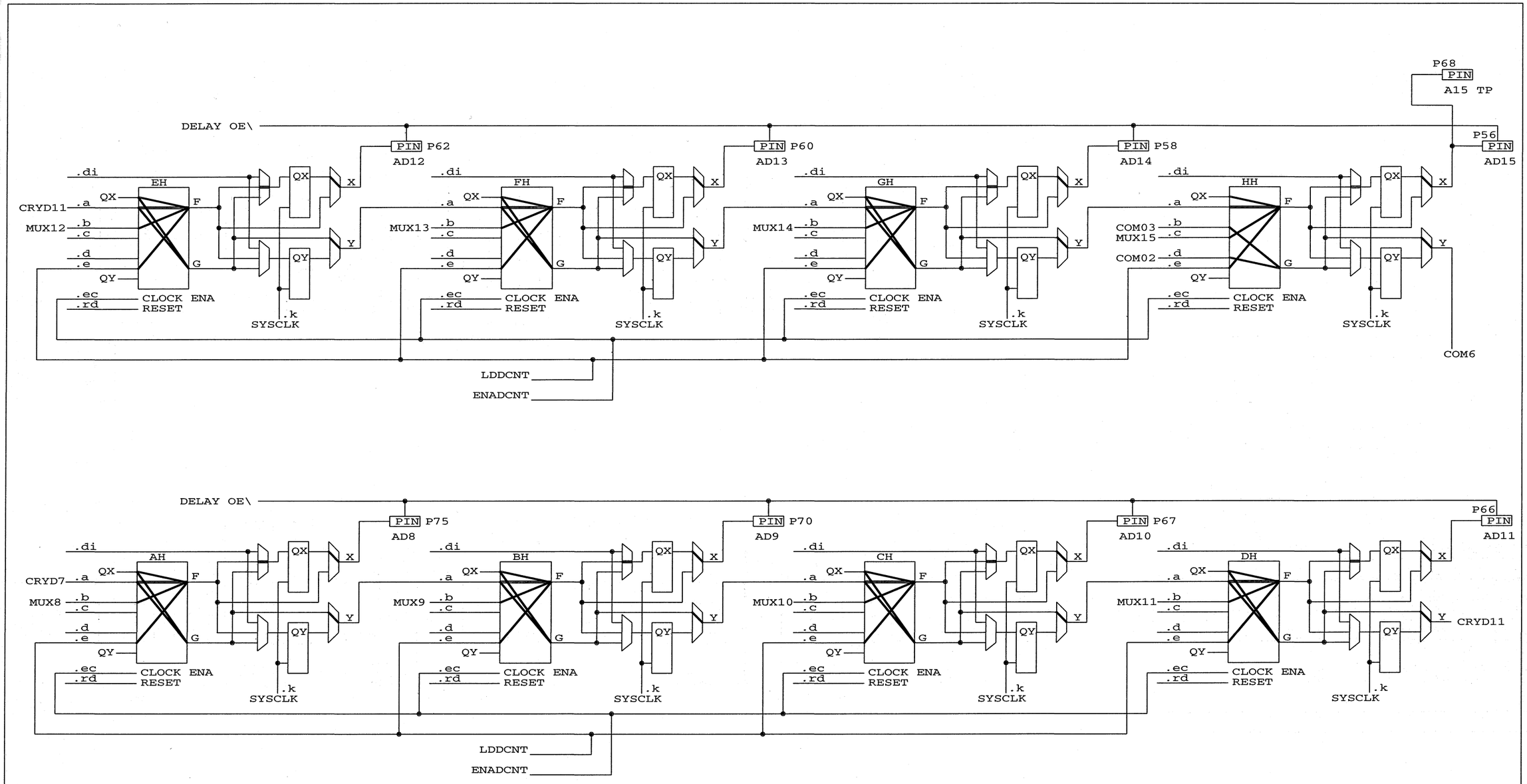
DELAY COUNTER SH 1

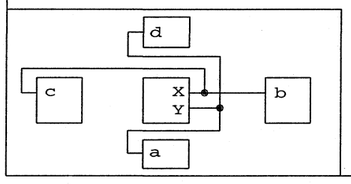
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DELAY CONTROL XILINX DESIGN

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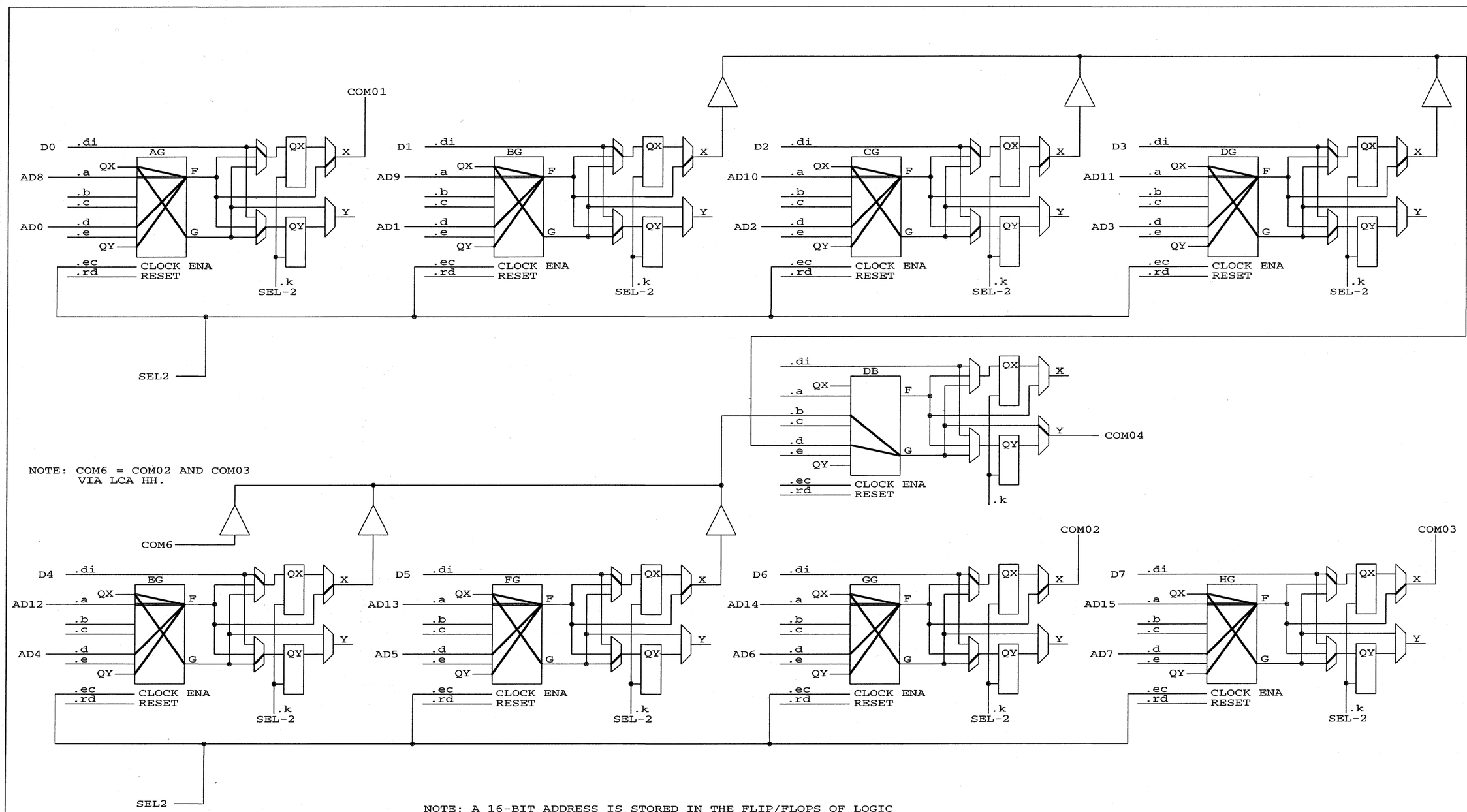
DELAY COUNTER SH 2

VLBA CORRELATOR PROJECT

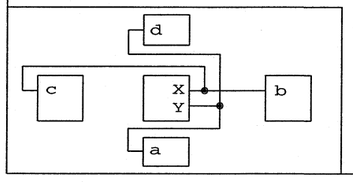
NATIONAL RADIO ASTRONOMY OBSERVATORY
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Title: DELAY CONTROL XILINX DESIGN

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NOTE: COM6 = COM02 AND COM03 VIA LCA HH.



NOTE: A 16-BIT ADDRESS IS STORED IN THE FLIP/FLOPS OF LOGIC BLOCKS AG THRU HG. THIS 16-BIT ADDRESS IS THE ADDRESS IN THE TRACK BUFFER RAM OF THE LAST NIBBLE OF A FRAME. WHEN THE COMPARATOR FINDS THAT THE DELAY ADDRESS COUNTER HAS REACHED THIS ADDRESS A NEW FRAME IS SIGNALED.

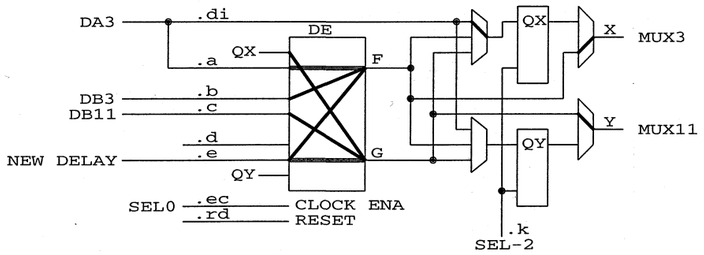
NOTE: SIGNAL SEL-2 IS THE MICROPROCESSOR ADDRESS SELECT FOR THIS XILINX CHIP. SIGNAL SEL2 (NO DASH) DECODES WHEN SEL-2 IS ACTIVE AND THE A0 A1 A2 ADDRESS IS 010.

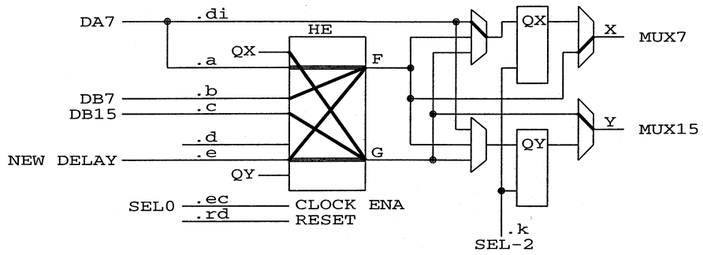
COMPARATOR

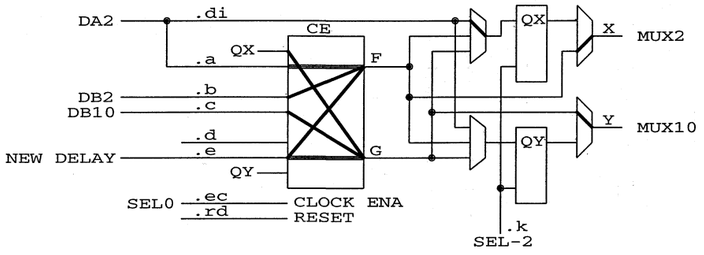
VLBA CORRELATOR PROJECT

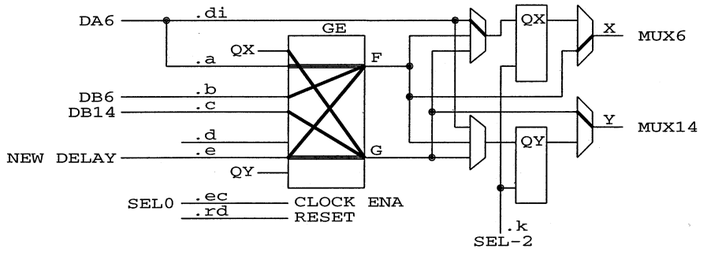
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

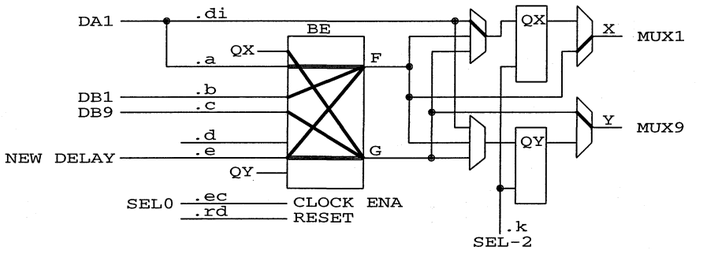
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Size: B	Document Number: 56000K009 (K009D05.BLK)	REV:
Date: February 12, 1990	Sheet: 5 of 10	

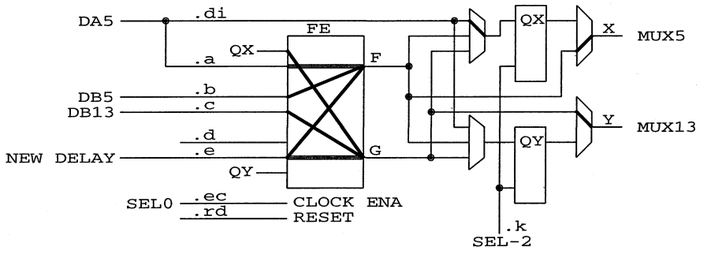


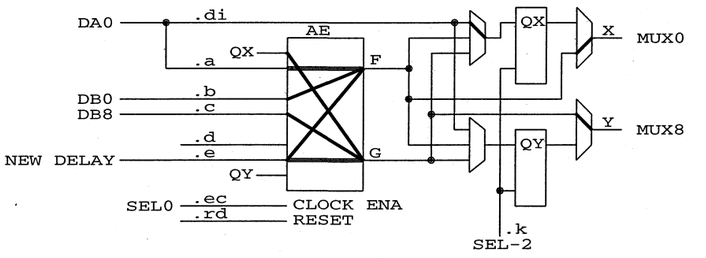


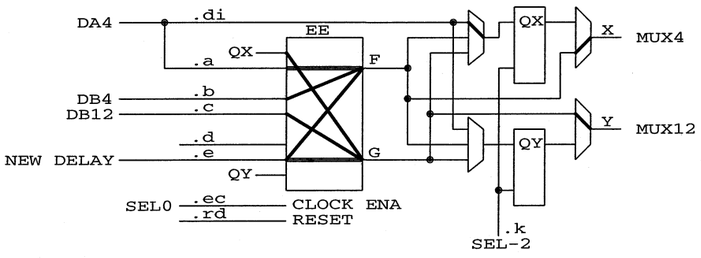


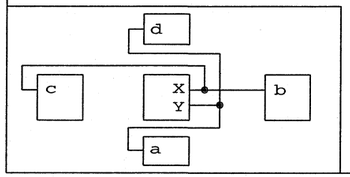












NOTE: THE MUX ABOVE WILL CONTROL WHETHER A NEW DELAY ININIAL DELAY ADDRESS OR A HEADER SKIP ADDRESS IS LOADED INTO THE DELAY COUNTER. THE HEADER SKIP ADDRESS IS STORED IN THE DBXX REGISTER AND THE INITIAL DELAY ADDRESS IS STORED IN THE DAX REGISTER, 8 BITS OF WHICH IS STORED IN THE MUX LOGIC BLOCKS.

MUX

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

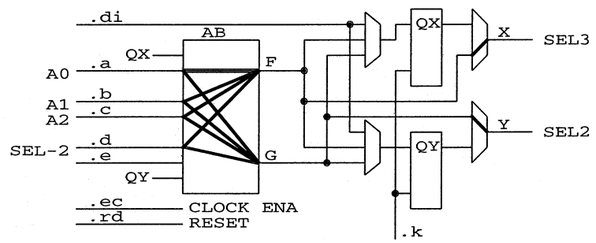
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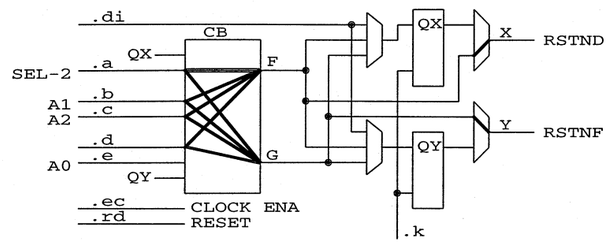
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Date: October 30, 1988	Sheet 6 of 10	

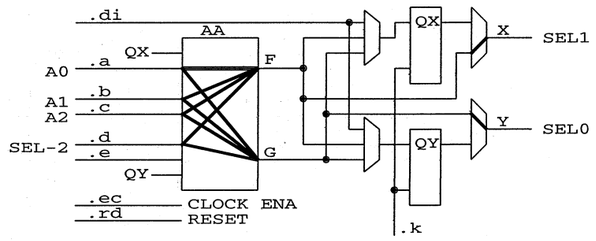
MICROPROCESSOR MEMORY MAP

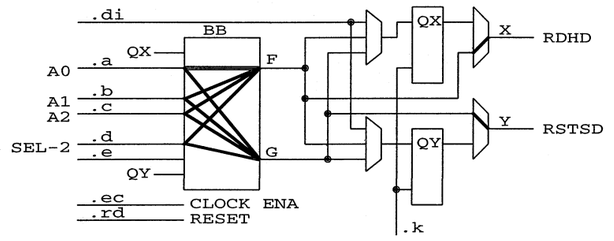
A2	A1	A0	SIGNAL	FUNCTION	
0	0	0	SEL0	WRITE INITIAL DELAY	6020
0	0	1	SEL1	WRITE HEADER SKIP ADDRESS	6021
0	1	0	SEL2	WRITE HEADER START ADDRESS	6022
0	1	1	SEL3	WRITE TRACK MIX PROGRAM BITS	6023
1	0	0	RDHD	READ MONITOR DATA	6024
1	0	1	RSTSD	RESET SYNC DET INTERRUPT	6025
1	1	0	RSTNF	RESET NEW FRAME INTERRUPT	6026
1	1	1	RSTND	RESET NEW DELAY INTERRUPT	6027

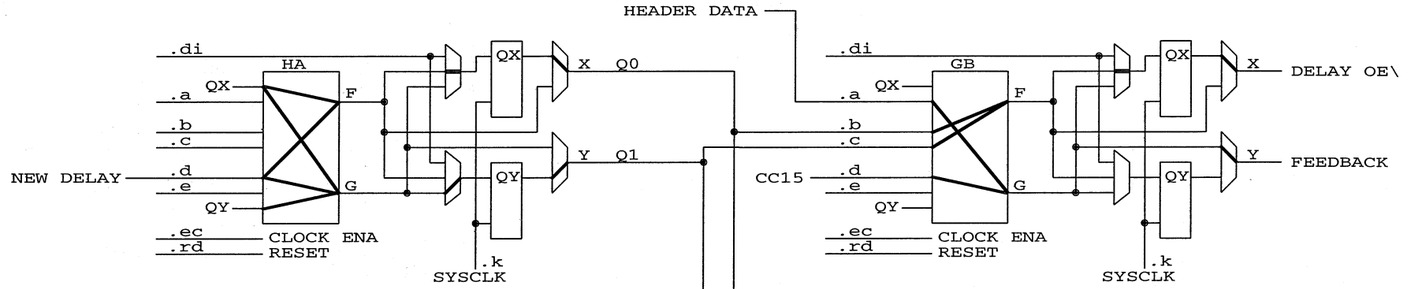
NOTE: SEL LINES ARE ACTIVE TRUE.

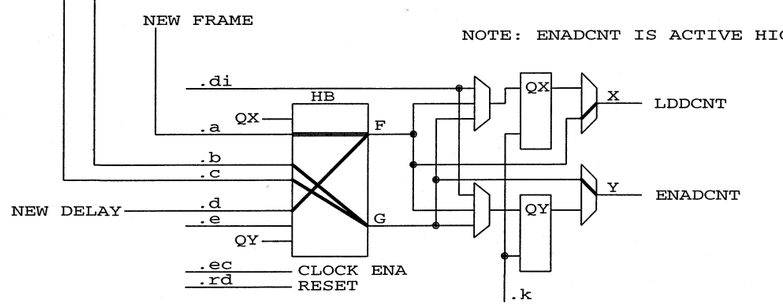




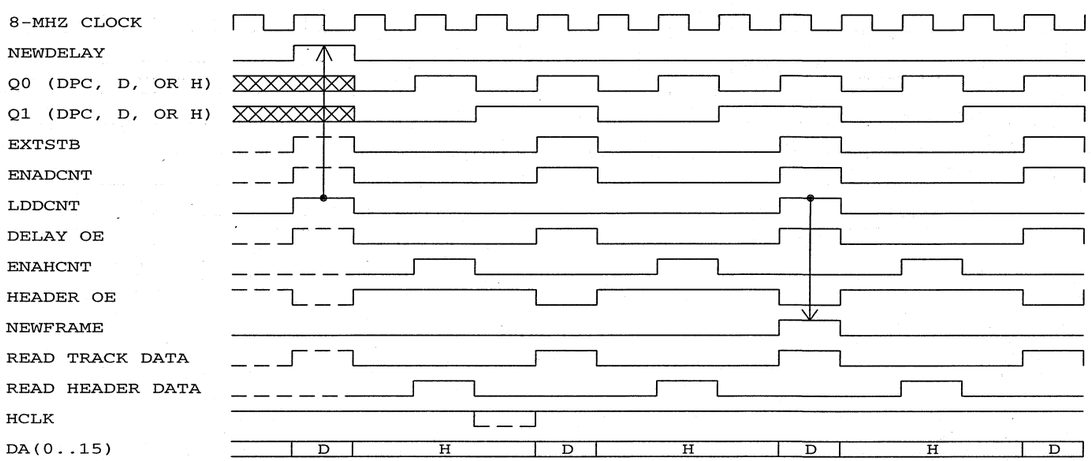








NOTE: ENADCNT IS ACTIVE HIGH.



D CONTROL LOGIC

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

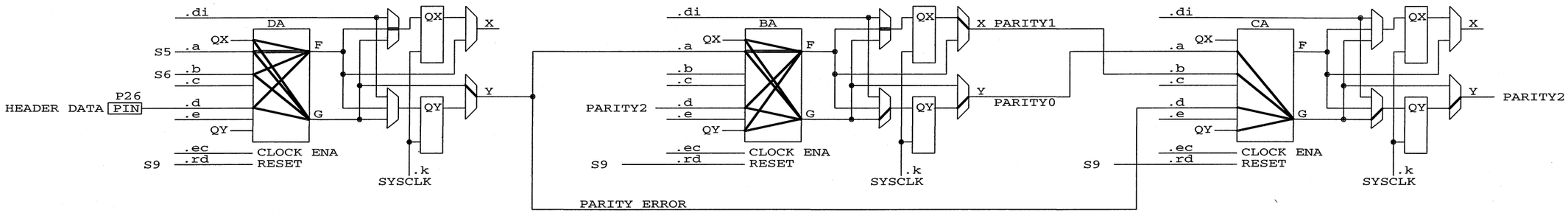
Title
DELAY CONTROL XILINX DESIGN

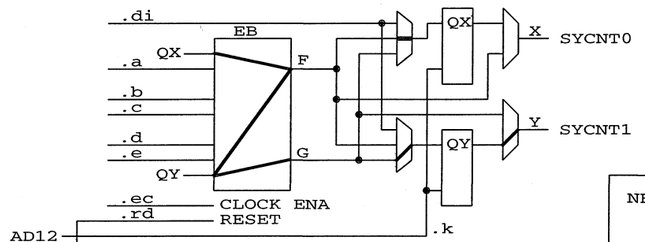
Size	Document Number	REV
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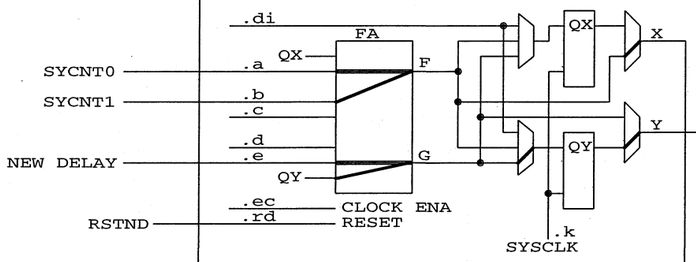
Date: December 19, 1996 Sheet 7 of 10

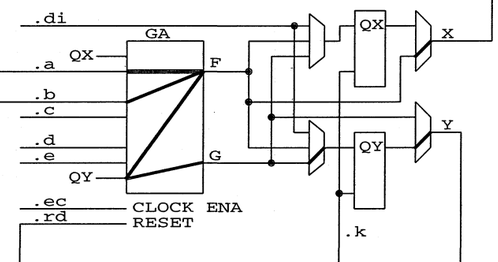
S6	S5	FUNCTION
0	0	HOLD
0	1	COUNT PARITY
1	0	CHECK ODD PARITY
1	1	CHECK EVEN PARITY

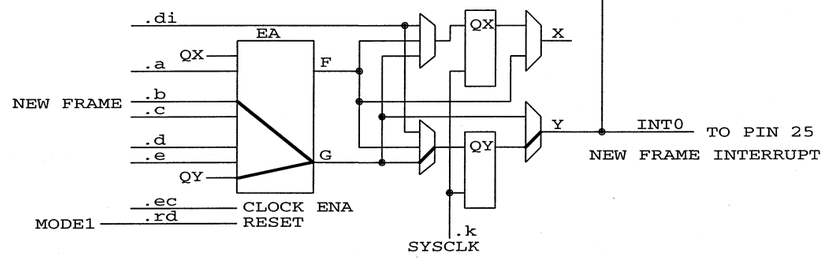
NOTE: WHEN HEADER PARITY ERROR IS HIGH THE THREE BIT COUNTER BELOW WILL INCREMENT (HOLDING AT 111).

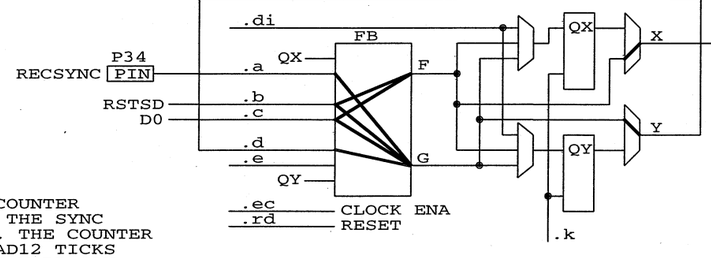












INT1 — TO PIN 27
NEW DELAY INTERRUPT

P30
PIN XINTRR
(LOGIC 0 = INTERRUPT ASSERTION)

INT2 — TO PIN 29
SYNC DETECTED INTERRUPT
(STATUS LINE READ BY 87C51)
(LOGIC 1 = INTERRUPT SOURCE IS SYNC)

○ = NEGATIVE EDGE CLOCK

P19 PIN — PARITY CONT 1 — S5
P21 PIN — PARITY CONT 2 — S6
P35 PIN — CRCC CLOCK ENABLE — S8
P33 PIN — HEADER RESET — S9

CLB EB IS A 2-BIT COUNTER THAT IS RESET WHEN THE SYNC INTERRUPT IS RESET. THE COUNTER MUST THEN COUNT 3 AD12 TICKS BEFORE ANOTHER SYNC WORD CAN BE DETECTED. THIS ACTION INSURES THAT THE DEF WILL HAVE SOME TIME TO TALK TO THE TRC uPROC EVEN WHEN THE TRACK DATA INPUT GOES WILD AND HAS MANY SYNC WORDS.

A uPROC SYNC INTERRUPT WILL OCCUR FROM EITHER A PULSE ON THE RECSYNC LINE OR THE uPROC CAN CAUSE ONE BY TRYING TO RESET THE INTERRUPT WITH D0 HIGH. THE FUNCTION OCCURS IN CLB FB.

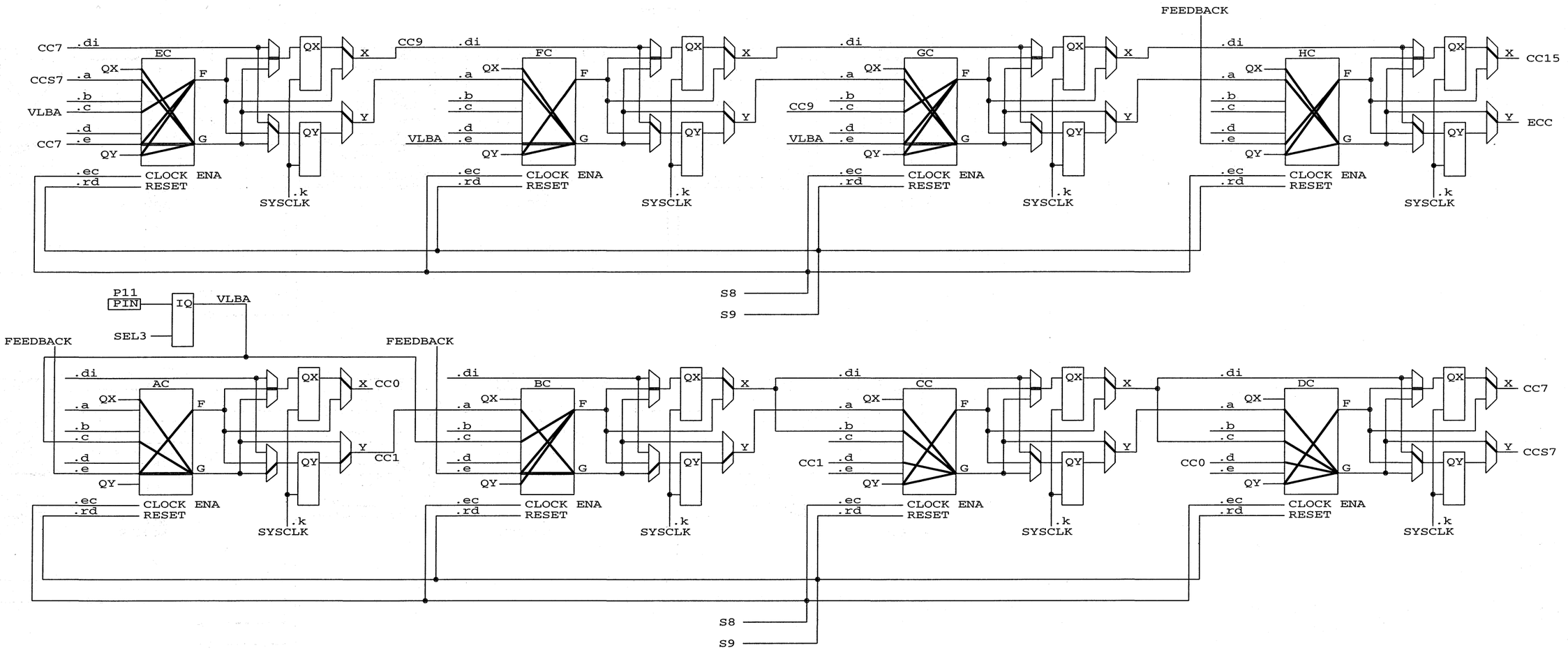
PARITY AND INTERRUPT

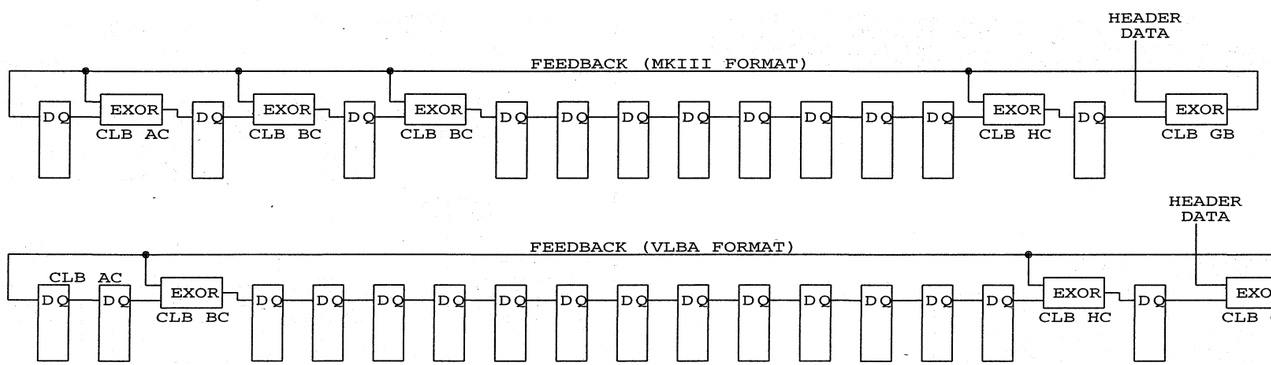
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DELAY CONTROL XILINX DESIGN

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NOTE: TO CKECK AN ECC WORD FOR ERRORS THE ECC REGISTER ABOVE IS RESET AND ALL BITS OF THE ECC WORD ARE CLOCKED INTO IT. IF AFTER THE LAST ECC WORD BIT IS CLOCKED THE ECC REGISTER IS AT ALL ZEROS, THE WORD IS VALID.

THE FF IN THE VLBA SIGNAL LINE IS THERE TO LOWER THE CHANCE OF A MICRO P1 PORT GLITCH FROM BEING CAPTURED. SEL3 IS A CONVIENT SIGNAL THAT OCCURS ONLY AT THE START OF AN OBSERVATION.

CRC CHECKER

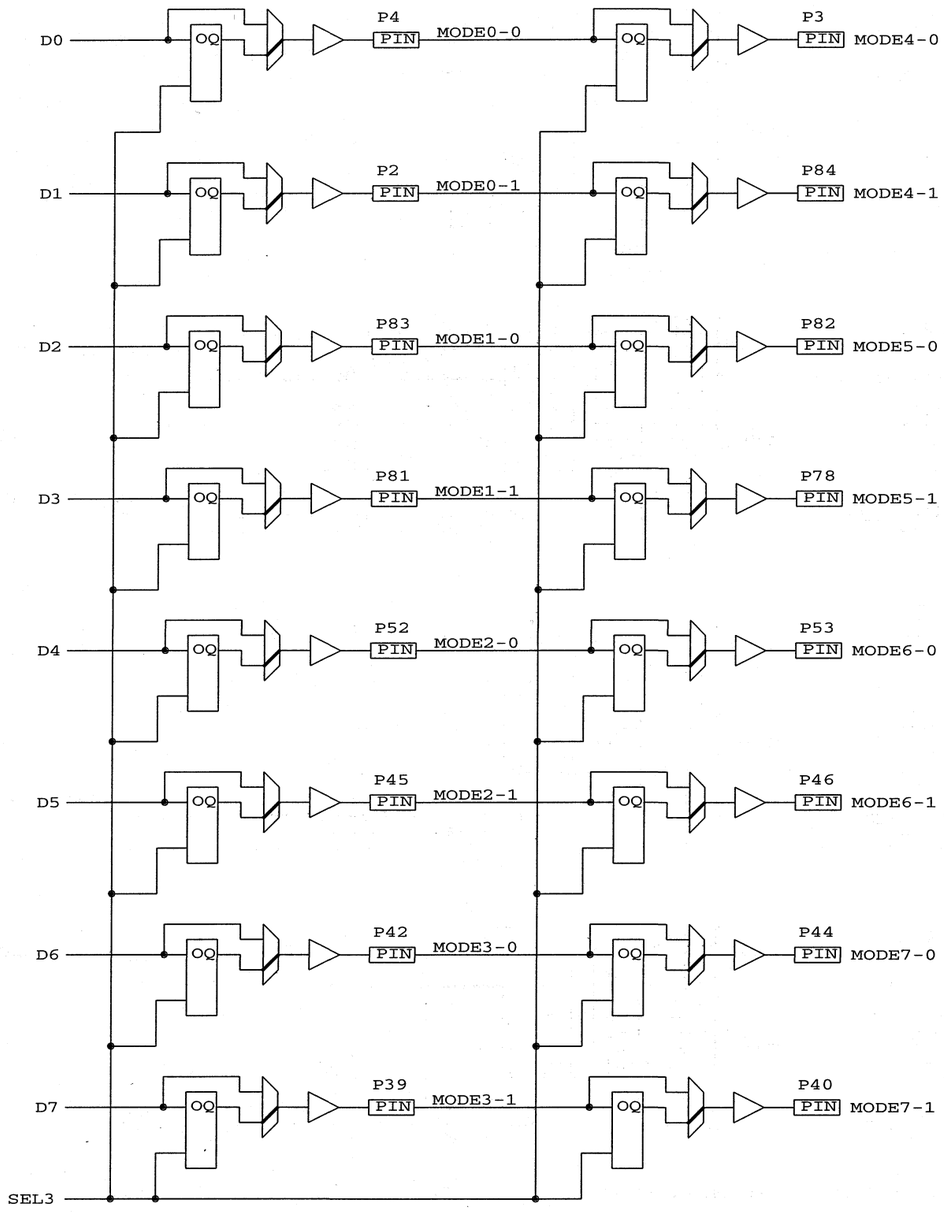
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

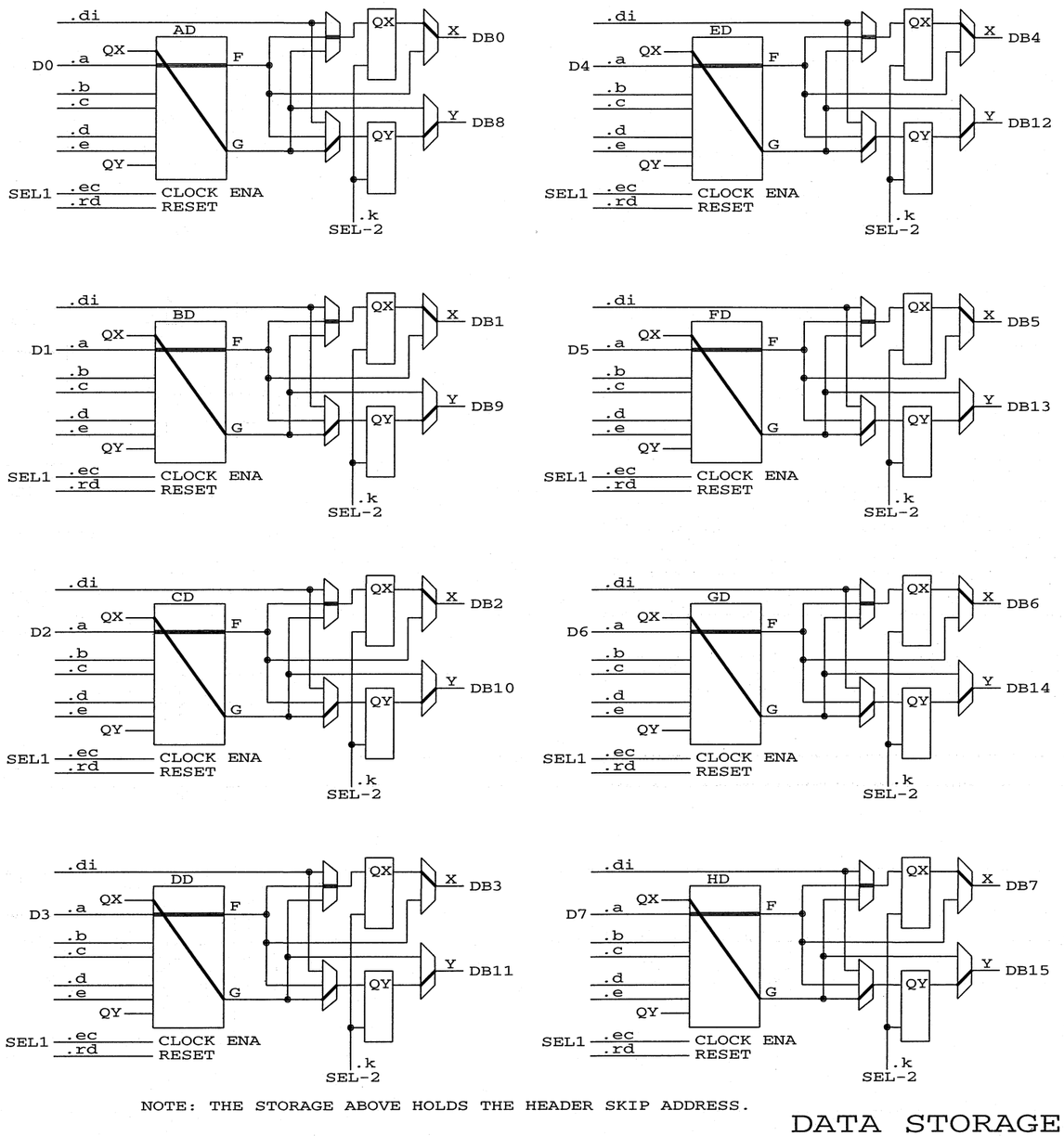
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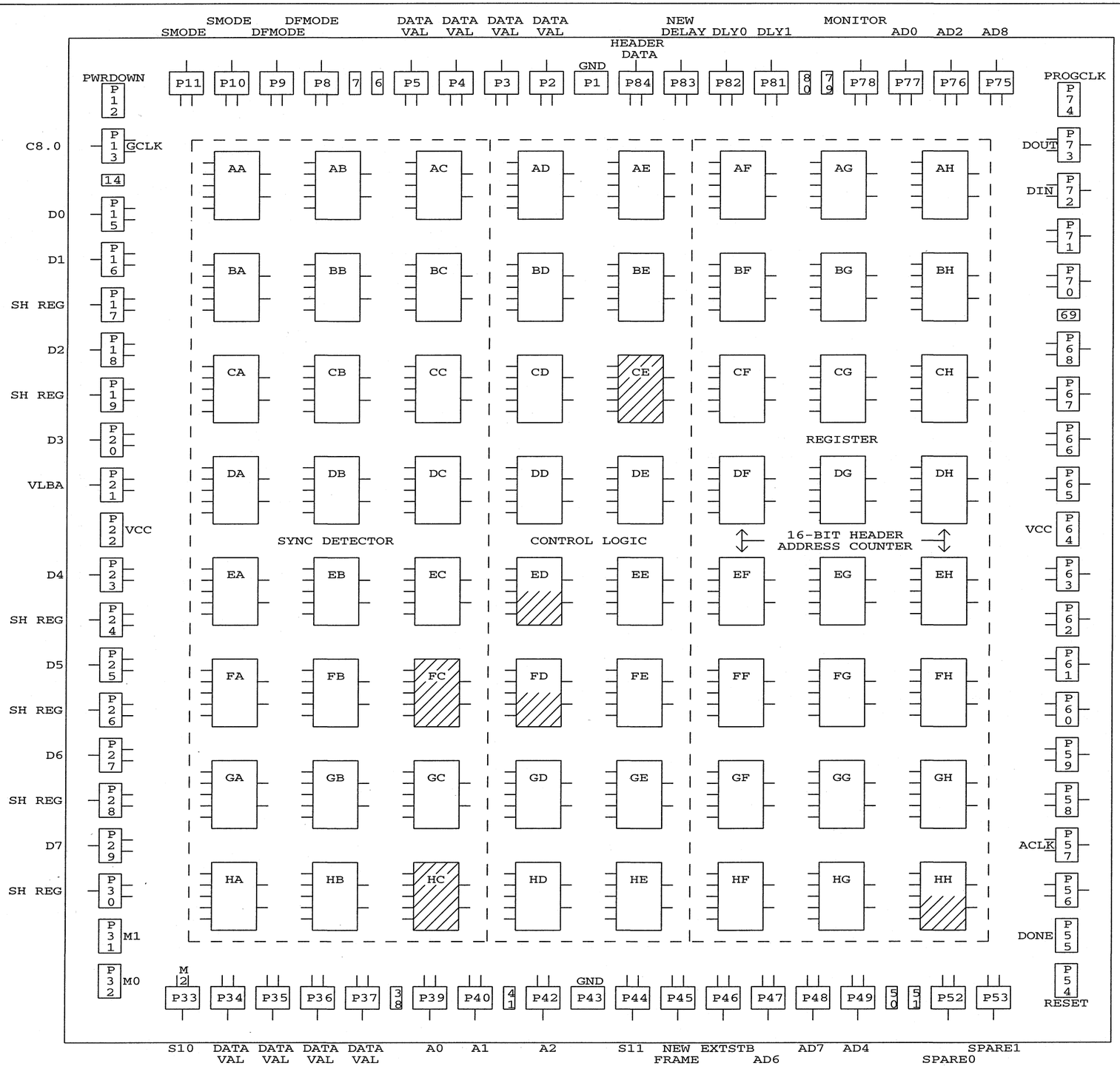
NOTE: THE OUTPUT PINS ABOVE PROGRAM THE TRACK MIX/TRACK COPY PALS.



NOTE: THE STORAGE ABOVE HOLDS THE HEADER SKIP ADDRESS.

DATA STORAGE

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DELAY CONTROL XILINX DESIGN		
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UPROC INPUT H
K010D02.BLK

HEADER CNTR SH1
K010D03.BLK

HEADER CNTR SH2
K010D04.BLK

SYNC DETECTOR SH1
K010D05.BLK

SYNC DETECTOR SH2
K010D06.BLK

SYNC DETECTOR SH3
K010D07.BLK

H CONTROL LOGIC
K010D08.BLK

DATA REGISTER
K010D09.BLK

MICROPROCESSOR ADDRESSES

WRITE:

HEADER START ADDRESS
CAL NEXT SYNC ADDR
VALIDITY BITS
SERVICE TRACK MIX BITS
DELAY
MONITOR BITS ADDR

READ:

HEADER DATA

MONITOR BITS:

ERROR TOLERANT SYNC DETECTED
SYNC IN WRONG PLACE

SEQUENCER CONTROL BITS

OUTPUT ENA HEADER DATA S10
SYNC PREDICT S11

H FLOOR PLAN

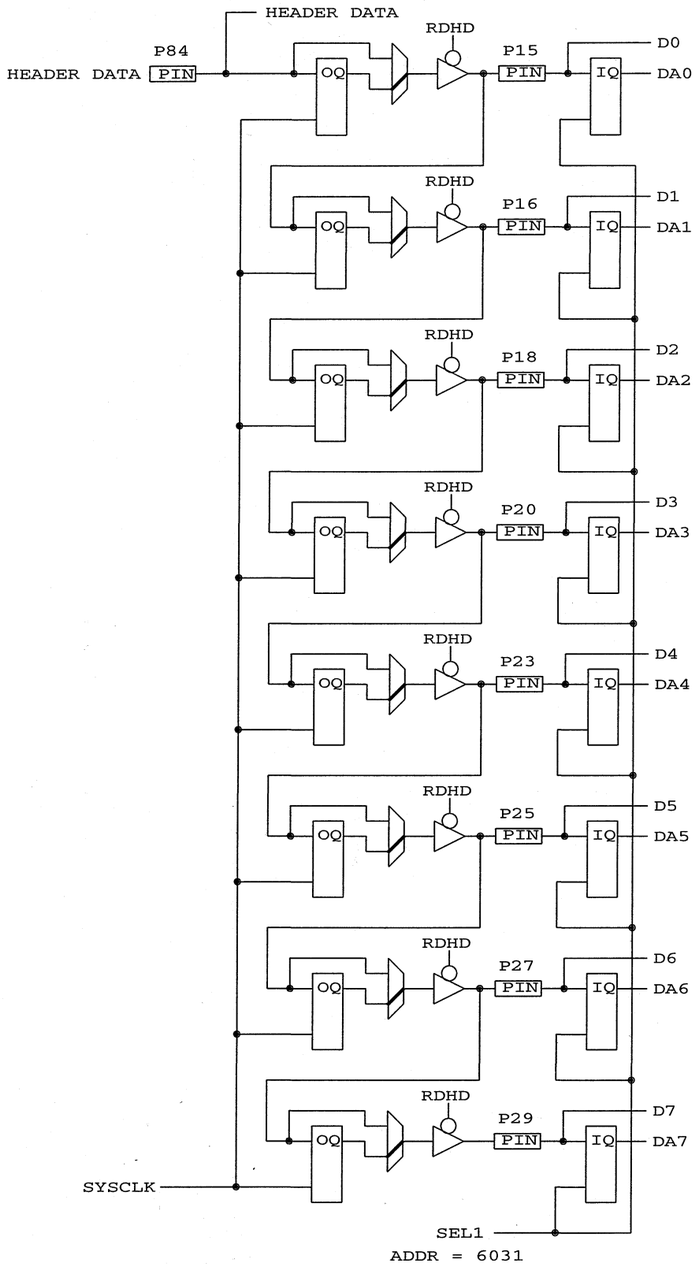
VLBA CORRELATOR PROJECT

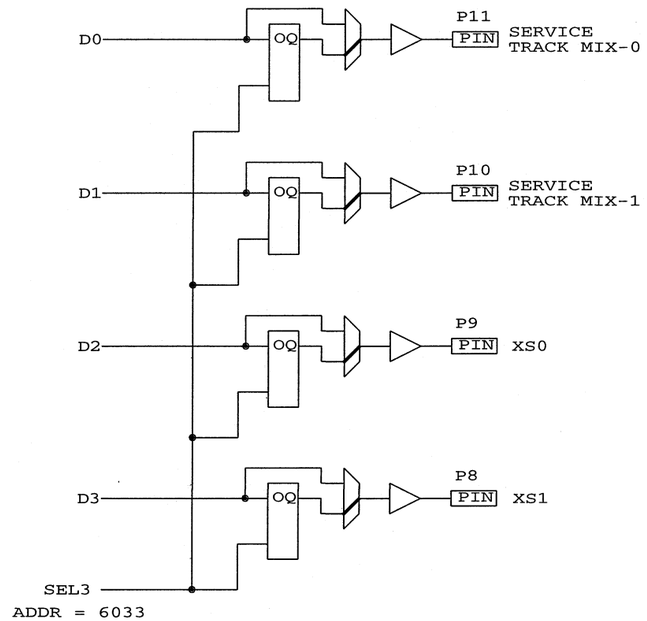
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: HEADER CONTROL XILINX DESIGN

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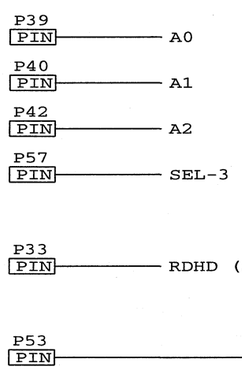
Date: December 19, 1996 Sheet 1 of 9

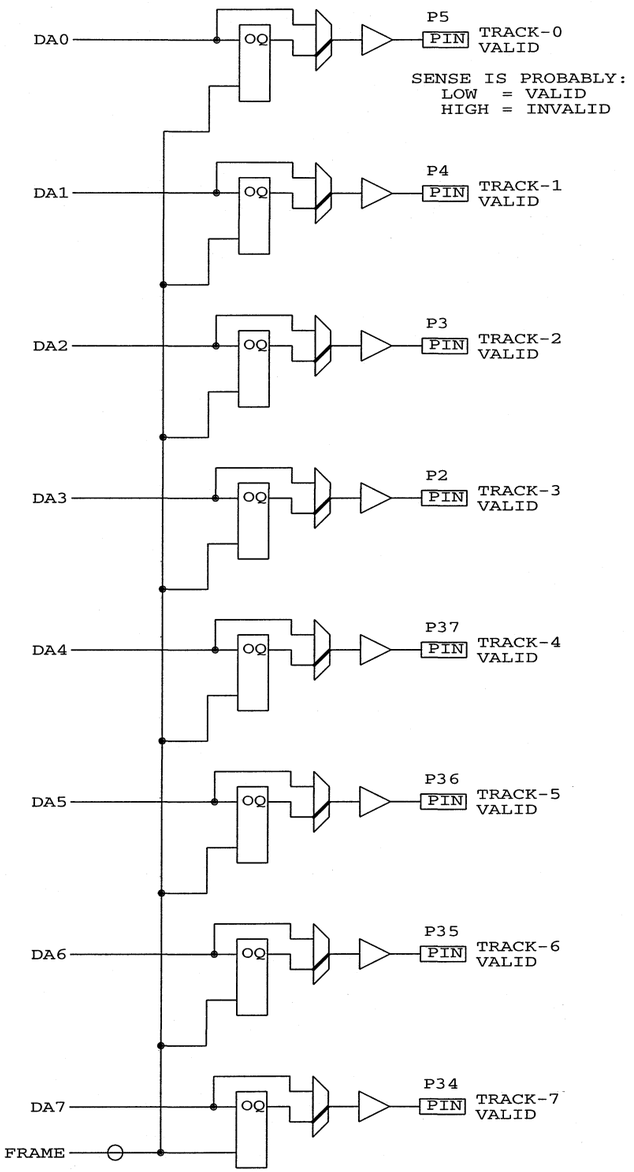




MEMORY MAP

A2	A1	A0	FUNCTION
0	0	0	HEADER ADDR/NEXT SYNC ADDR
0	0	1	WRITE DATA VALID BITS
0	1	0	WRITE MONITOR CODE
0	1	1	WRITE SERVICE TRACK MIX BITS
1	0	0	WRITE DELAY VALUE
1	0	1	
1	1	0	
1	1	1	





DA(0..7) ARE THE CHANNEL VALID BITS. THEY ARE STORED HERE AND CAPTURED ON THE NEW FRAME SIGNAL. (PROBABLY ONLY DA0 AND DA1 USED)

MICROPROCESSOR INPUT H

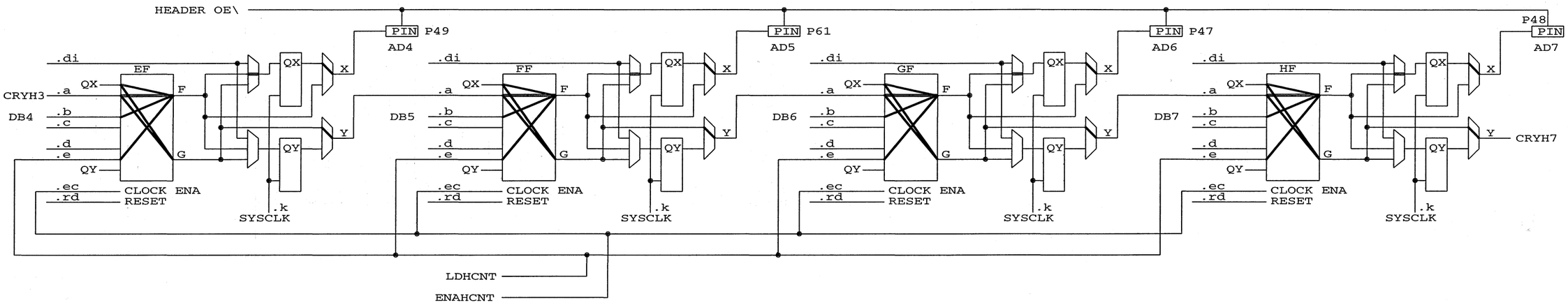
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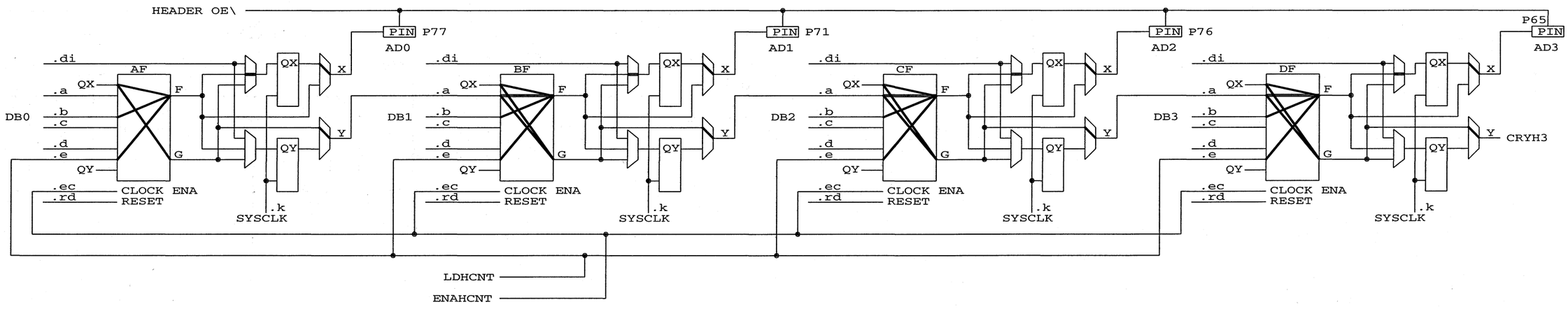
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

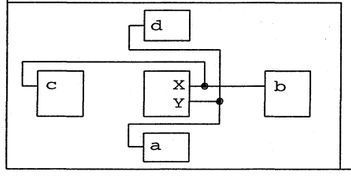
Title: HEADER CONTROL XILINX DESIGN

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THE 16-BIT COUNTER ON THIS AND THE NEXT SHEET HAS TWO FUNCTIONS. DURING HEADER DATA READOUT, IT IS PARALLEL LOADED WITH THE START ADDRESS OF THE TRACK HEADER IN THE TRACK RECOVERY RAM BUFFER AND COUNTES THROUGH THE HEADER CONTENTS FOR SHIFT OUT AND SUBSEQUENT DMA INTO THE uPROCESSOR MEMORY. EXCEPT FOR THIS BRIEF TIME IT SPENDS MOST OF THE TIME BEING PARALLEL LOADED WITH THE CALCULATED NEXT SYNC ADDRESS SO THAT WHEN THE TRACK RECOVERY XILINX CHIP DETECTS A SYNC CODE IN THE TRACK DATA, THE TRACK RECOVERY CHIPS' 16-BIT ADDRESS COUNTER WILL BE PARALLEL LOADED WITH THE PROPER ADDRESS. THIS ACTION IS NEEDED ONLY IF THE RECOVERED TRACK CLOCK LOST SYNC DURING THE LAST FRAME AND SLIPPED A BIT.

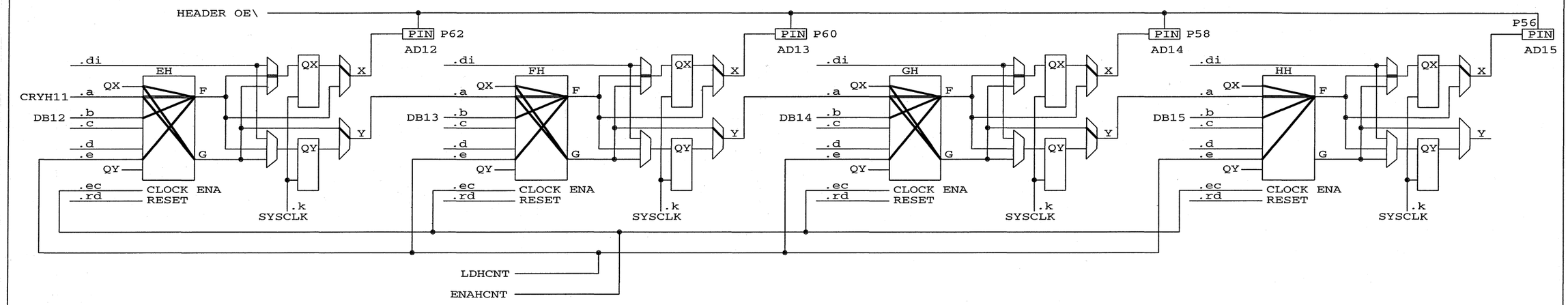
HEADER COUNTER SH 1

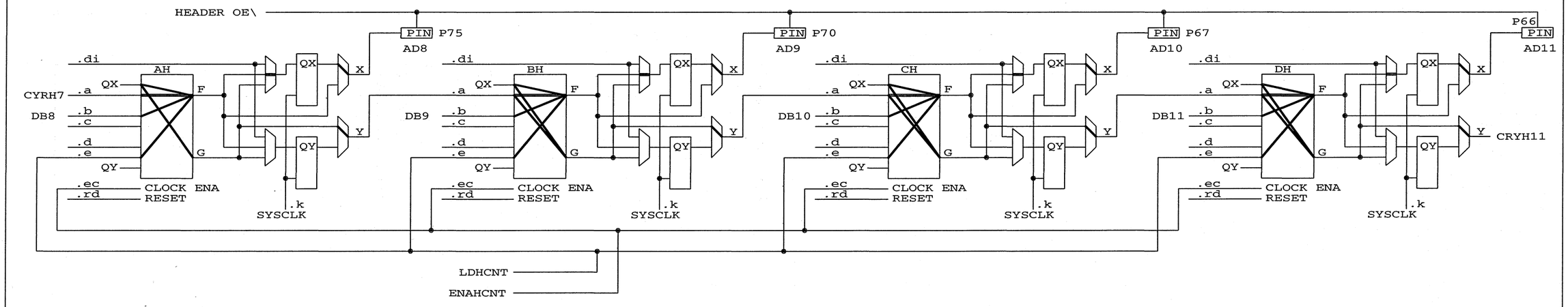
VLBA CORRELATOR PROJECT

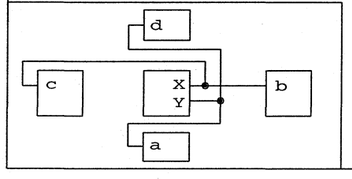
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
HEADER CONTROL XILINX DESIGN

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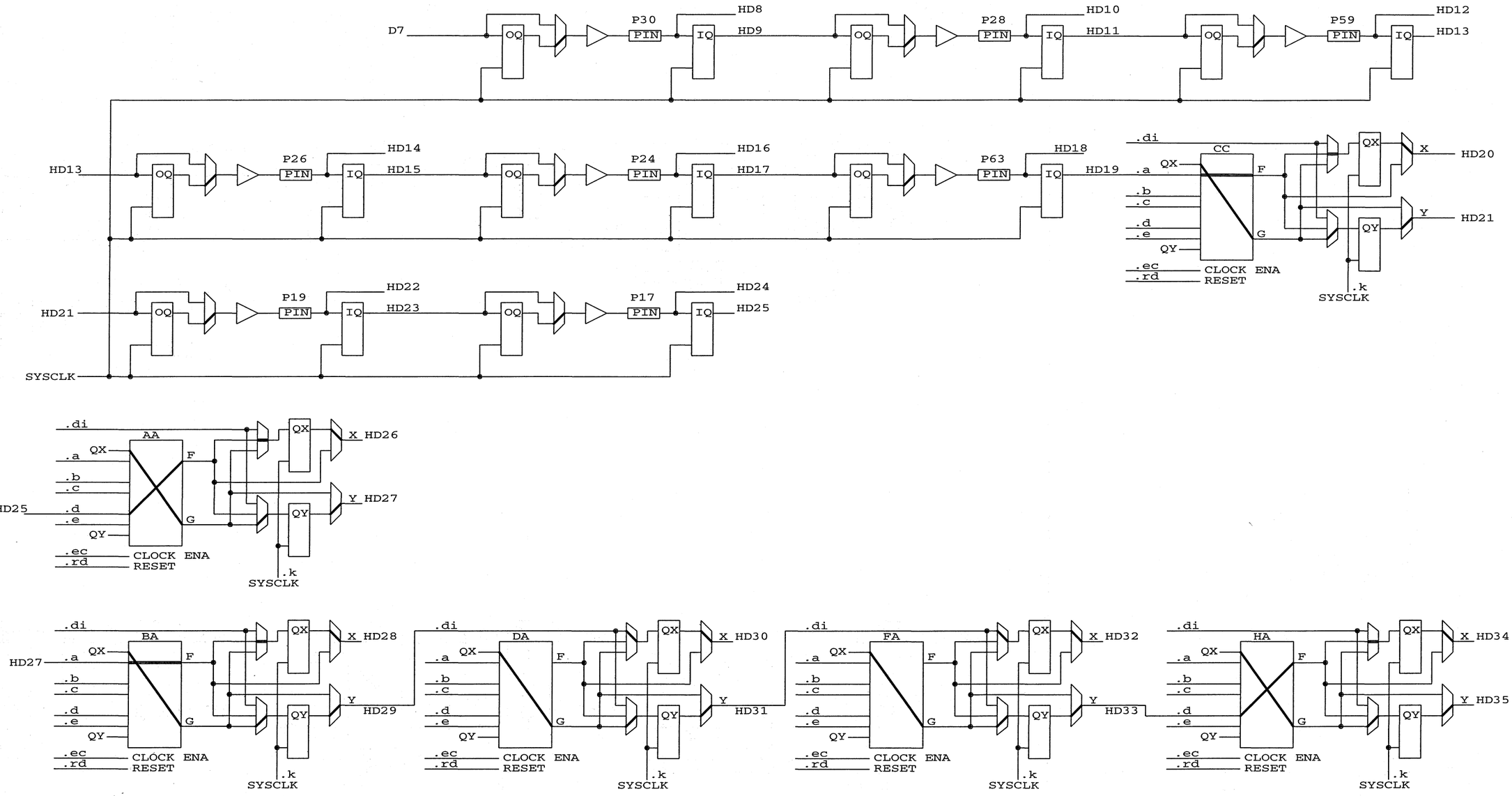
HEADER COUNTER SH 2

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: HEADER CONTROL XILINX DESIGN

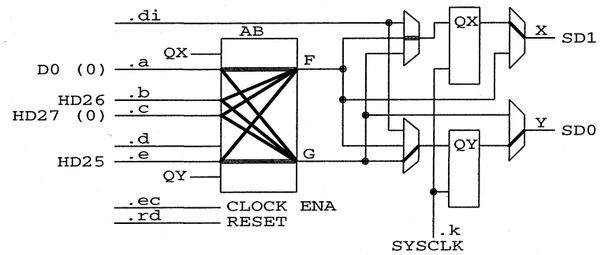
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Date: February 12, 1990	Sheet 4 of 9	

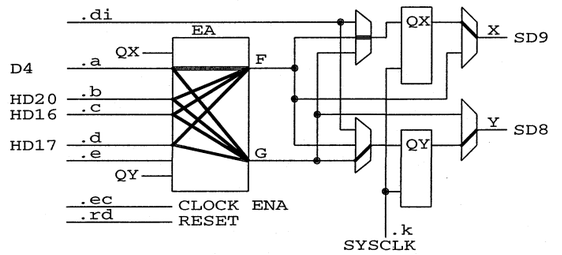


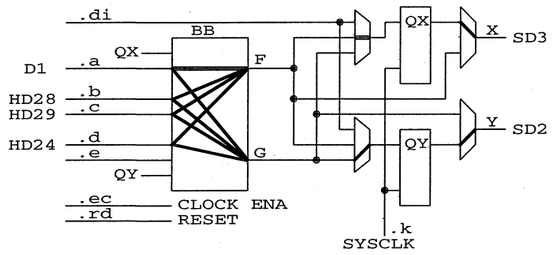
THIS LOGIC, TOGETHER WITH THE 8-BIT SHIFT REGISTER FORMED BY I/O PINS 12 THRU 23 ON SHEET 2, FORM A 40-BIT SHIFT REGISTER. THIS 40-BIT SHIFT REGISTER GIVES THE SYNC DETECT LOGIC A 40-BIT WINDOW IN THE HEADER DATA IN WHICH TO LOOK FOR THE SYNC CODE.

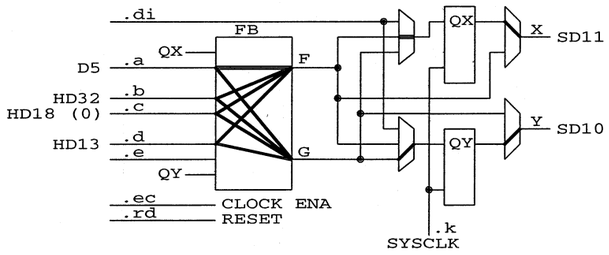
SYNC DETECTOR SH 1

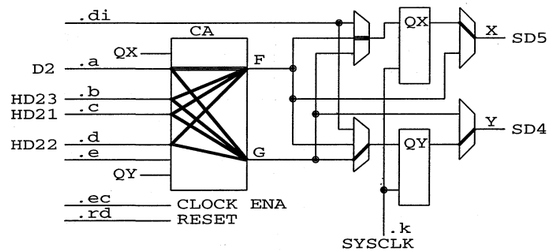
VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: HEADER CONTROL XILINX DESIGN		
Size: B	Document Number: 56000K010 (K010D05.BLK)	REV:
Date: February 14, 1991	Sheet 5 of 9	

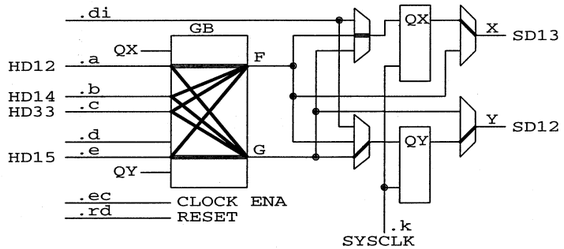


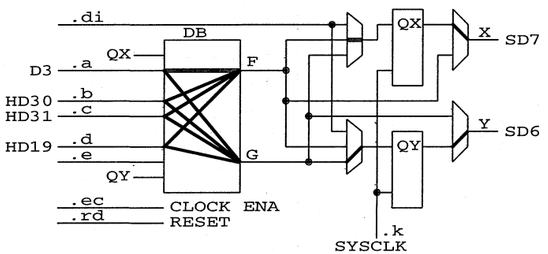


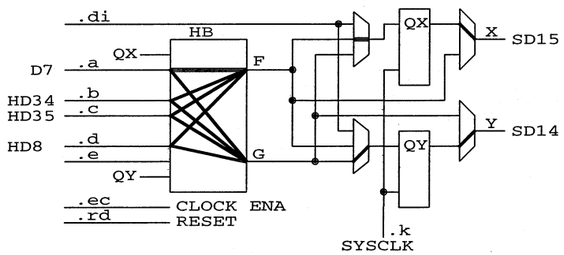


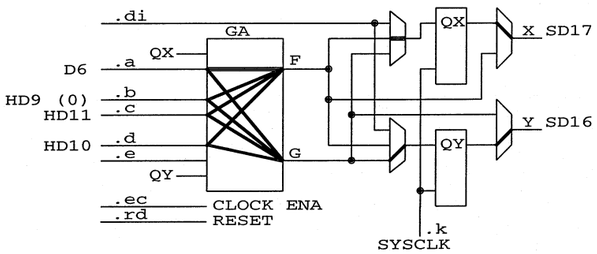










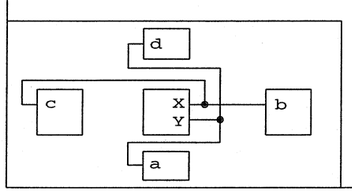


SIGNAL	MARK III SYNC PATTERN
D0	0 LAST BIT IN
D1	1
D2	1
D3	1
D4	1
D5	1
D6	1
D7	1
HD8	1
HD9	0
HD10	1
HD11	1
HD12	1
HD13	1
HD14	1
HD15	1
HD16	1
HD17	1
HD18	0
HD19	1
HD20	1
HD21	1
HD22	1
HD23	1
HD24	1
HD25	1
HD26	1
HD27	0
HD28	1
HD29	1
HD30	1
HD31	1
HD32	1
HD33	1
HD34	1
HD35	1 FIRST BIT IN

NOTE: EACH LOGIC BLOCK ABOVE LOOKS AT FOUR BITS OF SERIAL DATA AND PROVIDES AN OUTPUT THAT REFLECTS THE NUMBER OF BITS THAT DEVIATES FROM THE TRACK SYNC PATTERN. THE CHART BELOW FOR LOGIC BLOCK AB ILLUSTRATES THIS FUNCTION.

D0	HD26	HD27	HD25	NO. OF ERRORS	SD1	SD0
0	1	0	1	0	0	0
0	1	0	0	1	0	1
0	1	1	1	1	0	1
0	0	0	1	1	0	1
1	1	0	1	1	0	1
0	1	1	0	2	1	0
0	0	1	1	2	1	0
0	0	0	0	2	1	0
1	0	1	1	3	1	1
1	0	1	1	3	1	1
1	0	1	0	4	1	1

NOTE THAT THIS IS AN INCOMPLETE CHART, THERE ARE 3 ADDITIONAL WAYS TO MAKE 2 ERRORS AND 2 MORE WAYS TO MAKE 3 ERRORS. ALSO NOTE THAT THE ERROR COUNT LIMITS AT 3 ERRORS.



SYNC DETECTOR SH 2

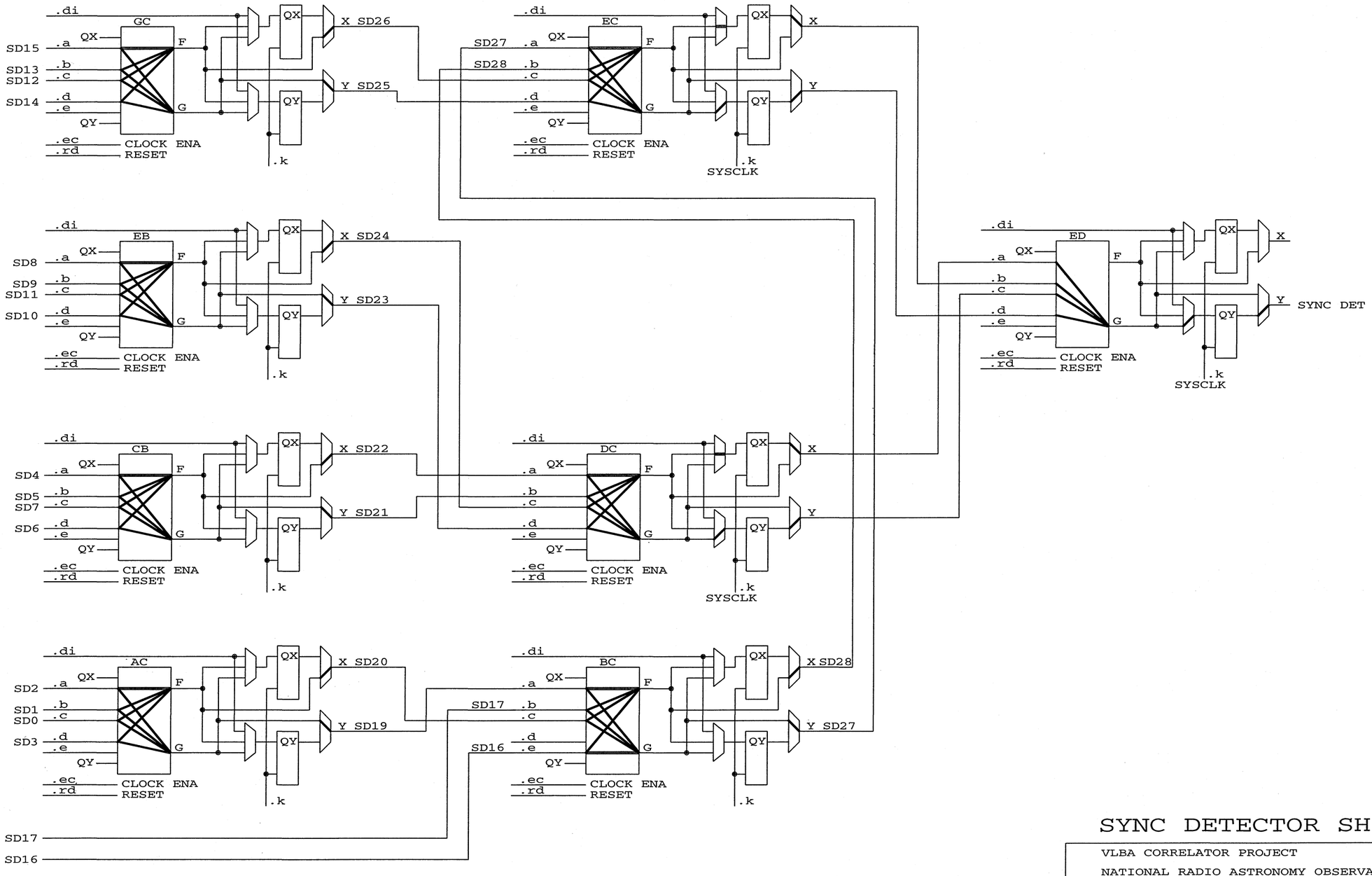
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: HEADER CONTROL XILINX DESIGN

Size	Document Number	REV
B	56000K010 (K010D06.BLK)	

Date: October 30, 1988 Sheet 6 of 9



THIS LOGIC FUNCTIONS AS AN ADDER. NINE TWO BIT INPUTS ARE SUMMED TOGETHER. IF THIS SUM, WHICH IS THE NUMBER OF BITS IN THE PRESENT 40-BIT WINDOW THAT DEPART FROM THE SYNC CODE, IS TWO OR LESS THE SYNC DET OUTPUT WILL GO HIGH.

SYNC DETECTOR SH 3

VLBA CORRELATOR PROJECT

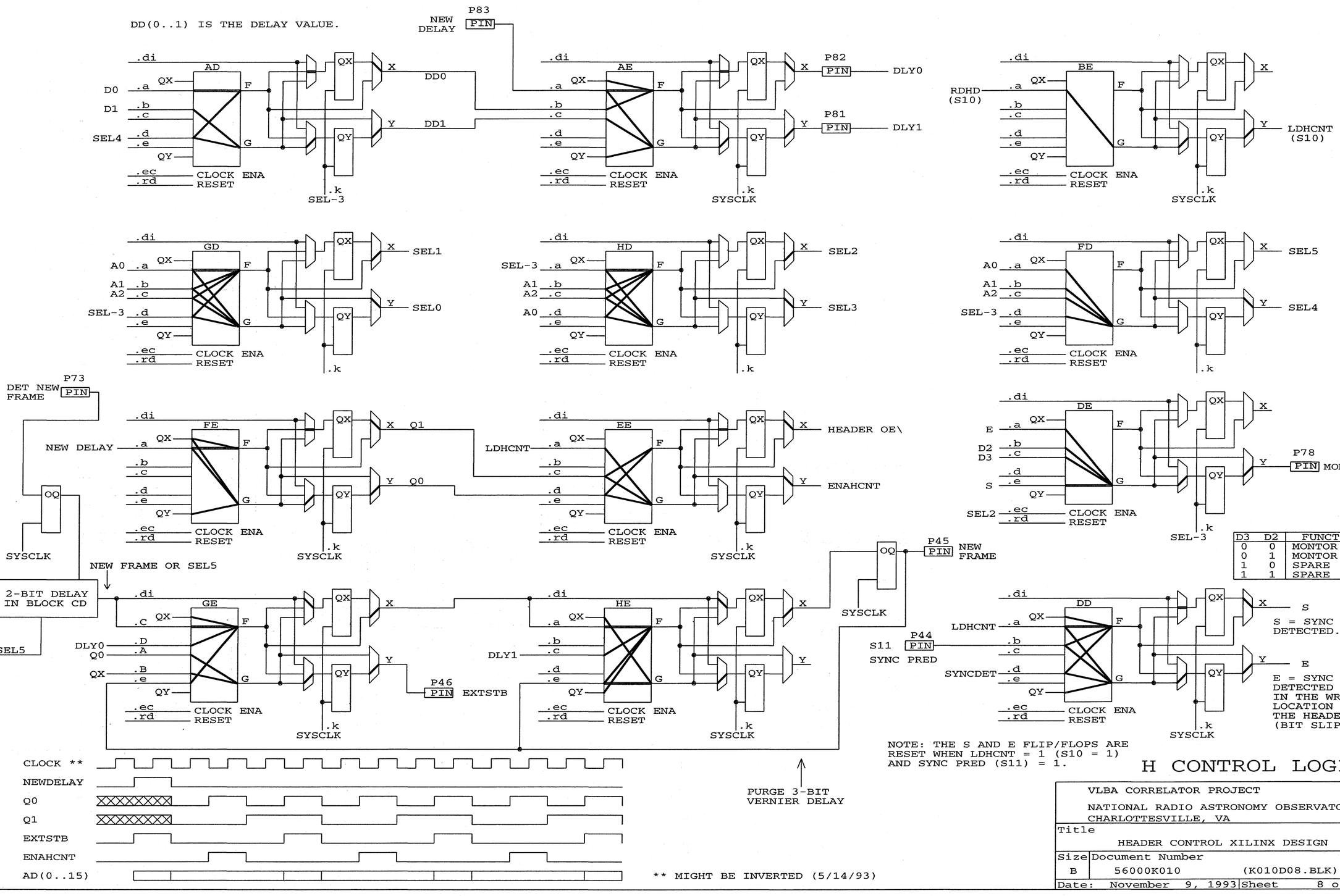
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: HEADER CONTROL XILINX DESIGN

Size	Document Number	REV
B	56000K010 (K010D07.BLK)	

Date: October 30, 1988 | Sheet 7 of 9

DD(0..1) IS THE DELAY VALUE.



D3	D2	FUNCTION
0	0	MONTOR = S
0	1	MONTOR = E
1	0	SPARE
1	1	SPARE

S = SYNC WORD DETECTED.

E = SYNC WAS DETECTED BUT IN THE WRONG LOCATION IN THE HEADER (BIT SLIP).

NOTE: THE S AND E FLIP/FLOPS ARE RESET WHEN LDHCNT = 1 (S10 = 1) AND SYNC PRED (S11) = 1.

** MIGHT BE INVERTED (5/14/93)

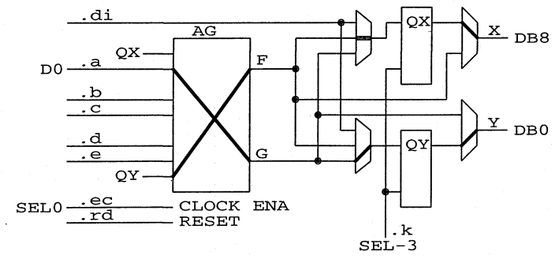
H CONTROL LOGIC

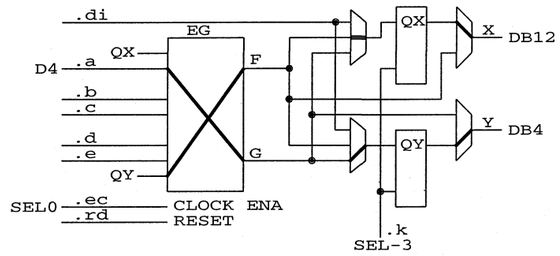
VLBA CORRELATOR PROJECT

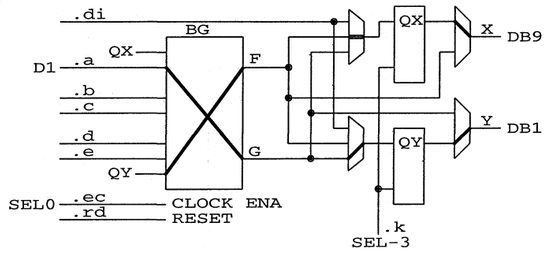
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

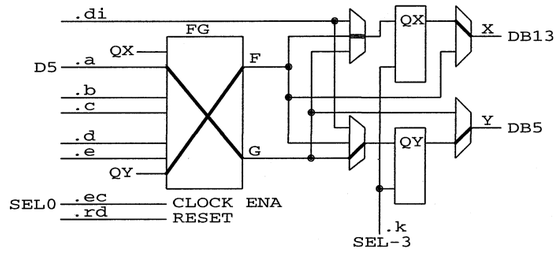
Title: HEADER CONTROL XILINX DESIGN

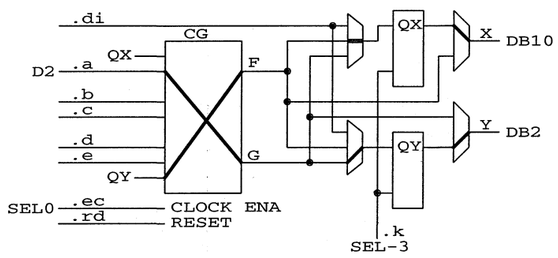
Size	Document Number	REV
B	56000K010 (K010D08.BLK)	
Date: November 9, 1993	Sheet 8 of 9	

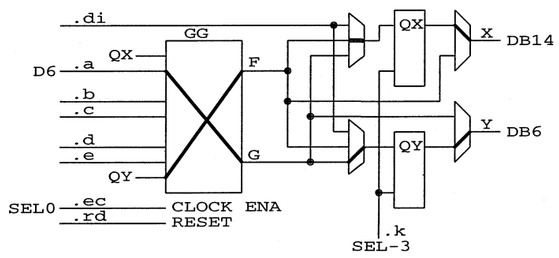


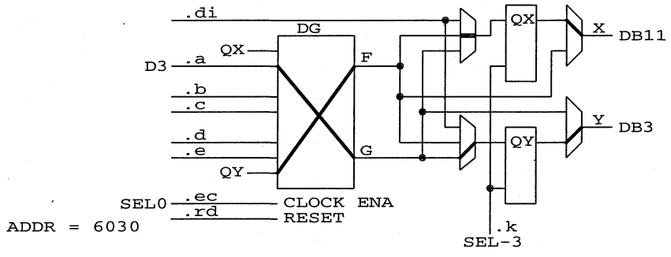




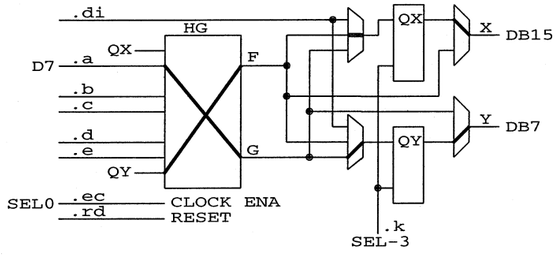








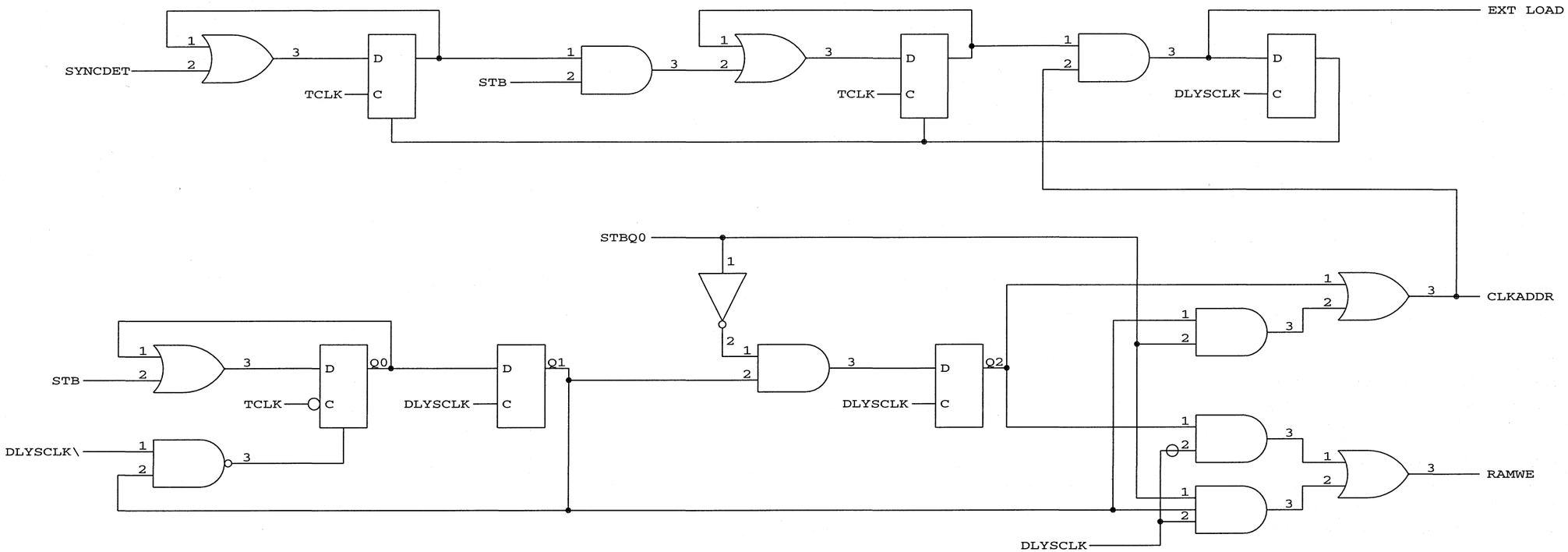
ADDR = 6030

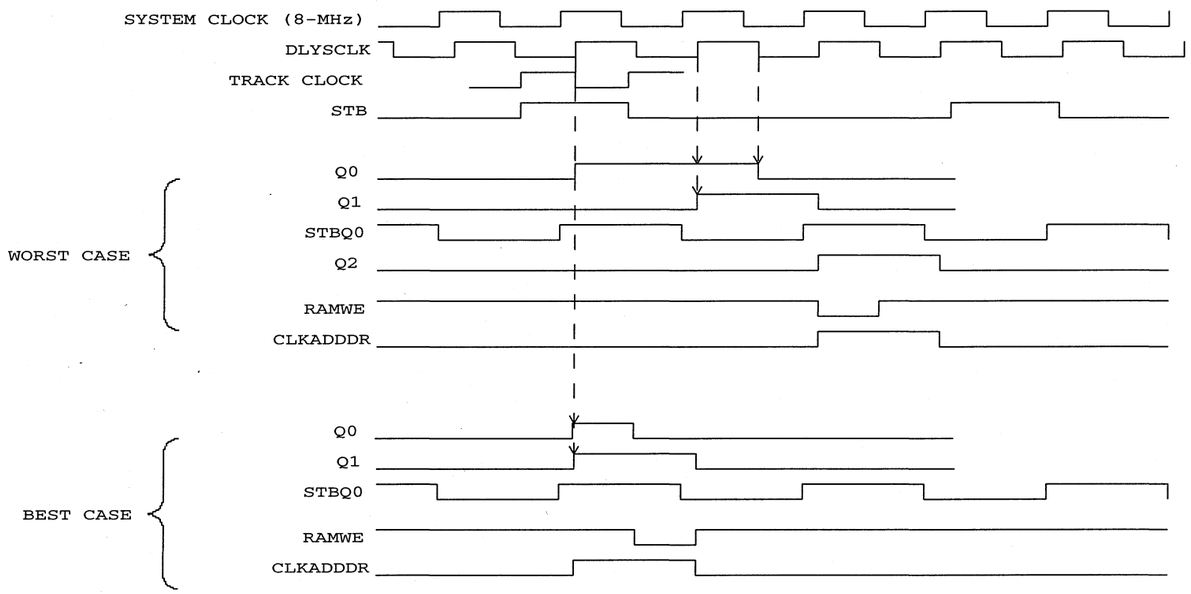


NOTE: THE STORAGE REGISTER HAS A DUAL FUNCTION. MOST OF THE TIME THE NEXT SYNC ADDRESS IS STORED IN IT BUT DURING HEADER READOUT TIME IT STORES THE HEADER START ADDRESS.

DATA REGISTER

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: HEADER CONTROL XILINX DESIGN		
Size: B	Document Number: 56000K010 (K010D09.BLK)	REV:
Date: November 25, 1989	Sheet 9 of 9	





Title: WRITE OPERATIONS INTO TRACK BUFFER		
Size: B	Document Number: WRITE.DPC	REV
Date: December 19, 1996	Sheet 1 of 1	

Volume 2 Section 2

Deformatter Card Drawings

Drawing Number and/or Filename	Title	Nr of Sheets
56000L008 (L008D01.SCH - L008D31.SCH)	Deformatter Schematics	31
56000Z009 (Z009D01.LAY - Z009D02.LAY)	Deformatter Layout	2
(DEFTOP.PAL, K014D01.PAL, K015D01.PAL, K015D02.PAL, K019D01.PAL, K019D02.PAL, K020D01.PAL, K021D03.PAL, K022D01.PAL, K022D02.PAL, K023D01.PAL, K023D02.PAL, K024D01.PAL, K025D01.PAL, K026D01.PAL)	Deformatter Pals	15
56000K012 (K012D01.xxx - K012D12.xxx)	Xilinx Barrel Roll Control	12
56000K013 (K013D01.xxx - K013D12.xxx)	Data Invalid Xilinx	12
BSP-0.SCH	Bit Shuffler Personality 0	1
BSP-1.SCH	Bit Shuffler Personality 1	1
(BSP2BLK.SCH, BSP2X01.SCH - BSP2X11.SCH)	Bit Shuffler Personality 2	12

(Bit Shuffler Personalities 3 through 9 not included)

P1A: GND, +5V, A0C71a, A0C7\1a, A0C60a, A0C6\0a, A0C41a, A0C4\1a, A0C31a, A0C3\1a, A0C20a, A0C2\0a, A0C01a, A0C0\1a, A0C71b, A0C7\1b, A0C60b, A0C6\0b, A0C41b, A0C4\1b, A0C31b, A0C3\1b, A0C20b, A0C2\0b, A0C01b, A0C0\1b, -5.2V, VAL-A3, +5V, VAL-A6, GND — DIN

P1B: GND, +5V, A0C70a, A0C7\0a, A0C51a, A0C5\1a, A0C40a, A0C4\0a, A0C30a, A0C3\0a, A0C11a, A0C1\1a, A0C00a, A0C0\0a, A0C70b, A0C7\0b, A0C51b, A0C5\1b, A0C40b, A0C4\0b, A0C30b, A0C3\0b, A0C11b, A0C1\1b, A0C00b, A0C0\0b, -5.2V, VAL-A4, +5V, VAL-A7, GND — DIN

P1C: GND, NMI_SW, +5V, A0C61a, A0C6\1a, A0C50a, A0C5\0a, A0C21a, A0C2\1a, A0C10a, A0C1\0a, TR_TEST_CYCLE_EN (no bkpln conn.), A0C61b, A0C6\1b, A0C50b, A0C5\0b, NEW_FRINGE_EN\, 131msTIC_EN, A0C21b, A0C2\1b, A0C10b, A0C1\0b, VAL-A0, VAL-A1, -5.2V, VAL-A2, +5V, VAL-A5, GND — DIN

VCC; Test fixture switch

P2A: GND, ---CK32, +5V, ---CK32\, -CK16a, aFFTV_A0C1, aFFTV_A0C4, aFFTV_A0C7, bFFTV_A0C2, bFFTV_A0C5, ACK, HCB\0, HCB1, HCB2, HCB3, HCB4, HCB5, HCB6, HCB7, CONTROL-D0, CONTROL-D1, CONTROL-D2, CONTROL-D3, CONTROL-D4, CONTROL-D5, CONTROL-D6, CONTROL-D7, -5.2V, NEW_FRAME\0, +5V, NEW_FRAME\3, GND — DIN

P2B: GND, -CK8a, +5V, -CK8b, -CK16b, aFFTV_A0C2, aFFTV_A0C5, bFFTV_A0C0, bFFTV_A0C3, bFFTV_A0C6, ACK\, HCB\0, HCB\1, HCB\2, HCB\3, HCB\4, HCB\5, HCB\6, HCB\7, HSKMICROC-1 READ2, HSKMICROC-2 WRITE2, HSKMICROC-0 IRQ2, HSKMICROC-3 CTS2, HSKMICROD-1 READ3, HSKMICROD-2 WRITE3, HSKMICROD-0 IRQ3, HSKMICROD-3 CTS3, -5.2V, NEW_FRAME\1, +5V, See note 2, GND — DIN

P2C: GND, FFT_INIT, +5V, FFT_INIT\, aFFTV_A0C0, aFFTV_A0C3, aFFTV_A0C6, aFFTV_A0C1, bFFTV_A0C4, bFFTV_A0C7, SELECT, SELECT\, STROBE, STROBE\, MODE0, MODE0\, MODE1, MODE1\, HSKMICROA-1 READ0, HSKMICROA-2 WRITE0, HSKMICROA-0 IRQ0, HSKMICROA-3 CTS0, HSKMICROB-1 READ1, HSKMICROB-2 WRITE1, HSKMICROB-0 IRQ1, HSKMICROB-3 CTS1, -5.2V, NEW_FRAME\2, +5V, See note 2, GND — DIN

VEE

P3A: GND, DELAY_CLKA, +5V, DELAY_CLKA\, DELAY_DATAA, DELAY_DATAA\, TERM_TXD, TERM_RXD, I/O_SPARE0 (DW DATA), I/O_SPARE2 (DW CLCK), NEW_DELAY\a, DLYDATA-S0, DLYDATA-S3, DLYDATA-0, DLYDATA-3, DLYDATA-6, DLYDATA-8, DLYDATA-11, DLYDATA-14, DLYDATA-16, DLYDATA-19, DLYDATA-22, DLYDATA-24, RESERVED, DLYDATA-27, +5V, DLYDATA-30, GND — DIN

P3B: GND, DELAY_CLKB, +5V, DELAY_CLKB\, DELAY_DATAB, DELAY_DATAB\, DELAY_DATAD, DELAY_DATAD\, I/O_SPARE1 (ROLL 0), I/O_SPARE3, NEW_DELAY\b, DLYDATA-S1, DLYDATA-1, DLYDATA-4, DLYDATA-7, DLYDATA-9, DLYDATA-12, DLYDATA-15, DLYDATA-17, DLYDATA-20, DLYDATA-23, DLYDATA-25, RESERVED, DLYDATA-28, +5V, DLYDATA-31, GND — DIN

P3C: GND, DELAY_CLKC, +5V, DELAY_CLKC\, DELAY_DATAC, DELAY_DATAC\, DELAY_CLKD, DELAY_CLKD\, TAPE_DR_TXD, TAPE_DR_RXD, RST, RESET, DLYDATA-S2, DLYDATA-2, DLYDATA-5, DLYDATA-10, DLYDATA-13, DLYDATA-18, DLYDATA-21, DLYDATA-26, RESERVED, DLYDATA-29, +5V, GND — DIN

TR_RESET

Enable/Disable TEST to PBD via MUX card.

Power on reset

VAL-A[0..7]

---CK32, ---CK32\, FFT_INIT, FFT_INIT\, NMI_SW, NEW_FRINGE_EN\, 131msTIC_EN

DATA_INVALID[0..7] → DATA_INV[0..7]

HCB[0..7] → HCB[0..7]

HCB\[0..7] → HCB\[0..7]

SELECT, SELECT\, STROBE, STROBE\, MODE0, MODE0\, MODE1, MODE1\

IRQ[0..3] → 8751_IRQ[0..3]

CTS[0..3] → 8751_CTS[0..3]

NEW_FRAME\[0..3] → NEW_FRAME\[0..3]

CONTROL-D[0..7] → 68K-8751_B[0..7]

I/O_SPARE[0..3] → I/O_SPARE[0..3]

RESET

DELAY_CLKA, DELAY_CLKA\, DELAY_DATAA, DELAY_DATAA\ → SC_DLY_MA, SC_DLY_MA\, SD_DLY_MA, SD_DLY_MA\

DELAY_CLKB, DELAY_CLKB\, DELAY_DATAB, DELAY_DATAB\ → SC_DLY_MB, SC_DLY_MB\, SD_DLY_MB, SD_DLY_MB\

DELAY_CLKC, DELAY_CLKC\, DELAY_DATAC, DELAY_DATAC\ → SC_DLY_MC, SC_DLY_MC\, SD_DLY_MC, SD_DLY_MC\

DELAY_CLKD, DELAY_CLKD\, DELAY_DATAD, DELAY_DATAD\ → SC_DLY_MD, SC_DLY_MD\, SD_DLY_MD, SD_DLY_MD\

TERM_TXD, TAPE_DR_TXD → TERM_TXD, TAPE_DR_TXD

DLYDATA-S0, DLYDATA-S1, DLYDATA-S2, DLYDATA-S3 → SYS_TRK_A, SYS_TRK_B, SYS_TRK_C, SYS_TRK_D

DLYDATA-[0..7] → TRK[0..7]
DLYDATA-[8..15] → TRK[8..15]
DLYDATA-[16..23] → TRK[16..23]
DLYDATA-[24..31] → TRK[24..31]

L008D02.SCH

L008D02.SCH: aFFTV_A0C[0..7], bFFTV_A0C[0..7], A0C0\1a, A0C01a, A0C0\0a, A0C00a, A0C1\1a, A0C11a, A0C1\0a, A0C10a, A0C2\1a, A0C21a, A0C2\0a, A0C20a, A0C3\1a, A0C31a, A0C3\0a, A0C30a, A0C4\1a, A0C41a, A0C4\0a, A0C40a, A0C5\1a, A0C51a, A0C5\0a, A0C50a, A0C6\1a, A0C61a, A0C6\0a, A0C60a, A0C7\1a, A0C71a, A0C7\0a, A0C70a, A0C0\1b, A0C01b, A0C0\0b, A0C00b, A0C1\1b, A0C11b, A0C1\0b, A0C10b, A0C2\1b, A0C21b, A0C2\0b, A0C20b, A0C3\1b, A0C31b, A0C3\0b, A0C30b, A0C4\1b, A0C41b, A0C4\0b, A0C40b, A0C5\1b, A0C51b, A0C5\0b, A0C50b, A0C6\1b, A0C61b, A0C6\0b, A0C60b, A0C7\1b, A0C71b, A0C7\0b, A0C70b, ACK, ACK\, -CK8a, -CK8b, -CK16a, -CK16b, NEW_DELAY\a, NEW_DELAY\b, 68K-8751_READ[0..3], 68K-8751_WRITE[0..3], TERM_RXD, TAPE_DR_RXD, TR_TEST_CYCLE_EN, TR_RESET

DEFORMATTER PALS
DEFTOP.PAL B SIZE

DATA INVALID XILINX
K013D01.BLK A SIZE

BARREL ROLL XILINX
K012D01.BLK B SIZE

BIT SHUFFLER 0
BSP-0.SCH C SIZE

BIT SHUFFLER 1
BSP-1.SCH D SIZE

BSP-0.SCH AND BSP-1.SCH ARE MAINTAINED IN VLBSOFT, SINCE THEY ARE THE ACTUAL INPUT FILES TO THE XILINX DESIGN PROCESS.

COPIES ARE KEPT IN THE DEF DESIGN FOR CONVENIENCE ONLY.

BIT SHUFFLER 2
BSP2BLK.SCH

BIT SHUFFLER 3
BSP3BLK.SCH

BIT SHUFFLER 4
BSP4BLK.SCH

BIT SHUFFLER 5
BSP5BLK.SCH

BIT SHUFFLER 6
BSP6BLK.SCH

BIT SHUFFLER 7
BSP7BLK.SCH

BIT SHUFFLER 8
BSP8BLK.SCH

BIT SHUFFLER 9
BSP9BLK.SCH

LAYOUT
Z009D01.LAY

ASSEMBLY DETAILS
Z009D02.LAY

OTHER FILES MAINTAINED IN THIS DESIGN DIRECTORY:

L008D01.SRC	ORCAD LIBRARY SOURCE
L008D01.LIB	ORCAD LIBRARY
B004T01.PRT	PARTLIST
W005T01.NET	NRAO NETLIST
CALAY.NET	TRI-CIRCUITS NETLIST

THERE ARE 208 ORCAD FILES PLUS THE ABOVE FIVE FILES FOR A TOTAL OF 213 FILES UNDER SCCS VERSION CONTROL IN THIS DESIGN DIRECTORY.

THE L008D01.LIB LIBRARY FILE IS THE ARCHIVED LIBRARY FOR THIS COMPLETE SET OF 208 ORCAD FILES.

THE DEFORMATTER MODE TABLE CAN BE FOUND IN THE HCB PROTOCOL DOCUMENT, D027DEF.HCB, WHICH IS MAINTAINED IN THE DEFASM COMPONENT OF THE SYSTEM SOFTWARE.

THE ORCAD DRAWING NUMBERS FOR THE MODE TABLE ARE K006D01.TBL AND K006D01A.TBL.

THE MODE TABLE AND OTHER FIGURES IN THE HCB PROTOCOL DOCUMENT ARE MAINTAINED HERE:

HCB PROTOCOL FIGURES AND TABLES
D027DEF.SCH

NOTES:

1 RESERVED is a dedicated power pin on I/O connector that is not used by this board.

2 This pin is used by the test fixture to route NEW DELAY to the TRACK RECOVERY card when the DEFORMATTER is not present.

THE DEFORMATTER DESIGN DIRECTORY IS:

/home/azalea/corrdwgs/def/SCCS

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER

Size	Document Number	REV
C	56000L008 (L008D01.SCH)	

Date: December 5, 1997 Sheet 1 of 31

BARREL ROLL & DEMUX-DELAY

Test Points

TOP (in test fixt)

TP_XI1	TP13	1	
TP_XI2	TP14	2	
TP_XI3	TP15	3	
TP_XI4	TP16	4	
TP_XI5	TP17	5	
TP_XI6	TP18	6	
Sheet 19	TP19	7	
Sheet 19	TP20	8	
NC	TP21	9	
Sheet 22	68K_SEL\36	TP22	10
Sheet 19	CK16f	TP23	11
Sheet 19	FFT_SYNC	TP24	12

HDR12

TP19 IS NEW_FRINGE
TP20 IS NEW_DELAY

Test Points

NPI0	TP1	1	
NPI1	TP2	2	
NPI2	TP3	3	
NPI3	TP4	4	
DI0	TP5	5	
DI1	TP6	6	
DI4	TP7	7	
DI3	TP8	8	
DI4	TP9	9	
DI5	TP10	10	
DI6	TP11	11	
DI7	TP12	12	

J1 HDR12 BOTTOM (in tst fix)

Modifacation to IC required
1. Short pins 3 & 4
2. Cut or bend pin 3 so it does't go into socket.

Netlist = W005T01.NET

USED TO GENERATE 16 BIT PARITY

PAR8

SYS_TRK_A

PAR16

PARITY
ACTION PAL

U81

T\[0..7]

TRK\[0..7]

TRK[0..7]

T[0..7]

U8

T0 T1 T2 T3 T4 T5 T6 T7

D1 D2 D3 D4 D5 D6 D7 D8

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8

CK8m

CLK
OC

74ALS574

U30

A B C D E F G H I

EVEN
ODD

74ALS280

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11

I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9

T\3 T\2 T\1 T\0

TRK_SEL0
TRK_SEL1
A_MODE0

CK8d

CLK/I0

22V10H-25
D009T02.ABL

A_MODE1

U58

T\7 T\6 T\5 T\4

TRK_SEL0
TRK_SEL1
B_MODE0

CK8k

CLK/I0

22V10H-25
D009T03.ABL

B_MODE1

PARITY_CTRL

PU4

Pull-up resistor

68K_SD

68K_S_CLK2

68K_L_CLK2

U104

SER
SRCLK
SRCLR
RCLK
RCLR

QA QB QC QD QE QF QG QH QH'

74LS594

TRK_SEL0
TRK_SEL1
A_MODE0
A_MODE1
B_MODE0
B_MODE1

P_O/E_SEL

P_16/8_SEL

68K_SD+8

PARITY CHECK

PARITY_CTRL (I input to 74F280)	PAR8 or PAR16 (74F280 output)
H = even parity ck	L = good even parity result H = bad even parity result
L = odd parity ck	L = good odd parity result H = bad odd parity result

B[0..15]

bD[0..15]

B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15

U142
74LS590

U116
74LS590

CK8c

CK8b

CK8b
CK8c
CK8d
CK8k
CK8m

P_CNT_RESET\ 68K_L_CLK1

P_CNT_STROBE\ NEW_FRAME\

P_CNT_READ\ 68K_SEL\13 ADR=2C0,000

28 Aug 89:
Changed PAL type from 20R8 to 22V10

Note:
Parity counters-
The count is not inhibited during New Delay.
This means that errors during this
time will be counted twice.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
CROSS TRACK PARITY CHECK

Size	Document Number	REV
B	56000L008 (L008D03.SCH)	

Date: June 21, 1990 Sheet 3 of 31

USED TO GENERATE 16 BIT PARITY

PAR8

SYS_TRK_B

PAR16

PARITY
ACTION PAL

U80

T\[8..15]

TRK\[8..15]

TRK[8..15]

T[8..15]

U7

T8 T9 T10 T11 T12 T13 T14 T15

D1 D2 D3 D4 D5 D6 D7 D8

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8

CK8m

CLK

OC

74ALS574

U29

A B C D E F G H I

EVEN

ODD

74ALS280

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11

I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9

T\11 T\10 T\9 T\8

TRK_SEL0
TRK_SEL1
A_MODE0

CK8d

CLK/I0

22V10H-25

D009T02.ABL

A_MODE1

U57

T\15 T\14 T\13 T\12

TRK_SEL0
TRK_SEL1
B_MODE0

CK8k

CLK/I0

22V10H-25

D009T03.ABL

B_MODE1

PARITY_CTRL

PU4

Pull-up resistor

68K_SD+8

68K_S_CLK2

68K_L_CLK2

U103

SER SRCLK SRCLR RCLK RCLR

QA QB QC QD QE QF QG QH QH'

74LS594

TRK_SEL0
TRK_SEL1
A_MODE0
A_MODE1
B_MODE0
B_MODE1

P_O/E_SEL

P_16/8_SEL

68K_SD+16

PARITY CHECK

PARITY_CTRL (I input to 74F280)	PAR8 or PAR16 (74F280 output)
H = even parity ck	L = good even parity result H = bad even parity result
L = odd parity ck	L = good odd parity result H = bad odd parity result

B[0..15]

bD[0..15]

U141
74LS590

U115
74LS590

CK8c

CK8b

CK8b
CK8c
CK8d
CK8k
CK8m

P_CNT_RESET\
P_CNT_STROBE\
P_CNT_READ\

68K_L_CLK1
NEW_FRAME\
68K_SEL\14

ADR=2E0,000

Note:
Parity counters-
The count is not inhibited during New Delay.
This means that errors during this
time will be counted twice.

28 Aug 89:
Changed PAL type from 20R8 to 22V10

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
CROSS TRACK PARITY CHECK

Size	Document Number	REV
B	56000L008 (L008D04.SCH)	

Date: June 21, 1990 Sheet 4 of 31

USED TO GENERATE 16 BIT PARITY

PAR8

SYS_TRK_C

PAR16

PARITY
ACTION PAL

U79

T\[16..23]

TRK\[16..23]

TRK[16..23]

T[16..23]

U6

T16 T17 T18 T19 T20 T21 T22 T23

D1 D2 D3 D4 D5 D6 D7 D8

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8

CK8m

CLK

OC

74ALS574

U28

A B C D E F G H I

EVEN

ODD

74ALS280

TRK_SEL0
TRK_SEL1
A_MODE0

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11

I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9

T\19 T\18 T\17 T\16

CK8d

CLK/I0

22V10H-25

D009T02.ABL

A_MODE1

U56

T\23 T\22 T\21 T\20

TRK_SEL0
TRK_SEL1
B_MODE0

CK8k

CLK/I0

22V10H-25

D009T03.ABL

B_MODE1

PARITY_CTRL

PU4

Pull-up resistor

68K_SD+16

68K_S_CLK2

68K_L_CLK2

U102

SER SRCLK SRCLR RCLK RCLR

QA QB QC QD QE QF QG QH QH'

74LS594

TRK_SEL0
TRK_SEL1
A_MODE0
A_MODE1
B_MODE0
B_MODE1

P_O/E_SEL

P_16/8_SEL

68K_SD+24

PARITY CHECK

PARITY_CTRL (I input to 74F280)	PAR8 or PAR16 (74F280 output)
H = even parity ck	L = good even parity result H = bad even parity result
L = odd parity ck	L = good odd parity result H = bad odd parity result

B[0..15]

bD[0..15]

U140

U114

74LS590

CK8c

CK8b

CK8b
CK8c
CK8d
CK8k
CK8m

P_CNT_RESET\

P_CNT_STROBE\

P_CNT_READ\

68K_L_CLK1

NEW_FRAME\

68K_SEL\15

ADR=300,000

Note:
Parity counters-
The count is not inhibited during New Delay.
This means that errors during this
time will be counted twice.

28 Aug 89:
Changed PAL type from 20R8 to 22V10

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
CROSS TRACK PARITY CHECK

Size	Document Number	REV
B	56000L008 (L008D05.SCH)	

Date: June 21, 1990 Sheet 5 of 31

USED TO GENERATE 16 BIT PARITY

PAR8

SYS_TRK_D

PAR16

PARITY
ACTION PAL

U78

T\[24..31]

TRK\[24..31]

TRK[24..31]

T[24..31]

U5

T24 T25 T26 T27 T28 T29 T30 T31

D1 D2 D3 D4 D5 D6 D7 D8

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8

CK8m

CLK
OC

74ALS574

U27

A B C D E F G H I

EVEN
ODD

74ALS280

TRK_SEL0
TRK_SEL1
A_MODE0

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11

I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9

T\27 T\26 T\25 T\24

CK8d

CLK/I0

22V10H-25
D009T02.ABL

A_MODE1

U55

T\31 T\30 T\29 T\28

TRK_SEL0
TRK_SEL1
B_MODE0

CK8k

CLK/I0

22V10H-25
D009T03.ABL

B_MODE1

PARITY_CTRL

PU4

Pull-up resistor

68K_SD+24

68K_S_CLK2

68K_L_CLK2

U101

SER SRCLK SRCLR RCLK RCLR

QA QB QC QD QE QF QG QH QH'

74LS594

TRK_SEL0
TRK_SEL1
A_MODE0
A_MODE1
B_MODE0
B_MODE1

P_O/E_SEL

P_16/8_SEL

P_16/8_SEL

PARITY CHECK

PARITY_CTRL (I input to 74F280)	PAR8 or PAR16 (74F280 output)
H = even parity ck	L = good even parity result H = bad even parity result
L = odd parity ck	L = good odd parity result H = bad odd parity result

B[0..15]

bD[0..15]

U139
74LS590

U113
74LS590

CK8c

CK8b

CK8b
CK8c
CK8d
CK8k
CK8m

P_CNT_RESET\
P_CNT_STROBE\
P_CNT_READ\

68K_L_CLK1
NEW_FRAME\
68K_SEL\16

ADR=320,000

Note:
Parity counters-
The count is not inhibited during New Delay.
This means that errors during this
time will be counted twice.

28 Aug 89:
Changed PAL type from 20R8 to 22V10

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
CROSS TRACK PARITY CHECK

Size	Document Number	REV
B	56000L008 (L008D06.SCH)	

Date: August 30, 1990 Sheet 6 of 31

ROLL PAL

U83 D009T04.ABL

TRK\[0..7] T\[0..7]

T\0 2
T\1 3
T\2 4
T\3 5
T\4 6
T\5 7
T\6 8
T\7 9
AR0 10
AR1 11
AR2 14
AR3 23

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12

Q0 22 T0
Q1 21 T1
Q2 20 T2
Q3 19 T3
Q4 18 T4
Q5 17 T5
Q6 16 T6
Q7 15 T7

A_ROLL[0..3] AR[0..3]

CK8d 1 CLK
13 OE

20R8A-2

AR 3 is a spare ctrl bit

T0 3 T8 4 T1 6 T9 5 T2 11 T10 12 T3 14 T11 13 1 WS

A1 A2 B1 B2 C1 C2 D1 D2

QA 2
QB 7
QC 10
QD 15

CK8a 9 CLK

U105
74ALS399

T4 3 T12 4 T5 6 T13 5 T6 11 T14 12 T7 14 T15 13 1 WS

CK8b 9 CLK

U117
74ALS399

68K_SD
68K_S_CLK3
DD_NEW_DELAY\
PU3 Pull-up resistor

U84

SER 14
SRCLK 11
SRCLR 10
RCLK 12
RCLR 13

QA 15
QB 1
QC 2
QD 3
QE 4
QF 5
QG 6
QH 7
QH' 9

74LS594

LSB
MSB

2 I1 3 I2 4 I3 5 I4 6 I5 7 I6 8 I7 9 I8 10 I9 11 I10 14 I11 23 I12

CK8a 1 CLK
13 OE

Q0 22 TR\0
Q1 21 TR\1
Q2 20 TR\2
Q3 19 TR\3
Q4 18
Q5 17
Q6 16
Q7 15

20R8A-2

K019D01.PAL
K019D02.PAL
D009T06.ABL
U89

TR\[0..7] TR\[0..7]

CK8a 1 CLK
13 OE

Q0 22 TR\4
Q1 21 TR\5
Q2 20 TR\6
Q3 19 TR\7
Q4 18
Q5 17
Q6 16
Q7 15

20R8A-2

K019D01.PAL
K019D02.PAL
D009T06.ABL
U88

TRK\[8..15] T\[8..15]

U82 D009T05.ABL

T\8 2
T\9 3
T\10 4
T\11 5
T\12 6
T\13 7
T\14 8
T\15 9
BR0 10
BR1 11
BR2 14
AR3 23

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12

Q0 22 T8
Q1 21 T9
Q2 20 T10
Q3 19 T11
Q4 18 T12
Q5 17 T13
Q6 16 T14
Q7 15 T15

CK8d 1 CLK
13 OE

20R8A-2

B_ROLL[0..3] BR[0..3] BR3 1=ROLL BY 16

NOTE:
Roll by 16 legal combinations -
tracks 0 thru 15 and 16 thru 31.

T8 3 T0 4 T9 6 T1 5 T10 11 T2 12 T11 14 T3 13 1 WS

A1 A2 B1 B2 C1 C2 D1 D2

QA 2
QB 7
QC 10
QD 15

CK8a 9 CLK

U106
74ALS399

T12 3 T4 4 T13 6 T5 5 T14 11 T6 12 T15 14 T7 13 1 WS

CK8b 9 CLK

U118
74ALS399

U121

SER 14
SRCLK 11
SRCLR 10
RCLK 12
RCLR 13

QA 15
QB 1
QC 2
QD 3
QE 4
QF 5
QG 6
QH 7
QH' 9

74LS594

2 I1 3 I2 4 I3 5 I4 6 I5 7 I6 8 I7 9 I8 10 I9 11 I10 14 I11 23 I12

CK8c 1 CLK
13 OE

Q0 22 TR\8
Q1 21 TR\9
Q2 20 TR\10
Q3 19 TR\11
Q4 18
Q5 17
Q6 16
Q7 15

20R8A-2

K019D01.PAL
K019D02.PAL
D009T06.ABL
U120

TR\[8..15] TR\[8..15]

CK8c 1 CLK
13 OE

Q0 22 TR\12
Q1 21 TR\13
Q2 20 TR\14
Q3 19 TR\15
Q4 18
Q5 17
Q6 16
Q7 15

20R8A-2

K019D01.PAL
K019D02.PAL
D009T06.ABL
U119

68K_SD+16

CK8a CK8a
CK8b CK8b
CK8c CK8c
CK8d CK8d

TEST_DATA

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
BARREL ROLLER and DEMUX-DELAY

Size	Document Number	REV
B	56000L008 (L008D07.SCH)	

Date: November 19, 1996 | Sheet 7 of 31

ROLL PAL

U60 D009T04.ABL

TRK\[16..23] T\[16..23]

T\16 2 I1 Q0 22 T16
T\17 3 I2 Q1 21 T17
T\18 4 I3 Q2 20 T18
T\19 5 I4 Q3 19 T19
T\20 6 I5 Q4 18 T20
T\21 7 I6 Q5 17 T21
T\22 8 I7 Q6 16 T22
T\23 9 I8 Q7 15 T23
CR0 10 I9
CR1 11 I10
CR2 14 I11
CR3 23 I12

C_ROLL[0..3] CR[0..3]

CK8j 1 CLK
13 OE

20R8A-2

AR 3 is a spare ctrl bit

68K_SD+16

68K_S_CLK3

DD_NEW_DELAY\

PU3 Pull-up resistor

T16 3 A1 QA 2
T24 4 A2
T17 6 B1 QB 7
T25 5 B2
T18 11 C1 QC 10
T26 12 C2
T19 14 D1 QD 15
T27 13 D2
1 WS
CK8h 9 CLK

U67

74ALS399

T20 3 A1 QA 2
T28 4 A2
T21 6 B1 QB 7
T29 5 B2
T22 11 C1 QC 10
T30 12 C2
T23 14 D1 QD 15
T31 13 D2
1 WS
CK8h 9 CLK

U66

74ALS399

U85

LSB

14 SER QA 15
QB 1
11 SRCLK QC 2
10 SRCLR QD 3
QE 4
12 RCLK QF 5
13 RCLR QG 6
QH 7
QH' 9

74LS594

2 I1 Q0 22 TR\16
3 I2 Q1 21 TR\17
4 I3 Q2 20 TR\18
5 I4 Q3 19 TR\19
6 I5 Q4 18
7 I6 Q5 17
8 I7 Q6 16
9 I8 Q7 15
10 I9
11 I10
14 I11
23 I12

K019D01.PAL
K019D02.PAL
D009T06.ABL

CK8e 1 CLK
13 OE

U69

20R8A-2

TR\[16..23] TR\[16..23]

2 I1 Q0 22 TR\20
3 I2 Q1 21 TR\21
4 I3 Q2 20 TR\22
5 I4 Q3 19 TR\23
6 I5 Q4 18
7 I6 Q5 17
8 I7 Q6 16
9 I8 Q7 15
10 I9
11 I10
14 I11
23 I12

K019D01.PAL
K019D02.PAL
D009T06.ABL

CK8e 1 CLK
13 OE

U68

20R8A-2

TRK\[24..31] T\[24..31]

U59 D009T05.ABL

T\24 2 I1 Q0 22 T24
T\25 3 I2 Q1 21 T25
T\26 4 I3 Q2 20 T26
T\27 5 I4 Q3 19 T27
T\28 6 I5 Q4 18 T28
T\29 7 I6 Q5 17 T29
T\30 8 I7 Q6 16 T30
T\31 9 I8 Q7 15 T31
DR0 10 I9
DR1 11 I10
DR2 14 I11
CR3 23 I12

CK8j 1 CLK
13 OE

20R8A-2

T24 3 A1 QA 2
T16 4 A2
T25 6 B1 QB 7
T17 5 B2
T26 11 C1 QC 10
T18 12 C2
T27 14 D1 QD 15
T19 13 D2
1 WS
CK8j 9 CLK

U50

74ALS399

T28 3 A1 QA 2
T20 4 A2
T29 6 B1 QB 7
T21 5 B2
T30 11 C1 QC 10
T22 12 C2
T31 14 D1 QD 15
T23 13 D2
1 WS
CK8j 9 CLK

U49

74ALS399

U61

14 SER QA 15
QB 1
11 SRCLK QC 2
10 SRCLR QD 3
QE 4
12 RCLK QF 5
13 RCLR QG 6
QH 7 MSB
QH' 9

74LS594

2 I1 Q0 22 TR\24
3 I2 Q1 21 TR\25
4 I3 Q2 20 TR\26
5 I4 Q3 19 TR\27
6 I5 Q4 18
7 I6 Q5 17
8 I7 Q6 16
9 I8 Q7 15
10 I9
11 I10
14 I11
23 I12

K019D01.PAL
K019D02.PAL
D009T06.ABL

CK8h 1 CLK
13 OE

U39

20R8A-2

TR\[24..31] TR\[24..31]

2 I1 Q0 22 TR\28
3 I2 Q1 21 TR\29
4 I3 Q2 20 TR\30
5 I4 Q3 19 TR\31
6 I5 Q4 18
7 I6 Q5 17
8 I7 Q6 16
9 I8 Q7 15
10 I9
11 I10
14 I11
23 I12

K019D01.PAL
K019D02.PAL
D009T06.ABL

CK8h 1 CLK
13 OE

U38

20R8A-2

D_ROLL[0..3] DR[0..3] DR3 1=ROLL BY 16

NOTE:
Roll by 16 legal combinations -
tracks 0 thru 15 and 16 thru 31.

CK8e CK8e

CK8h CK8h

CK8j CK8j

TEST_DATA

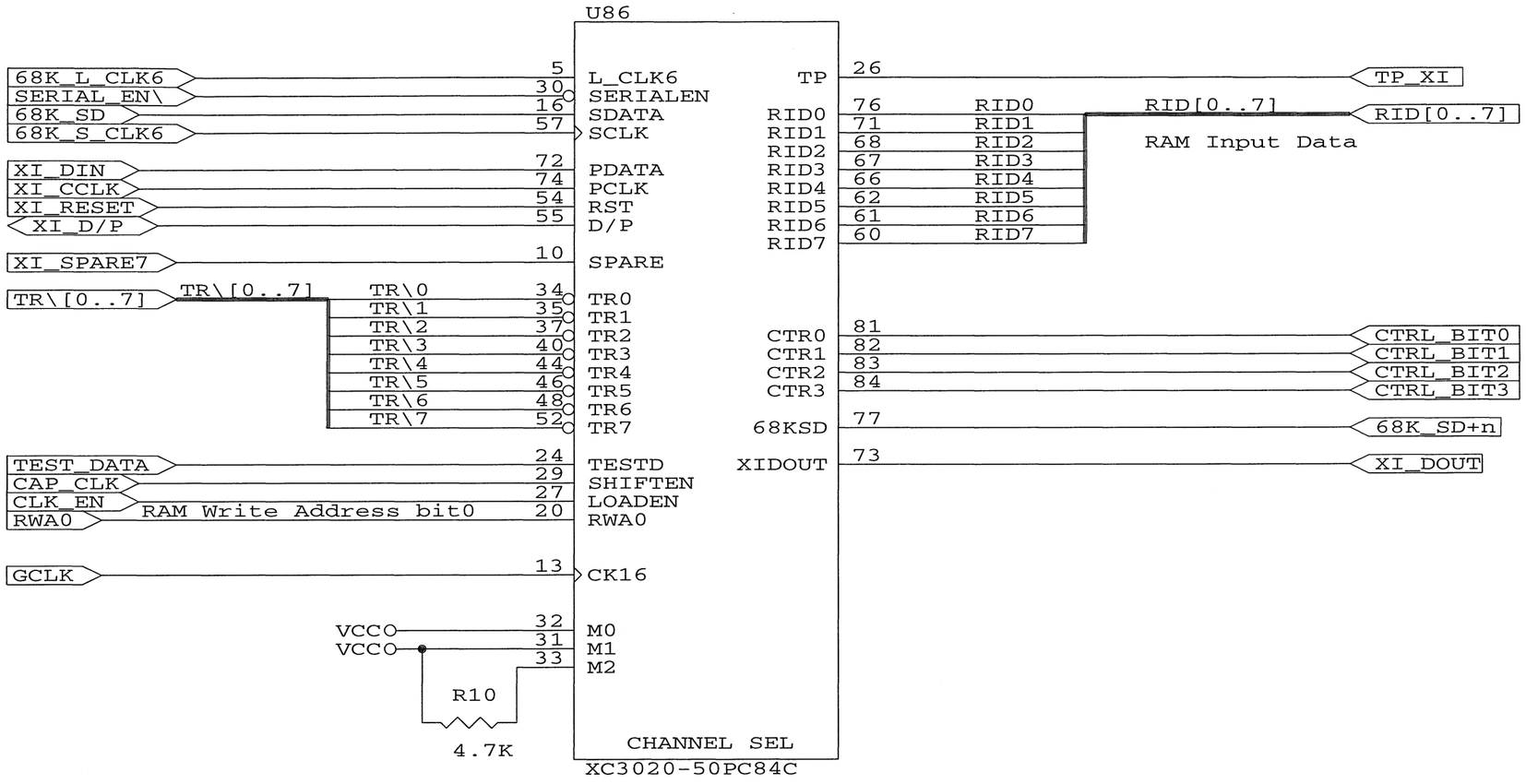
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
BARREL ROLLER and DEMUX-DELAY (16-31)

Size	Document Number	REV
B	56000L008 (L008D08.SCH)	

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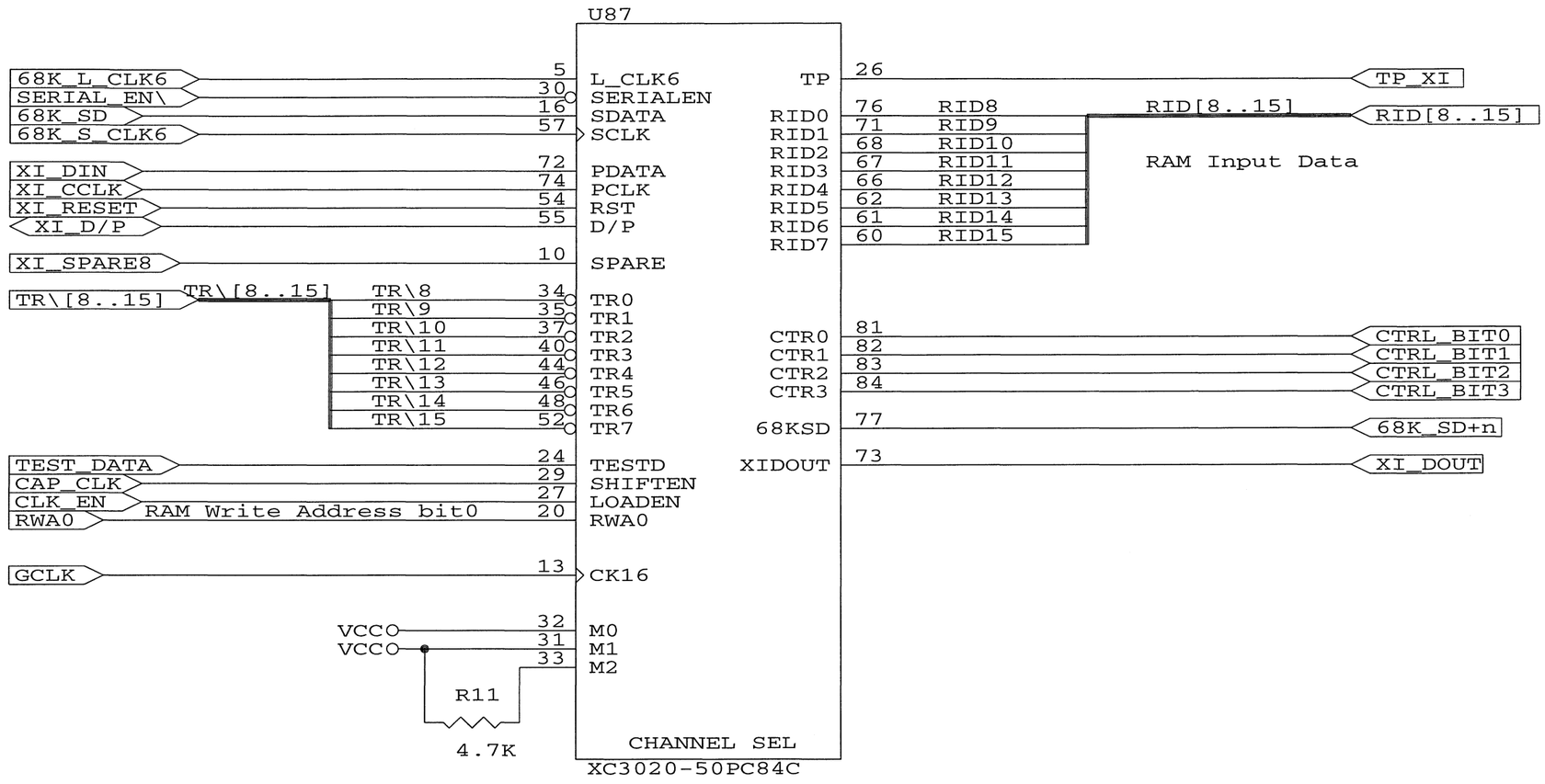


Notes:
- VCC - 22,64
- GND - 1,63
- CAP_CLK - Captures the data at the input to the Bit Shuffler Xilinx's. Required for the following modes:
  1. Oversampled (by > 2) bit stream.
  2. 2 bitstreams on 1 track.
  3. 4 bitstreams on 1 track.
- CLK_EN - Clock Enable to the serial shift register in the Bit Shuffler Xilinx's. Not required by all personalities of the Xilinx's.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER CHANNEL SELECT TRACKS 0-7	
Size: A	Document Number: 56000L008 (L008D09.SCH)	REV:
Date: November 19, 1996	Sheet 9 of 31	



Notes:
- VCC - 22,64
- GND - 1,63
- CAP_CLK - Captures the data at the input to the Bit Shuffler Xilinx's. Required for the following modes:
  1. Oversampled (by > 2) bit stream.
  2. 2 bitstreams on 1 track.
  3. 4 bitstreams on 1 track.
- CLK_EN - Clock Enable to the serial shift register in the Bit Shuffler Xilinx's. Not required by all personalities of the Xilinx's.

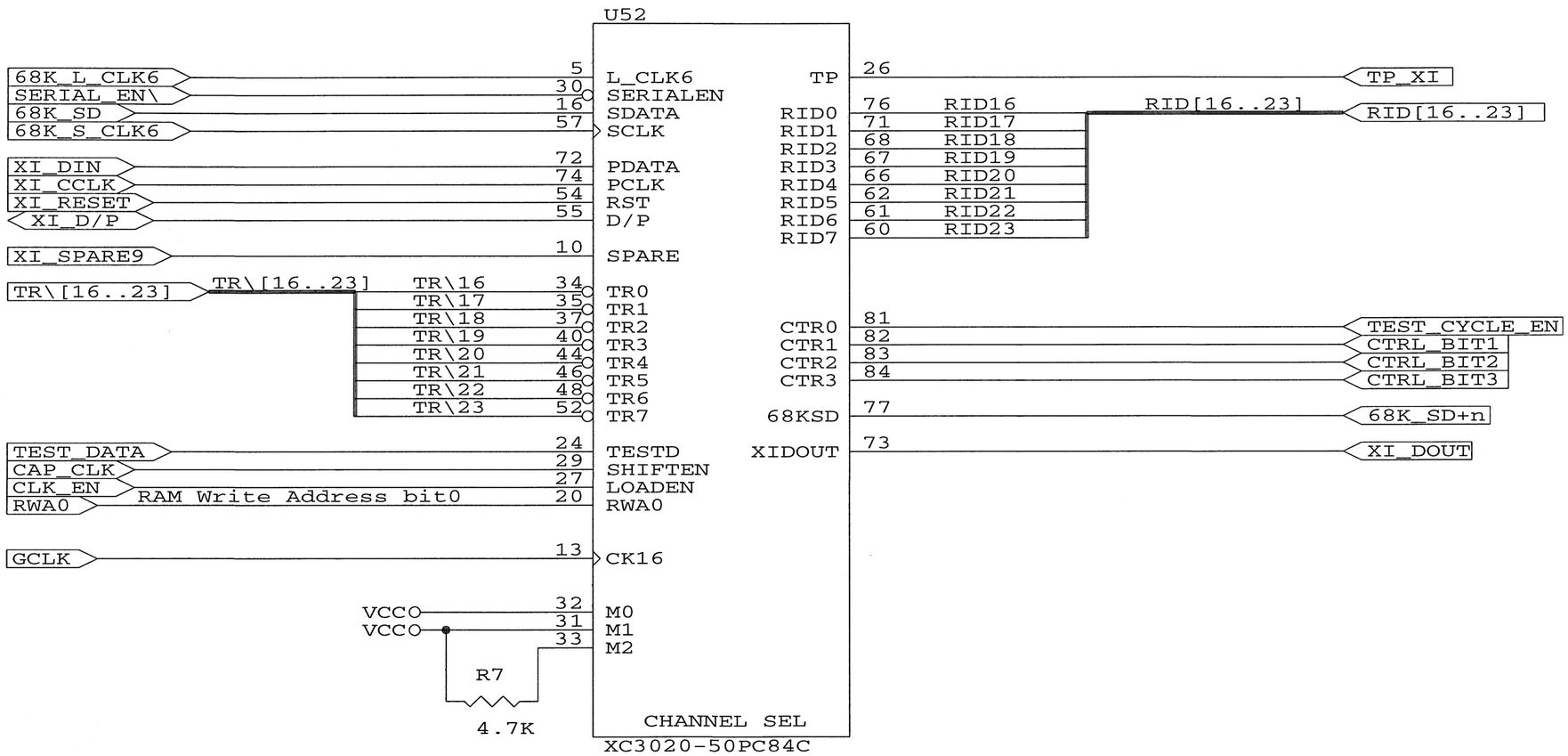
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER
CHANNEL SELECT TRACKS 8-15

Size	Document Number	REV
A	56000L008 (L008D10.SCH)	

Date: November 19, 1996 Sheet 10 of 31



Notes:
- VCC - 22,64
- GND - 1,63
- CAP_CLK - Captures the data at the input to the Bit Shuffler Xilinx's. Required for the following modes:
  1. Oversampled (by > 2) bit stream.
  2. 2 bitstreams on 1 track.
  3. 4 bitstreams on 1 track.
- CLK_EN - Clock Enable to the serial shift register in the Bit Shuffler Xilinx's. Not required by all personalities of the Xilinx's.

VLBA CORRELATOR PROJECT

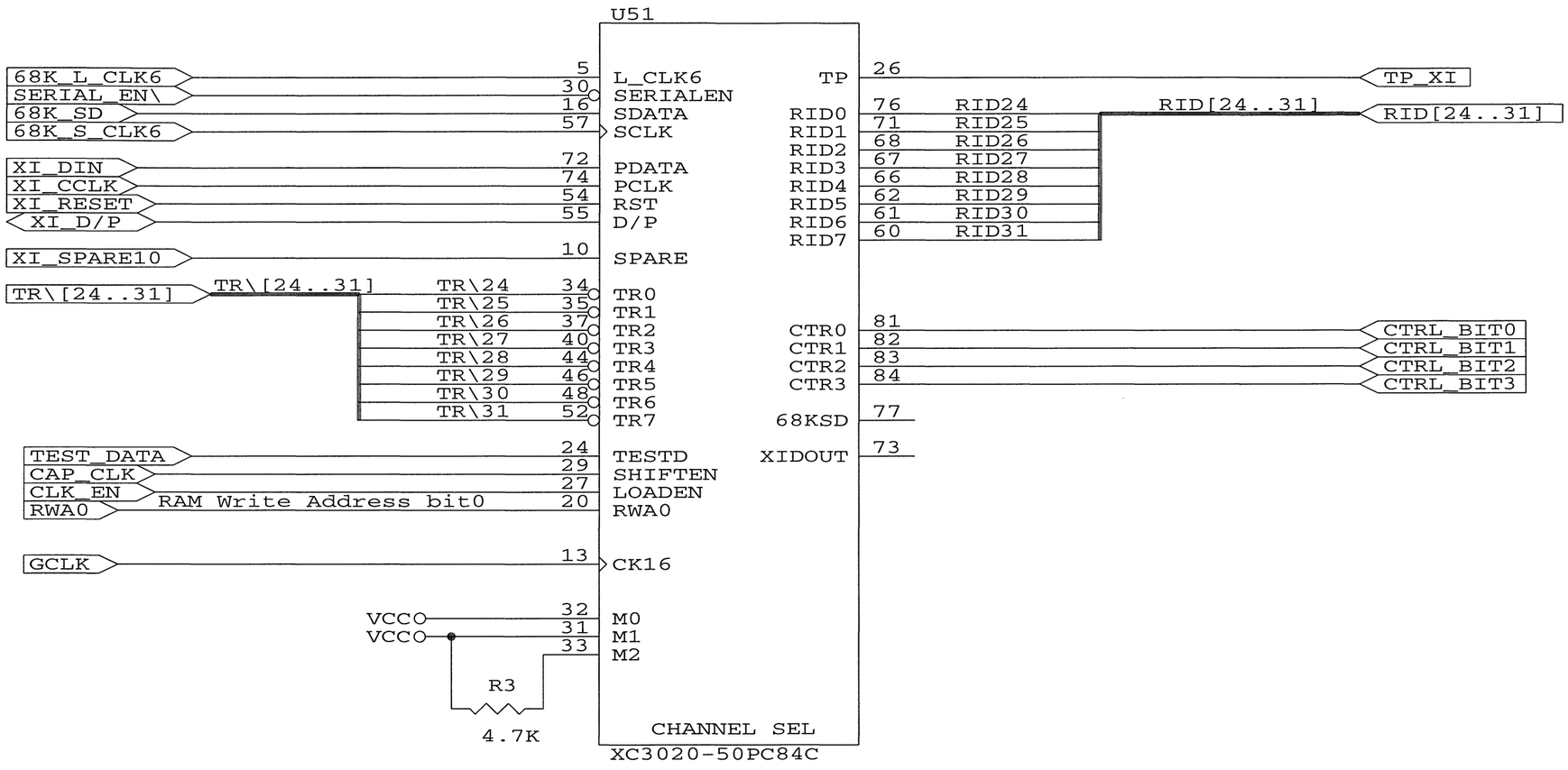
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER

CHANNEL SELECT TRACKS 16-23

Size	Document Number	REV
A	56000L008 (L008D11.SCH)	

Date: November 19, 1996 Sheet 11 of 31



Notes:
- VCC - 22,64
- GND - 1,63
- CAP_CLK - Captures the data at the input to the Bit Shuffler Xilinx's. Required for the following modes:
  1. Oversampled (by > 2) bit stream.
  2. 2 bitstreams on 1 track.
  3. 4 bitstreams on 1 track.
- CLK_EN - Clock Enable to the serial shift register in the Bit Shuffler Xilinx's. Not required by all personalities of the Xilinx's.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER
CHANNEL SELECT TRACKS 24-31

Size	Document Number	REV
A	56000L008 (L008D12.SCH)	

Date: November 19, 1996 Sheet 12 of 31

WRITE_ADR_CNT_EN\
CK16d
PU5
Pull-up resistor
G_RA_NEW_DELAY\

+5V = PIN 16
GND = PIN 6

U129 74F579

U130 74F579

To Bit Shufflers
RWA0
WA[0..11]

RAM WRITE
ADDRESS COUNTER

WD[0..15]
D[0..15]

FRINGE CYCLE SEQUENCER

Sequencer 3

U168 P4C422-12

BIT 8
BIT 9
BIT 10
BIT 11
SPARE1
OVERLAP

NEW_DELAY_EN
D13_SPARE

PU9
Pull-up resistor

WA[1..8]
A[1..8]

U171 74F163
U201 74F163

CK16a

68K_SEL\27 ADR= 4A0000
68K_SEL\28 ADR= 4A0000
FROM U218 PIN 22, SHT. 22

U137 P4C422-12
U138 P4C422-12

CA[0..7]
SEQUENCER OUTPUT

WRITTEN BY uP

RAM READ
OFFSET REGISTER
(NORMALLY ZERO)

U161 74ALS574

RAM READ OFFSET NOT USED. IT WAS INTENDED FOR OVERLAPPED FFTs IN ADJACENT PIPELINES.

U193 74ALS574

68K_SEL\29 ADR=4C0,000

RAM READ
OFFSET ADDER

U108 U111 U132 74F283

OSRA[9..11]
OSRA[9..11]

D13_CTRL_BIT

CKA16a\
CK32f

U107 U110 U131 74F399

ORA[0..11]
ORA[0..11]

ODD BANK
RAM ADDRESS

WS	A1	A2	C	Q
0	0	x	↑	0
0	1	x	↑	1
1	x	0	↑	0
1	x	1	↑	1

Spare
CNTx2 En

U135 PAL23S8-20
D009T07.ABL
K023D01.PAL

XI_SPARE3
G_RA_NEW_FRINGE\
FROM U156 PIN 20, SHT. 19
SPARE1
RESET
Mode 1= no overlap, 0= overlap
CK16b

U134 PAL23S8-20
D009T08.ABL
K023D02.PAL

RA[0..11]

U197C 74F04
U197F 74F04

OVERLAP DOWN COUNTER
LOAD
NEW_FFT\
COUNT=0
STORE
LOAD COUNT

U136 74F269
+5V = PIN 19
GND = PIN 7
STOP AT 0

RAM READ
ADDRESS
COUNTER

U112 U109 U133 74F399

ERA[0..11]
ERA[0..11]

EVEN BANK
RAM ADDRESS

RA[9..11]

CK16b\
CK32d

The RAM READ ADDRESS COUNTER state gets captured when CAPTURE goes trueThis captured address is then used as the start address for the overlapped FFT.

BUFFER RAM READ COUNTER CONTROL

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER RAM ADDRESS GENERATOR	
Size C	Document Number 56000L008 (L008D13.SCH)	REV
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131msDLYD\ — If 131nsDLYD\ AND TEST_CYCLE_EN then generate TEST CYCLE (PUT OUT THE TEST PATTERN)

EVEN

ERA[0..11] — E[0..11]

RID[0..7] — RID[0..7]

RID[8..15] — RID[7..15]

RID[16..23] — RID[16..23]

RID[24..31] — RID[24..31]

R/W0 — R/W0

R/W1 — R/W1

R/W2 — R/W2

R/W3 — R/W3

CK16c\ — CK16c\

CK16g\ — CK16g\

CK32e — CK32e

TEST_CYCLE_EN — TEST_CYCLE_EN

CTRL_BIT1 — SPARE2

SWAP\ — SWAP\

FOR SPECIAL POLARIZATION MODE

RID10 RID8 RID2 RID0 — U98 RAM 1 4K X 4 — P4C1682-15

RID11 RID9 RID3 RID1 — U77 RAM 2 4K X 4 — P4C1682-15

RID26 RID24 RID18 RID16 — U75 RAM 3 4K X 4 — P4C1682-15

RID27 RID25 RID19 RID17 — U65 RAM 4 4K X 4 — P4C1682-15

R/W0 R/W1 — WE CE

U99 — 20R8-10 — D009T09.ABL

CK16c\ — CK16c\

TEST_DATA_S TEST_DATA_M 68K_TEST_EN — TEST_CYCLE_EN SPARE2 SWAP\

U100 — 20R6-7 — D009T10.ABL

CK32e — CK32e

MUX_SEL — S0 M0 S2 M2

U72 — 20R8-10 — D009T09.ABL

U73 — 20R6-7 — D009T11.ABL

MUX_SEL — S4 M4 S6 M6

Buffered CK16

ODD

ORA[0..11] — O[0..11]

RID14 RID12 RID6 RID4 — U94 RAM 5 4K X 4 — P4C1682-15

RID15 RID13 RID7 RID5 — U76 RAM 6 4K X 4 — P4C1682-15

RID30 RID28 RID22 RID20 — U74 RAM 7 4K X 4 — P4C1682-15

RID31 RID29 RID23 RID21 — U64 RAM 8 4K X 4 — P4C1682-15

R/W2 R/W3 — WE CE

SWAP\ SWAPS THE TWO DATA STREAMS FOR 1-4, 2 BIT MAC POLARIZATION MODE.

U96 — 20R8-10 — D009T09.ABL

TEST_DATA_S TEST_DATA_M 68K_TEST_EN — CK16c\

MUX_SEL — S1 M1 S3 M3

U97 — 22V10-15 — D009T12.ABL

TEST_CYCLE_EN SPARE2 SWAP\ — CK32e

U70 — 20R8-10 — D009T09.ABL

U71 — 22V10-15 — D009T13.ABL

MUX_SEL — S5 M5 S7 M7

TEST_CYCLE_EN

TEST CYCLE

TEST CYCLE

PAL FUNCTIONS:

1) VLBA MODE:
   2-1 MUX (internal divider)
   I1 & I5 TO O1
   I2 & I6 TO O2
   I3 & I7 TO O3
   I4 & I8 TO O4

2) MARK III MODE:
   Same as above.
   Same as 1 bitstream to 4 tracks.
   The FFT engine will properly order the bits.

ON FRAME BOUNDARY

dDATA_VAL[0..7] — dDATA_VAL[0..7]

RID9 RID8 RID2 RID0 — U54 RAM 9 4K X 4 — P4C1682-15

dDATA_VAL0 dDATA_VAL2 dDATA_VAL4 dDATA_VAL6

RID14 RID12 RID6 RID4 — U53 RAM 10 4K X 4 — P4C1682-15

dDATA_VAL1 dDATA_VAL3 dDATA_VAL5 dDATA_VAL7

DV_NEW_FRINGE\

U63 — 20V8-15 — K021D03.PAL D009T14.ABL

VC0 VC2 VC4 VC6

U62 — 20V8-15 — K021D03.PAL D009T14.ABL

VC1 VC3 VC5 VC7

VALID=LOGIC 1

FROM SHT.13

RA[9..11] — RA[9..11]

RA9 RA10 RA11

NEW_FFT\ — NEW_FFT\

G_DV_NEW_DELAY\ — G_DV_NEW_DELAY\

DV_NEW_FRINGE\ — DV_NEW_FRINGE\

ND_NF_INTERVAL_INVALID — ND_NF_INTERVAL_INVALID\

ND_NF_INTERVAL_INVALID\ NEW_FFT\ G_DV_NEW_DELAY\ 68K_TEST_EN

TEST_DATA_S — TEST_DATA_S

TEST_DATA_M — TEST_DATA_M

68K_CTRL5 — 68K_TEST_EN
Static test, select test data

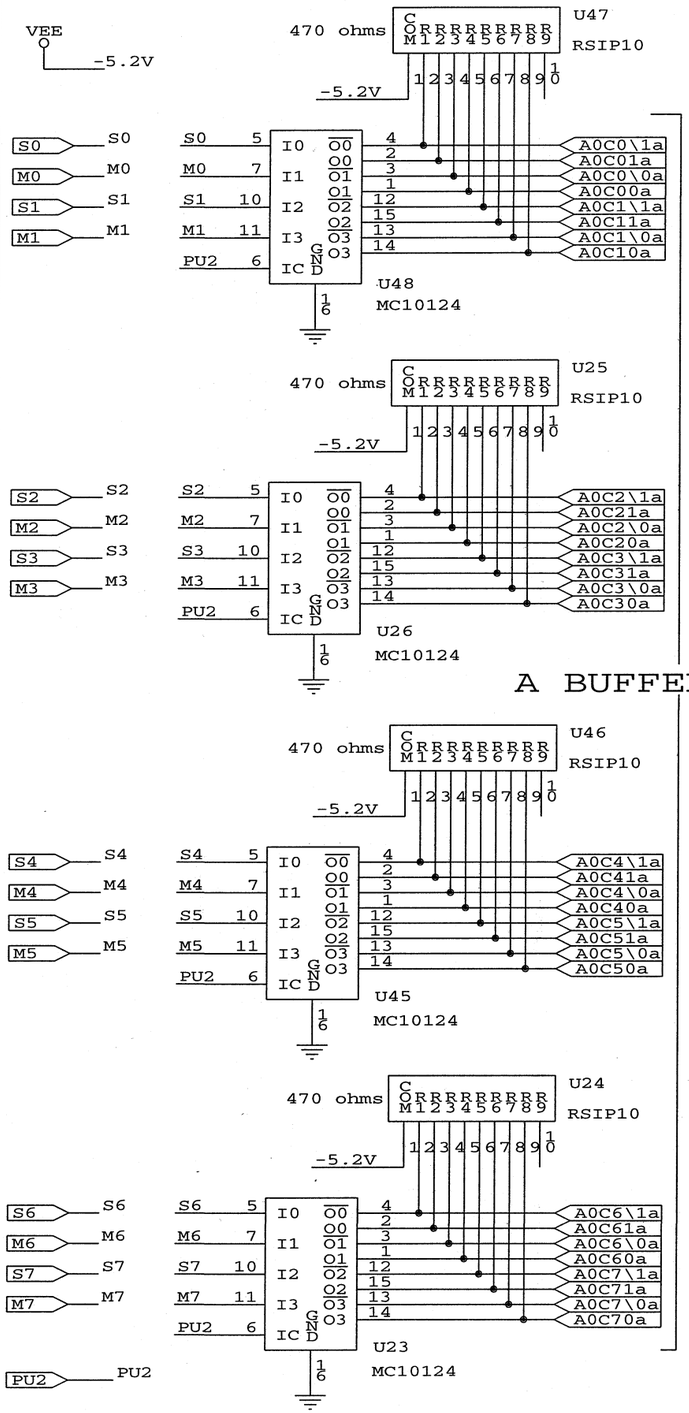
OSRA[9..11] — OSRA[9..11]

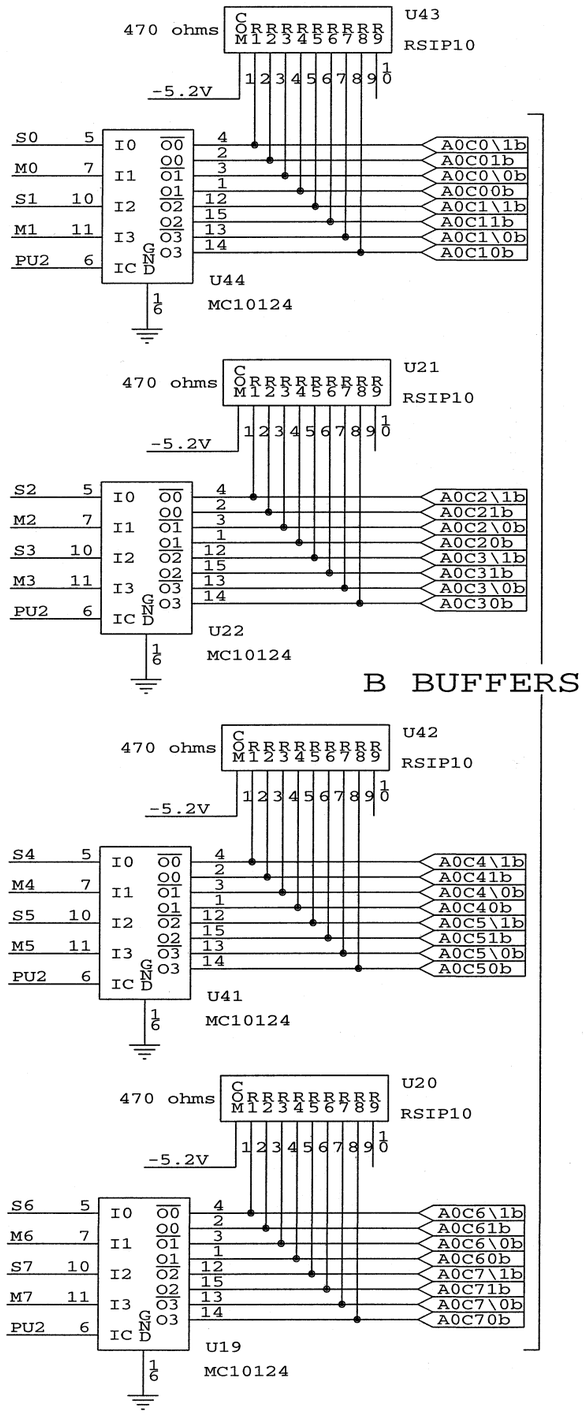
OSRA9 OSRA10 OSRA11

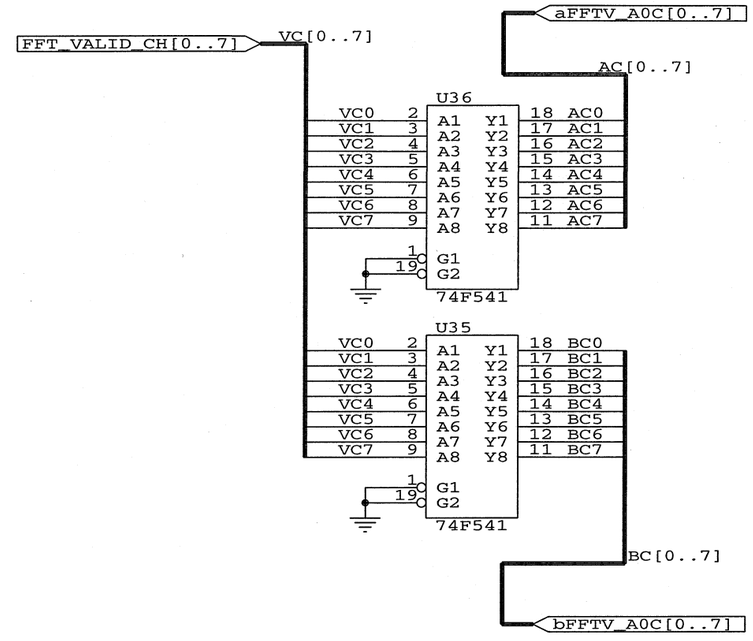
ND_NF_INTERVAL_INVALID\ NEW_FFT\ G_DV_NEW_DELAY\ 68K_TEST_EN

VC[0..7] — TO SHT.15 — FFT_VALID_CH[0..7]

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER BUFFER RAM		
Size: C	Document Number: 56000L008 (L008D14.SCH)	REV
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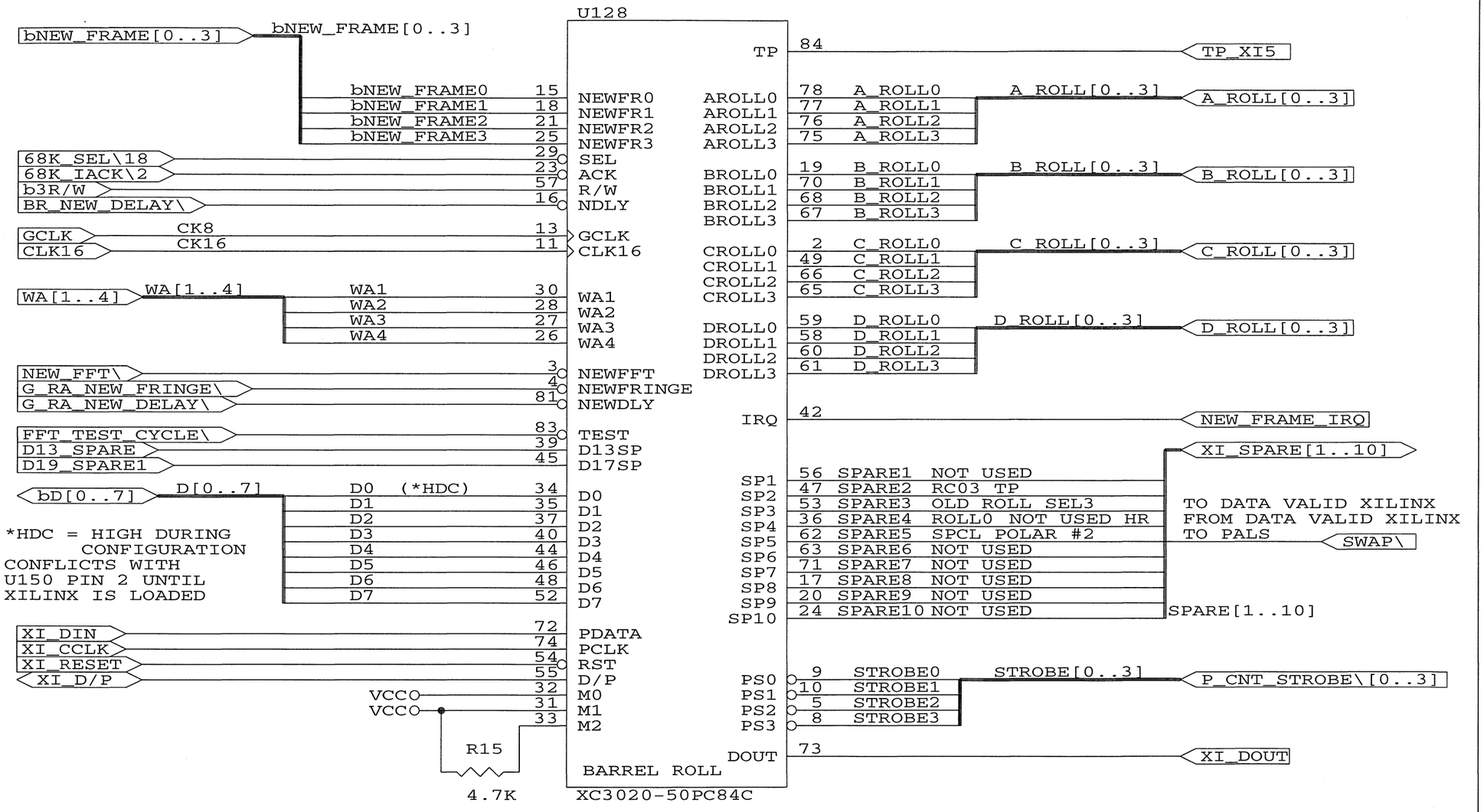
FFT VALID buffers

NOMENCLATURE EXAMPLE:

A0C00

- 0=MAGNITUTE, 1=SIGN
- CHANNEL NUMBER, 0-7
- ANTENNA NUMBER, 0-19

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: OUTPUT BUFFERS		
Size: B	Document Number: 56000L008 (L008D15.SCH)	REV:
Date: November 19, 1996	Sheet 15 of 31	



Notes:
VCC - 22,64
GND - 1,43

BARREL ROLL XILINX

K012D01.BLK B SIZE

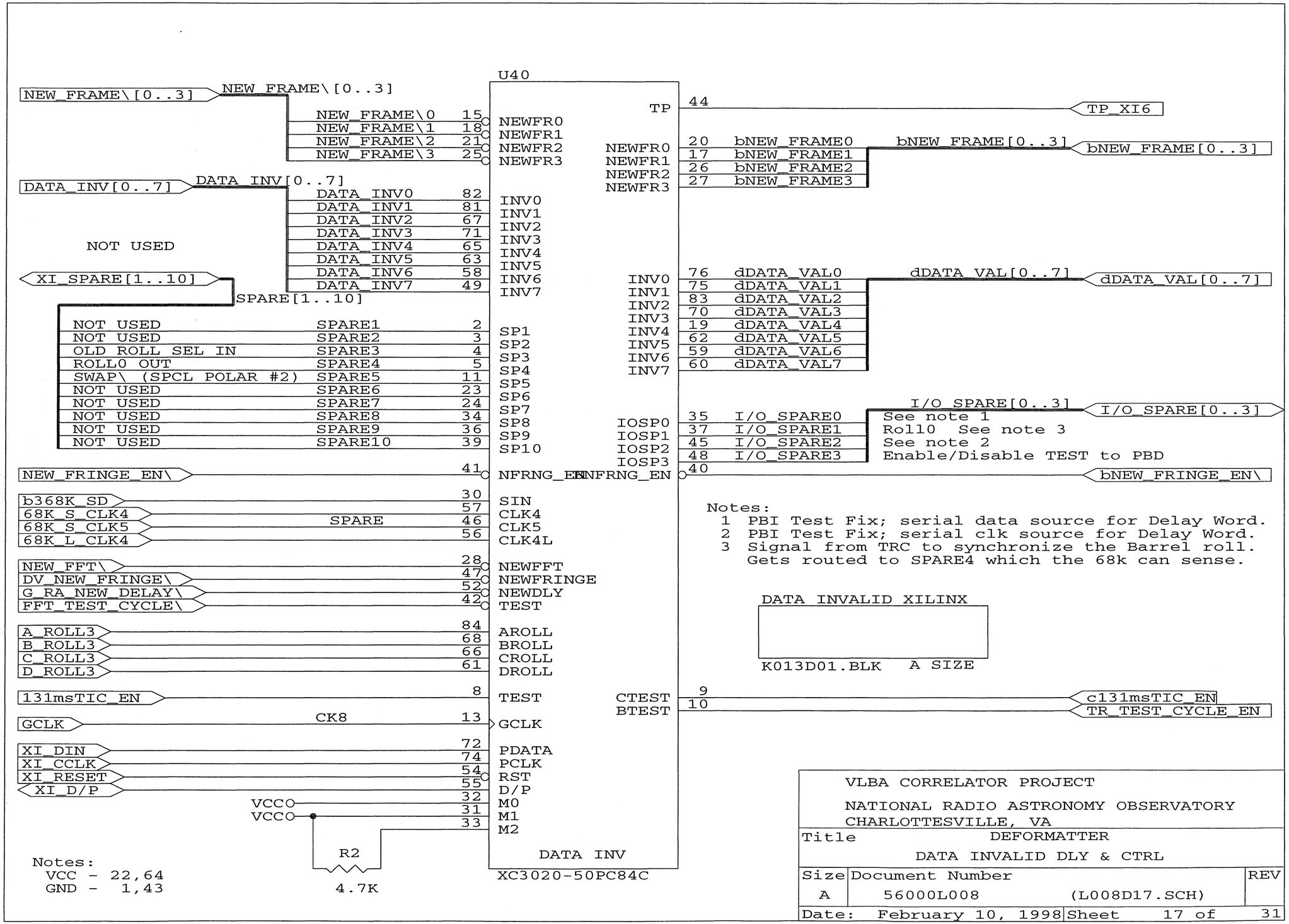
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title DEFORMATTER
BARREL ROLL CONTROL

Size	Document Number	REV
A	56000L008 (L008D16.SCH)	

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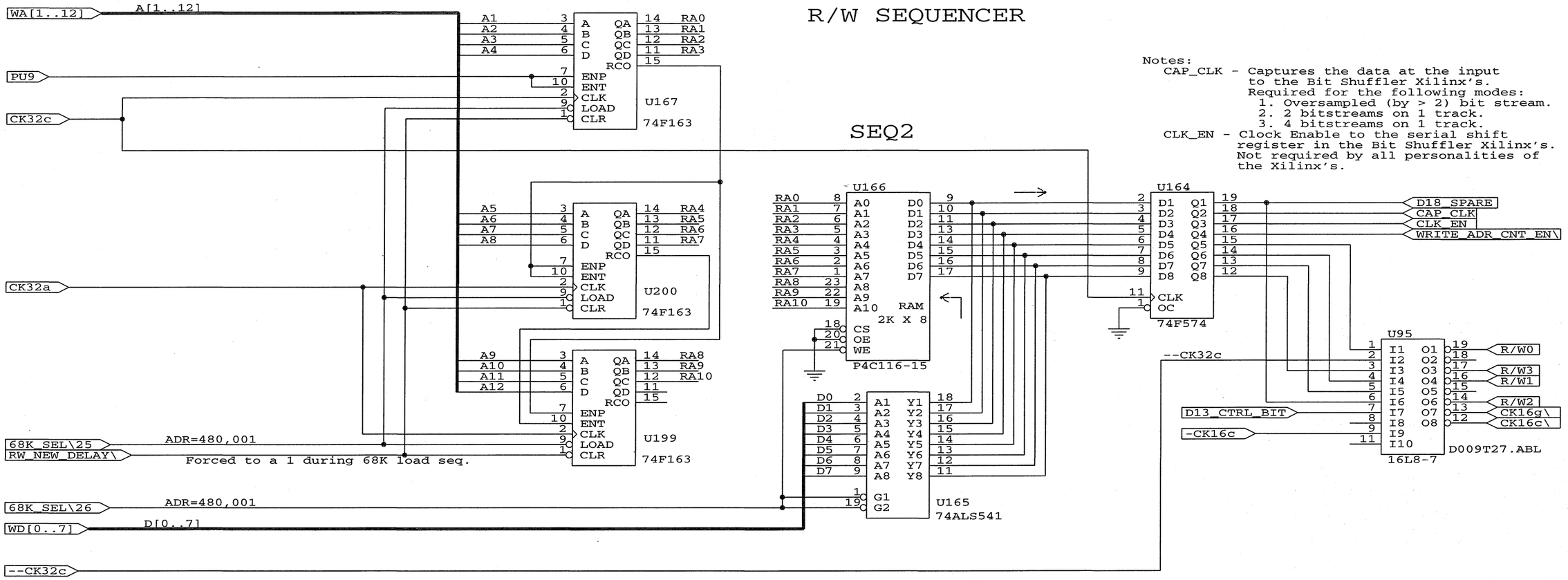

U40
NEW_FRAME\[0..3]
NEW_FRAME\0 15
NEW_FRAME\1 18
NEW_FRAME\2 21
NEW_FRAME\3 25
NEWFR0
NEWFR1
NEWFR2
NEWFR3
DATA_INV[0..7]
DATA_INV0 82
DATA_INV1 81
DATA_INV2 67
DATA_INV3 71
DATA_INV4 65
DATA_INV5 63
DATA_INV6 58
DATA_INV7 49
INV0
INV1
INV2
INV3
INV4
INV5
INV6
INV7
NOT USED
XI_SPARE[1..10]
SPARE[1..10]
NOT USED SPARE1 2
NOT USED SPARE2 3
OLD ROLL SEL IN SPARE3 4
ROLL0 OUT SPARE4 5
SWAP\ (SPCL POLAR #2) SPARE5 11
NOT USED SPARE6 23
NOT USED SPARE7 24
NOT USED SPARE8 34
NOT USED SPARE9 36
NOT USED SPARE10 39
SP1
SP2
SP3
SP4
SP5
SP6
SP7
SP8
SP9
SP10
NEW_FRINGE_EN\ 41
NFRNG_EN
b368K_SD 30
SIN
68K_S_CLK4 57
CLK4
SPARE
68K_S_CLK5 46
CLK5
68K_L_CLK4 56
CLK4L
NEW_FFT\ 28
NEWFFT
DV_NEW_FRINGE\ 47
NEWFRINGE
G_RA_NEW_DELAY\ 52
NEWDLY
FFT_TEST_CYCLE\ 42
TEST
A_ROLL3 84
AROLL
B_ROLL3 68
BROLL
C_ROLL3 66
CROLL
D_ROLL3 61
DROLL
131msTIC_EN 8
TEST
CK8
GCLK 13
GCLK
XI_DIN 72
PDATA
XI_CCLK 74
PCLK
XI_RESET 54
RST
XI_D/P 55
D/P
VCCO 32
M0
VCCO 31
M1
33
M2
R2
4.7K
DATA INV
XC3020-50PC84C
TP 44
TP_XI6
NEWFR0 20 bNEW_FRAME0
NEWFR1 17 bNEW_FRAME1
NEWFR2 26 bNEW_FRAME2
NEWFR3 27 bNEW_FRAME3
bNEW_FRAME[0..3]
bNEW_FRAME[0..3]
INV0 76 dDATA_VAL0
INV1 75 dDATA_VAL1
INV2 83 dDATA_VAL2
INV3 70 dDATA_VAL3
INV4 19 dDATA_VAL4
INV5 62 dDATA_VAL5
INV6 59 dDATA_VAL6
INV7 60 dDATA_VAL7
dDATA_VAL[0..7]
dDATA_VAL[0..7]
I/O_SPARE[0..3]
I/O_SPARE[0..3]
IOSP0 35 I/O_SPARE0 See note 1
IOSP1 37 I/O_SPARE1 Roll0 See note 3
IOSP2 45 I/O_SPARE2 See note 2
IOSP3 48 I/O_SPARE3 Enable/Disable TEST to PBD
NFRNG_EN 40
bNEW_FRINGE_EN\
Notes:
1 PBI Test Fix; serial data source for Delay Word.
2 PBI Test Fix; serial clk source for Delay Word.
3 Signal from TRC to synchronize the Barrel roll.
Gets routed to SPARE4 which the 68k can sense.
DATA INVALID XILINX
K013D01.BLK A SIZE
CTEST 9
BTEST 10
c131msTIC_EN
TR_TEST_CYCLE_EN
Notes:
VCC - 22,64
GND - 1,43
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
DEFORMATTER
DATA INVALID DLY & CTRL
Size A
Document Number 56000L008 (L008D17.SCH)
REV
Date: February 10, 1998
Sheet 17 of 31

R/W SEQUENCER

SEQ2

Notes:
CAP_CLK - Captures the data at the input to the Bit Shuffler Xilinx's. Required for the following modes:
1. Oversampled (by > 2) bit stream.
2. 2 bitstreams on 1 track.
3. 4 bitstreams on 1 track.

CLK_EN - Clock Enable to the serial shift register in the Bit Shuffler Xilinx's. Not required by all personalities of the Xilinx's.



NOTES:

Count seq. 0-2047, 64uS
Repeating pattern length in RAM depends on configuration
64.45.. RAM cycles (0-2047) for each FRINGE/DELAY cycle.

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: R/W SEQUENCER		
Size: B	Document Number: 56000L008 (L008D18.SCH)	REV
Date: November 19, 1996	Sheet 18 of 31	

Sequencer 1

LOOPS EVERY 2 FFT CYCLES

18ns

CK8 to TRACK RECOVERY is generated from seperate RAM bit so that clock skew between caeds can be compensated for.

(Make sure that FFT INIT does not interfere with loading the RAMs)

PIN 7, NEW_FRINGE_EN\ SELECTS THE FFT CYCLE WHERE PINS 2 AND 3 DETERMINE PLACEMENT IN THE FFT CYCLE.

NEW DELAY USED TO SYNCHRONIZE 131 MS. PIN 3 NOT USED IN PAL.

Force outputs inactive while 68K loads seq RAMs

Also used on L23 in U181 to mask IRQ2

NOTES:

RAM seq. 0-515 (1FFT cycle)
FFT cycle 16.125uS

Sync to system FFT INIT
NEW DELAY: Station dependent.
Proceeds NEW FRINGE by enough time to fill the BUFFER RAM.
BR: NEW DELAY to Barrel Roll ctrl logic.
RA: NEW DELAY to Ram Addressing logic.
G RA: RA NEW DELAY * PPT TEST * 68K CTRL (Reset ctrl to BUF RAM write adr counter)
G DV: FFT VALID flag to FFT VALID PALs.
DD: NEW DELAY to DEMUX-DELAY logic.
TR: NEW DELAY to Track Recovery logic.
DATA INVALID WINDOW : Can be used to prevent: A FFT discarded because of a couple of bad data bits. Force DATA VALID a few bit periods before the end and at the beginning of an FFT cycle.
NEW FFT\: True for 1 CK32 at the end of ea. FFT cycle.
-NEW DELAY\: Captured by CK8 on TRACK RECOVERY bd.

68K CTRLn: Enabled only when delay actually changes. This prevents FFTs from being discarded when data is good.

VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title: FFT SEQUENCER and CLOCK GENERATOR	
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DLY WORD A&B

L008D26.SCH

PU6
SC_DLY_MA\
SC_DLY_MA
SD_DLY_MA\
SD_DLY_MA
SC_DLY_MB\
SC_DLY_MB
SD_DLY_MB\
SD_DLY_MB
SC_DLY_MC\
SC_DLY_MC
SD_DLY_MC\
SD_DLY_MC
SC_DLY_MD\
SC_DLY_MD
SD_DLY_MD\
SD_DLY_MD
DELAY_SR_SEL
68K_SEL\11
68K_SEL\12

bD[0..15]

L008D26.SCH

SERIAL OUT

L008D28.SCH

PU8
b2LDS\
68K_SEL\20
68K_SEL\21
68K_SEL22
WD[0..15]
CK12.5

68K_SD
68K_S_CLK[0..7]
68K_L_CLK[0..7]
SERIAL_EN\
SERIAL_CTS
68K-XI2_D/P
68K-XI1_D/P

L008D28.SCH

HCB Interface

L008D29.SCH

PU1
SELECT
SELECT\
STROBE
STROBE\
MODE0
MODE0\
MODE1
MODE1\
68K_SEL\9
68K_SEL\10
READ\
WRITE\
bD[0..7]
D[0..7]

HCB[0..7]
HCB\[0..7]
ACK
ACK\
RESET_68K
MDATARDY
MASTER_CTS\
MASTER_IRQ\

L008D29.SCH

DUART

L008D30.SCH

IACK\3
TERM_TXD
TAPE_DR_TXD
b2R/W
68K_SEL\8
68K_RESET\
bA[1..4]
D[0..7]

TAPE_DR_RXD
TERM_RXD
OP3_COUNTER/TIMER
OP4_ChA_RX_RDY
OP6_ChA_TX_RDY
DUART_DTACK\
DUART_IRQ\

L008D30.SCH

IRQ & SENSE

L008D23.SCH

SERIAL_CTS
68K-XI1_D/P
68K-XI2_D/P
IACK\[1..7]
G_RA_NEW_FRINGE\
DV_NEW_FRINGE\
G_RA_NEW_DELAY\
DD_NEW_DELAY\
131msTIC\
NEW_FRAME_IRQ
8751_IRQ[0..3]
8751_CTS[0..3]
NMI_SW
SPARE_IRQ
XI_SPARE4
MDATARDY
MASTER_IRQ\
MASTER_CTS\
OP3_COUNTER/TIMER
OP4_ChA_RX_RDY
OP6_ChA_TX_RDY
DUART_IRQ\
68K_SEL\6
68K_SEL\7
68K_CTRL4
68K_CTRL6
b1AS\
BOOT\
FC[0..2]
bA[1..3]
AUTOVECTOR\
IPL\[0..2]

bD[0..15]
CK12.5a

L008D23.SCH

ROM

L008D25.SCH

68K_SEL\3
bA[1..16]
D[0..15]

L008D25.SCH

ADR DECODE

L008D22.SCH

PU11
IACK\7
CK12.5
bA[17..23]
b2LDS\
b2UDS\
b3AS\
b1R/W
DUART_DTACK\
BOOT\
DTACK\
BERR\
68K_SEL\[3..36]
68K_SEL\[3..45]
68K-8751_READ[0..3]
68K-8751_WRITE[0..3]
68K_SEL22
RAM_\L0
RAM_\U0
RAM_\L1
RAM_\U1
EN_IOD_BUS\
EN_bD_BUS\

L008D22.SCH

RAM

L008D24.SCH

RAM_\L0
RAM_\U0
RAM_\L1
RAM_\U1
b2R/W
bA[1..16]
D[0..15]

L008D24.SCH

BUFFERS

L008D21.SCH

EN_IOD_BUS\
EN_bD_BUS\
68K_SEL\30
A[1..23]
D[0..15]
R/W
LDS\
UDS\
AS\
bA[1..23]
bD[0..15]
WD[0..15]
WA[1..13]
68K-8751_B[0..7]
b1R/W
b2R/W
b3R/W
b4R/W
b1LDS\
b2LDS\
b1UDS\
b2UDS\
b1AS\
b2AS\
b3AS\

L008D21.SCH

U144

74ALS574

bD0 2 D1 Q1 19 68K_CTRL0
bD1 3 D2 Q2 18 68K_CTRL1
bD2 4 D3 Q3 17 68K_CTRL2
bD3 5 D4 Q4 16 68K_CTRL3
bD4 6 D5 Q5 15
bD5 7 D6 Q6 14 68K_CTRL5
bD6 8 D7 Q7 13 68K_CTRL4
bD7 9 D8 Q8 12 68K_CTRL7
68K_SEL\19 11 CLK
1 OC
ADR=380,001

68K_CTRL[0..7]

68K_CTRL4 Added 1=Enable TR IRQ
68K_CTRL6 To sh 23

Destination:
0 XILINX- reset, Bit Shufflers, 4 plcs.
1 XILINX reset, Barrel Roll & Data Valid ctrl
2 D19, FFT SEQ, 0= same delay value.
3 D19, FFT SEQ, 0= 68K writing into seq RAMs.
4 D19, spare xxxxxxxxxx see above
5 D14, 68K TEST EN.
6 D23, IRQ EN/RESET
7 Track Recovery Reset term, ORed with 68K_RESET\

IACK\2
68K_IACK\2

68K-XI1_D/P
68K-XI2_D/P

Oscillator U222 Removed
From Sht.19
uPC16
U220F 74F04
U220A 74F04
CK12.5a
CK12.5b

Added wire
PU10

U210 68000RC
E1 CLK
VPA G2 VPA
IPL\0 J2 IPL0
IPL\1 H3 IPL1
IPL\2 H2 IPL2
BGACK\ C1 BGACK
BR\ D1 BR
DTACK\ B1 DTACK
BERR\ J1 BERR
FC0 K3 FC0
FC1 J3 FC1
FC2 K2 FC2
BG\ C2 BG
VMA\ G1 VMA
E H1 E
F1 HALT
F2 RESET
A2 AS
B3 UDS
B2 LDS
C3 R/W
A1 A1 ... A23
K4 A1 ... K1 A23
D0 ... D15
B4 D0 ... B10 D15

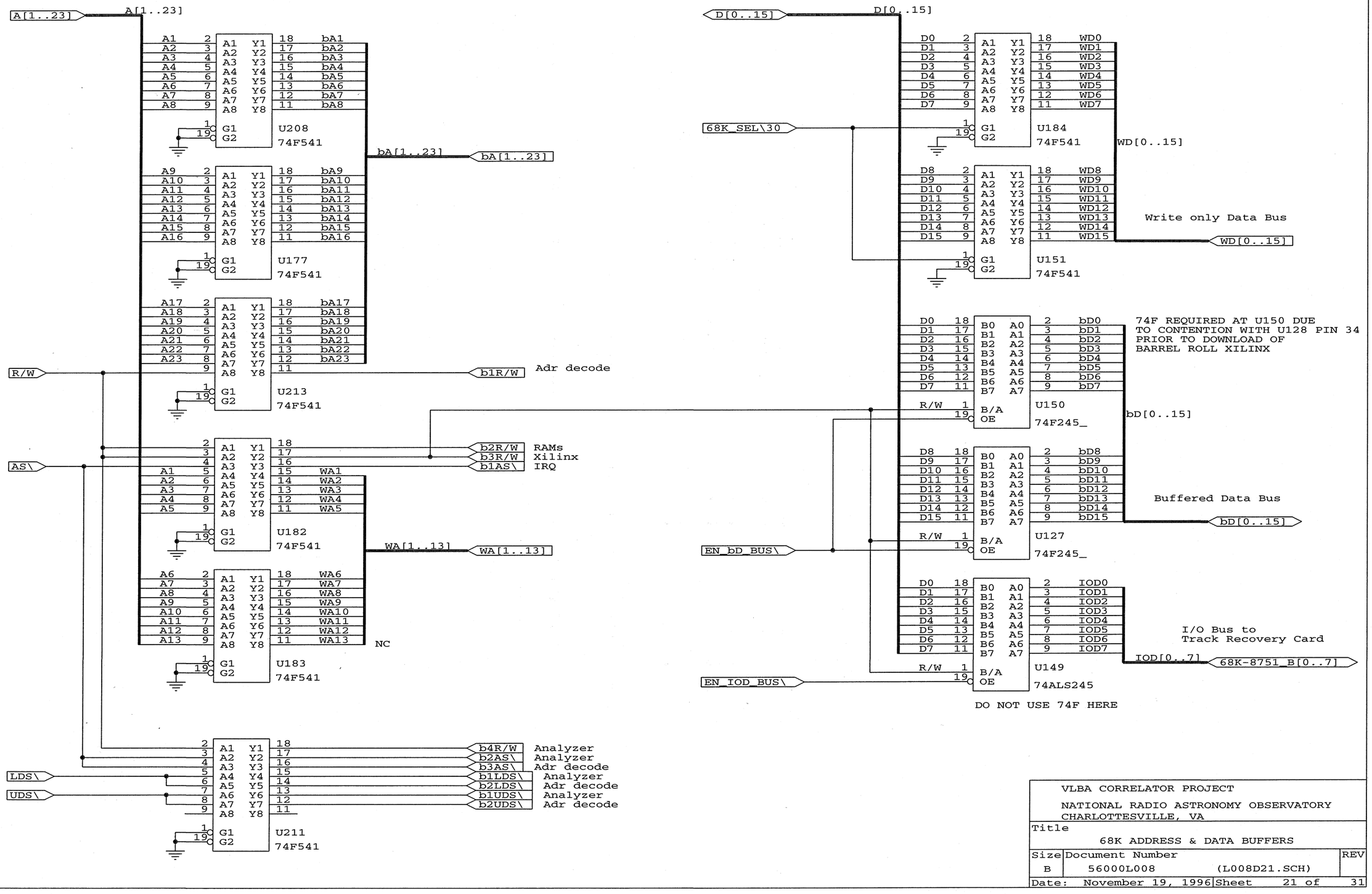
VCC
R23 3K
R1 3K

Logic analyzer connector
J2
3M64
D4 D3 D2 D1 D0 b2AS\ b1UDS\ b1LDS\ b4R/W DTACK\ BG\ BGACK\ BR\ CK12.5b BOOT\ RESET\ VMA\ E VPA\ BERR\ IPL\2 IPL\1 IPL\0 FC2 FC1 FC0 A1 A2 A3 A4
D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5

74LS33
U209B
U209A
RESET_68K
RESET
HALT\
RESET\
To J2
BOOT\
68K_RESET\ To sheet 30

ORed with 68K_CTRLT to TRACK RECOVERY cards

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title DEFORMATTER 68K MICRO
Size C | Document Number 56000L008 (L008D20.SCH) | REV
Date: November 19, 1996 | Sheet 20 of 31



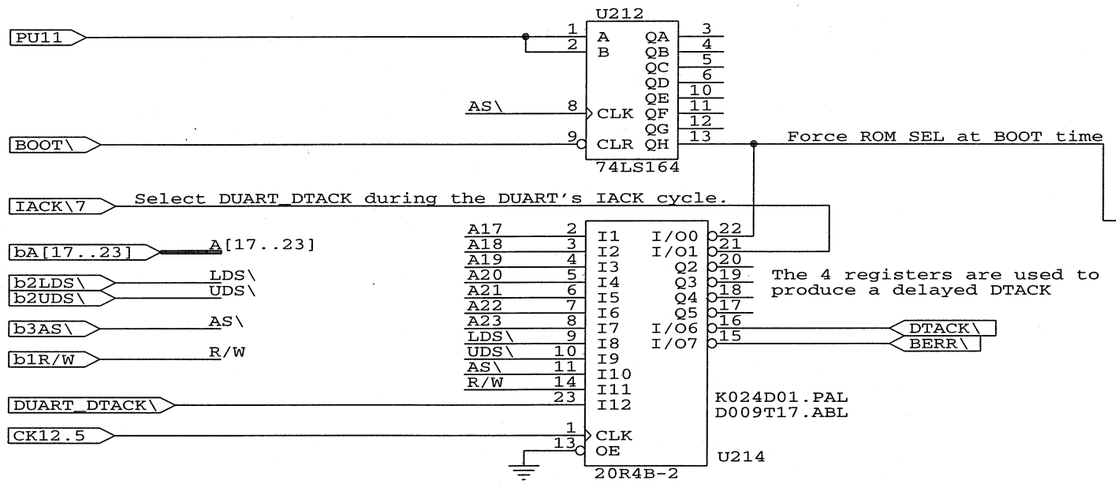
VLBA CORRELATOR PROJECT

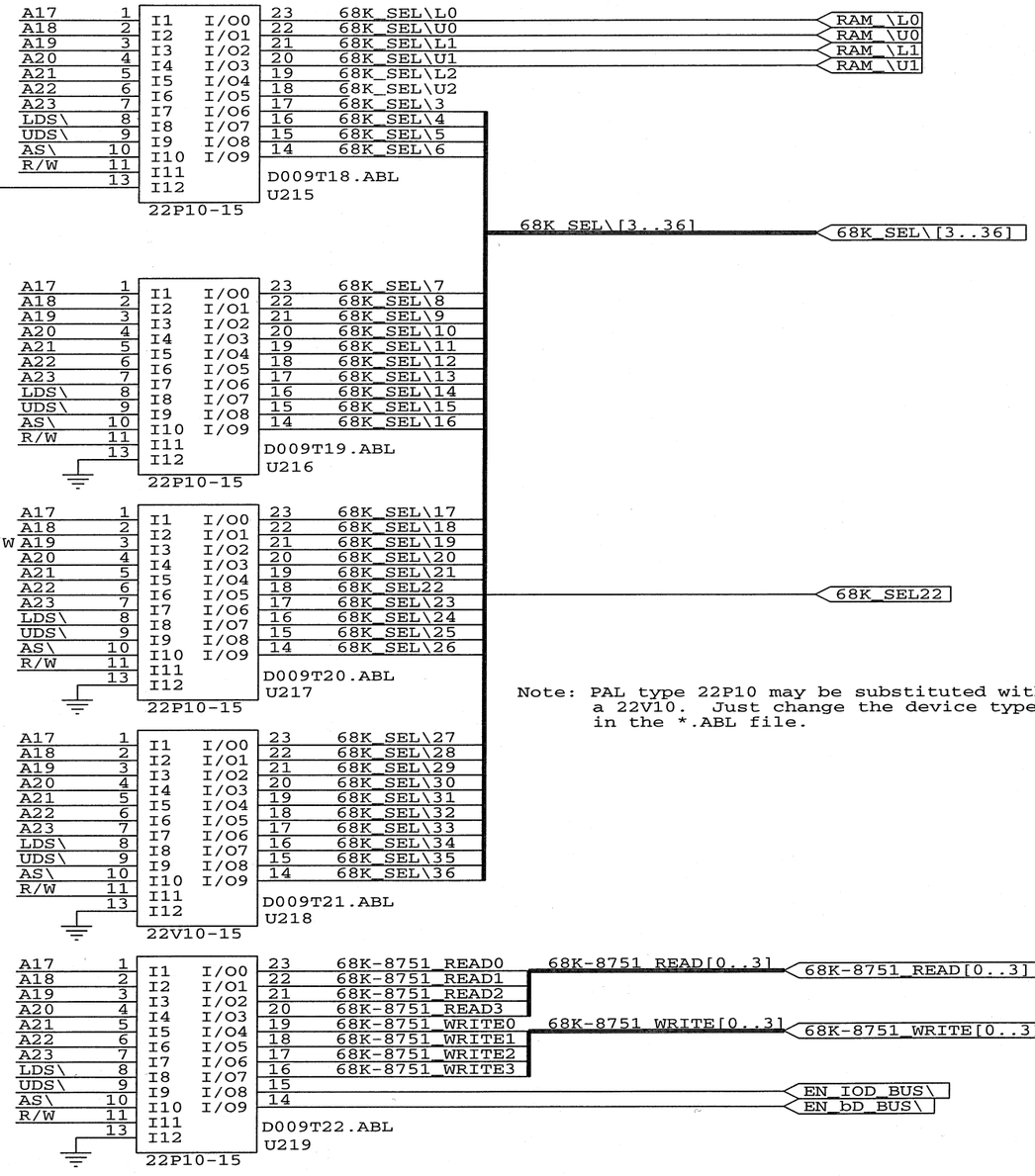
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title

68K ADDRESS & DATA BUFFERS

Size	Document Number	REV
B	56000L008 (L008D21.SCH)	
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Note: PAL type 22P10 may be substituted with a 22V10. Just change the device type in the *.ABL file.

MEMORY DECODE:

Notes:
1. A23 - controls DTACK
2. A22 A21 - selects data bus
   - 0 0 - D[n,n] bus, main bus
   - 0 1 - bD[n,n] bus, buffered R/W
   - 1 0 - WD[n,n] bus, write only
   - 1 1 - IOD[n,n] bus to 8751's
3. A4-A24 are 1's during the IAK cycle of the DUART.

A23	A22	A21	A20	A19	A18	A17		68k Adr.	Decoder Select	Description
8	4	2	1	8	4	2				
0	0	0	0	0	0	0	=	000,000	0	RAM 1 (sh 24)
0	0	0	0	0	0	1	=	020,000	1	RAM 2 (sh 24)
0	0	0	0	0	1	0	=	040,000	2	
1	0	0	0	0	1	1	=	860,000	3	P ROM (sh 25)
0	0	0	0	1	0	0	=	080,000	4	
0	0	0	0	1	0	1	=	0A0,000	5	
0	0	1	0	0	0	0	=	200,000	6	IRQ ID (sh 23)
1	0	0	0	0	1	0	=	840,000		Decoded as bus error
0	0	1	0	0	0	1	=	220,000	7	Sense input (sh 23)
1	0	0	0	1	1	0	=	8C0,001	8	DUART (sh 30)
0	0	1	0	0	1	0	=	240,001	9	HCB Read (sh 29)
0	0	1	0	0	1	1	=	260,001	10	HCB Write (sh 29)
0	0	1	0	1	0	0	=	280,000	11	DLY WD 1 (sh 26)
0	0	1	0	1	0	1	=	2A0,000	12	DLY WD 2 (sh 26)
0	0	1	0	1	1	0	=	2C0,000	13	PARITY CNT 1 (sh 3)
0	0	1	0	1	1	1	=	2E0,000	14	PARITY CNT 2 (sh 4)
0	0	1	1	0	0	0	=	300,000	15	PARITY CNT 3 (sh 5)
0	0	1	1	0	0	1	=	320,000	16	PARITY CNT 4 (sh 6)
0	0	1	1	0	1	0	=	340,000	17	
0	0	1	1	0	1	1	=	360,001	18	Barrel Roll Xilinx read & write (sh 16)
0	0	1	1	1	0	0	=	380,001	19	Control Byte Register (sh 20)
0	1	0	0	0	0	0	=	400,001	20	SER DATA: Destination address load (sh 28)
0	1	0	0	0	0	1	=	420,001	21	SER DATA: Strobe data at destination (sh 28)
0	1	0	0	0	1	0	=	440,000	22	SER DATA: Start serial data xfer (sh 28)
0	1	0	0	0	1	1	=	460,000	23	FFT SEQ RAM Load f163 (An * AS) (sh 19)
0	1	0	0	0	1	1	=	460,000	24	WE to RAM (An * AS * LDS * UDS) (sh 19)
0	1	0	0	1	0	0	=	480,000	25	DLY SEQ RAM Load f163 (An * AS) (sh 18)
0	1	0	0	1	0	0	=	480,000	26	WE to RAM (An * AS * LDS * UDS) (sh 18)
0	1	0	0	1	0	1	=	4A0,000	27	BUF RAM ADDR SEQ Load f163 (An * AS) (sh 13)
0	1	0	0	1	0	1	=	4A0,000	28	WE to RAM (An * AS * LDS * UDS) (sh 13)
0	1	0	0	1	1	0	=	4C0,000	29	RAM READ OFFSET ADR REG (sh 13)
X	1	0	X	X	X	X			30	Enable WD bus buffer, write only
0	0	1	1	1	0	1	=	3A0,000	31	DLY WD 3 (sh 26)
0	0	1	1	1	1	0	=	3C0,000	32	DLY WD 4 (sh 26)
0	0	0	1	X	X	X	=		33	PBI Test Fix Data Gen WW card.
							=		34	
							=		35	
0	0	0	0	1	1	1	=		36	TP22Sync, Test Point 22
0	1	1	0	0	0	0	=	600,000	37	8751 A READ (to Track Recovery card)
0	1	1	0	0	0	1	=	620,000	38	8751 B READ (to Track Recovery card)
0	1	1	0	0	1	0	=	640,000	39	8751 C READ (to Track Recovery card)
0	1	1	0	0	1	1	=	660,000	40	8751 D READ (to Track Recovery card)
0	1	1	0	0	0	0	=	600,000	41	8751 A WRITE (to Track Recovery card)
0	1	1	0	0	0	1	=	620,000	42	8751 B WRITE (to Track Recovery card)
0	1	1	0	0	1	0	=	640,000	43	8751 C WRITE (to Track Recovery card)
0	1	1	0	0	1	1	=	660,000	44	8751 D WRITE (to Track Recovery card)
0	1	1	0	1	0	0	=	680,000	[41,43]	8751 A & C WRITE (Micro A on both Track Recovery cards)
0	1	1	0	1	1	0	=	6C0,000	[42,44]	8751 B & D WRITE (Micro B on both Track Recovery cards)
0	1	1	0	1	1	1	=	6E0,000	[41..44]	Write both micros on both Track Recovery cards.
0	1	1	X	X	X	X	=		XX	Enable Input/Oupt Data Bus to Track Recovery Cards (sh 21). See note 3.
X	0	1	X	X	X	X	=		XX	Enable buffered Data Bus, R/W (sh 21)

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: 68K MEMORY DECODE

Size	Document Number	REV
B	56000L008 (L008D22.SCH)	

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Note: IACK#'s don't match IPL#'s

U179

bA[1..3] → A[1..3]
FC[0..2] → FC[0..2]
b1AS\
DV_NEW_FRINGE\
G_RA_NEW_FRINGE\
G_RA_NEW_DELAY\
DD_NEW_DELAY\

A1 1, A2 2, A3 3, FC0 4, FC1 5, FC2 6, AS\ 7, 8, 9, 10, 11, 13

I1 I/O0 23 IACK\1
I2 I/O1 22 IACK\2
I3 I/O2 21 IACK\3
I4 I/O3 20 IACK\4
I5 I/O4 19 IACK\5
I6 I/O5 18
I7 I/O6 17 IACK\7
I8 I/O7 16
I9 I/O8 15 SR1\
I10 I/O9 14 SR2\
I11
I12

IACK\[1..7] → IACK\[1..7]
AUTOVECTOR\

NEW FRAME DUART

IACK\6 NMI ACK
Ctrl DUART's DTACK IACK cycle.

D009T23.ABL
22V10-15

PAL hardcoded to select 2 of 4 inputs to feed to the S-R IRQ logic in U180.

68k IPL Source Table

IPL	Description	External ctrl
0	none, no IRQ active	
1	MASTER_IRQ	BOOT resets latch
2	U8751- 4 inputs ORed in U181.	Start/Stop obsv
3	not used	
4	NEW_DLEAY	68K_CTRL6
5	NEW_FRAME_IRQ	68K reg in Xilinx
6	DUART	DUAT mask
7	NMI from PBI Test Fix switch	Test Fix only.

S-R logic:

Set by IRQ device.
Reset by 68K INTR ACK.
IRQ signal must be gone when 68K services the INTR.
Max of 4 IRQ sources.

U180, PIN 10 IS STILL WIRED TO U156, PIN 19, WHICH IS NOW 131msDLYD\ (BUT NOT USED HERE)

MASTER_IRQ\
68K_CTRL6
BOOT\
131msTic\
Enable/reset inputs

BOOT\

U180

A1 1, A2 2, A3 3, FC0 4, FC1 5, FC2 6, AS\ 7, SR1\ 8, SR2\ 9, 10, 11, 13, 14, 23

I1 O0 22 Q1
I2 I/O1 21 Q2
I3 I/O2 19
I4 I/O3 18 Q3
I5 I/O4 17
I6 I/O5 16 Q4
I7 I/O6 15
I8 O7
I9
I10
I11
I12
I13
I14

The Qn outputs are internally fead back

IRQ1
IRQ2
d131msTic
IRQ4

22V10-15
D009T24.ABL
K025D01.PAL

U181

NEW_FRINGE_IRQ\ 1
NEW_DELAY_IRQ\ 2
3
MASTER_IRQ\ 4
OP3_COUNTER/TIMER 5
OP4_ChA_RX_RDY 6
OP6_ChA_TX_RDY 7
DUART_IRQ\ 8
NEW_FRAME_IRQ 9
SPARE_IRQ 10
REQ0 11
REQ1 13
REQ2 14
REQ3 23

I1 O0 22 IPL\0
I2 I/O1 21 IPL\1
I3 I/O2 20
I4 I/O3 19
I5 I/O4 18
I6 I/O5 17 gNF\
I7 I/O6 16 U8751\
I8 O7 15 IPL\2
I9
I10
I11
I12
I13
I14

IPL\[0..2] → IPL\[0..2]

NMI input

1=en u8751 & NF IRQ

68K_CTRL4

Functions:
1. 5 OR gates (internal)
The output of the OR gates can be used as inputs to the encoder
2. LS148 encoder
see source table above.

20L8B-2
D009T25.ABL

The 4 REQn lines are ORed together in PAL

8751_IRQ[0..3]
REQ[0..3]

REQ0 2, REQ1 3, REQ2 4, REQ3 5, NEW_FRINGE_IRQ\ 6, NEW_DELAY_IRQ\ 7, d131msTic 8, 9

D1 Q1 19 D0
D2 Q2 18 D1
D3 Q3 17 D2
D4 Q4 16 D3
D5 Q5 15 D4
D6 Q6 14 D5
D7 Q7 13 D6
D8 Q8 12 D7

11 CLK
1 OC

U148
74ALS574

D[0..15] → bD[0..15]

IRQ SOURCE

68K_SEL\6
ADR=200,000

U220B
3 → 4
74F04

OP3_COUNTER/TIMER
OP4_ChA_RX_RDY
OP6_ChA_TX_RDY
DUART_IRQ\
NEW_FRAME_IRQ
SPARE_IRQ

OP3_COUNTER/TIMER 2, OP4_ChA_RX_RDY 3, OP6_ChA_TX_RDY 4, DUART_IRQ\ 5, NEW_FRAME_IRQ 6, SPARE_IRQ 8, 9

D1 Q1 19 D8
D2 Q2 18 D9
D3 Q3 17 D10
D4 Q4 16 D11
D5 Q5 15 D12
D6 Q6 14 D13
D7 Q7 13 D14
D8 Q8 12 D15

11 CLK
1 OC

U125
74ALS574

VCC
R27
3K

8751_CTS[0..3]
CTS[0..3]

CTS0 2, CTS1 3, CTS2 4, CTS3 5, 6, 7, 8, 9

D1 Q1 19 D0
D2 Q2 18 D1
D3 Q3 17 D2
D4 Q4 16 D3
D5 Q5 15 D4
D6 Q6 14 D5
D7 Q7 13 D6
D8 Q8 12 D7

11 CLK
1 OC

U147
74ALS574

Clear To Send sense inputs to 68K

68K-XI1_D/P
68K-XI2_D/P
MASTER_CTS\
MDATARDY\

SENSE INPUT

Test Fix only

NMI_SW P1C2
BOOT\
IACK\6

U198

I1 I/O0 22
I2 I/O1 21
I3 Q2 20 cSW
I4 Q3 19 dcSW
I5 Q4 18 NMI\
I6 Q5 17
I7 I/O6 16
I8 I/O7 15
I9
I10
I11
I12
CK12.5a → 1 CLK
13 OE

20R4B-2
D009T29.ABL

SERIAL_CTS
XI_SPARE4
ROLL0 from the TRC, synchronize roll.

2 D1 Q1 19 D8
3 D2 Q2 18 D9
4 D3 Q3 17 D10
5 D4 Q4 16 D11
6 D5 Q5 15 D12
7 D6 Q6 14 D13
8 D7 Q7 13 D14
9 D8 Q8 12 D15

11 CLK
1 OC

U124
74ALS574

68K_SEL\7
ADR=220,000

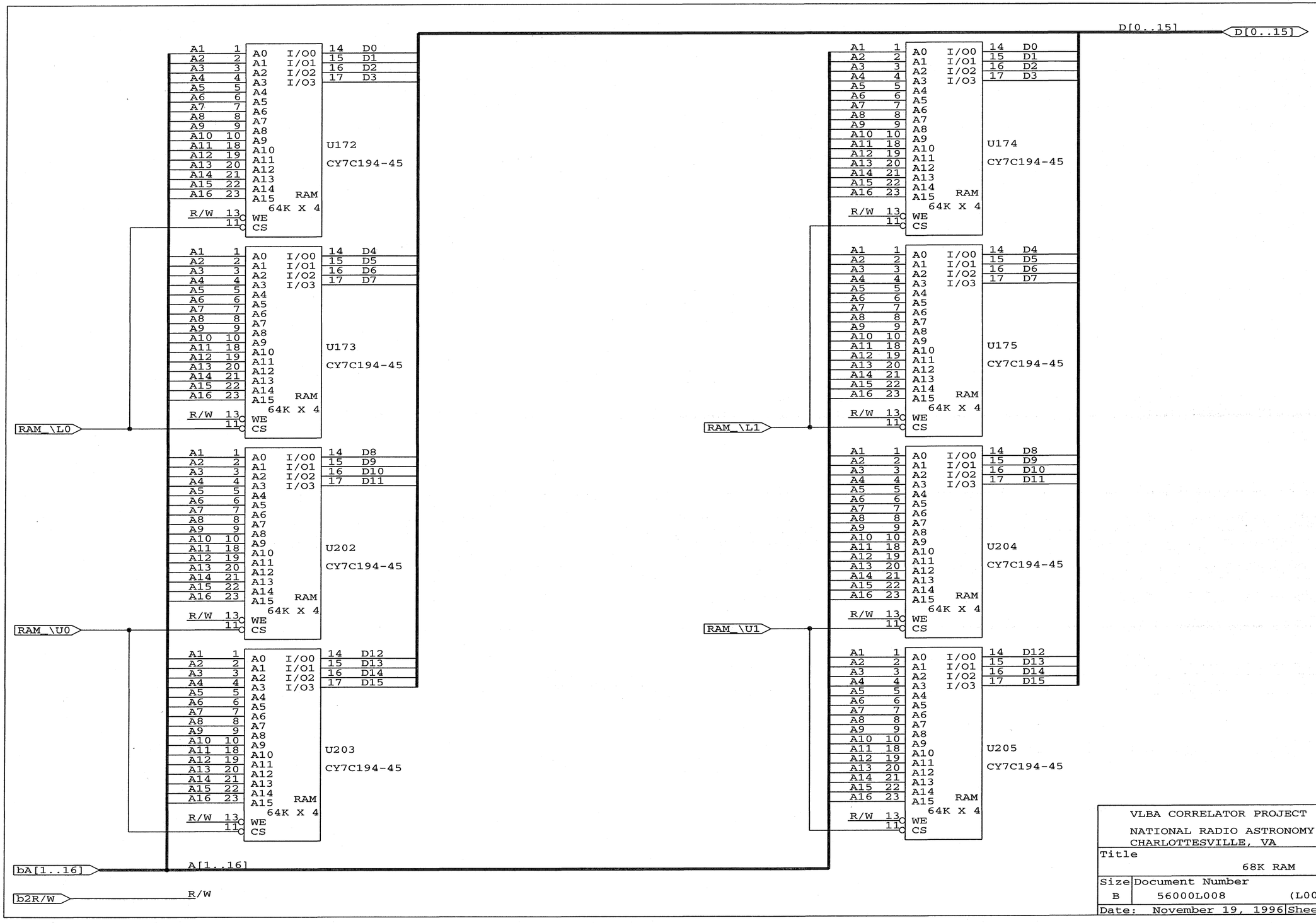
U220E
11 → 10
74F04

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER
68K IRQ & INPUT SENSE LOGIC

Size	Document Number	REV
B	56000L008 (L008D23.SCH)	

Date: November 19, 1996 Sheet 23 of 31



VLBA CORRELATOR PROJECT

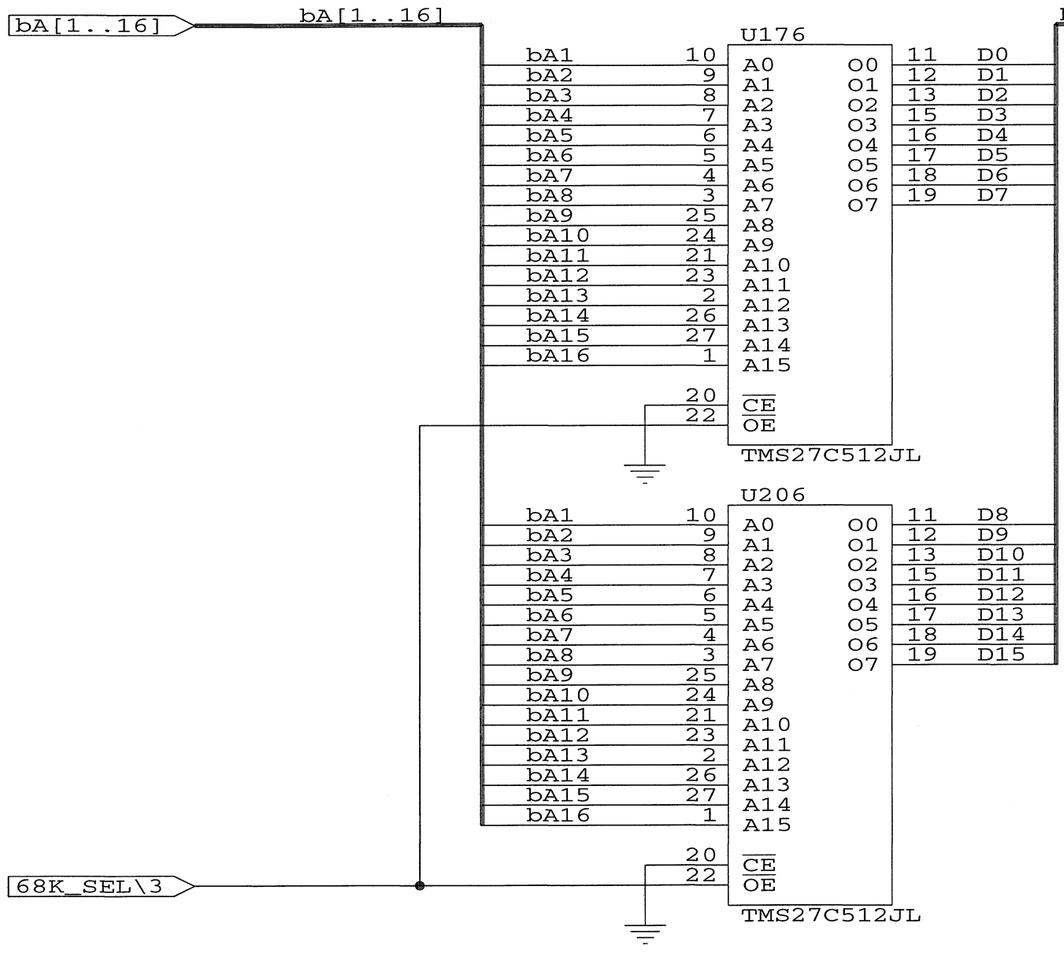
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title

68K RAM

Size	Document Number	REV
B	56000L008 (L008D24.SCH)	

Date: November 19, 1996 Sheet 24 of 31



VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title

68K ROM

Size	Document Number	REV
A	56000L008 (L008D25.SCH)	

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68K_SEL\31 ADR=3A0,000

PU6

68K_SEL\11 ADR=280,000

68K_SEL\32 ADR=3C0,000

68K_SEL\12 ADR=2A0,000

INTEGER DELAY WORD CAN COME FROM ONE OF TWO
FCC, AS A FUNCTION OF THE CROSSBAR SETTING

U9
100 OHM
RRRRRRRRR
1 1 2 3 4
ABABABABAB

DELAY CENTERS 2 & 3

1 2 3 4 5 6 7 8

VCC - 9
VEE - 8
GND - 16

U33

NORM
- —
ALT

SC_DLY_MA\ P3A4
SC_DLY_MA P3A2
SD_DLY_MA P3A6
SD_DLY_MA P3A5
SC_DLY_MC\ P3C4
SC_DLY_MC P3C2
SD_DLY_MC\ P3C6
SD_DLY_MC P3C5

I1N O1 I1 I2N O2 I2 I3N O3 I3 I4N O4 I4

10125_

68K ADDRESS 0xBF5 = MODEL OFFSET SOURCE SELECTION
= 1 FOR NORMAL
= 2 FOR ALTERNATE

U10
100 OHM
RRRRRRRRR
1 1 2 3 4
ABABABABAB

DELAY CENTERS 0 & 1

1 2 3 4 5 6 7 8

VCC - 9
VEE - 8
GND - 16

U11

NORM
- —
ALT

SC_DLY_MB\ P3B4
SC_DLY_MB P3B2
SD_DLY_MB\ P3B6
SD_DLY_MB P3B5
SC_DLY_MD\ P3C7
SC_DLY_MD P3B8
SD_DLY_MD\ P3B7
SD_DLY_MD P3C8

I1N O1 I1 I2N O2 I2 I3N O3 I3 I4N O4 I4

10125_

DELAY_SR_SEL LOW SELECTS A

INPUT A = NORMAL
INPUT B = ALTERNATE

U34

1A 1Y 4 clk
1B
2A 2Y 7 data
2B
3A 3Y 9 clk
3B
4A 4Y 12 data
4B

G
A/B

74F257

LSb first

74F299 mode: Shift left

74F299 U145-TOP

74F299 U122-TOP

74F299 U145-BOTTOM

74F299 U122-BOTTOM

74F299 U146-TOP

74F299 U123-TOP

74F299 U146-BOTTOM

74F299 U123-BOTTOM

G1 G2 S0 S1 CLK CLR SR SL
QA' A/QA B/QB C/QC D/QD E/QE F/QF G/QG H/QH QH'
bD0 bD1 bD2 bD3 bD4 bD5 bD6 bD7 bD8 bD9 bD10 bD11 bD12 bD13 bD14 bD15

bD[0..15] bD[0..15]

Delay Word For:
Delay Center 2
TRC micro 2, CallOffset2

Delay Word For:
Delay Center 3
TRC micro 3, CallOffset3

Delay Word For:
Delay Center 0
TRC micro 0, CallOffset0

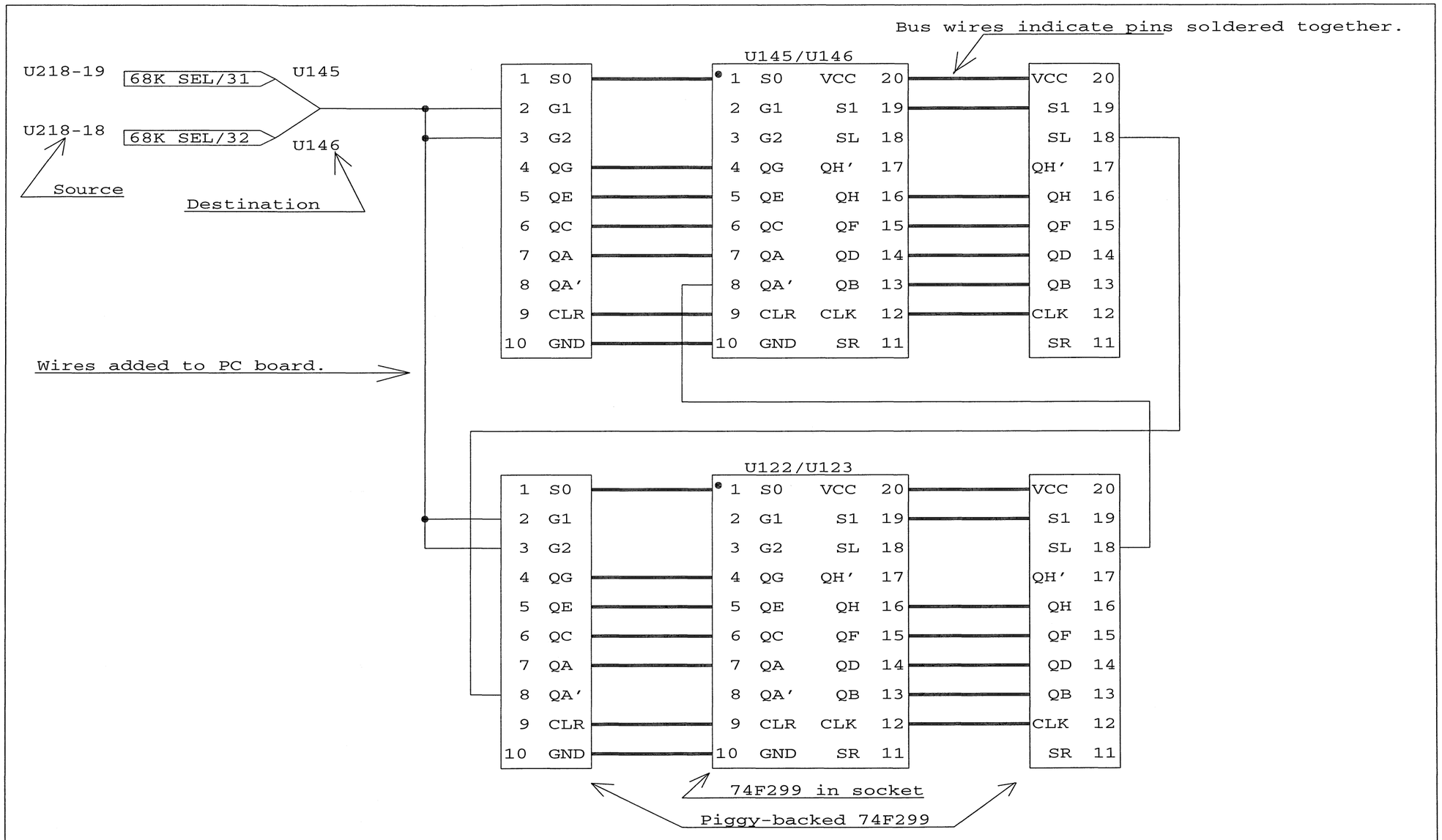
Delay Word For:
Delay Center 1
TRC micro 1, CallOffset1

L008D27.SCH
Board Fix
L008D27.SCH

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DELAY MODEL WORDS

Size	Document Number	REV
E	56000L008 (L008D26.SCH)	
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Purpose: To convert the 16 bit serial shift registers at U122 - U145 and at U123 - U146 into 32 bit shift registers.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER PIGGY-BACKED 74F299s	
Size A	Document Number 56000L008 (L008D27.SCH)	REV
Date: November 19, 1996	Sheet 27 of 31	

WD[0..15]

D[0..15]

For WORD instructions 16 bits are shifted out.
For BYTE instructions 8 bits (D8-D15) are shifted out.

U162

D0 2 D1 Q1 19 ADR0
D1 3 D2 Q2 18 ADR1
D2 4 D3 Q3 17 ADR2 > Destination address
D3 5 D4 Q4 16 ADR3 Enable decoders
D4 6 D5 Q5 15 ADR4
D5 7 D6 Q6 14 ADR5 > NOTE: ADR[4..6] are spares.
D6 8 D7 Q7 13 ADR6 Enable XILINX D/P bit
D7 9 D8 Q8 12 ADR7

Serial destination address strobe
ADR=400,001

68K_SEL\20 → 11 CLK, 1 OC

74ALS574

4 SI

D0 7 D1 8 D2 9 D3 10 D4 11 D5 13 D6 14 D7 15 D8 16 D9 17 D10 18 D11 19 D12 20 D13 21 D14 22 D15 23

P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 SO 6 → 68K_SD

5 L/S, 2 CP, 1 CS

U163

74F676

U220D

b2LDS\ → 9 8

74F04

U159

24 PE TC 14
15 D7 Q7 10
16 D6 Q6 9
17 D5 Q5 8
18 D4 Q4 6
20 D3 Q3 5
21 D2 Q2 4
22 D1 Q1 3
23 D0 Q0 2

1 U/D
11 CLK
13 CET
12 CEP

GND=7
VCC=19

74F269

U197B

3 → 4

74F04

U197D

9 → 8

74F04

SERIAL_CTS

U194

ADR0 1 ADR1 2 ADR2 3 ADR3 6

A B C G1 G2A G2B

Y0 15 SC0 — XILINX, BIT SHUFFLERS, PGM
Y1 14 SC1 — XILINX, BR & DV, PGM
Y2 13 SC2 — X-Parity ctrl wd.
Y3 12 SC3 — DEMUX-DELAY ctrl wd.
Y4 11 SC4 — Data Valid Xilinx ctrl wd.
Y5 10 SC5 — Data Valid Xilinx sp ctrl wd.
Y6 9 SC6 — Bit Shufflers Xilinx ctrl wd.
Y7 7 SC7 — NC

74F138

SC[0..7] → 68K_S_CLK[0..7]

LC[0..7] → 68K_L_CLK[0..7]

U195

ADR0 1 ADR1 2 ADR2 3 ADR3 6

A B C G1 G2A G2B

Y0 15 LC0 — Reset Parity counters
Y1 14 LC1 — X-Parity load.
Y2 13 LC2
Y3 12 LC3 — Data Valid load.
Y4 11 LC4
Y5 10 LC5 — Bit Shuffler load.
Y6 9 LC6
Y7 7 LC7

74F138

Destination strobe
ADR=420,000

68K_SEL\21

PU8

Start serial data xfer.
ADR=440,000

68K_SEL22

U221A

74LS74_

S D Q 4, 2, 5 START, 3 C, Q 6, R, 1

U160

TC\ 2
ADR0 4
ADR1 5
ADR2 6
ADR3 7
ADR4 8
ADR5 9
ADR6 10
ADR7 11

I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 23

I/O0 22 CLK
I/O1 21
Q2 20 LOAD\
Q3 19
Q4 18 Used internally
Q5 17
I/O6 16
I/O7 15

1 CLK, 13 OE

20R4B-2

D009T26.ABL
K026D01.PAL

To Xilinx, Bit Shufflers.
True only during sending data to Xilinx.
Prevents 3st contention within Xilinx.

SERIAL_EN\

68K-XI1_D/P
68K-XI2_D/P

U196

3 A 4 B 5 C 6 D — QA 14, QB 13, QC 12, QD 11, RCO 15

7 ENP
10 ENT
2 CLK
9 LOAD
1 CLR

CK.78125

74ALS161

CK12.5 → CK12.5

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER 68K SERIAL OUTPUT	
Size B	Document Number 56000L008 (L008D28.SCH)	REV
Date: November 19, 1996	Sheet 28 of 31	

PAL OUTPUTS

ACK: FOR WRITES FROM MASTER TO 2950, ACK GOES LOW WHEN 2950 IS BUSY, GOES HIGH WHEN 2950 IS READY FOR MORE DATA.

FOR READS OF 2950 BY MASTER, ACK GOES LOW WHEN 2950 HAS NEW DATA, HIGH WHEN MASTER HAS READ THE DATA.

FOR ATTENTION REQUEST FROM SLAVE TO MASTER, ACK GOES LOW; CLEARS WHEN MASTER INTEROGATES SLAVE.

RCVENA\: ENABLE DATA FROM HCB BUS TO LOCAL BUS

BUSENA: ENABLE DATA FROM LOCAL BUS TO HCB BUS

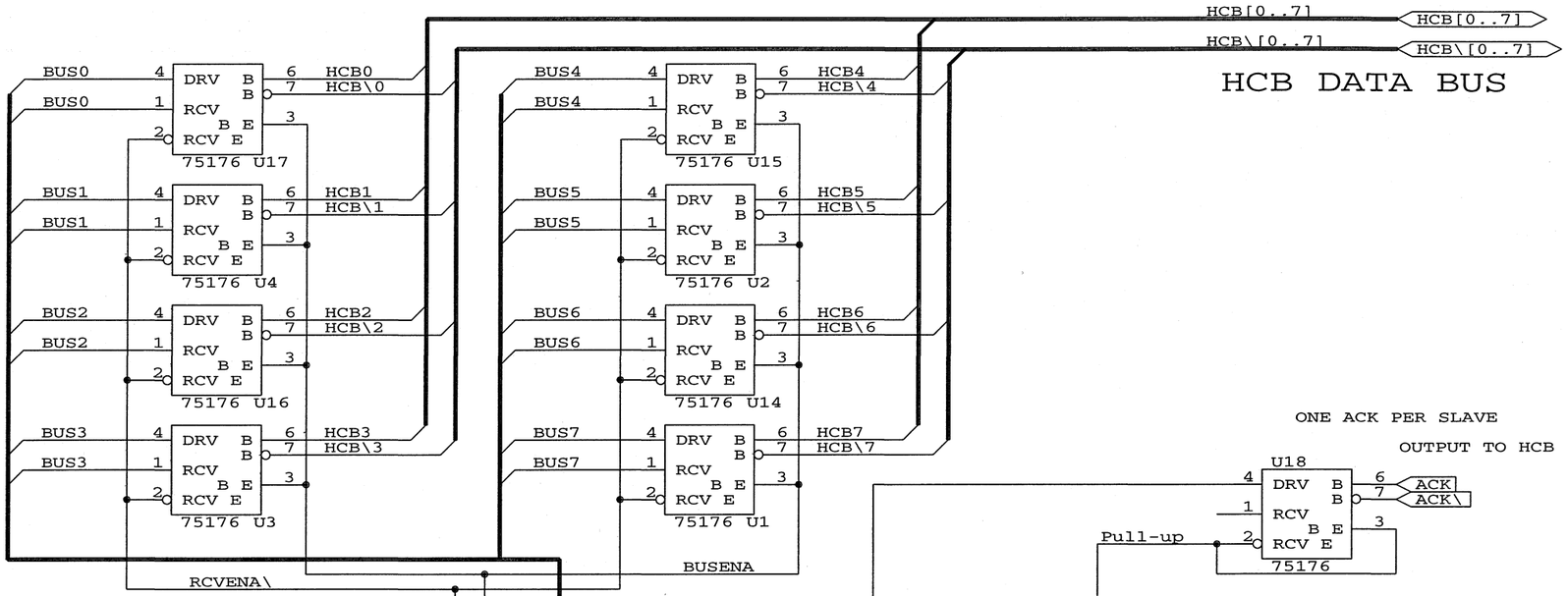
OEA\: ENABLE DATA FROM 2950 PORT A TO LOCAL BUS

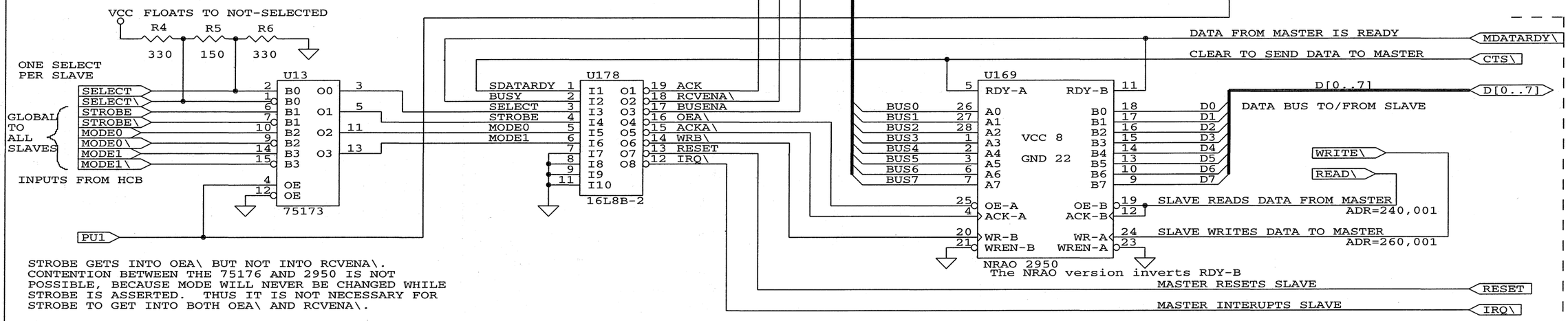
ACKA\: ACK PULSE TO 2950 FOR BOTH READ AND WRITE (PULSES LOW, TRAILING EDGE IS ACTIVE)

WRB\: WRITE PULSE TO 2950 FOR WRITES BY MASTER (PULSES LOW, TRAILING EDGE IS ACTIVE)

RESET: HIGH TRUE RESET PULSE

IRQ\: LOW TRUE INTR RQST PULSE TO SLAVE INDICATES NEXT BYTE IS FIRST BYTE OF A TRANSFER FROM MASTER TO SLAVE.





STROBE GETS INTO OEA\ BUT NOT INTO RCVENA\. CONTENTION BETWEEN THE 75176 AND 2950 IS NOT POSSIBLE, BECAUSE MODE WILL NEVER BE CHANGED WHILE STROBE IS ASSERTED. THUS IT IS NOT NECESSARY FOR STROBE TO GET INTO BOTH OEA\ AND RCVENA\.

IF STROBE WAS IN RCVENA\, THEN IT WOULD BE NECESSARY TO MAKE SURE THAT SUFFICIENT HOLD TIME EXISTS WHEN WRITING DATA FROM THE MASTER TO THE 2950.

A SLAVE CAN INITIATE AN ATTENTION REQUEST ONLY WHEN MODE = 0 AND THE TARGET IS NOT SELECTED. THUS WHEN ONE OR MORE SLAVES ARE SELECTED FOR WRITING, OR A SINGLE SLAVE IS SELECTED FOR READING, ALL NON-SELECTED SLAVES WILL HOLD ACK/IRQ HIGH.

A SLAVE MUST ABORT ANY PENDING COMMUNCIATION PROCESS CURRENTLY ACTIVE WHENEVER AN IRQ IS RECEIVED. IRQ INDICATES THAT THE NEXT BYTE RCVD IS FIRST BYTE.

STROBE\ GETS INTO ACKA\ DURING WRITES TO THE SLAVE TO INSURE THAT NO DATA FROM THE SLAVE IS LEFT PENDING IN THE 2950.

MINIMUM STROBE PULSE WIDTH IS 1.7 uS:
(8751 REQUIRES 24 CLOCK PERIODS FOR RESET = 1.5 uS AT 16MHz)
(68000 REQUIRES 10 CLOCK PERIODS FOR RESET = 800 nS AT 12.5 MHz)
(68681 REQUIRES 1 uS)

Each function code

SELECT	STROBE	MODE1	MODE0	FUNCTION	ACK	RCVENA\	BUSENA	OEA\	ACKA\	WRB\	RESET	IRQ\
0	X	0	0	ALLOW SLAVE TO ASSERT ATTENTION	SDATARDY\	1	0	1	1	1	0	1
0	X	0	1	IDLE	1	1	0	1	1	1	0	1
0	X	1	0	IDLE	1	1	0	1	1	1	0	1
0	X	1	1	IDLE	1	1	0	1	1	1	0	1
1	_/‾_	0	0	MASTER SENDS IRQ TO SLAVE	1	1	1	1	STROBE\	STROBE\	0	STROBE\
1	_/‾_	0	1	MASTER WRITES TO SLAVE	BUSY\	0	0	1	STROBE\	STROBE\	0	1
1	_/‾_	1	0	MASTER READS FROM SLAVE	SDATARDY\	1	STROBE	STROBE\	STROBE\	1	0	1
1	_/‾_	1	1	MASTER RESETS SLAVE (HARD RESET)	1	1	0	1	STROBE\	1	STROBE	1

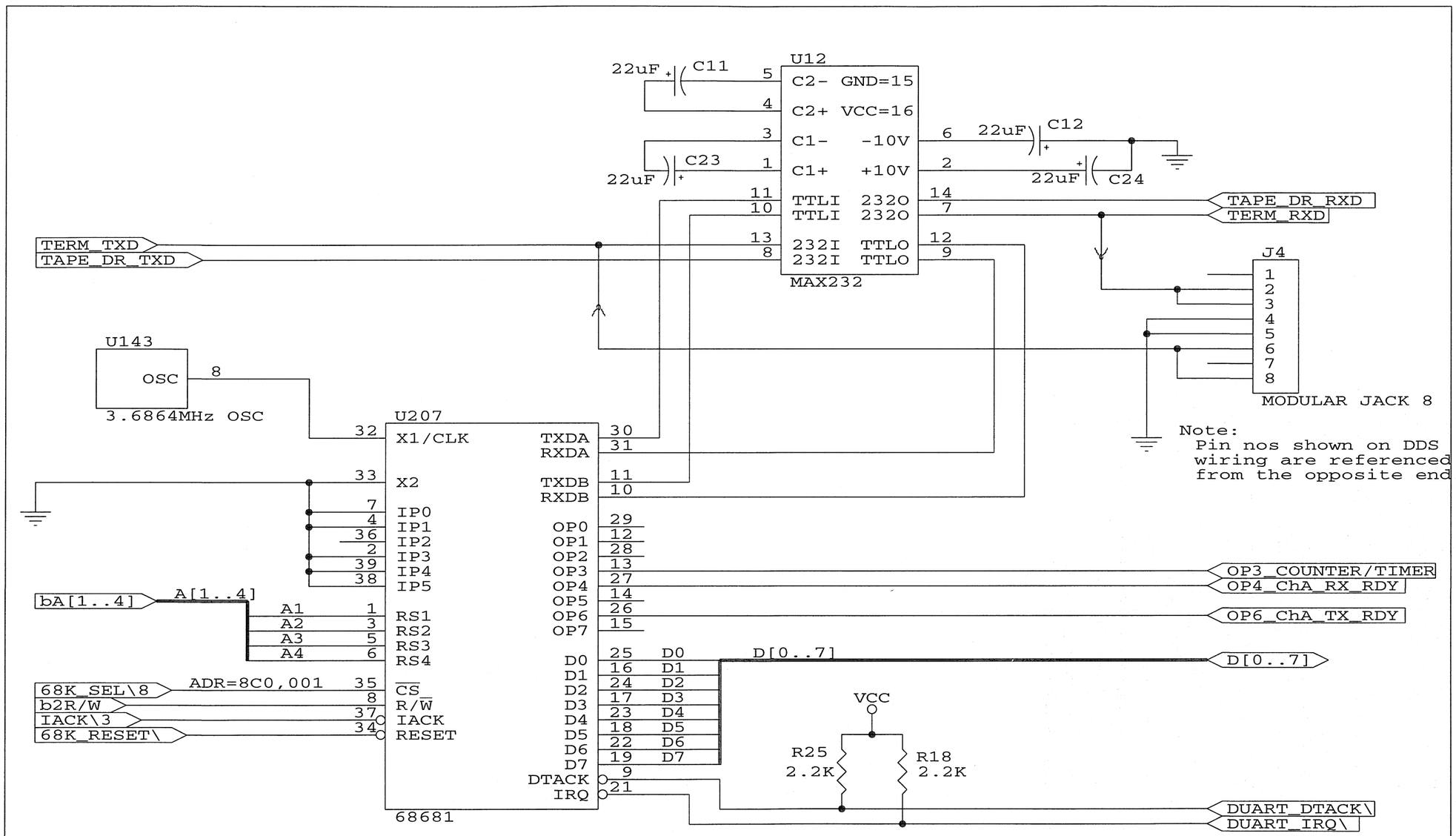
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: HARDWARE CONTROL BUS (HCB) SLAVE INTERFACE

Size	Document Number	REV
B	56000L008 (L008D29.SCH)	

Date: November 19, 1996 Sheet 29 of 31



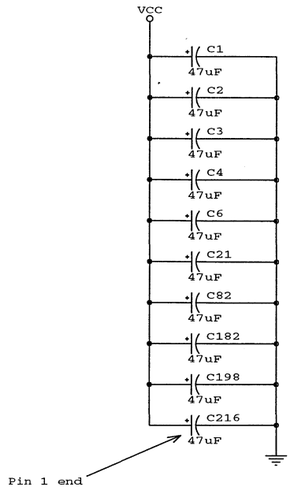
Note:
Pin nos shown on DDS wiring are referenced from the opposite end.

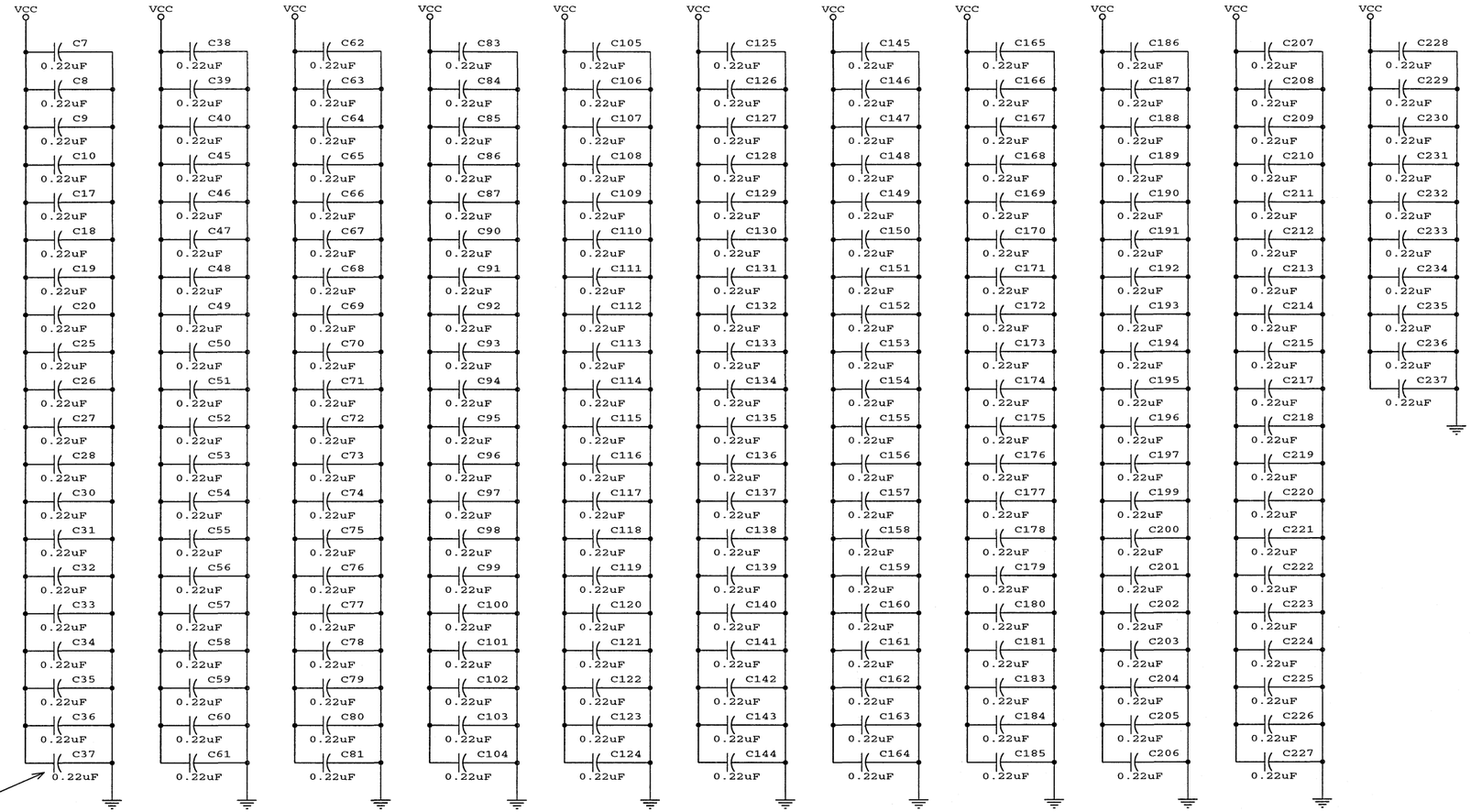
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

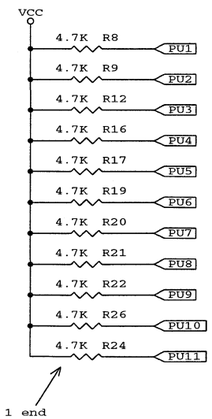
Title		
68K DUART		
Size	Document Number	REV
A	56000L008 (L008D30.SCH)	
Date: November 19, 1996	Sheet 30 of 31	

VCC decoupling

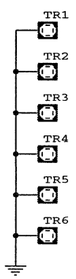




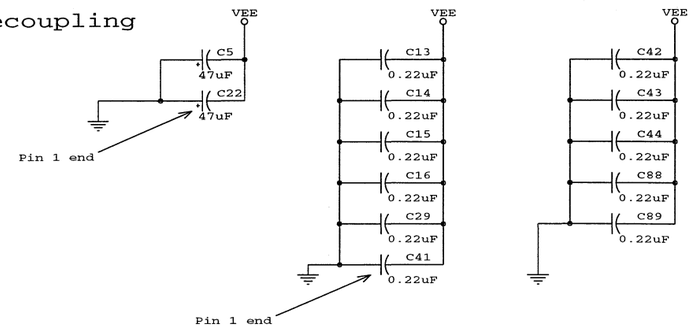
General pull-up ressitors



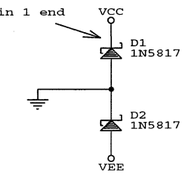
Ground Turrets



VEE decoupling



Protection against transients upon card insertion.



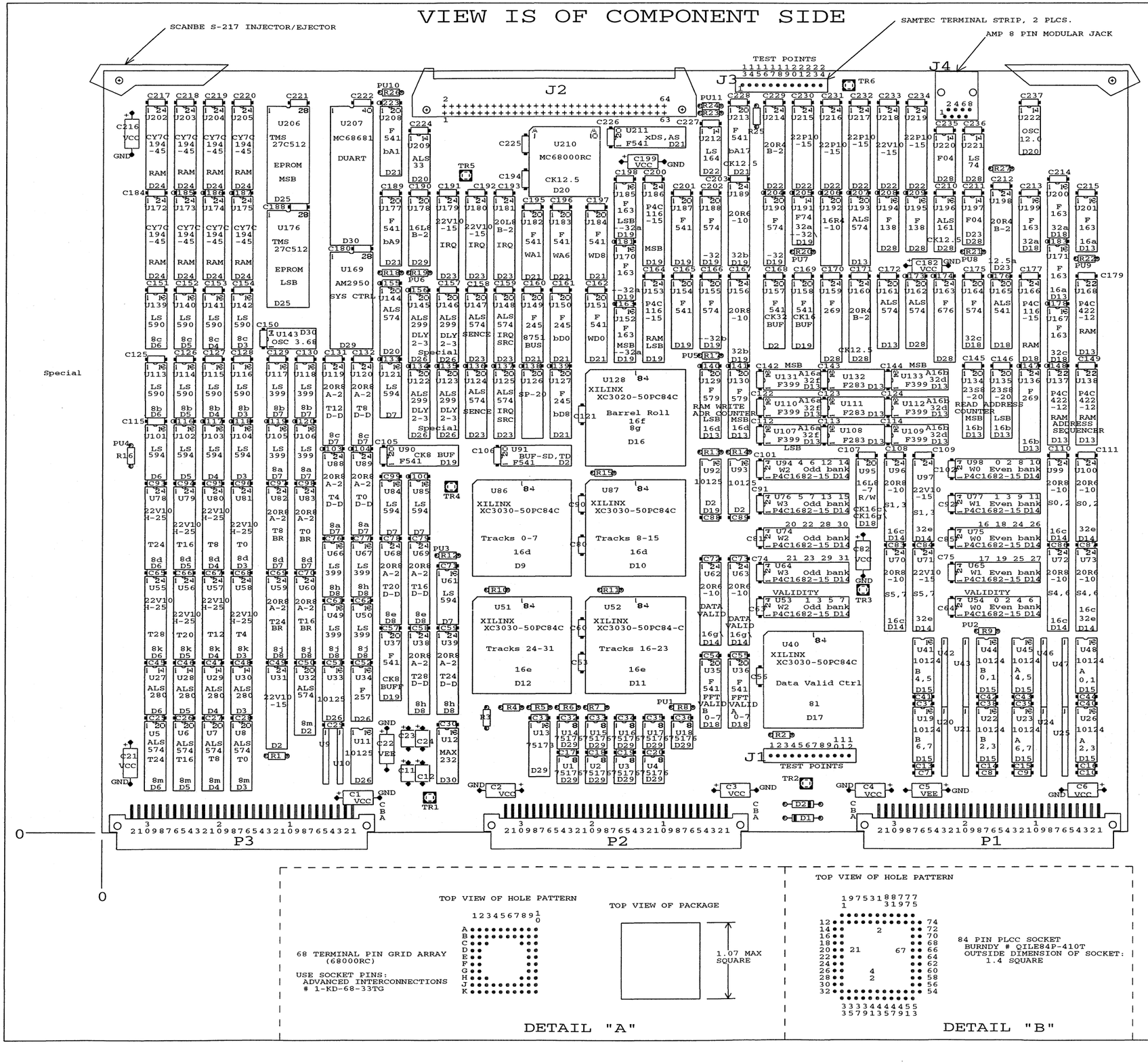
20 V MAX REV
15 AMP SURGE
1 AMP AVE

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER
DECOUPLING AND PULL-UPS

Size	Document Number	REV
C	56000L008 (L008D31.SCH)	
Date: November 19, 1996	Sheet 31 of 31	

VIEW IS OF COMPONENT SIDE



Notes:

1. 9U X 280 mm EUROCARD
2. SEE NRAO DRAWING # 56000M003 FOR MECHANICAL DETAILS OF CARD.
3. THIS SKETCH DETAILS THE APPROXIMATE LOCATIONS OF ALL COMPONENTS.
4. ALL COMPONENTS WILL BE ON 0.1 GRID UNLESS OTHERWISE NOTED.
5. PIN ORIENTATIONS:
   - "HORIZONTAL" DIPS - LOWER LEFT CORNER.
   - "VERTICAL" DIPS - UPPER LEFT CORNER.
   - PIN GRID ARRAY (1 PLACE) - SEE DETAIL "A".
   - PLCC (6 PLACES) - SEE DETAIL "B".
   - ALL CONNECTORS - AS SHOWN.
   - DESCRETE RESISTORS:

     PIN 1 ON RIGHT SIDE

     PIN 1 AT TOP
   - DESCRETE CERAMIC CAPACITORS

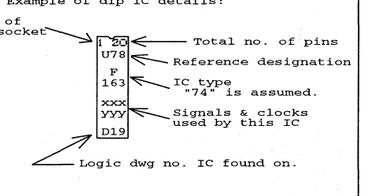
     PIN 1 ON RIGHT SIDE

     PIN 1 AT TOP
   - POLORIZED (TATALUM) CAPACITORS - THE + SIGN ON THIS SKETCH INDICATES PIN 1 END OF CAPACITOR.
6. THIS SYMBOL REPRESENTS A MOUNTING PAD FOR KEYSTONE TURRET #1593-3, 6 TOTAL EACH CONNECTED TO GROUND.

   These turrets are included in the netlist as TR1 1 thru TR6 1.
7. ALL DIP IC's SOCKETED: TI C93xx FAMILY.
8. There is one spare IC hole pattern. The pattern has VCC and GND connected as follows:

Location	pins	VCC	GND
U126	20	20	10

9. Example of dip IC details:



10. See BILL OF MATERIALS DWG A56000B004, REV C Text file B004T01C.PRT

TOP VIEW OF HOLE PATTERN

68 TERMINAL PIN GRID ARRAY (68000RC)

USE SOCKET PINS: ADVANCED INTERCONNECTIONS # 1-KD-68-33TG

TOP VIEW OF PACKAGE

DETAIL "A"

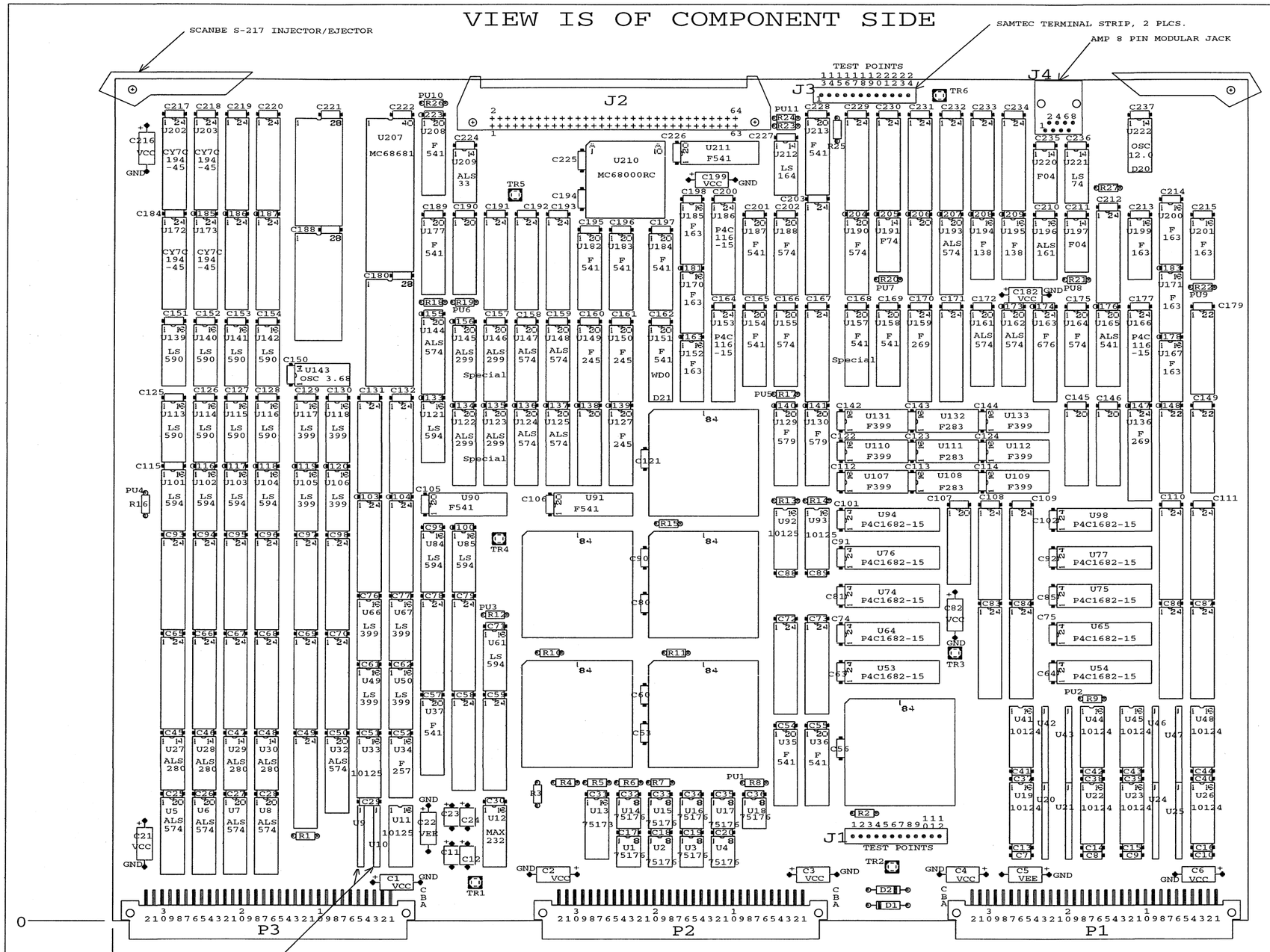
TOP VIEW OF HOLE PATTERN

84 PIN PLCC SOCKET
BURNDY # QILE84P-410T
OUTSIDE DIMENSION OF SOCKET: 1.4 SQUARE

DETAIL "B"

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER LAYOUT, 9U x 280 mm CARD		
Size: C	Document Number: 56000Z009 (Z009D01.LAY)	REV: C
Date: January 11, 1995	Sheet 1 of 2	

VIEW IS OF COMPONENT SIDE

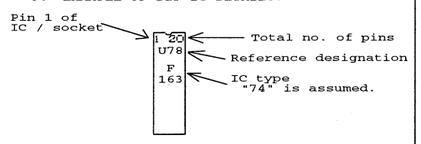


Notes:

1. 9U X 280 mm EUROCARD
2. SEE NRAO DRAWING # 56000M003 FOR MECHANICAL DETAILS OF CARD.
3. THIS SKETCH DETAILS THE APPROXIMATE LOCATIONS OF ALL COMPONENTS.
4. ALL COMPONENTS WILL BE ON 0.1 GRID UNLESS OTHERWISE NOTED.
5. PIN ORIENTATIONS:
   - "HORIZONTAL" DIPS - LOWER LEFT CORNER.
   - "VERTICAL" DIPS - UPPER LEFT CORNER.
   - PIN GRID ARRAY (1 PLACE) - SEE DETAIL "A".
   - PLCC (6 PLACES) - SEE DETAIL "B".
   - ALL CONNECTORS - AS SHOWN.
   - DESCRETE RESISTORS:
     PIN 1 ON RIGHT SIDE
     PIN 1 AT TOP
   - DESCRETE CERAMIC CAPACITORS
     PIN 1 ON RIGHT SIDE
     PIN 1 AT TOP
   - POLORIZED (TATALUM) CAPACITORS - THE + SIGN ON THIS SKETCH INDICATES PIN 1 END OF CAPACITOR.
6. THIS SYMBOL REPRESENTS A MOUNTING PAD FOR KEYSTONE TURRET #1593-3. 6 TOTAL EACH CONNECTED TO GROUND.
   These turrets are included in the netlist as TR1 1 thru TR6 1.
7. ALL DIP IC's SOCKETED: TI C93xxx FAMILY & ROBINSON NUGENT ICB-223-S8TG, 3 PLCS.
8. There is one spare IC hole pattern. The pattern has VCC and GND connected as follows:

Location	pins	VCC	GND
U126	20	20	10

9. EXAMPLE OF DIP IC DETAILS:

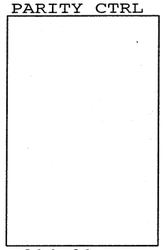


10. See BILL OF MATERIALS DWG A56000B004, REV C Text file B004T01C.PRT
11. LOCATIONS WITHOUT A REFERENCE & IC TYPE: ASSEMBLER SHALL INSTALL SOCKET ONLY. NRAO WILL INSERT IC.
12. BOARD ASSEMBLER DOES NOT NEED SHEET ONE OF THIS DRAWING.

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER CARD ASSEMBLY DETAILS		
Size: C	Document Number: 56000Z009 (Z009D02.LAY)	REV: C
Date: October 20, 1992	Sheet 2 of 2	

1 SHEET
B SIZE

PARITY CTRL



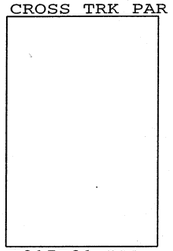
K014D01.PAL

U31
D009T01.ABL

L008D02.SCH

2 SHEETS
A SIZE

CROSS TRK PAR



K015D01.PAL

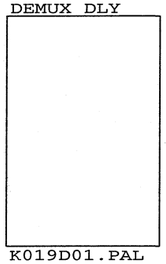
U78 U79 U80 U81
D009T02.ABL

U55 U56 U57 U58
D009T03.ABL

L008D03 - D06.SCH

2 SHEETS
B SIZE

DEMUX DLY



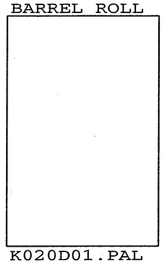
K019D01.PAL

U38 U39 U68 U69
U88 U89 U119 U120
D009T06.ABL

L008D07 - D08.SCH

1 SHEET
A SIZE

BARREL ROLL



K020D01.PAL

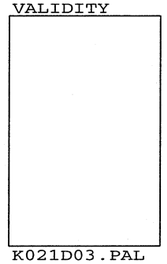
U60 U83
D009T04.ABL

U59 U82
D009T05.ABL

L008D07 - D08.SCH

1 SHEET
A SIZE

VALIDITY



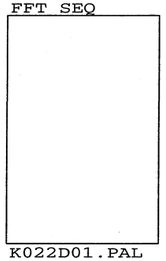
K021D03.PAL

U62 U63
D009T14.ABL

L008D14.SCH

2 SHEETS
A SIZE

FFT SEQ



K022D01.PAL

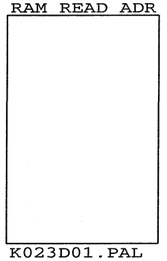
U156
D009T15.ABL

U189
D009T16.ABL

L008D19.SCH

2 SHEETS
B & A SIZE

RAM READ ADR



K023D01.PAL

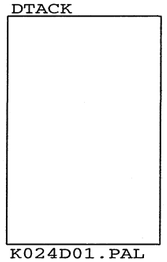
U135
D009T07.ABL

U134
D009T08.ABL

L008D13.SCH

1 SHEET
A SIZE

DTACK



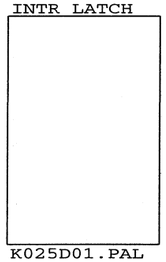
K024D01.PAL

U214
D009T17.ABL

L008D22.SCH

1 SHEET
B SIZE

INTR LATCH



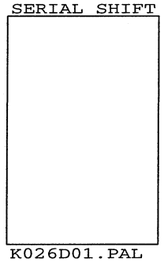
K025D01.PAL

U180
D009T24.ABL

L008D23.SCH

1 SHEET
B SIZE

SERIAL SHIFT



K026D01.PAL

U160
D009T26.ABL

L008D28.SCH

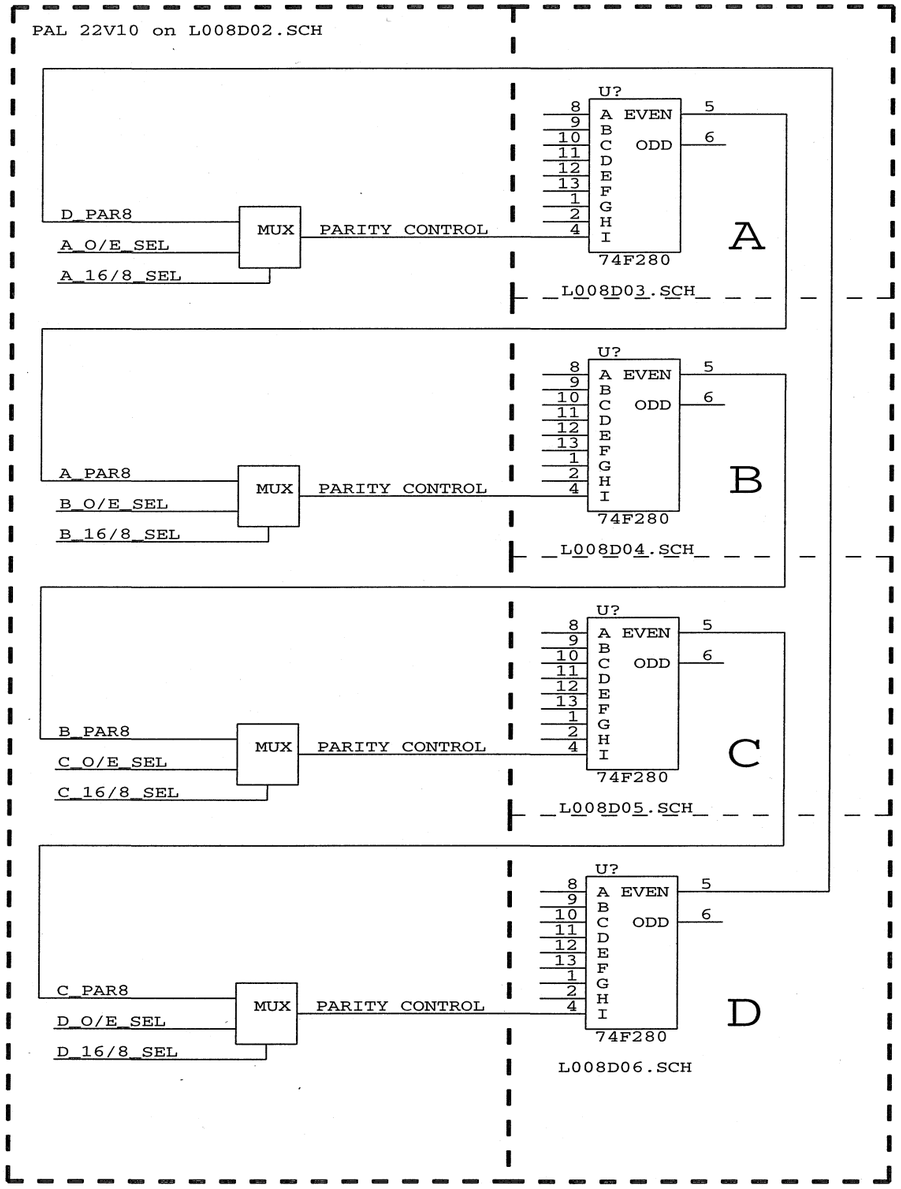
REPRESENTATIVE LOGIC	ABEL SOURCE	U #	SCHEMATIC SHEET #	FUNCTION
K014D01.PAL	D009T01.ABL	U31	L008D02.SCH	PARITY CTRL
K015D01.PAL	D009T02.ABL	U78,U79,U80,U81	L008D03 - D06.SCH	CROSS TRK PAR
K015D02.PAL	D009T03.ABL	U55,U56,U57,U58	L008D03 - D06.SCH	CROSS TRK PAR
K020D01.PAL	D009T04.ABL	U60,U83	L008D07 - D08.SCH	BARREL ROLL
K020D01.PAL	D009T05.ABL	U59,U82	L008D07 - D08.SCH	BARREL ROLL
K019D01.PAL	D009T06.ABL	U38,U39,U68,U69 U88,U89,U119,U120	L008D07 - D08.SCH L008D07 - D08.SCH	DEMUX DELAY
K023D01.PAL	D009T07.ABL	U135	L008D13.SCH	RAM READ ADR
K023D02.PAL	D009T08.ABL	U134	L008D13.SCH	RAM READ ADR
	D009T09.ABL	U70,U72,U96,U99	L008D14.SCH	TEST PAT SEL
	D009T10.ABL	U100	L008D14.SCH	OUTPUT
	D009T11.ABL	U73	L008D14.SCH	OUTPUT
	D009T12.ABL	U97	L008D14.SCH	OUTPUT
	D009T13.ABL	U71	L008D14.SCH	OUTPUT
K021D03.PAL	D009T14.ABL	U62,U63	L008D14.SCH	VALIDITY
K022D01.PAL	D009T15.ABL	U156	L008D19.SCH	FFT SEQ
K022D02.PAL	D009T16.ABL	U189	L008D19.SCH	FFT SEQ
K024D01.PAL	D009T17.ABL	U214	L008D22.SCH	DTACK
	D009T18.ABL	U215	L008D22.SCH	SEL 0-6
	D009T19.ABL	U216	L008D22.SCH	SEL 7-16
	D009T20.ABL	U217	L008D22.SCH	SEL 17-26
	D009T21.ABL	U218	L008D22.SCH	SEL 27-36
	D009T22.ABL	U219	L008D22.SCH	R/W
	D009T23.ABL	U179	L008D23.SCH	IACK
K025D01.PAL	D009T24.ABL	U180	L008D23.SCH	INTR LATCH
	D009T25.ABL	U181	L008D23.SCH	IPL
K026D01.PAL	D009T26.ABL	U160	L008D28.SCH	68K SERIAL
	D009T27.ABL	U95	L008D18.SCH	R/W
	D009T28.ABL	U192	L008D19.SCH	68K CLK
	D009T29.ABL	U198	L008D23.SCH	IRQ7
	D009T30.ABL	U178	L008D29.SCH	HCB

TOP LEVEL FOR ENTRY
INTO REPRESENTATIVE LOGIC
DRAWINGS FOR ALL DEF PALS

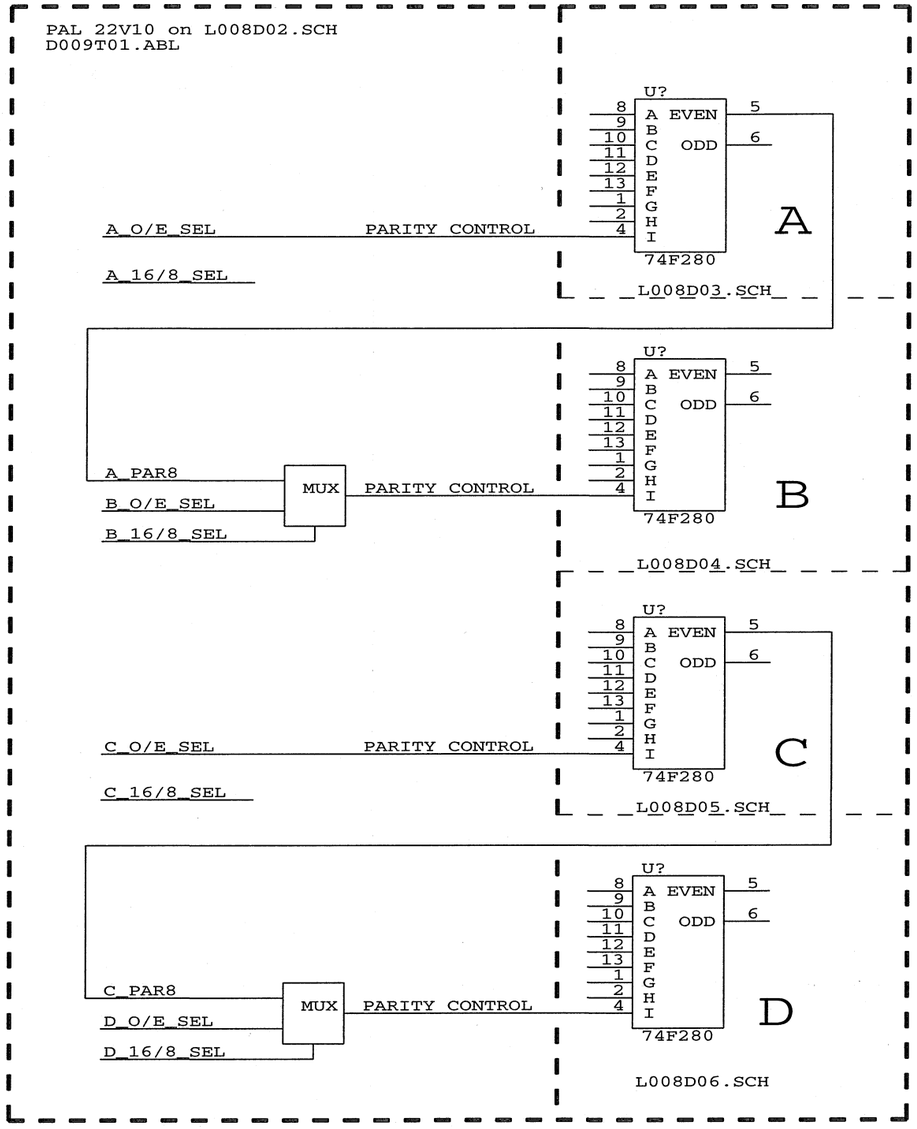
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NM

Size	Document Number	REV
B	DEFTOP.PAL	
Date: April 4, 1997	Sheet 1 of 1	

HARDWARE FUNCTIONALITY OF PARITY

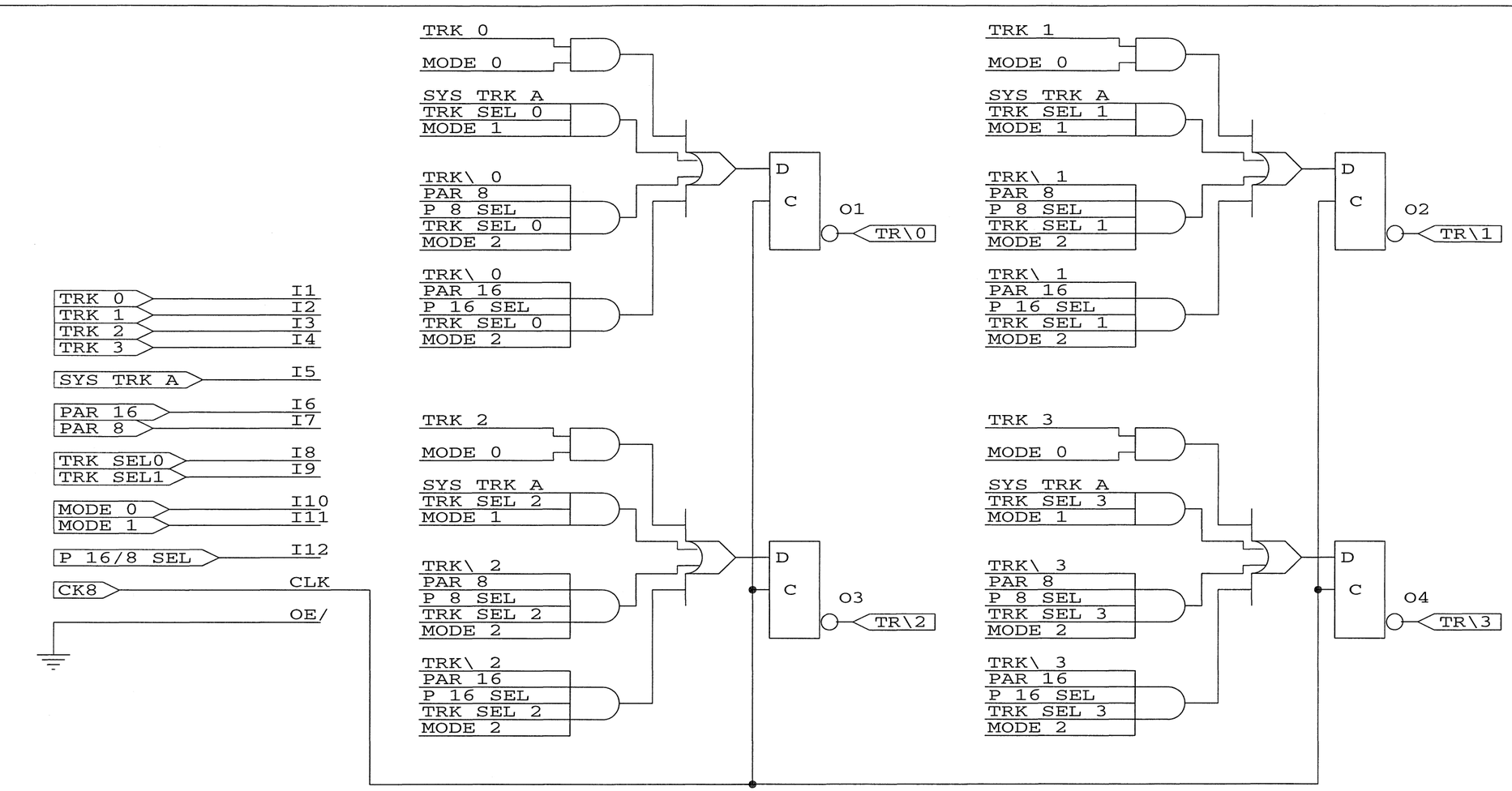


PAL IMPLEMENTATION



U31
D009T01.ABL
L008D02.SCH

VLBA CORRELATOR PROJECTVLBA CORRELATOR PROJE		
NATIONAL RADIO ASTRONOMY OBSERVATORYNATIONAL CHARLOTTESVILLE, VACHARLOTTESVILLE, VA		
Title: PARITY CONTROL PAL		
Size: B	Document Number: 56000K014 (K014D01.PAL)	REV:
Date: April 4, 1997	Sheet 1 of 1	



TRK SELn:
Selects 1 of 4 tracks.

MODE:
0- Pass all tracks.
1- Substitute SYS TRK for the selected track.
2- Invert selected track's data whenever bad parity is detected.

PAL2

K015D02.PAL

All terms not shown, see equations!

U78, U79, U80, U81

D009T02.ABL

L008D03 - D06.SCH

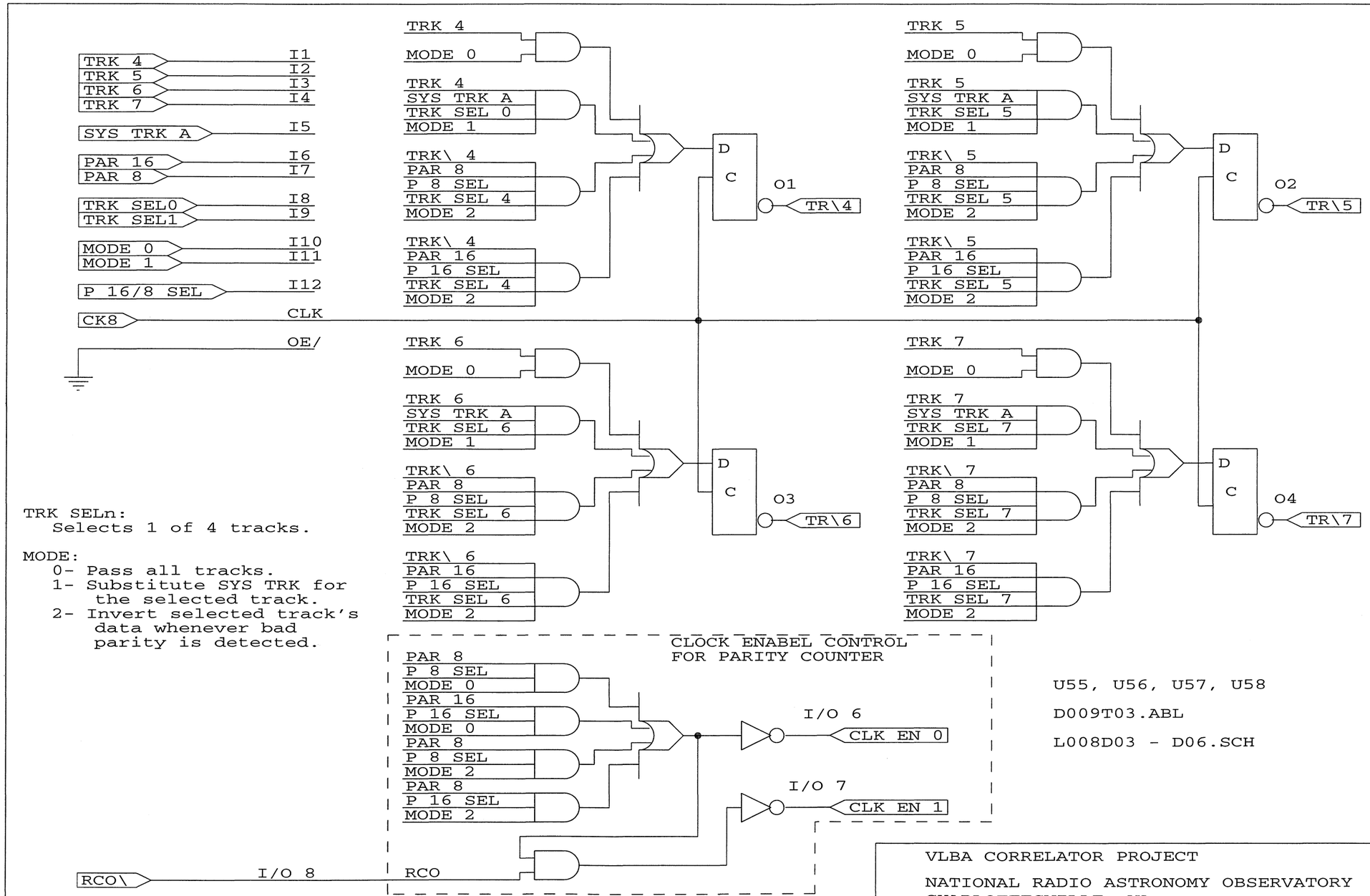
VLBA CORRELATOR PROJECT

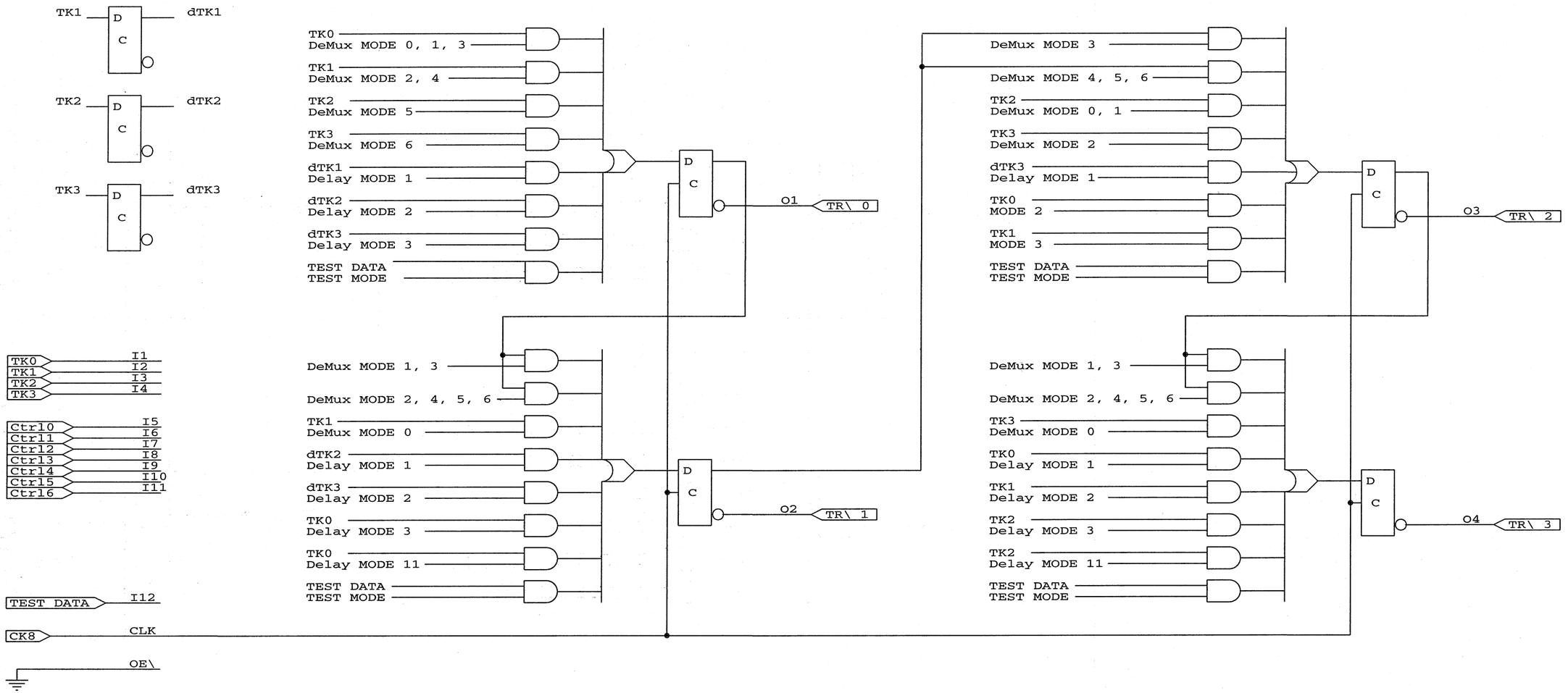
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
CROSS TRACK PARITY ACTION PAL 1

Size	Document Number	REV
A	56000K015 (K015D01.PAL)	

Date: April 4, 1997 Sheet 1 of 2


TRK 4
TRK 5
TRK 6
TRK 7
SYS TRK A
PAR 16
PAR 8
TRK SEL0
TRK SEL1
MODE 0
MODE 1
P 16/8 SEL
CK8
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I12
CLK
OE/
TRK 4
MODE 0
TRK 4
SYS TRK A
TRK SEL 0
MODE 1
TRK\ 4
PAR 8
P 8 SEL
TRK SEL 4
MODE 2
TRK\ 4
PAR 16
P 16 SEL
TRK SEL 4
MODE 2
D
C
O1
TR\4
TRK 5
MODE 0
TRK 5
SYS TRK A
TRK SEL 5
MODE 1
TRK\ 5
PAR 8
P 8 SEL
TRK SEL 5
MODE 2
TRK\ 5
PAR 16
P 16 SEL
TRK SEL 5
MODE 2
D
C
O2
TR\5
TRK 6
MODE 0
TRK 6
SYS TRK A
TRK SEL 6
MODE 1
TRK\ 6
PAR 8
P 8 SEL
TRK SEL 6
MODE 2
TRK\ 6
PAR 16
P 16 SEL
TRK SEL 6
MODE 2
D
C
O3
TR\6
TRK 7
MODE 0
TRK 7
SYS TRK A
TRK SEL 7
MODE 1
TRK\ 7
PAR 8
P 8 SEL
TRK SEL 7
MODE 2
TRK\ 7
PAR 16
P 16 SEL
TRK SEL 7
MODE 2
D
C
O4
TR\7
TRK SELn:
Selects 1 of 4 tracks.
MODE:
0- Pass all tracks.
1- Substitute SYS TRK for the selected track.
2- Invert selected track's data whenever bad parity is detected.
CLOCK ENABEL CONTROL FOR PARITY COUNTER
PAR 8
P 8 SEL
MODE 0
PAR 16
P 16 SEL
MODE 0
PAR 8
P 8 SEL
MODE 2
PAR 8
P 16 SEL
MODE 2
I/O 6
CLK EN 0
I/O 7
CLK EN 1
RCO\
I/O 8
RCO
U55, U56, U57, U58
D009T03.ABL
L008D03 - D06.SCH
All terms not shown, see equations!
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
CROSS TRACK PARITY ACTION PAL 2
Size
A
Document Number
56000K015 (K015D02.PAL)
REV
Date: April 4, 1997
Sheet 2 of 2



Ctrl decode table A

Ctrl6	Ctrl[5..0]	DeMux MODE	DEMUX FUNCTION
0	h00	0	4 Tracks in 4 out, pass thru
0	h01	1	Tracks 0 & 2 in, 4 out. 2 bitstreams on 1 track.
0	h36	2	Tracks 1 & 3 in, 4 out. 2 bitstreams on 1 track.
0	h03	3	Track 0 in, 4 out. 4 bitstreams on 1 track.
0	h37	4	Track 1 in, 4 out. 4 bitstreams on 1 track.
0	h35	5	Track 2 in, 4 out. 4 bitstreams on 1 track.
0	h3F	6	Track 3 in, 4 out. 4 bitstreams on 1 track.

Ctrl decode table B

Ctrl6	Ctrl[4..0]	Delay MODE	TEST-DELAY FUNCTION
1	0	0	Output test data on the 4 outputs.
1	3	3	1 bit delay. 1 bitstream on 4 tracks.
1	2	2	2 bit delay. 1 bitstream on 4 tracks.
1	1	1	3 bit delay. 1 bitstream on 4 tracks.
1	h11	11	1 bit delay. 1 bitstream on 2 tracks.

See sheet 2 for more info on delay.

Notes:
1 In Demux mode; eg 4 bitstreams to 1 track, TR0 input is routed to TR\3 output.

U38,U39,U68,U69 D009T06.ABL

U88,U89,U119,U120 L008D07 - D08.SCH

K019D02.PAL

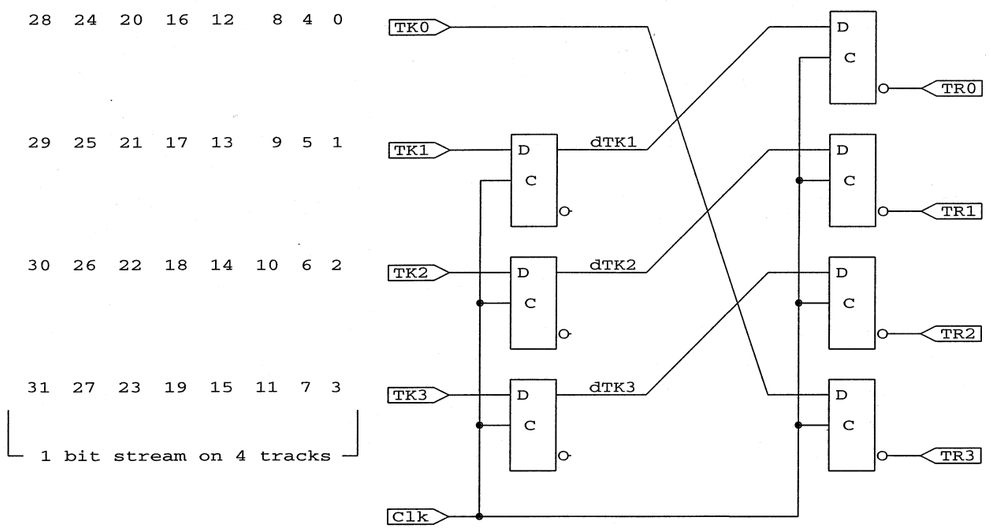
K019D02.PAL
Delay Functions

VLBA CORRELATOR PROJECT

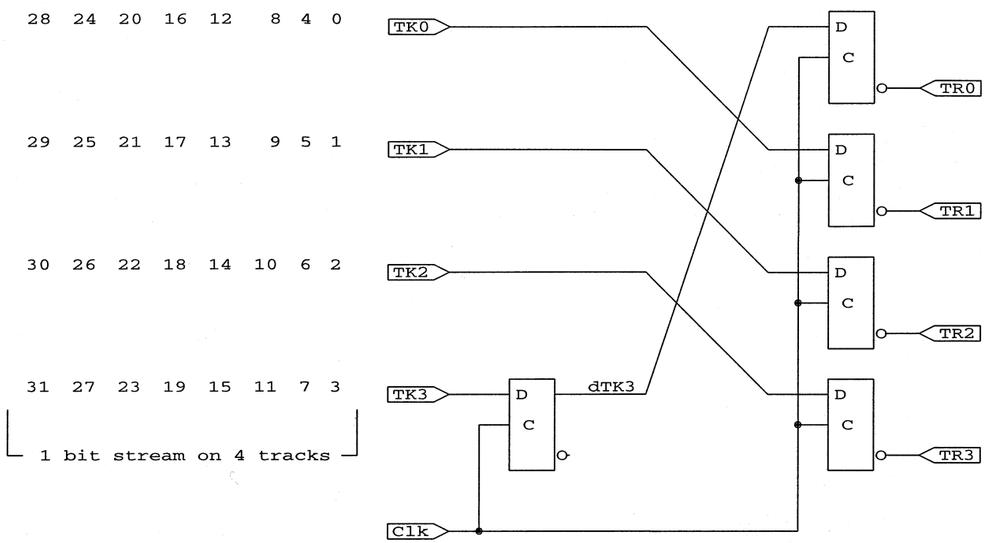
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
TRACK DEMUX-DELAY PAL

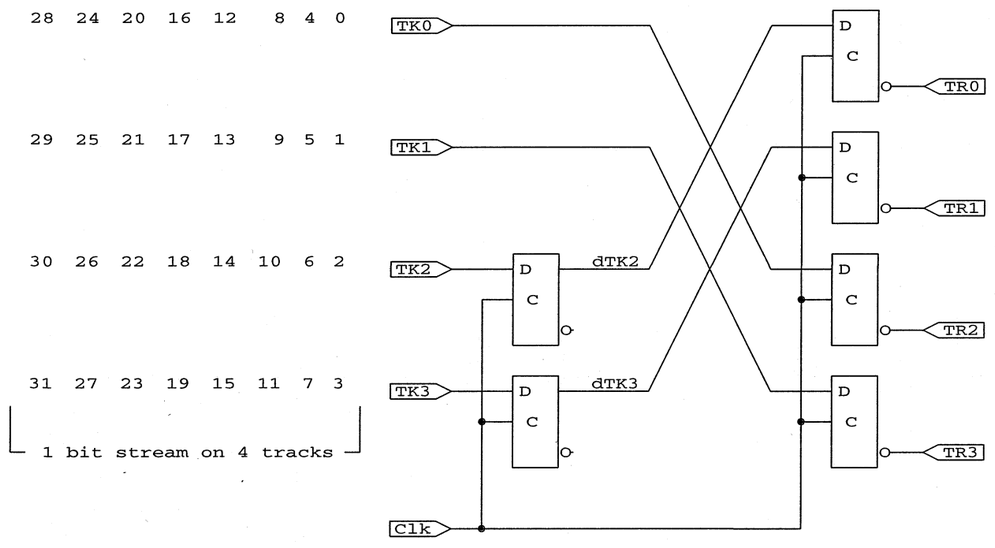
Size	Document Number	REV
B	56000K019 (K019D01.PAL)	
Date: April 4, 1997	Sheet 1 of 2	



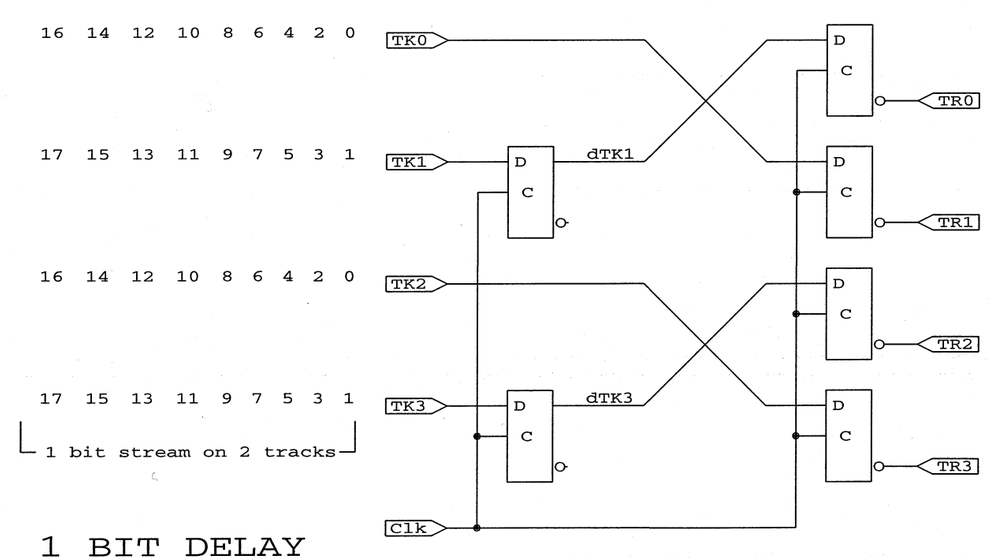
3 BIT DELAY



1 BIT DELAY



2 BIT DELAY



1 BIT DELAY

The Track Recovery Card cannot provide single bit delay
when 1 bit stream is recorded on more then one track.

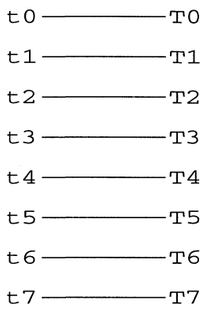
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title		
TRACK DEMUX-DELAY PAL		
Size	Document Number	REV
B	56000K019 (K019D02.PAL)	
Date: February 3, 1992	Sheet 2 of 2	

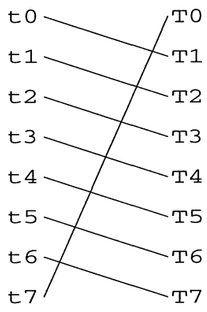
3 bit address to Roll PALs on the DEF card.

Input sel = 0



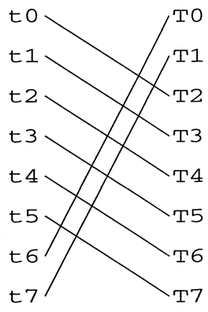
Formatter Roll of 0
DEF Roll of 0

Input sel = 1



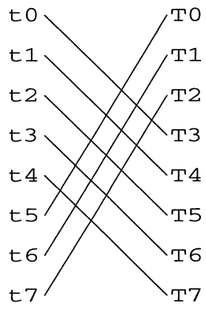
Formatter Roll of 7
DEF Roll of 1

Input sel = 2



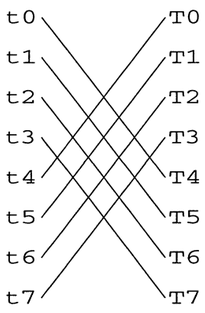
Formatter Roll of 6
DEF Roll of 2

Input sel = 3



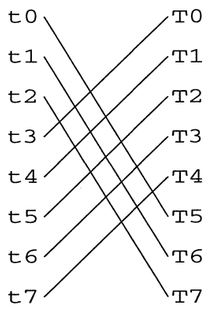
Formatter Roll of 5
DEF Roll of 3

Input sel = 4



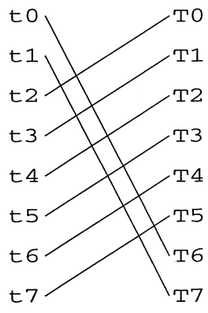
Formatter Roll of 4
DEF Roll of 4

Input sel = 5



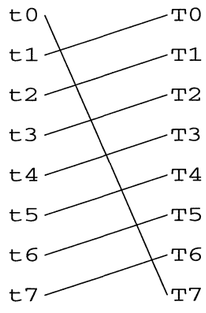
Formatter Roll of 3
DEF Roll of 5

Input sel = 6



Formatter Roll of 2
DEF Roll of 6

Input sel = 7



Formatter Roll of 1
DEF Roll of 7

Notes:
1. tx= inputs to roll PAL.
2. Tx= outputs of from PAL.

U60, U83 D009T04.ABL

U59, U82 D009T05.ABL

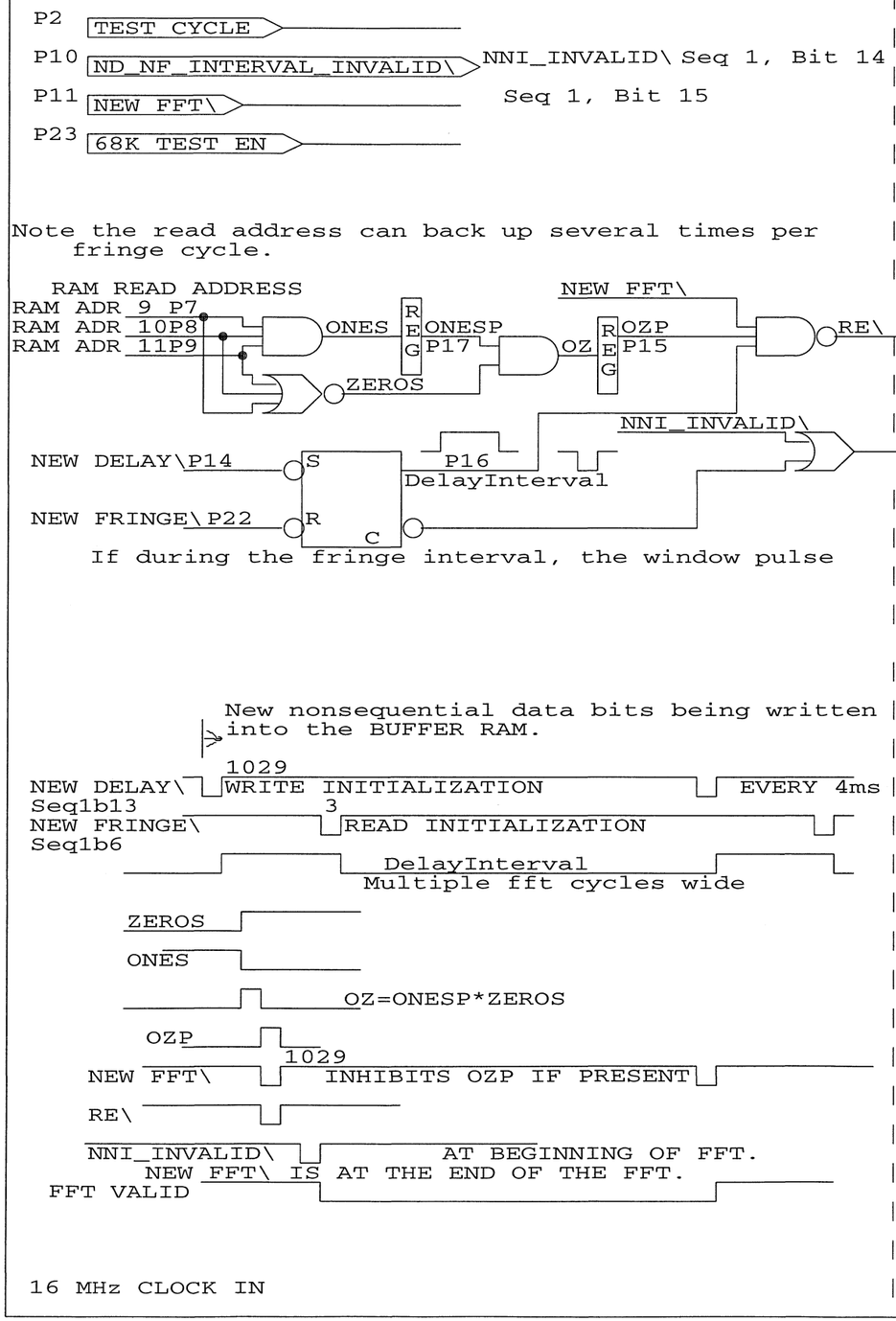
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: BARREL ROLL PAL

Size	Document Number	REV
A	56000K020 (K020D01.PAL)	

Date: April 4, 1997 Sheet 1 of 1



FUNCTIONS:

1. DATA VALID\ BIT from RAM controls validity.
2. When the read address transitions to 0 in the interval between write and read initialization, declare invalid. The read address should only transition to zero before write initialization or at read initialization.
3. If output goes invalid (0) then hold invalid until:
   a. NEW FFT
   b. 68K TEST EN
4. Force FFT VALID true during:
   a. During FFT TEST CYCLE.
   b. Upon cammand from 68K.
   c. During NEW FFT.
5. For modes with overlap of 32 or 64, the input ND_NF_INTERVAL_INVALID\ gives a negative pulse. When this occurs in the interval from NEW DELAY to NEW FRINGE, latch the output invalid.

20V8
SEE L008D14.SCH
U62 AND U63
U62.JED
SEE D009T14.ABL

K021D03: THE 03 IS AN ARTIFACT SINCE THERE IS ONLY ONE SHEET.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER FFT VALID PAL	
Size	Document Number	REV
A	56000K21 M:\DEF\DEFPALS\K021D03.PAL	
Date: April 4, 1997	Sheet 1 of 1	

0 when delay does not change. Used for low BW mode. Also used to inhibit counter clear when sequencer 3 is being loaded by the uP.

68K_CTRL2 P10
RA_FRINGE P2 Select place in fft cycle.

Select fft cycle
NEW_FRINGE_EN\ P7

A
1
2

DV _FRINGE P3 Select place in fft cycle.

D
C

P20 G_RA_NEW_FRINGE\

To Seq3 counter clear.

D
C

P21 DV_NEW_FRINGE\

New Fringe duration

FFT duration
Seq1 cycle

NEW_FRINGE_EN\
c131msTic(combinatorial input)
SYNC_TIC P4
c131msTic
TestCycleEn
TestCycle\

4.128ms

68k rcvs fnct to enable TestCycle

68k disables TestCycle

PAL2
K022D02.PAL

P18
D19_SPARE1

CONTROLS SWITCHING TO SELF TEST PATTERN.
P19 ON SHT. 14

D
C

c131msDLYD

P7
NEW_FRINGE_EN\

SYNC_TIC P4

c131msTIC_EN P6

D
C

c131msTIC

P22 c131msTIC\

TO SHT. 20, THEN SHT. 23

TIMING NOT CRITICAL AT THE 32 MHz CLOCK LEVEL

L008D19.SCH

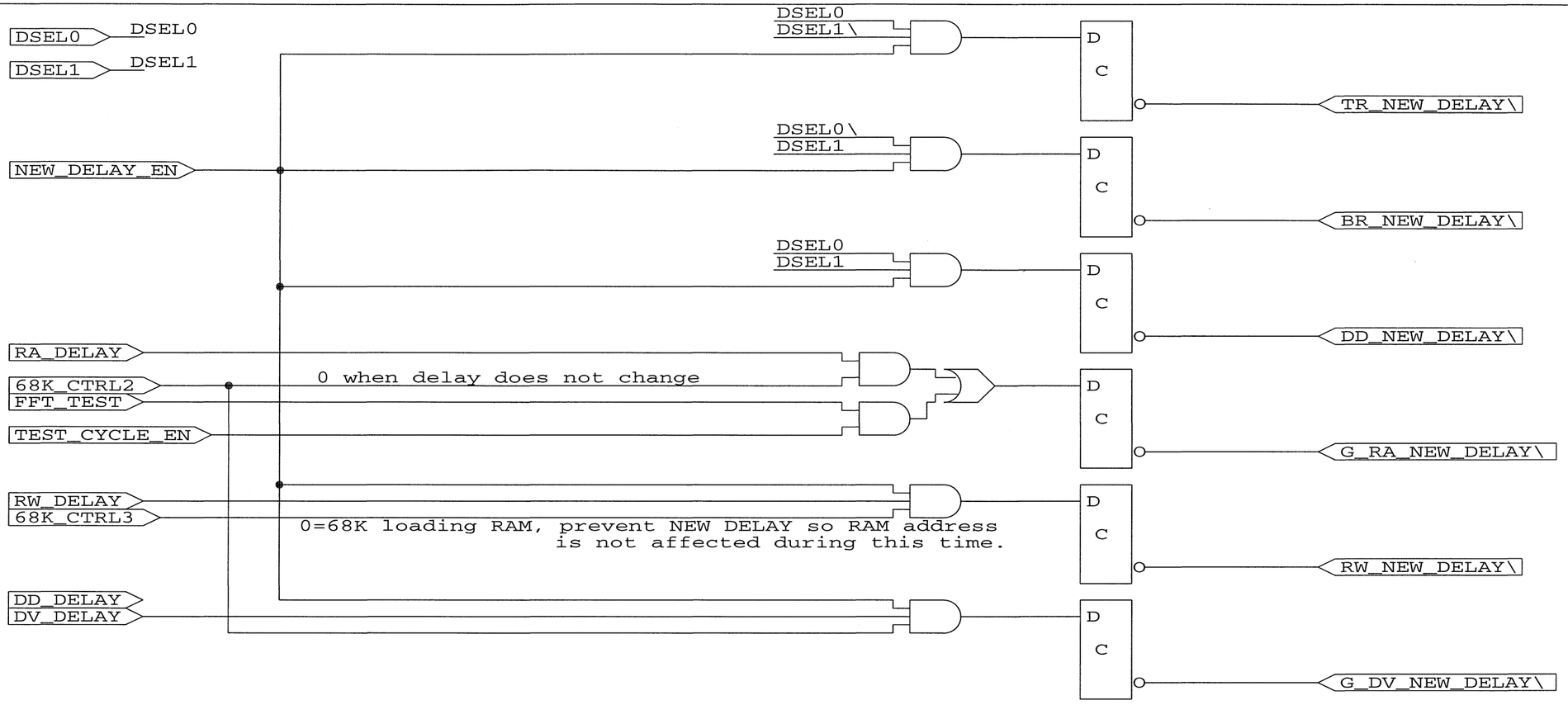
U156

D009T15.ABL

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER FFT SEQUENCER PAL 1	
Size A	Document Number 56000K022 (K022D01.PAL)	REV
Date: April 4, 1997	Sheet 1 of 2	



U189

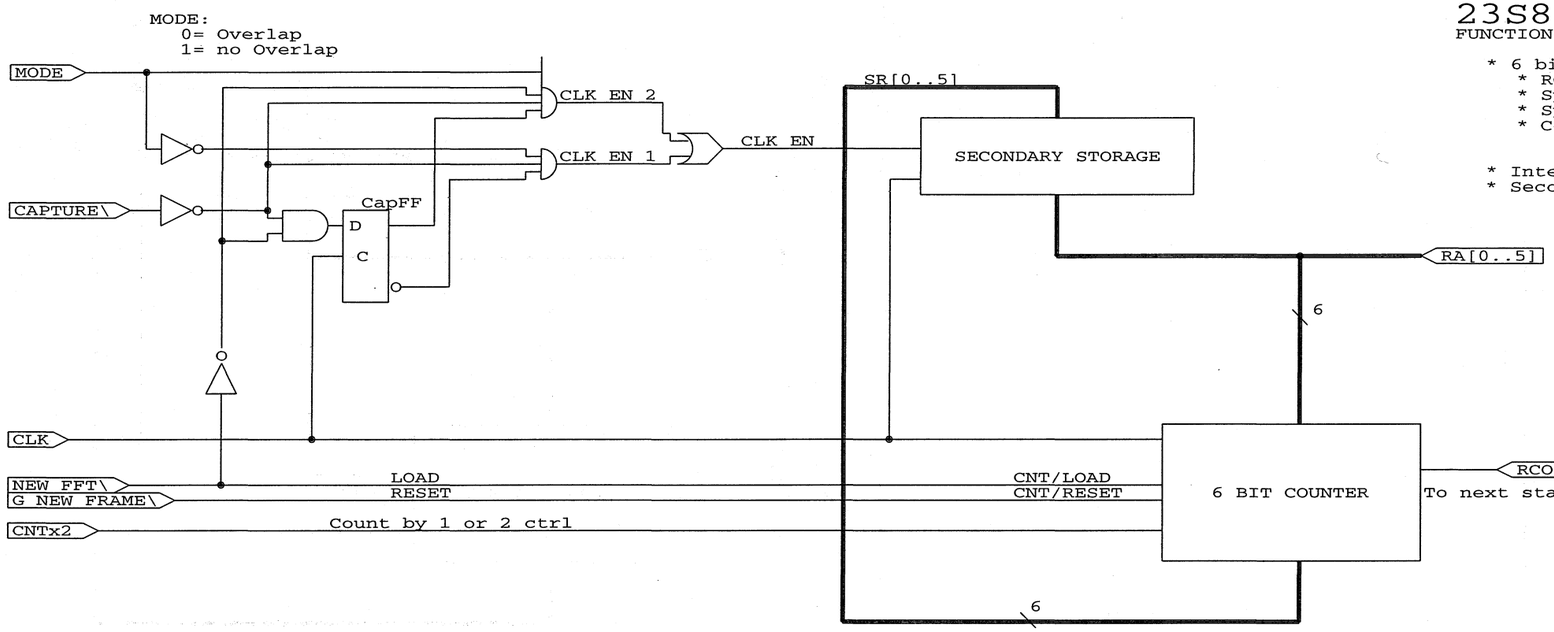
D009T16.ABL

L008D19.SCH

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

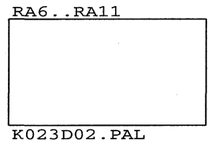
Title: DEFORMATTER FFT SEQUENCER PAL 2		
Size: A	Document Number: 56000K022 (K022D02.PAL)	REV:
Date: April 4, 1997	Sheet 2 of 2	



23S8 PAL

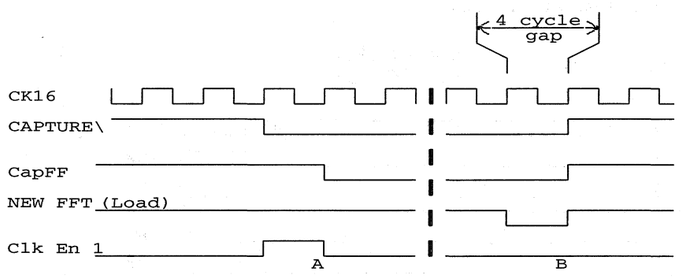
FUNCTIONS:

* 6 bit sync counter.
  * RCO to next stage.
  * Sync reset.
  * Sync load from internal storage register.
  * Count by 1 or 2
    When counting by 2:
    The state of the LSB is determined by LSBctrl
* Internal storage reg to caputure the current state of counter.
* Secondary storage clk enable logic.

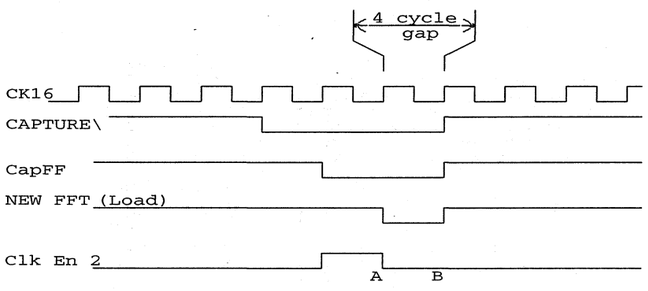


Note: remember each address state produces 2 bits to the FFT engines.

MODE=0
(overlapped FFTs)

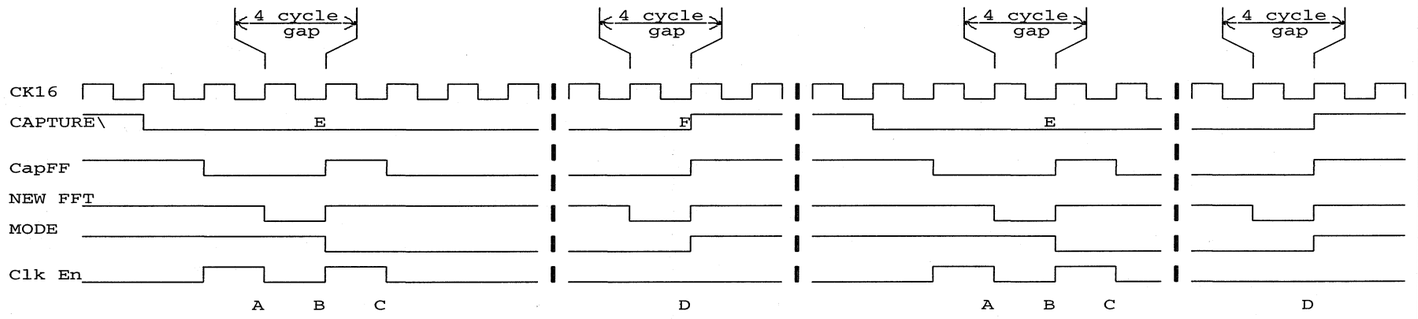


MODE=1
(non overlapped FFTs)



MODE = dynamic

(for oversampled FFTs, 1-4 512 pt shown)



Sequence:
- A -Strobe counter contents into secondary storage.
- B -Load counter from secondary storage.
- C -Strobe counter contents into secondary storage.
- D -Load counter from secondary storage.
- E -Capture counter gets loaded with 0, thus CAPTURE\ stays low.
- F -Capture counter gets loaded with ff.

Count sequence is as follows:

```
FFT cycle 1 - 0 2 .. 508 510 512 514
FFT cycle 2 - 1 3 .. 509 511 513 515
FFT cycle 3 - 512 514 .. 1020 1022 1024 1026   ] last 2 states of ea
FFT cycle 4 - 513 515 .. 1021 1023 1025 1026   ] are in 4 cycle gap.
FFT cycle 5 - 1024 1026 .. 1532 1534 1536 1538
FFT cycle 6 - 1025 1027 .. etc
```

U135

D009T07.ABL

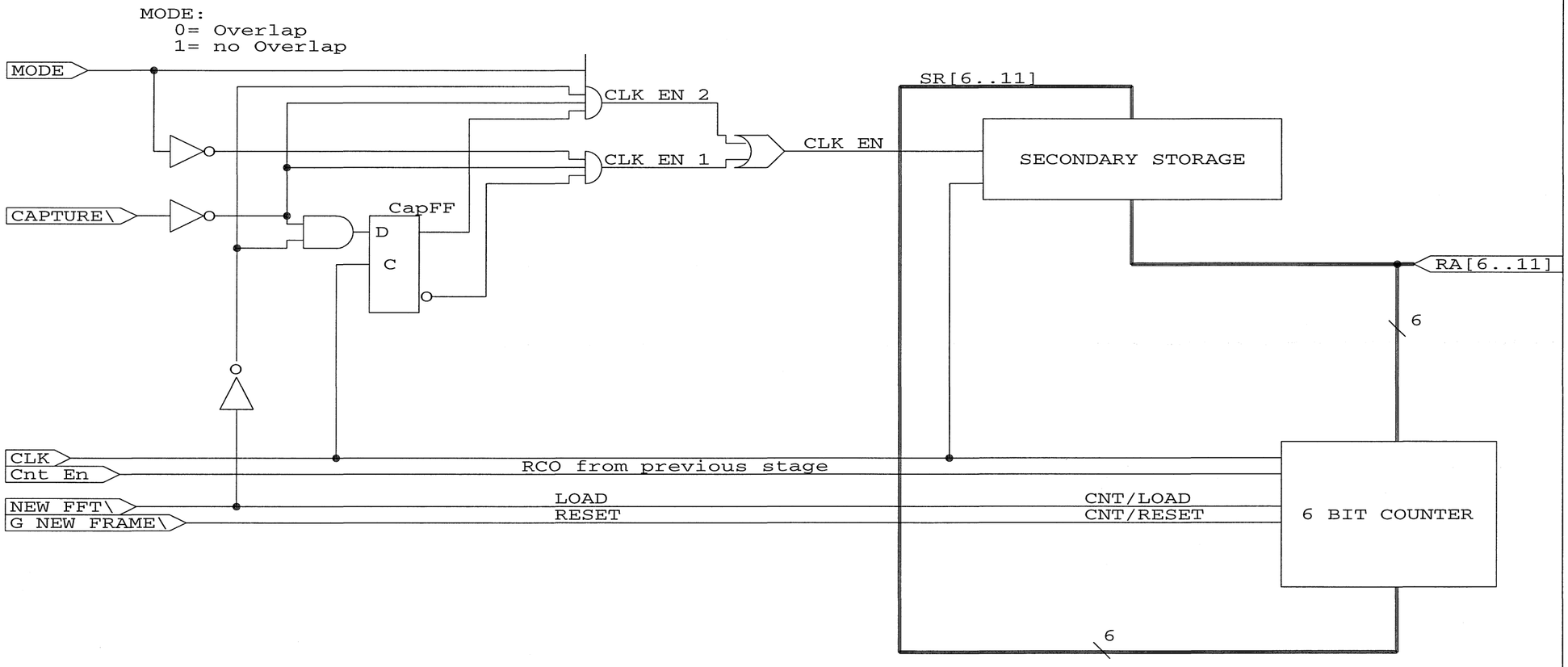
L008D13.SCH

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER BUFFER RAM READ ADR COUNTER (RA0..RA5)		
Size: B	Document Number: 56000K023 (K023D01.PAL)	REV:
Date: April 4, 1997	Sheet 1 of 2	

23S8 PAL

FUNCTIONS:

* 6 bit sync counter.
  * Sync reset.
  * Sync load from internal storage register.
  * Cnt En is RCO from previous stage (U136).
* Internal storage reg to caputure the current state of counter.
* Secondary storage clk enable logic.



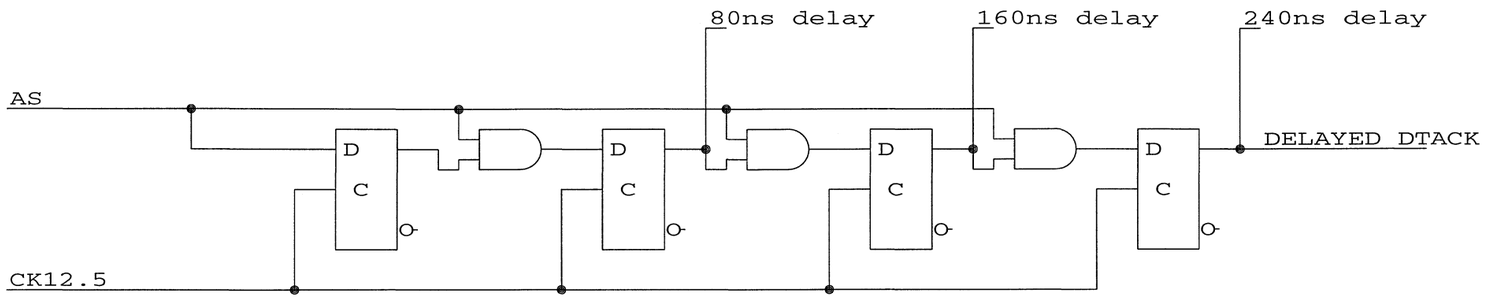
See timing on dwg K023D2.PAL

U134

D009T08.ABL

L008D13.SCH

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER BUFFER RAM READ ADR COUNTER (RA6..RA11)		
Size: A	Document Number: 56000K023 (K023D02.PAL)	REV
Date: April 4, 1997	Sheet 2 of 2	



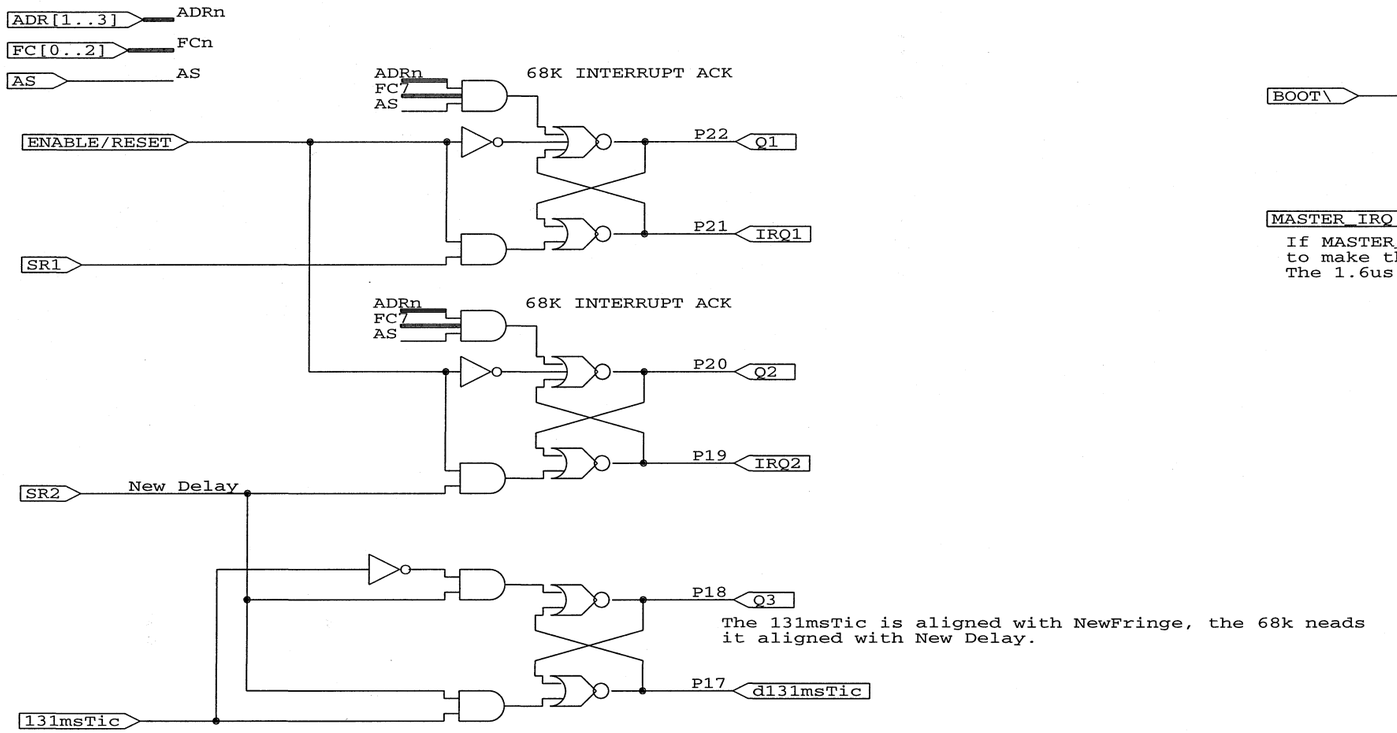
DTACK cannot go low >50ns before data is ready to be read by 68k

U214

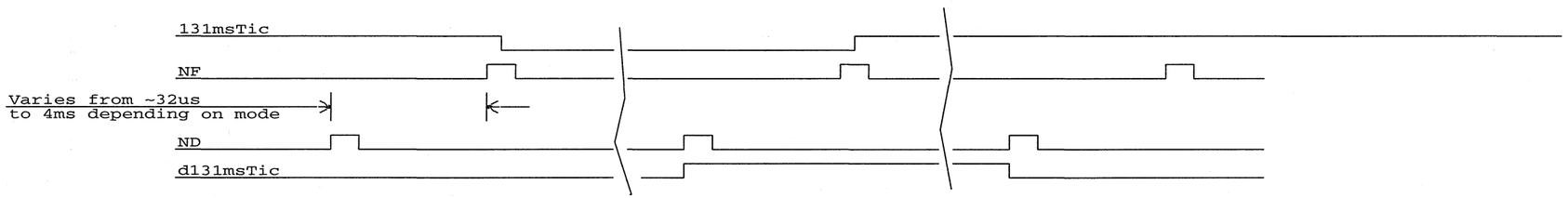
D009T17.ABL

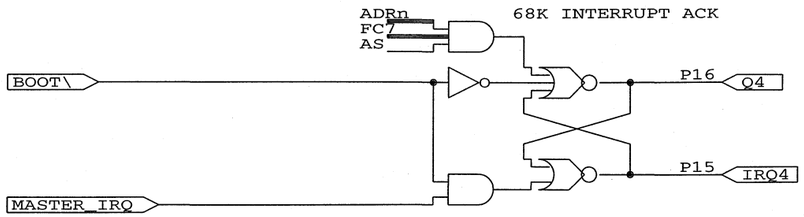
L008D22.SCH

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title 68K DTACK PAL		
Size A	Document Number 56000K024 (K024D01.PAL)	REV
Date: April 4, 1997	Sheet 1 of 1	



The 131msTic is aligned with NewFringe, the 68k neads it aligned with New Delay.

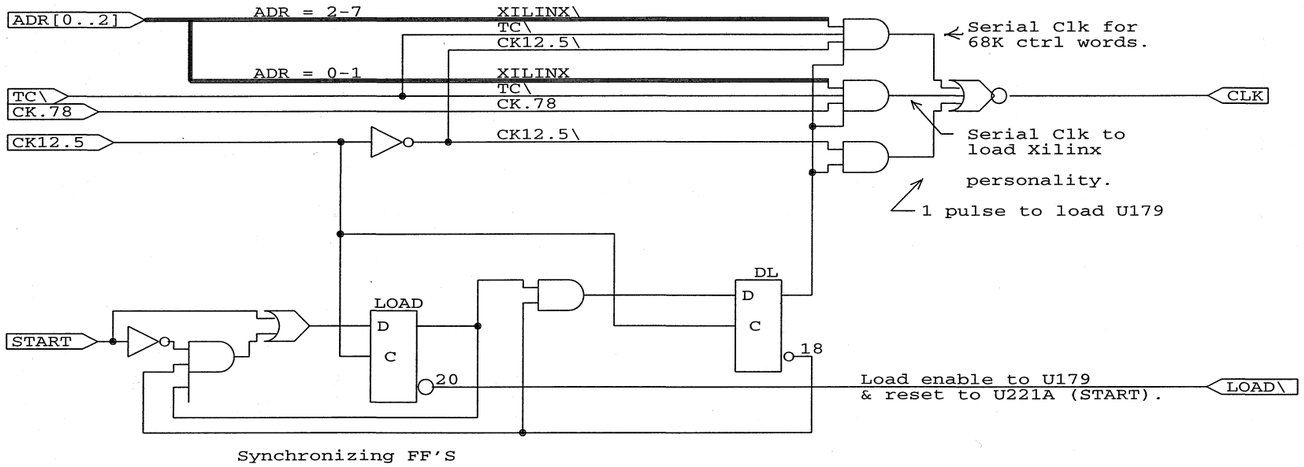




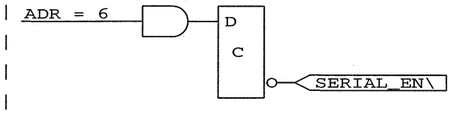
If MASTER_IRQ duration is >1.6us then IRQ4 equation must be changed to make the request de-asert by the time 68K finishes it IACK cycle. The 1.6us is based upon a 12.5mhz 68k.

U180
D009T24.ABL
L008D23.SCH

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER INTERRUPT LATCH		
Size: B	Document Number: 56000K025 (K025D01.PAL)	REV:
Date: April 4, 1997	Sheet 1 of 1	

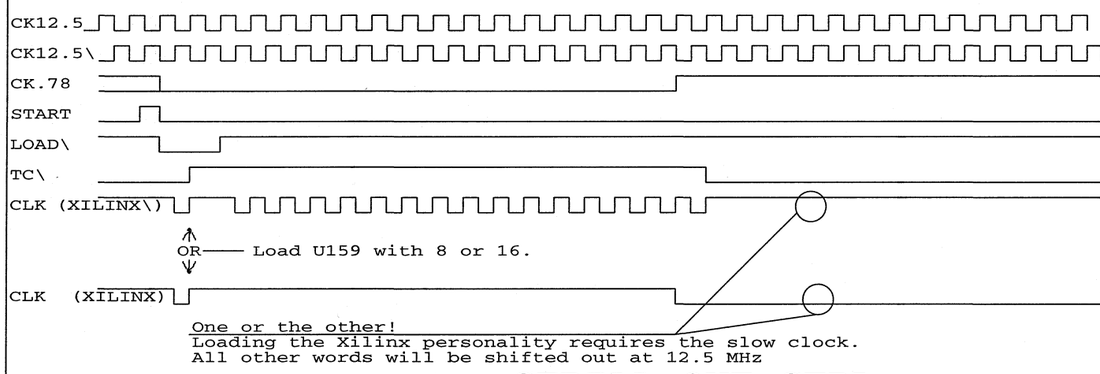


Synchronizing FF'S



Active when loading ctrl words into Bit Shufflers. Prevents 3st contention within Xilinx.

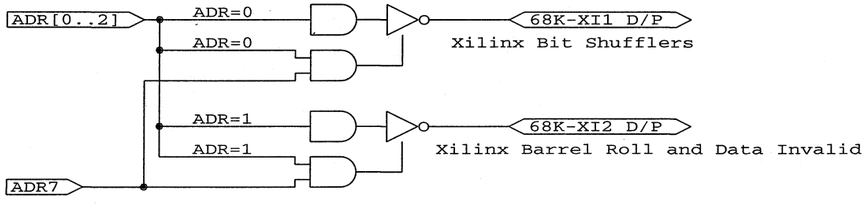
68K must select another adr. after the serial load is complete.



SERIAL OUT CTRL

XILINX PRGM CTRL

The XILINX's D/P input control.
The 68k takes D/P low before sending program words into XILINX.
The XILINX will then drive this signal high upon being successfully programmed.

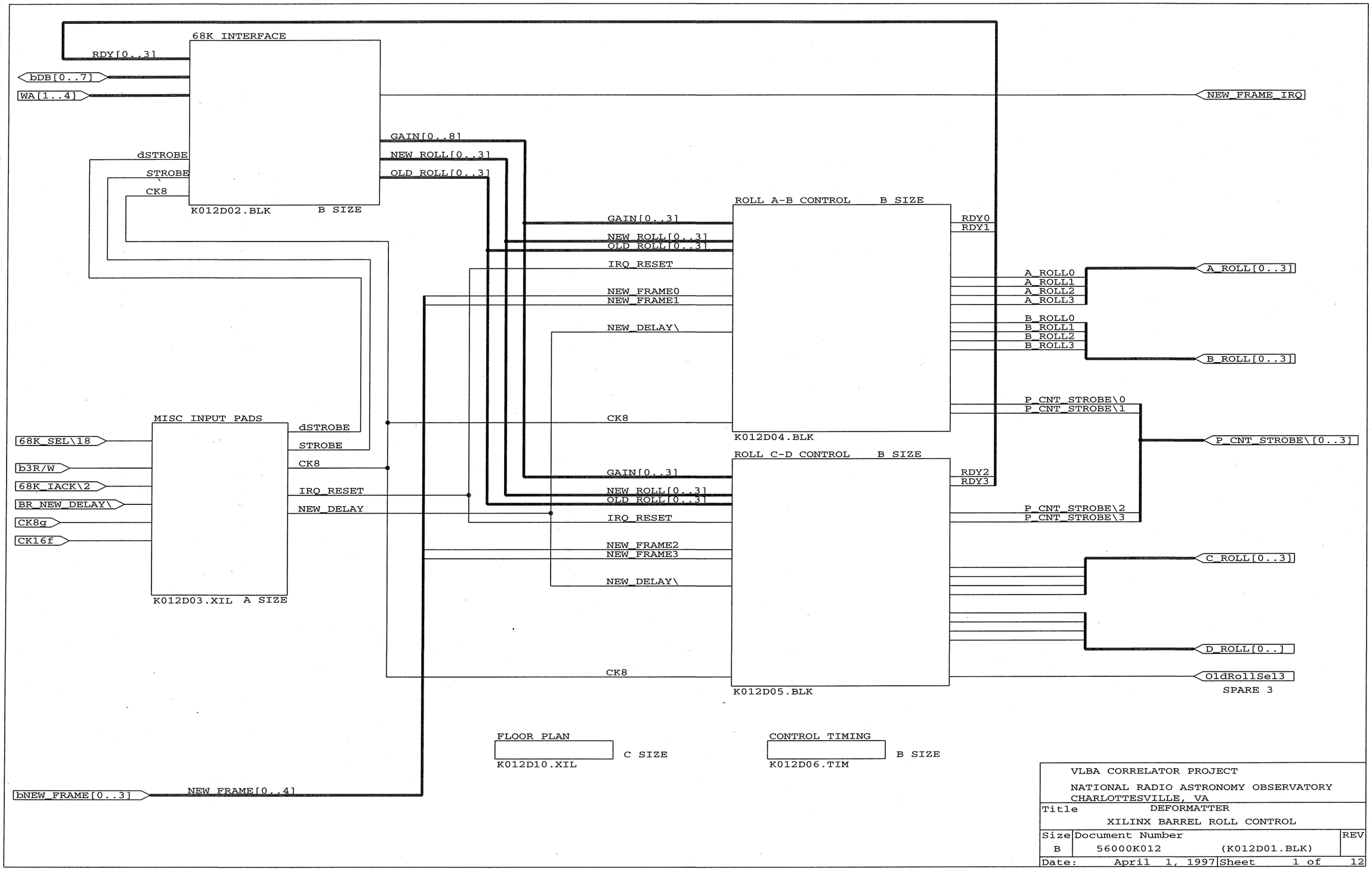


U160

D009T26.ABL

L008D28.SCH

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER SERIAL SHIFT CONTROL PAL		
Size: B	Document Number: 56000K26 (K026D01.PAL)	REV:
Date: April 4, 1997	Sheet 1 of 1	



VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER XILINX BARREL ROLL CONTROL	
Size B	Document Number 56000K012 (K012D01.BLK)	REV
Date: April 1, 1997	Sheet 1 of 12	

D[0..7]

CONTROL

K012D07.XIL E SIZE

U?

74F574

D0 2 D1 19 GAIN0
D1 3 D2 18 GAIN1
D2 4 D3 17 GAIN2
D3 5 D4 16 GAIN3
D4 6 D5 15 GAIN4
D5 7 D6 14 GAIN5
D6 8 D7 13 GAIN6
D7 9 D8 12 GAIN7
11 CLK
1 OC

GAIN[0..8]

SEL0
adr= 360,001 BRgain1

U?

74F574

D0 2 D1 19 GAIN8
D1 3 D2 18 GAIN9
D2 4 D3 17 GAIN10
D3 5 D4 16
D4 6 D5 15
D5 7 D6 14
D6 8 D7 13
D7 9 D8 12
11 CLK
1 OC

SEL2
adr= 360,005 BRgain2

U?

74F574

D0 2 D1 19 NEW_ROLL0
D1 3 D2 18 NEW_ROLL1
D2 4 D3 17 NEW_ROLL2
D3 5 D4 16 NEW_ROLL3
D4 6 D5 15 OLD_ROLL0
D5 7 D6 14 OLD_ROLL1
D6 8 D7 13 OLD_ROLL2
D7 9 D8 12 OLD_ROLL3
11 CLK
1 OC

NEW_ROLL[0..3]

OLD_ROLL[0..3]

SEL1
adr= 360,003 BRroll

RDY3

RDY3

D0 D C IRQ_DISABLE\

NEW_FRAME_IRQ

dSTROBE

D1 D C

SEL3
adr= 360,007 BRrdy

0= NORMAL
D0
1= SWAP D C

CONTROL BIT FOR SPECIAL POLAR MODE #2
PALS SWAP ODD NUMBERED CHANNELS WHEN
SWAP COMMANDED

PIN 62
1= NORMAL
0= SWAP

SEL4
ADR= 360,009

A[1..4]

A1
A2
A3
A4

SEL0
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7

68K_SEL\18

STROBE

DECODER

Note: SEL5-7 not decoded.

68K INTERFACE

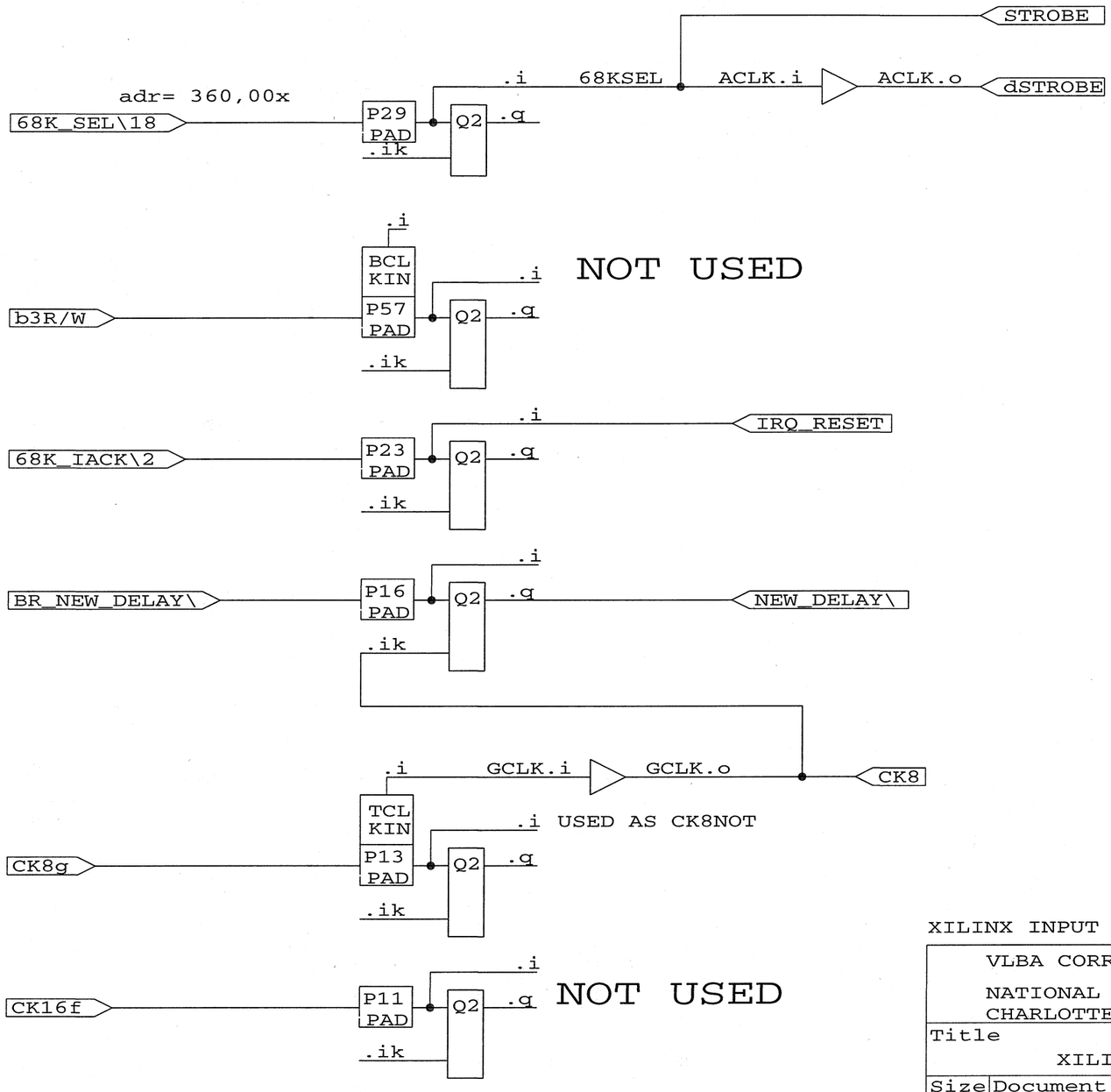
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title DEFORMATTER

XILINX BARELL ROLL CONTROLL

Size	Document Number	REV
B	56000K012 (K012D02.BLK)	
Date: April 1, 1997	Sheet 2 of 12	



XACT FILE= ROLL9.MAC

XILINX INPUT PADS

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER XILINX BARREL ROLL CONTROL	
Size A	Document Number 56000K012 (K012D03.XIL)	REV
Date: April 3, 1997	Sheet 3 of 12	

A & B COUNTERS

K012D08.XIL C SIZE

A & B ROLL MUXES

K012D11.XIL B SIZE

NOTE:
Roll by 16
tracks 0 thru 15 and 16 thru 31.
legal combinations -

Truth Table

NEW FRAME	RCO\	NEW DELAY\	FUNCTION
0	0	0	Strobe Old Barrel Roll
0	0	1	Do Nothing
0	1	0	Do Nothing
0	1	1	Do Nothing
1	0	0	Do Nothing
1	0	1	Strobe New Barrel Roll
1	1	0	Do Nothing
1	1	1	Strobe New Barrel Roll

U?

NEW ROLL 0 3 — A1
OLD ROLL 0 4 — A2
NEW ROLL 1 6 — B1
OLD ROLL 1 5 — B2
NEW ROLL 2 11 — C1
OLD ROLL 2 12 — C2
NEW ROLL 3 14 — D1
OLD ROLL 3 13 — D2
1 — WS
9 — CLK

QA 2 — A ROLL 0
QB 7 — A ROLL 1
QC 10 — A ROLL 2
QD 15 — A ROLL 3

74F399

MUX SEL
CLOCK ENA

Notes:

* One of 4 identical logic functions, except as noted.
* Each of the 2 XILINX dwgs (K012D08.XIL & K012D09.XIL) conatin the logic for 2 functions depicted on this sheet.
* The WAIT function is only implemented for RDY3 which generates the IRQ. The other 3 RDY signals are not used.

NEW_DELAY\

NEW_FRAME0

NEW FRAME0
CK8\
P CNT STROBE\0

This is a pseudo random counter that is to function similar to a 74269 counter.

GAIN represents the amount the BUFFER RAM's Read pointer has gained on the write pointer.

Hold current state until reset

reset

D C

WAIT - a NewDelay is going to back us up thru a NewFrame; so wait until we see the second NewFrame.

STOP0

Tcnt0

J C K

RCO\
0=counting

ExOR

D D D D D D D D D D D D

LOAD

GAIN[0..8]

GAIN0
GAIN1
GAIN2
GAIN3
GAIN4
GAIN5
GAIN6
GAIN7
GAIN8
GAIN9
GAIN10

D C

J C K

RDY3

IRQ_RESET

We are going to get a second NewFrame because NewDelay is backing us up thru a NewFrame boundry.

This logic is implemented only for PHASE CENTER 3

NOTE: For low bandwidth modes the 68k changes the GAIN word during the observation. This can cause the counter to get loaded with any value. However, this should be okay because there will not be a NewDelay until the counter can expire. The NewDelay is what resulted in the loading of a new GAIN value. The coincidence of NewDelay and the counter counting is the only combination that can have an adverse effect.

In other words, the GAIN value loaded must be correct only to ensure the proper decoding of line 1 in the truth table above.

ROLL A-B CONTROL

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFROMATTER
XILINX BARREL ROLL CONTROL

Size	Document Number	REV
B	56000K012 (K012D04.BLK)	

Date: April 1, 1997 Sheet 4 of 12

C & D COUNTERS

C SIZE

K012D09.XIL

C & D ROLL MUXES

B SIZE

K012D12.XIL

NOTE:
Roll by 16
tracks 0 thru 15 and 16 thru 31.
legal combinations -

Truth Table

NEW FRAME	RCO\	NEW DELAY\	FUNCTION
0	0	0	Strobe Old Barrel Roll
0	0	1	Do Nothing
0	1	0	Do Nothing
0	1	1	Do Nothing
1	0	0	Do Nothing
1	0	1	Strobe New Barrel Roll
1	1	0	Do Nothing
1	1	1	Strobe New Barrel Roll

U?

NEW ROLL 0 3 — A1 — QA 2 — A ROLL 0
OLD ROLL 0 4 — A2
NEW ROLL 1 6 — B1 — QB 7 — A ROLL 1
OLD ROLL 1 5 — B2
NEW ROLL 2 11 — C1 — QC 10 — A ROLL 2
OLD ROLL 2 12 — C2
NEW ROLL 3 14 — D1 — QD 15 — A ROLL 3
OLD ROLL 3 13 — D2
1 — WS
9 — CLK

74F399

MUX SEL

CLOCK ENA

Notes:

* One of 4 identical logic functions, except as noted.
* Each of the 2 XILINX dwgs (K012D08.XIL & K012D09.XIL) conatin the logic for 2 functions depicted on this sheet.
* The WAIT function is only implemented for RDY3 which generates the IRQ. The other 3 RDY signals are not used.

NEW_DELAY\

NEW_FRAME0

NEW FRAME0

CK8\

P CNT STROBE\0

This is a pseudo random counter that is to function similar to a 74269 counter.

GAIN represents the amount the BUFFER RAM's Read pointer has gained on the write pointer.

Hold current state until reset

reset

D C

WAIT - a NewDelay is going to back us up thru a NewFrame; so wait until we see the second NewFrame.

J C K

RDY3

IRQ_RESET

We are going to get a second NewFrame because NewDelay is backing us up thru a NewFrame boundry.

This logic is implemented only for PHASE CENTER 3

STOP0

Tcnt0

RCO\
0=counting

ExOR

D D D D D D D D D D D D

LOAD

GAIN[0..8]

GAIN0
GAIN1
GAIN2
GAIN3
GAIN4
GAIN5
GAIN6
GAIN7
GAIN8
GAIN9
GAIN10

NOTE: For low bandwidth modes the 68k changes the GAIN word during the observation. This can cause the counter to get loaded with any value. However, this should be okay because there will not be a NewDelay until the counter can expire. The NewDelay is what resulted in the loading of a new GAIN value. The coincidence of NewDelay and the counter counting is the only combination that can have an adverse effect.

In other words, the GAIN value loaded must be correct only to ensure the proper decoding of line 1 in the truth table above.

ROLL C-D CONTROL

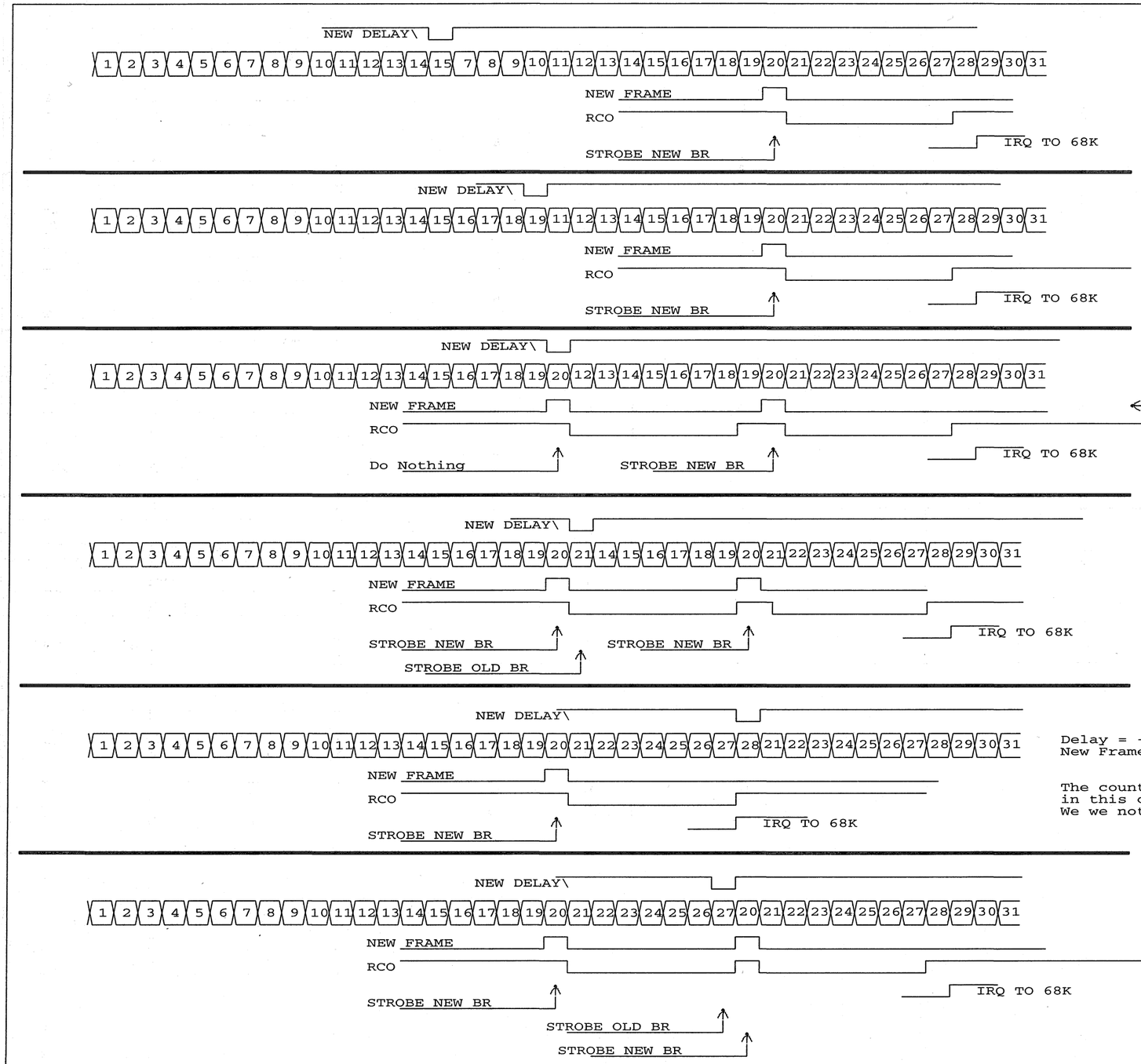
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFROMATTER
XILINX BARREL ROLL CONTROL

Size	Document Number	REV
B	56000K012 (K012D05.BLK)	

Date: April 1, 1997 Sheet 5 of 12



BR = Barell Roll

DELAY:
- Effective delay = +- 1 bit.
- Actual Delay = (bits gained) +- 1 bit.
  Bits Gained = The amount the write pointer gains on the read pointer during a New Delay Cycle.

NEW FRAME signal:
1. Strobe enable to new Barell Roll value.
2. Loads a counter with a value = (Write pntr gain on Read pntr) - 1 ???

RCO = 0 -The counter is counting.

← For this case the parity counter will get strobed 2 times, but doesn't matter since the counters are not reset.

NEW FRAME	RCO\	NEW DELAY\	FUNCTION
0	0	0	Strobe Old Barrel Roll
0	0	1	Do Nothing
0	1	0	Do Nothing
0	1	1	Do Nothing
1	0	0	Do Nothing
1	0	1	Strobe New Barrel Roll
1	1	0	Do Nothing
1	1	1	Strobe New Barrel Roll

Delay = -1, thus the bit that produces the New Frame pulse gets swallowed.

The count must be short enough so that RCO is not active in this case because the New Frame bit gets swallowed. We we not see the New Frame repeated!

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: BARREL ROLL CONTROL TIMING

Size	Document Number	REV
B	56000V003 (K012D06.TIM)	

Date: April 1, 1997 Sheet 6 of 12

GAIN0 GAIN1 GAIN2 GAIN3

HA HB HC HD

.di .a .b .c .d .e .ec .rd .k

SEL0 D0 SEL1 — D1 — D2 — SEL1\ — D3

QX QY X Y F G

NEW ROLL 0 NEW ROLL 1 NEW ROLL 2 NEW ROLL 3

CLOCK ENA RESET

NEW_ROLL[0..3]

GAIN[0..10]

GAIN4 GAIN5 GAIN6 GAIN7

HE HF HG HH

D4 — D5 — D6 — SEL1\ — D7

OLD ROLL 0 OLD ROLL 1 OLD ROLL 2 OLD ROLL 3

OLD_ROLL[0..3]

dSTROBE

WA[1..4]
FROM OUTSIDE CHIP

WA1 P30 PAD .i A1 .ik .q Q2
WA2 P28 PAD .i A2 .ik .q Q2
WA3 P27 PAD .i A3 .ik .q Q2
WA4 P26 PAD .i A4 not used .ik .q Q2

GA
A1 .a
A2 .b
A3 .c
.d .e
.QX .QY
.x SEL1 adr=360,003
.y SEL0 adr= 360,001

FA
.x SEL3 adr= 360,007
.y SEL2\ adr= 360,005

STROBE
adr= 360,00x

DA
A1 .a .x
A2 .b
A3 .e
D0 .d .k
P62 SPARE5 SPECIAL POLAR MODE #2
SEL4 ADR = 360,009

FB
D0 .a .b
D1 .c .d .e
.x .y
Spare Ctrl bit NOT USED

IRQ_DISABLE
RDY3

GD
.x .y

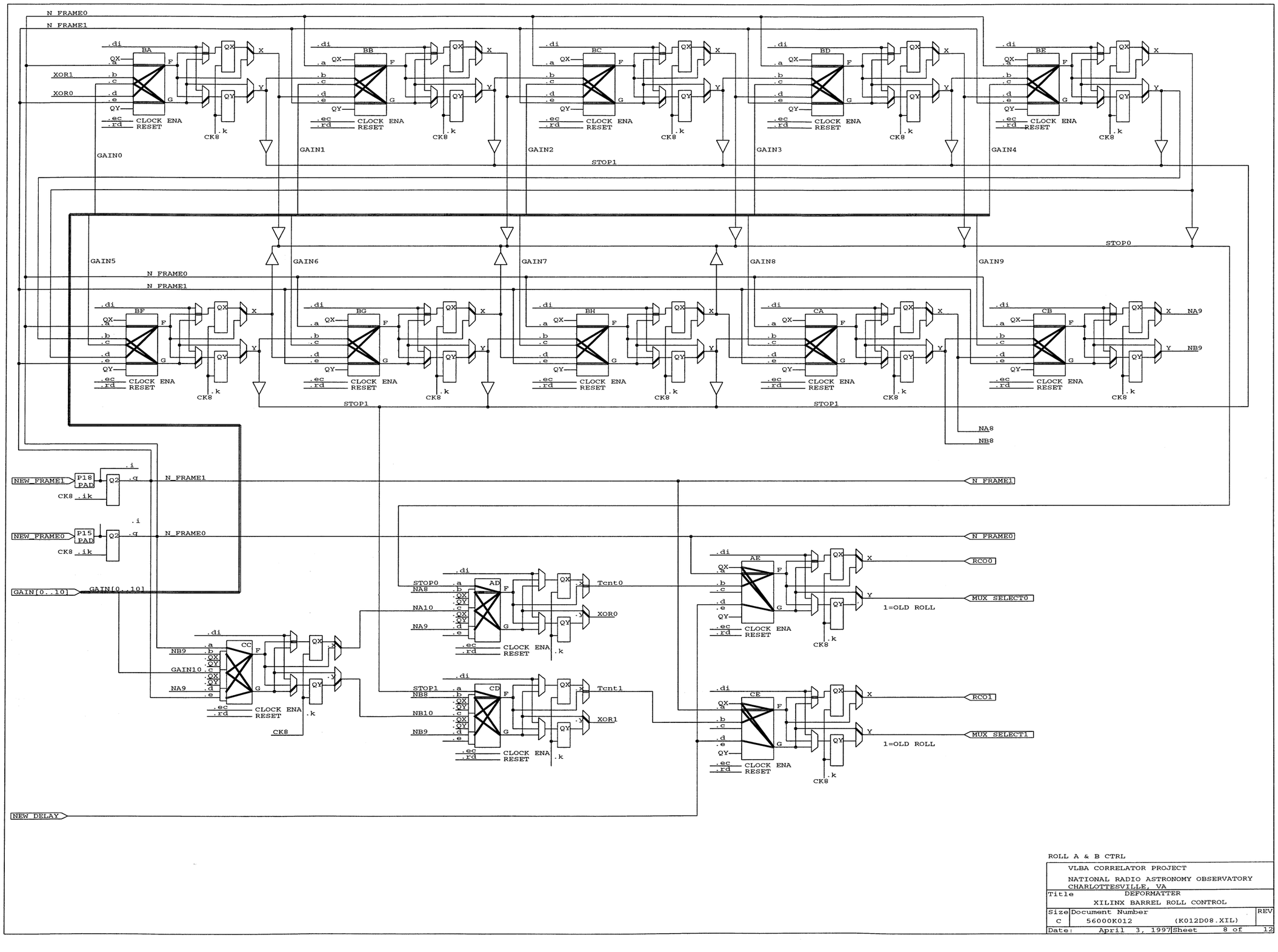
P44 PIN IQ D4
P34 PIN IQ D0 GAIN8
P46 PIN IQ D5
P35 PIN IQ D1 GAIN9
P48 PIN IQ D6
P37 PIN IQ D2 GAIN10
P52 PIN IQ D7
P40 PIN IQ D3

.o .ok .t Q1
P42 PAD NEW_FRAME_IRQ

68K INTERFACE

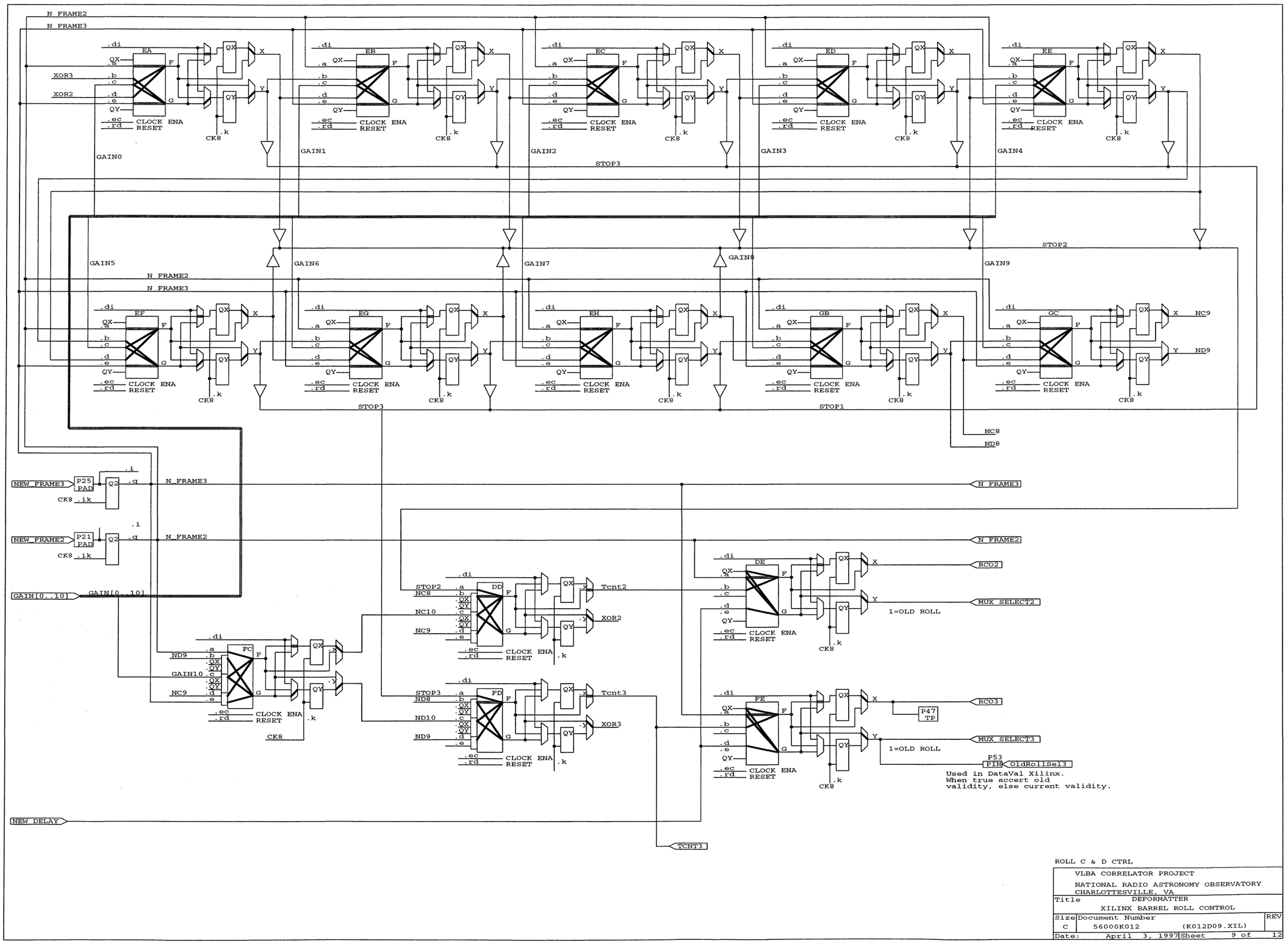
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER XILINX BARELL ROLL CONTROL	
Size E	Document Number 56000K012 (K012D07.XIL)	REV
Date: April 3, 1997	Sheet 7 of 12	



ROLL A & B CTRL

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title	DEFORMATTER XILINX BARREL ROLL CONTROL	
Size: C	Document Number: 56000K012 (K012D08.XIL)	REV
Date: April 3, 1997	Sheet 8 of 12	

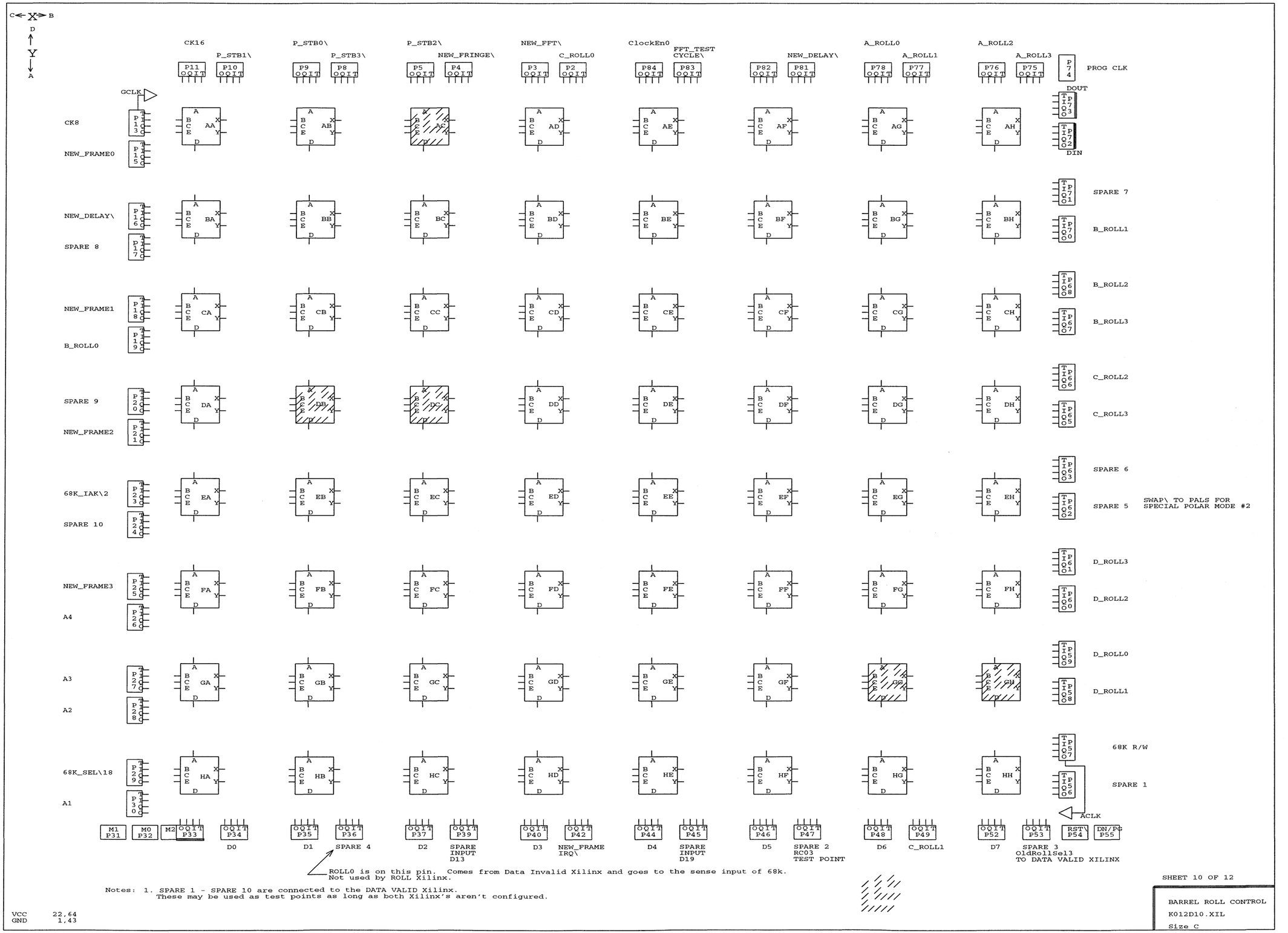


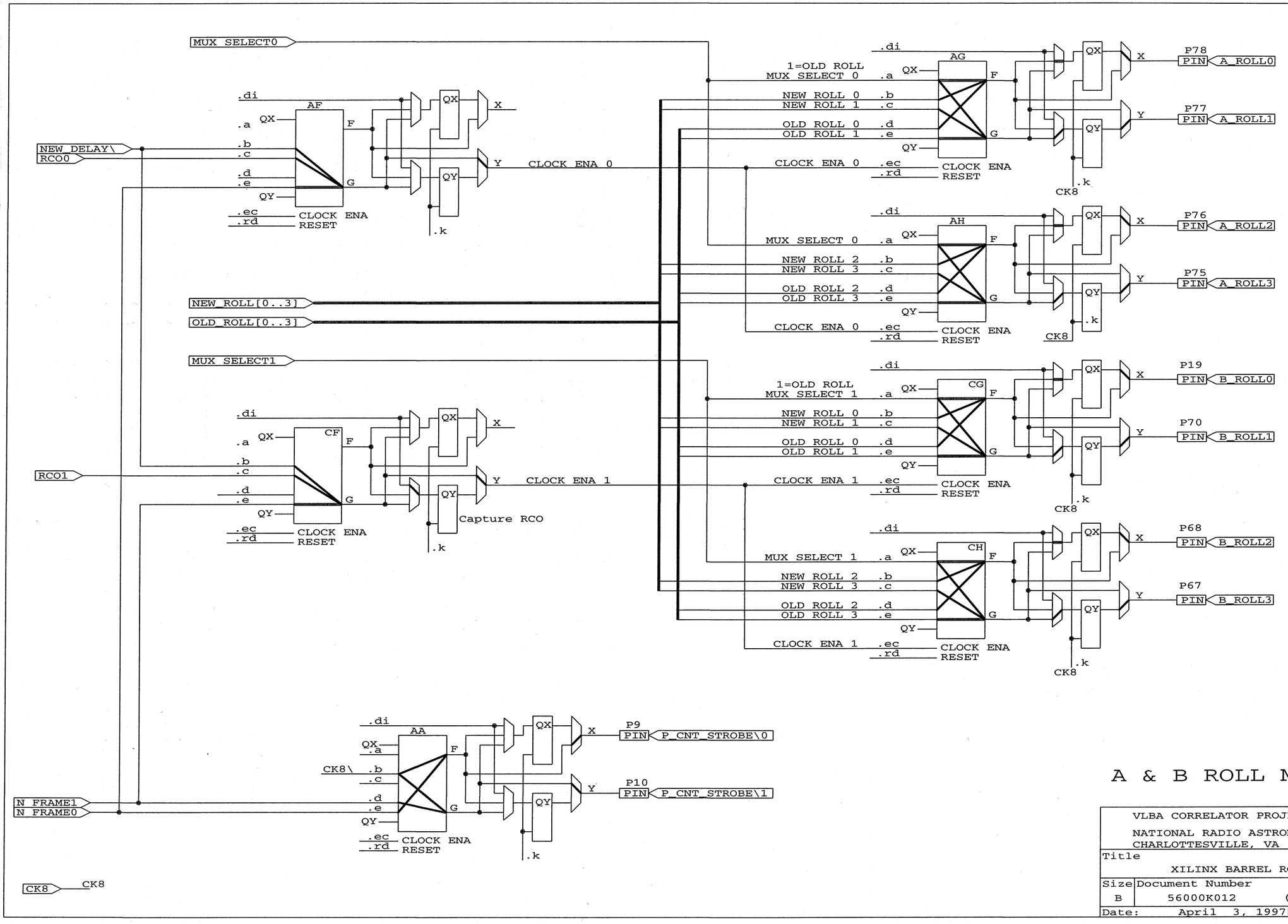
ROLL C & D CTRL

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFORMATTER XILINX BARREL ROLL CONTROL	
Size: C	Document Number: 56000K012 (K012D09.XIL)	REV
Date: April 3, 1997	Sheet 9 of 12	


C X B
D
Y
A
CK16
P_STB1\
P_STB0\
P_STB3\
P_STB2\
NEW_FRINGE\
NEW_FFT\
C_ROLL0
ClockEn0
FFT_TEST
CYCLE\
NEW_DELAY\
A_ROLL0
A_ROLL1
A_ROLL2
A_ROLL3
P11
P10
P9
P8
P5
P4
P3
P2
P84
P83
P82
P81
P78
P77
P76
P75
P74
PROG CLK
DOUT
DIN
GCLK
CK8
NEW_FRAME0
NEW_DELAY\
SPARE 8
NEW_FRAME1
B_ROLL0
SPARE 9
NEW_FRAME2
68K_IAK\2
SPARE 10
NEW_FRAME3
A4
A3
A2
68K_SEL\18
A1
SPARE 7
B_ROLL1
B_ROLL2
B_ROLL3
C_ROLL2
C_ROLL3
SPARE 6
SPARE 5
SWAP\ TO PALS FOR
SPECIAL POLAR MODE #2
D_ROLL3
D_ROLL2
D_ROLL0
D_ROLL1
68K R/W
SPARE 1
ACLK
M1
P31
M0
P32
M2
P33
P34
D0
P35
D1
P36
SPARE 4
P37
D2
P39
SPARE
INPUT
D13
P40
D3
P42
NEW_FRAME
IRQ\
P44
D4
P45
SPARE
INPUT
D19
P46
D5
P47
SPARE 2
RC03
TEST POINT
P48
D6
P49
C_ROLL1
P52
D7
P53
SPARE 3
OldRollSel3
TO DATA VALID XILINX
RST\
P54
DN/PG
P55
ROLL0 is on this pin. Comes from Data Invalid Xilinx and goes to the sense input of 68k.
Not used by ROLL Xilinx.
Notes: 1. SPARE 1 - SPARE 10 are connected to the DATA VALID Xilinx.
These may be used as test points as long as both Xilinx's aren't configured.
VCC 22,64
GND 1,43
SHEET 10 OF 12
BARREL ROLL CONTROL
K012D10.XIL
Size C



A & B ROLL MUXES

VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title: XILINX BARREL ROLL CONTROL	
Size: B	Document Number: 56000K012 (K012D11.XIL) REV:
Date: April 3, 1997	Sheet 11 of 12

C & D ROLL MUXES

CK8

RCO2

N_FRAME2

NEW_DELAY\

RCO3

N_FRAME3

N FRAME3

N FRAME2

CK8\

1=OLD ROLL

MUX SELECT2

NEW_ROLL[0..3]

OLD_ROLL[0..3]

CLOCK ENA 2

CLOCK ENA 3

MUX SELECT 2 .a
NEW ROLL 0 .b
NEW ROLL 1 .c
OLD ROLL 0 .d
OLD ROLL 1 .e
CLOCK ENA 2 .ec
.rd

MUX SELECT 3 .a
NEW ROLL 0 .b
NEW ROLL 1 .c
OLD ROLL 0 .d
OLD ROLL 1 .e
CLOCK ENA 3 .ec
.rd

MUX SELECT 2 .a
NEW ROLL 2 .b
NEW ROLL 3 .c
OLD ROLL 2 .d
OLD ROLL 3 .e
CLOCK ENA 2 .ec
.rd

MUX SELECT 3 .a
NEW ROLL 2 .b
NEW ROLL 3 .c
OLD ROLL 2 .d
OLD ROLL 3 .e
CLOCK ENA 3 .ec
.rd

CLOCK ENA
RESET

DF DG DH FG FH FF AB GF GE

P2 PIN C_ROLL0
P49 PIN C_ROLL1
P66 PIN C_ROLL2
P65 PIN C_ROLL3
P59 PIN D_ROLL0
P58 PIN D_ROLL1
P60 PIN D_ROLL2
P61 PIN D_ROLL3
P5 PIN P_CNT_STROBE\2
P8 PIN P_CNT_STROBE\3

IRQ_RESET
NFRAME3
TCNT3
Capture RCO
RSEQ0
RSEQ1
RDY3

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
XILINX BARREL ROLL CONTROL

Size	Document Number	REV
B	56000K012 (K012D12.XIL)	
Date: April 3, 1997	Sheet 12 of 12	

SERIAL CTRL REG

68K_SD
68K_S_CLK4
68K_L_CLK4
68K_S_CLK5

I/O SPARE0 — In PBI test fixture- data source for DELAY WORD
I/O SPARE2 — In PBI test fixture- clk source for DELAY WORD.
I/O SPARE1 — ROLL0 input from TRC, gets routed to XI_SPARE4
I/O SPARE3 — TESTEN to associated Play-Back Drive.

INV[0..7]
DLY[0..6]

A SIZE
K013D02.BLK

DATA INV[0..3]

IN 1997, THE ORIGINAL DATA INVALID XILINX DESIGN WAS COPIED AND THEN MODIFIED TO MAKE A VERSION TO BLANK THE MKIII / IV HEADER POLLUTION.

SEE MORE DETAILED NOTES ON SHEET 2.

DELAY & CONTROL

INV[0..3]
DLY[0..6]
N FRAME\0
N FRAME\1
OldRollSel
CK8

dDATA VAL0
dDATA VAL1
dDATA VAL2
dDATA VAL3

E SIZE
K013D04.BLK

DELAY & CONTROL

INV[4..7]
DLY[0..6]
N FRAME\2
N FRAME\3
OldRollSel
CK8

dDATA VAL4
dDATA VAL5
dDATA VAL6
dDATA VAL7

E SIZE
K013D05.BLK

DATA INV[4..7]

MISC I/O PADS

NEW FRAME\0
NEW FRAME\1
NEW FRAME\2
NEW FRAME\3
OldRollSel3
CK81

TEST CYCLE EN
NEW_FRINGE_EN\

bNEW FRAME0
bNEW FRAME1
bNEW FRAME2
bNEW FRAME3
cTEST CYCLE EN
TR TEST CYCLE EN
bNEW_FRINGE_EN\

B SIZE
K013D03.XIL

OVERALL BLOCK DIAG
K013D12.XIL B SIZE

FLOOR PLAN
K013D09.XIL C SIZE

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DEFORMATTER DATA INVALID XILINX		
Size: A	Document Number: 56000K013 (K013D01.BLK)	REV:
Date: November 17, 1997	Sheet 1 of 12	

Used in PBI TEST FIXTURE only.
Clk source for DELAY WORD.

68K_S_CLK5 → I/O SPARE2

I/O SPARE0

Used in PBI TEST FIXTURE only.
Data source for DELAY WORD.

C SIZE

DELAY & CONTROL

K013D06.XIL

68K_SD → U? 74LS594 SER

68K_S_CLK4 / 68K_L_CLK4 → SER CLK S / SER CLK L → SRCLK, SRCLR

RCLK, RCLR

QA DLY 0, QB DLY 1, QC DLY 2, QD DLY 3, QE DLY 4, QF DLY 5, QG DLY 6 → DLY [0..6]

QH → I/O SPARE3 (TEST DRIVE x)

QH' → U? 74LS594

Ctrl signal to the PBD via the MUX CARD.
Enables TEST DATA & TEST CLK to and back
from the PBD.

IN THE ORIGINAL VLBA PERSONALITY, INV[0..7] GO TO SHEETS 4 & 5.

QA INV 0, QB INV 1, QC INV 2, QD INV 3, QE INV 4, QF INV 5, QG INV 6, QH INV 7 → INV [0..7]

IN THE NEW (ALTERNATE) MARK III / MARK IV PERSONALITY INV[0..7] ARE RE-ROUTED TO THE NEW BLOCKS, SHOWN FUNCTIONALLY BELOW, AND ARE GATED BEFORE CONTINUING ON TO THE ORIGINAL DESTINATIONS ON SHEETS 4 & 5.

ORIGINAL PERSONALITY GENERATED FROM INV.MAC, INV-C.MAC AND INV-R.MAC
THE MCS FILE IS NAMED DEFCTRL.MCS

NEW PERSONALITY GENERATED FROM MK3INV.MAC, MK3INV-C.MAC AND MK3INV-R.MAC
THE MCS FILE IS NAMED MK3CTRL.MCS

FOUR COPIES

ONE FOR EACH NF[0..3]

NEWFRAME SIGNALS COME FROM SHEET 3, USING THE INPUT PINS OF THE BUFFERED NF OUTPUTS

FROM INV[0..7] ABOVE → ORIGINAL INV0 → NEW INV0

FROM INV[0..7] ABOVE → ORIGINAL INV1 → NEW INV1

LOGIC 1 → D P R Q, CLK, C L Q

NF0

NEW_FFT

NEW OUTPUTS GO TO ORIGINAL DESTINATIONS ON SHEETS 4 & 5.

FORCE DATA INVALID ON NEWFRAME

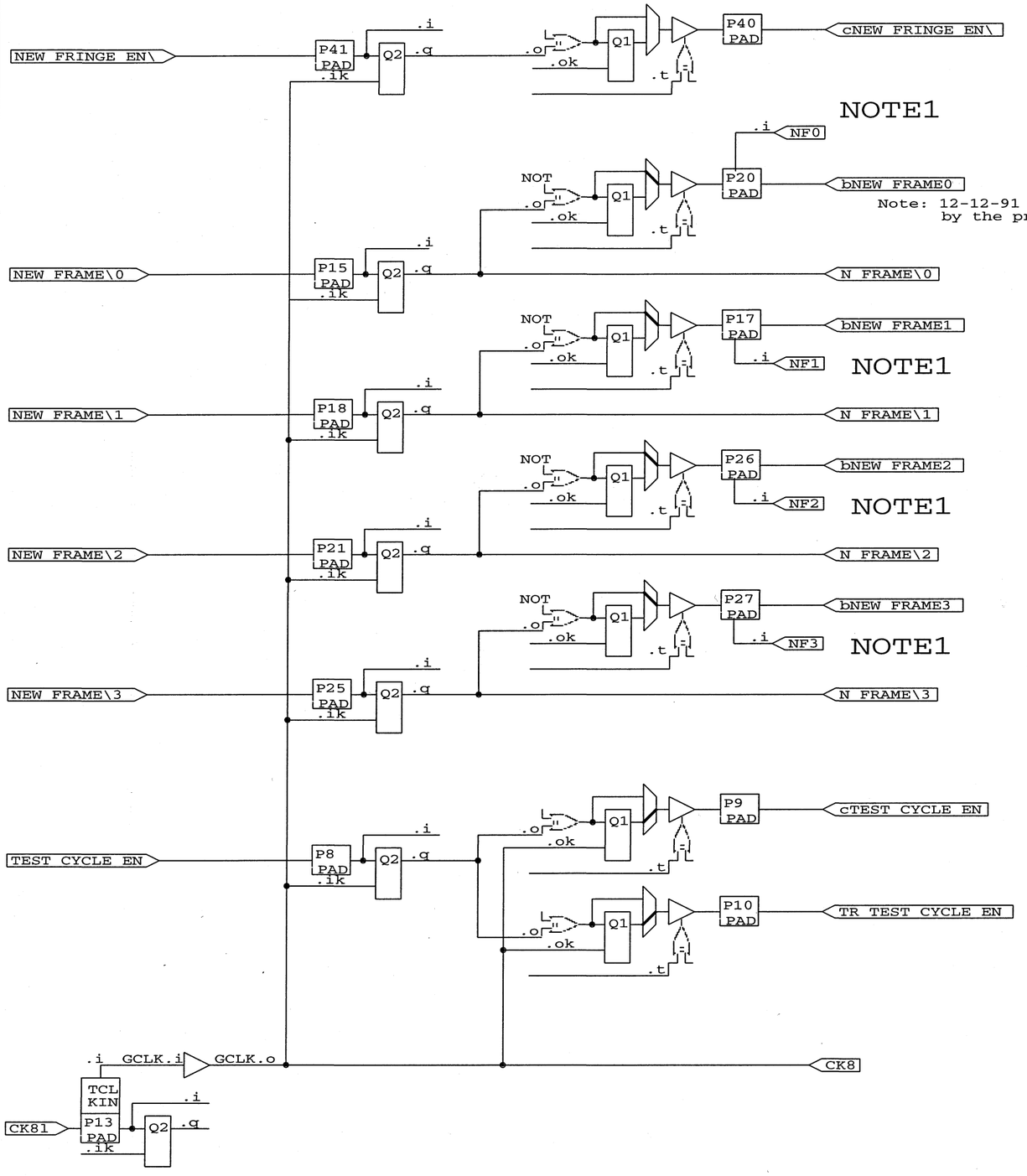
REMOVE THE FORCED INVALID ON THIRD NEW_FFT AFTER THE NEWFRAME

NEW LOGIC
ALTERNATE PERSONALITY FOR MARK III / IV
TO BLANK OUT HEADER POLLUTION

DEFORMATTER

Serial program control register

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DATA INVALID XILINX		
Size: B	Document Number: 56000K013 (K013D02.BLK)	REV:
Date: November 17, 1997	Sheet 2 of 12	

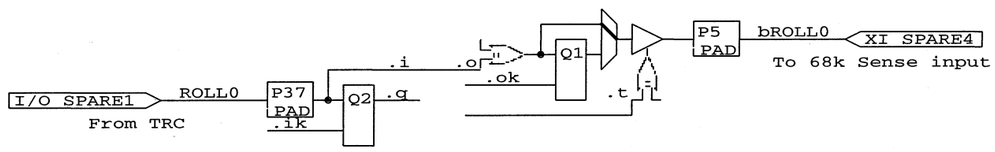


Note: 12-12-91 The 1 clk time difference between the two can be compensated for by the programmed delay loaded into the DataValid counters.

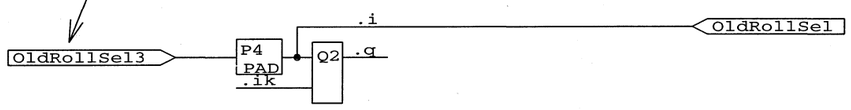
NOTE1

THE FOUR NF0 THRU NF3 SIGNALS
ARE USED ONLY IN THE MK3CTRL.MCS VERSION
TRUE VERSIONS OF NEWFRAME WERE NEEDED
TO FORCE DATA INVALID AT EACH NEW FRAME

THESE GO TO THE NEW CLBs ON SHEET 6
(FUNCTIONAL LOGIC SHOWN ON SHEET 2)



From ROLL Xilinx, true for 125ns when a NewDelay causes us to back-up across a frame boundry.



MISC INPUT/OUTPUT PADS

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title DEFORMATTER

XILINX DATA INVALID DELAY & CONTROL

Size	Document Number	REV
B	56000K013 (K013D03.XIL)	
Date: November 17, 1997	Sheet 3 of 12	

CK8\

CK8\

INV[0..3]

force invalid

This is a pseudo randam counter that is to function similar to a 74269 counter.

The delay value/counter aligns the DATA INVALID bit with its correspondent data bits.

CK8

RCO0

J C K

CK8

J C K

RESET0

NEW FRAME\0

LOAD

DLY 0
DLY 1
DLY 2
DLY 3
DLY 4
DLY 5
DLY 6

OldRollSel coincided with counter active; thus we need to inhibit the first occurance of RESET0.

DLY [0..6]

Barrel Rolls <16 are taken care of on the Track Recovery bd. ROLL3 takes care of rolls by 16.

DATA INV0
DATA INV2
DATA INV1
DATA INV3
A ROLL3

Dual 2-1 Mux

D INV0-2
D INV1-3

DATA INV[0..3]

Muxes take care of rolls of 16.

DATA INV2
DATA INV0
DATA INV3
DATA INV1
B ROLL3

Dual 2-1 Mux

D INV2-0
D INV3-1

NewDinv0
Inv0
OldInv0

RAM input

dDATA VAL CH0

NewDinv1
Inv1
OldInv1

RAM input

dDATA VAL CH1

F1

F2

F1- store Data Validity from prevoius frame.
F2- if a New Delay backs us up across a frame boundry (OldRollSel), then put out old validity until we pass the frame boundry the second time.

CK8

C SIZE COUNTERS
K013D07.XIL

C SIZE COUNTERS
K013D10.XIL

OldInv2
Inv2
NewDinv2

RAM input

dDATA VAL CH2

OldInv3
Inv3
NewDinv3

RAM input

dDATA VAL CH3

OldRollSel

True for 125ns when we are going to back up thru a NF boundry.

CK8

RCO1

J C K

CK8

J C K

RESET1

See note above.

NEW FRAME\1

DLY 0
DLY 1
DLY 2
DLY 3
DLY 4
DLY 5
DLY 6

This is a pseudo randam counter that is to function similar to a 74269 counter.

The delay value/counter aligns the DATA INVALID bit with its correspondent data bits.

Data Invalid Delay Counters 1 & 2

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	DEFROMATTER XILINX DATA INVALID DELAY & CONTROL	
Size E	Document Number 56000K013 (K013D04.BLK)	REV
Date: March 13, 1997	Sheet 4 of 12	

CK8\ CK8\

INV[4..7] force invalid

This is a pseudo randam counter that is to function similar to a 74269 counter.

The delay value/counter aligns the DATA INVALID bit with its correspondent data bits.

NEW FRAME\2 LOAD

DLY 0
DLY 1
DLY 2
DLY 3
DLY 4
DLY 5
DLY 6

DLY [0..6]

RCO2

CK8

OldRollSel coincided with counter active; thus we need to inhibit the first occurance of RESET2.

RESET2

F1

F2

NewDinv4
Inv4
OldInv4
RAM input
dDATA VAL CH4

NewDinv5
Inv5
OldInv5
RAM input
dDATA VAL CH5

F1- store Data Validity from prevoius frame.
F2- if a New Delay backs us up across a frame boundry (OldRollSel), then put out old validity until we pass the frame boundry the second time.

Barrel Rolls <16 are taken care of on the Track Recovery bd. ROLL3 takes care of rolls by 16.

DATA INV4
DATA INV6
DATA INV5
DATA INV7
C ROLL3
Dual 2-1 Mux
D INV4-6
D INV5-7

DATA INV[4..7]

Muxes take care of rolls of 16.

DATA INV6
DATA INV4
DATA INV5
DATA INV7
D ROLL3
Dual 2-1 Mux
D INV6-4
D INV7-5

K013D08.XIL
K013D08.XIL
Counters XILINX logic

K013D11.XIL
K013D11.XIL

OldRollSel True for 125ns when we are going to back up thru a NF boundry.

OldInv6
Inv6
NewDinv6
RAM input
dDATA VAL CH6

OldInv7
Inv7
NewDinv7
RAM input
dDATA VAL CH7

RCO3

RESET3

See note above.

NEW FRAME\3

DLY 0
DLY 1
DLY 2
DLY 3
DLY 4
DLY 5
DLY 6

This is a pseudo randam counter that is to function similar to a 74269 counter.

The delay value/counter aligns the DATA INVALID bit with its correspondent data bits.

Data Invalid Delay Counters 3 & 4

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFROMATTER		
XILINX DATA INVALID DELAY & CONTROL		
Size: E	Document Number: 56000K013 (K013D05.BLK)	REV
Date: November 14, 1997	Sheet 5 of 12	

IN THE ORIGINAL PERSONALITY, INV[0..7] GO TO SHEETS 10 & 11

IN THE ALTERNATE PERSONALITY FOR MARK III / IV, INV[0..7] GO TO THE NEW LOGIC ON THIS SHEET, TO BE GATED BEFORE CONTINUING ON TO THE ORIGINAL DESTINATIONS.

GH → INV1, INV0 | GF → INV3, INV2 | GI → INV5, INV4 | HI → INV6, INV7

JE | JF | JG | JH

GA → DLY1, DLY0 | GC → DLY3, DLY2 | GE → DLY5, DLY4 | GG → DLY6

I/O SPARE3
TEST DRIVE x
P48
TP

JA | JB | JC | JD

dSDIN

68K_SD → P30 PAD → Q2 → Q1 → P29 PAD → Q2

Delay the Serial Data

68K_S_CLK4 → P57 PAD → Q2 → BCL KIN → ACLK.i → ACLK.o → SER CLK S

68K_S_CLK5 → P46 PAD → P45 PAD → I/O SPARE2

P35 PAD → I/O SPARE0

Test fixture use.

SERIAL PROGRAM WORD INPUT
AND SECONDARY STORAGE

68K_L_CLK4 → P56 PAD → Q2 → SER CLK L

SERIAL CONTROL REGISTER

THIS LOGIC IS THE NEW SUPPORT FOR THE ALTERNATE MK3CTRL.MCS PERSONALITY.

THE ORIGINAL INV[0..7] ARE ROUTED HERE AND GATED BEFORE CONTINUING ON TO SHEETS 10 AND 11.

NF3 → NEWFFT → ORIG INV6 → NEW INV6 | ORIG INV7 → NEW INV7

F = A + !A
FAKES A LOGIC 1
A MUST BE CONNECTED TO SOMETHING
SO CONNECTED TO NF0 ARBITRARILY

NF0 → FIRST TWO STAGES OF 3 BIT REG IN THIS CLB → NEWFFT

ORIG INV0 → NEW INV0 | ORIG INV1 → NEW INV1

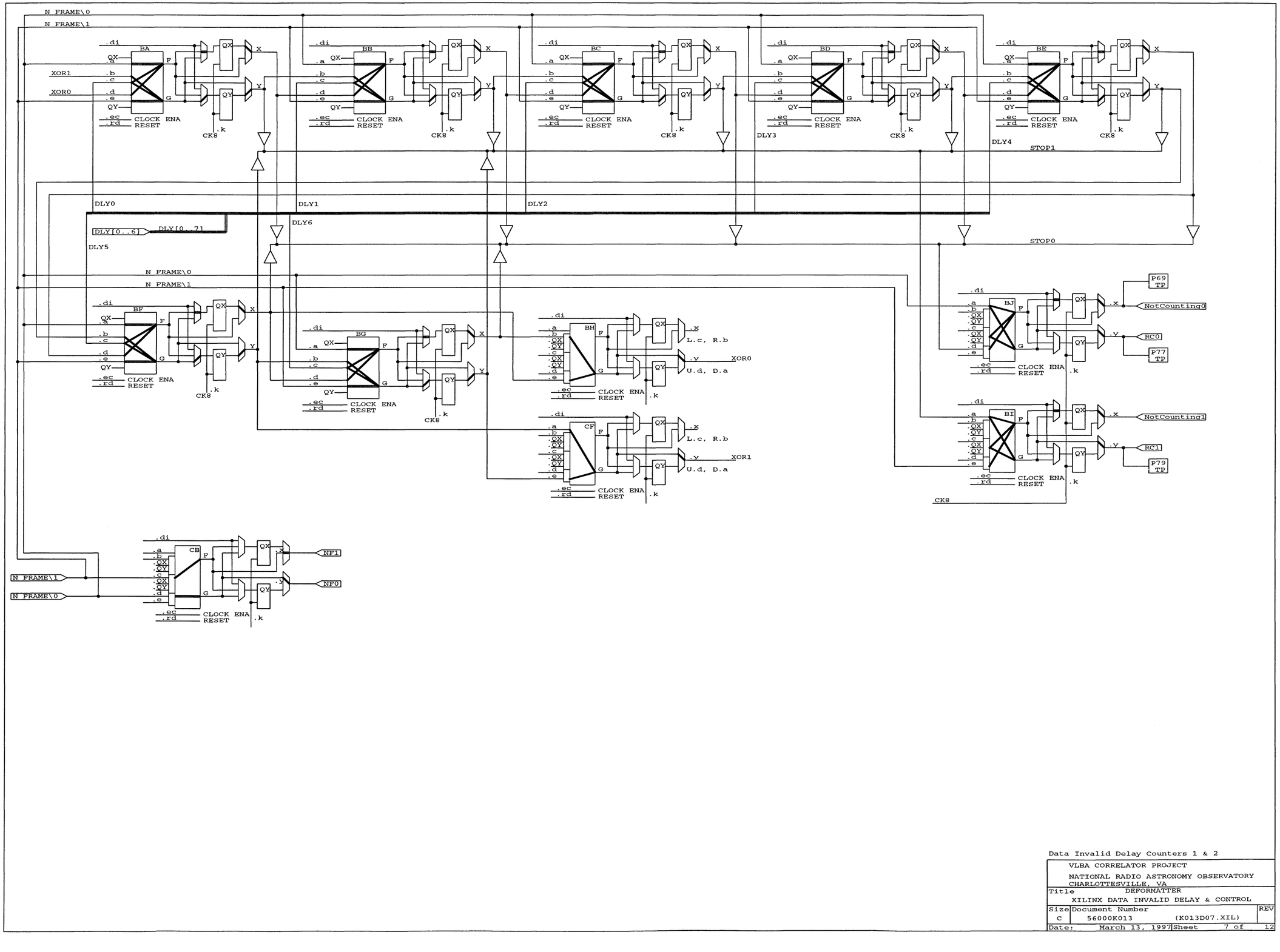
LAST STAGE OF 3 BIT REG IN THIS CLB FOLLOWED BY THE TWO NAND GATES

NF1 → NEWFFT → ORIG INV2 → NEW INV2 | ORIG INV3 → NEW INV3

NF2 → NEWFFT → ORIG INV4 → NEW INV4 | ORIG INV5 → NEW INV5

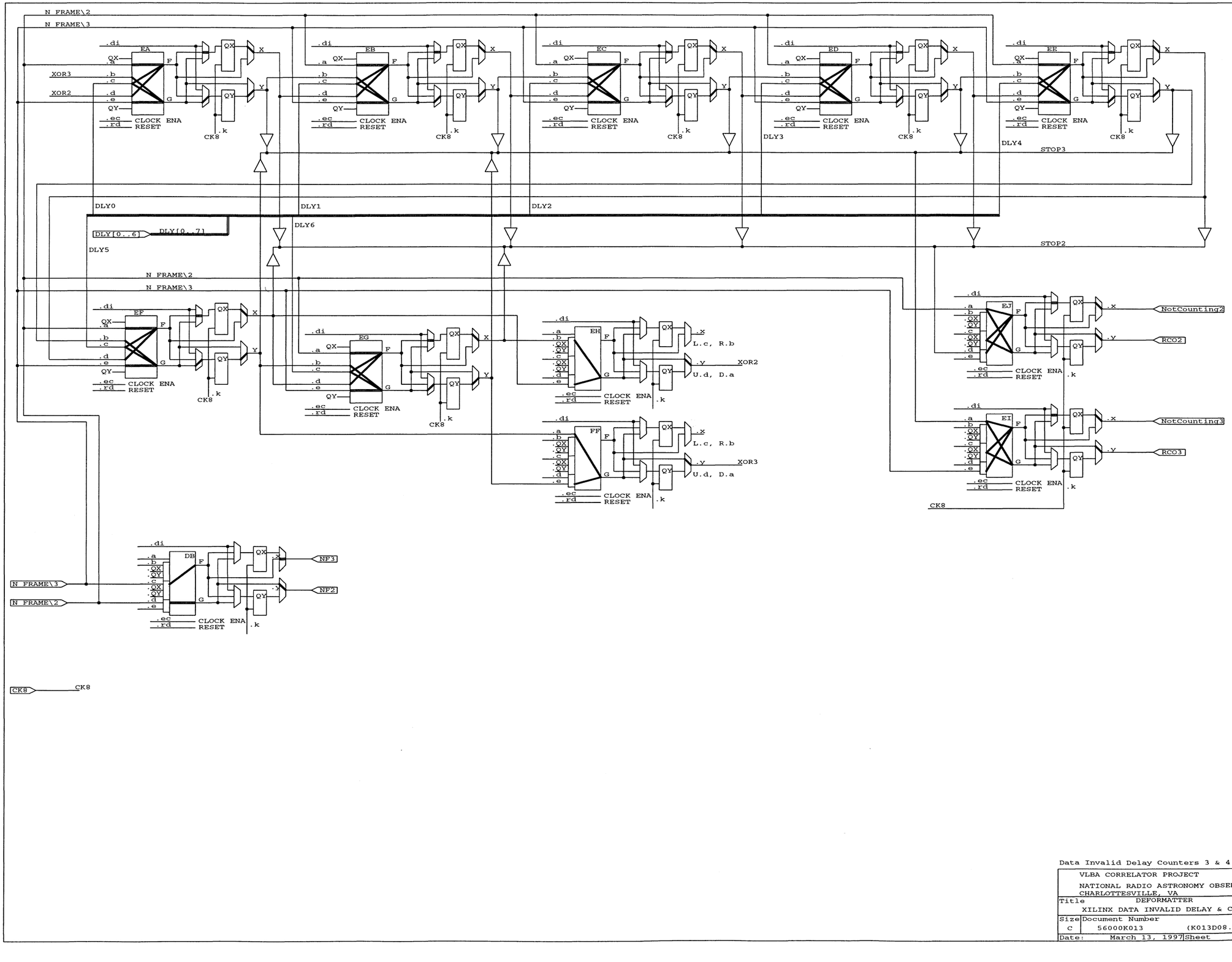
SOURCE OF NF[0..3] IS FROM THE INPUT PINS OF THE FOUR BUFFERED NF OUTPUTS ON SHEET 3

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: XILINX DATA INVALID DELAY & CONTROL		
Size: C	Document Number: 56000K013 (K013D06.XIL)	REV
Date: November 17, 1997	Sheet 6 of 12	



Data Invalid Delay Counters 1 & 2

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER XILINX DATA INVALID DELAY & CONTROL		
Size: C	Document Number: 56000K013 (K013D07.XIL)	REV
Date: March 13, 1997	Sheet 7 of 12	



Data Invalid Delay Counters 3 & 4

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DEFORMATTER XILINX DATA INVALID DELAY & CONTROL		
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Date: March 13, 1997	Sheet 8 of 12	

C X B
D Y A

SP5 IS SWAP\
COMES FROM ROLL XILINX;
(SPCL POLAR #2)

TR TEST CYCLE EN
c131msTIC_EN
131msTIC_EN

ROLL0 to 68k Sense input from TRC (VIA P37)
FROM ROLL XILINX oldRollSel3

A ROLL 3

P11 P10 P9 P8 P7 P6 P5 SP4 P4 P3 SP3 P2 SP2 P1 P84 P83 P82 P81 P80 P79 P78 P77 P76 P75 P74

SP5 bDATA INV2 DATA INV0 DATA INV1 TP rco1 TP rco0 bDATA INV0 bDATA INV1 PROG CLK

GCLK

CK81 — P13 P14

AA AB AC AD AE AF dDATA INV2 AG AH dDATA INV3 AI dDATA INV0 AJ dDATA INV1

DOUT TIO03 TP703 TIO02 TP702 DIN

NEW FRAME\0 — P15 U77

BA CNT0-0 CNT1-0 | BB CNT0-1 CNT1-1 | BC CNT0-2 CNT1-2 | BD CNT0-3 CNT1-3 | BE CNT0-4 CNT1-4 | BF CNT0-5 CNT1-5 | BG CNT0-6 CNT1-6 | BH XOR0 | BI RCO1 | BJ RCO0

TIO01 TP701 DATA INV3
TIO00 TP700 dDATA INV3

bNEW FRAME1 — P16 P17

CA CB CC CD CE CF XOR1 CG CH CI CJ

TIO05 TU205 TP609 TP TERM COUNT 0

USED IN ALTERNATE PERSONALITY (MK3CTRL.MCS

NEW FRAME\1 — P18
dDATA INV4 — P19

DA DB DC DD DE DF DG DH DI DJ

TIO08 TP608 B ROLL 3
TIO07 TP607 DATA INV2

bNEW FRAME0 — P20
NEW FRAME\2 — P21

EA CNT2-0 CNT3-0 | EB CNT2-1 CNT3-1 | EC CNT2-2 CNT3-2 | ED CNT2-3 CNT3-3 | EE CNT2-4 CNT3-4 | EF CNT2-5 CNT3-5 | EG CNT2-6 CNT3-6 | EH XOR2 | EI RCO3 | EJ RCO2

TIO06 TP606 C ROLL 3
TIO05 TP605 DATA INV4

USED IN ALTERNATE PERSONALITY (MK3CTRL.MCS

SP6 — P23
SP7 — P24

FA FB FC FD FE FF XOR3 FG FH FI dDATA INV4 FJ dDATA INV5

TIO03 TP603 DATA INV5
TIO02 TP602 dDATA INV5

NEW FRAME\3 — P25
bNEW FRAME2 — P26

GA DLY1 DLY0 | GB DLY3 DLY2 | GC DLY5 DLY4 | GD INV3 INV2 | GE DLY7 DLY6 | GF INV1 INV0 | GG INV5 INV4 | GH dDATA INV7 | GI dDATA INV6 | GJ

TIO01 TP601 D ROLL 3
TIO00 TP600 dDATA INV7

bNEW FRAME3 — P27 U65

HA HB HC HD HE HF HG HH INV7 INV6 HI dDATA INV6 HJ

TIO05 TU305 TP509 dDATA INV6

NEW FFT\ — P28 U63

IA IB IC ID IE IF IG IH II IJ

TIO07 TU307 TP508 DATA INV6

Delay the data in — P29 P30 bSD 68K SD

JA SR1 SR0 | JB SR3 SR2 | JC SR5 SR4 | JD SR7 SR6 | JE SR9 SR8 | JF SR11 SR10 | JG SR13 SR12 | JH SR15 SR14 | JI | JJ

TIO04 TP504 68K S CLK4
TIO06 TP506 68K L CLK4
ACLK

M1 P31 M0 P32 M2 P33 P34 SP8 | P35 I/O SP0 P36 SP9 | P37 I/O SP1 P38 | P39 SP10 P40 bNF EN\ out | P41 NF EN\ in P42 FFT TEST CYCLE | P44 TEST POINT 18 P45 I/O SP2 | P46 68K SPARE S-CLK5 P47 G RA NEW FRINGE | P48 TEST DRIVE x I/O SP3 P49 DATA INV7 | P50 P51 | P52 G RA NEW DELAY P53 | P54 RST\ P55 DN/PG

ROLL0 signal from TRC

Used in PBI TEST FIXTURE as source of DELAY WORD (SD DLY Mx)

Used in PBI TEST FIXTURE as source of DELAY CLK (SC DLY Mx)

To PBD via MUX CARD

VCC 22,64
GND 1,43

DATA INVALID XILINX
Filename = K013D09.XIL
C SIZE SHEET 9 OF 12

2-1 Muxes

Capture Validity

Old Validity Assertion

DATA INV0 — P82 PAD — Q2 — .q DATA INV0
DATA INV1 — P81 PAD — Q2 — .q DATA INV1
DATA INV2 — P67 PAD — Q2 — .q DATA INV2
DATA INV3 — P71 PAD — Q2 — .q DATA INV3
CK8 — CK8

DATA INV0 / DATA INV2 — AD — DInv0-2 / DInv2-0
DATA INV1 / DATA INV3 — AE — DInv1-3 / DInv3-1
NewDInv0 / NewDInv1 — CD — OI0 / OI1 — NF0
NewDInv2 / NewDInv3 — CE — OI2 / OI3 — NF1
Reset0 — CG — OldInv0 / OldInv1
Reset1 — CH — OldInv2 / OldInv3

CLOCK ENA, RESET

A ROLL3 — P84 PAD — Q2
B ROLL3 — P68 PAD — Q2

SPECIAL POLAR MODE #2
SWAP\ to sheet 11
swap\ — P11 PAD — Q2

OldRollSel
RCO0
NotCountint0 — CJ — Reset0 — N FRAME\0
NotCountint1 — CI — Reset1 — N FRAME\1
RCO2

Inv0 / OldInv0 — AI — NewDInv0
Inv1 / OldInv1 — AJ — NewDInv1
Inv2 / OldInv2 — AF — NewDInv2
Inv3 / OldInv3 — AH — NewDInv3

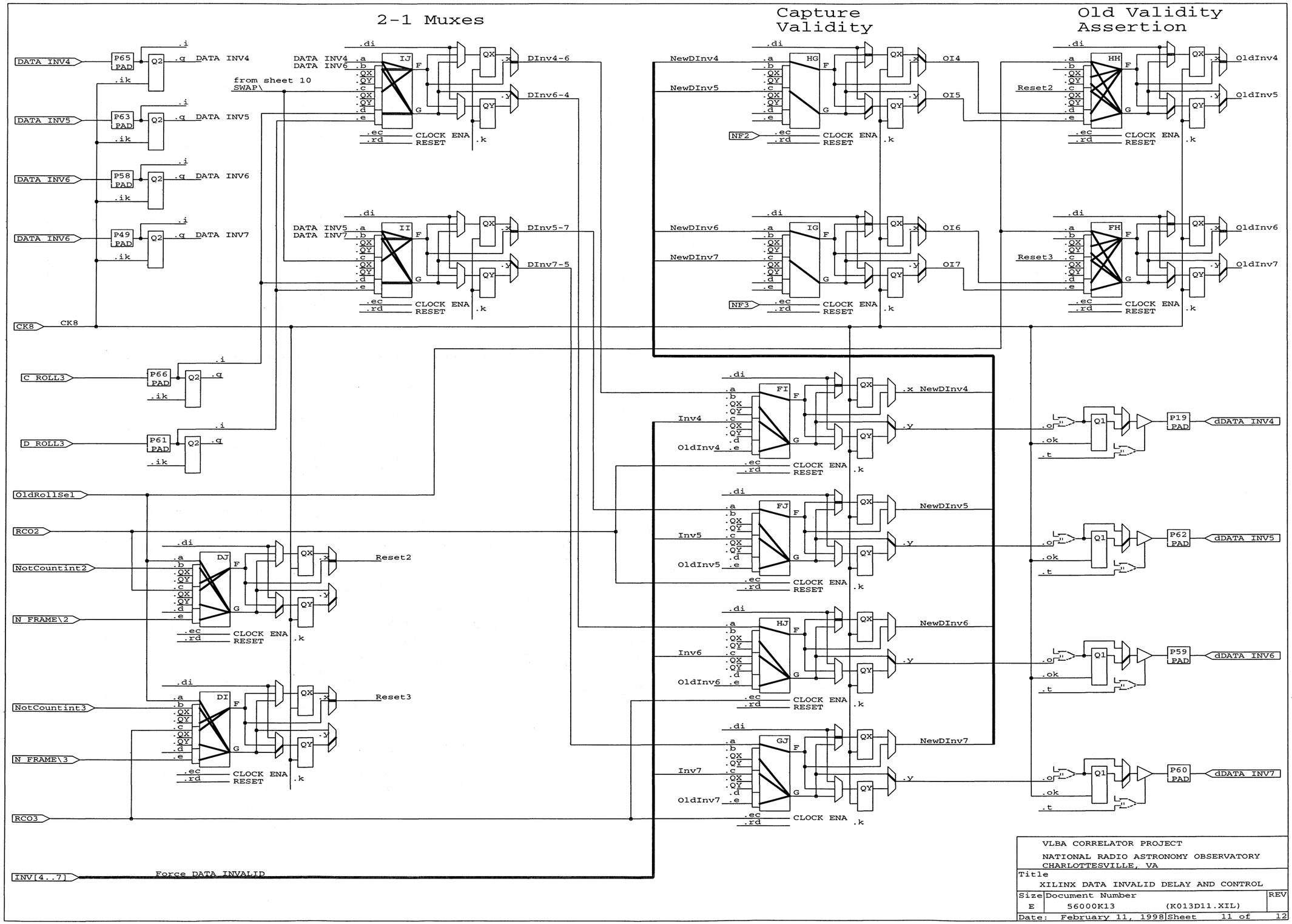
NewDInv0 — Q1 — P76 PAD — dDATA INV0
NewDInv1 — Q1 — P75 PAD — dDATA INV1
NewDInv2 — Q1 — P83 PAD — dDATA INV2
NewDInv3 — Q1 — P70 PAD — dDATA INV3

INV[0..3] — Force DATA INVALID

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: XILINX DATA INVALID DELAY AND CONTROL

Size	Document Number	REV
E	56000K13 (K013D10.XIL)	
Date: February 11, 1998	Sheet 10 of 12	



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NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
XILINX DATA INVALID DELAY AND CONTROL

Size	Document Number	REV
E	56000K13 (K013D11.XIL)	

Date: February 11, 1998 Sheet 11 of 12

TEST_CYCLE_EN

CK8

D
C

cTEST_CYCLE_EN

TR_TEST_CYCLE_EN

To Track Recovery logic

TEST CYCLE EN capture logic

PUn

68K SD

68K S CLK n

68K L CLK n

U?

74LS594

SER, SRCLK, SRCLR, RCLK, RCLR, QA, QB, QC, QD, QE, QF, QG, QH, QH'

DLY 0, DLY 1, DLY 2, DLY 3, DLY 4

To each of the
4 delay counters.

Delay value depends upon mode.

Common logic block

To each of the other 3 logic blocks

68K can selectively force DATA INVALID on a channel basis.
(e.g. high # of cross track parity errors)

bNEW_FRAME\[0..3]

A ROLL 3
B ROLL 3
C ROLL 3
D ROLL 3

A ROLL 3
B ROLL 3
C ROLL 3
D ROLL 3

NOTE:
Roll by 16 legal combinations -
tracks 0 thru 15 and 16 thru 31.

NEW_FRAME\[0..3]

NEW_FRAME\[0..3]

DATA INV [0..7]

DATA INV [0..7]

CK8n

CK8

One of 4 identical logic blocks.

A ROLL 3

ROLL 3 takes care of 16 bit rolls.

Rolls <16 are taken care of on the
track recovery board.

DATA INVALID n+2
16 bit roll
DATA INVALID n

DATA INVALID n+3
16 bit roll
DATA INVALID n+1

D
C

RAM input

dDATA INV CHn

dDATA INV CHn+1

CK8\

NEW FRAME\ n

U?

74F269

PE, TC, D7, D6, D5, D4, D3, D2, D1, D0, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0

DLY 4
DLY 3
DLY 2
DLY 1
DLY 0

U/D, CLK, CET, CEP

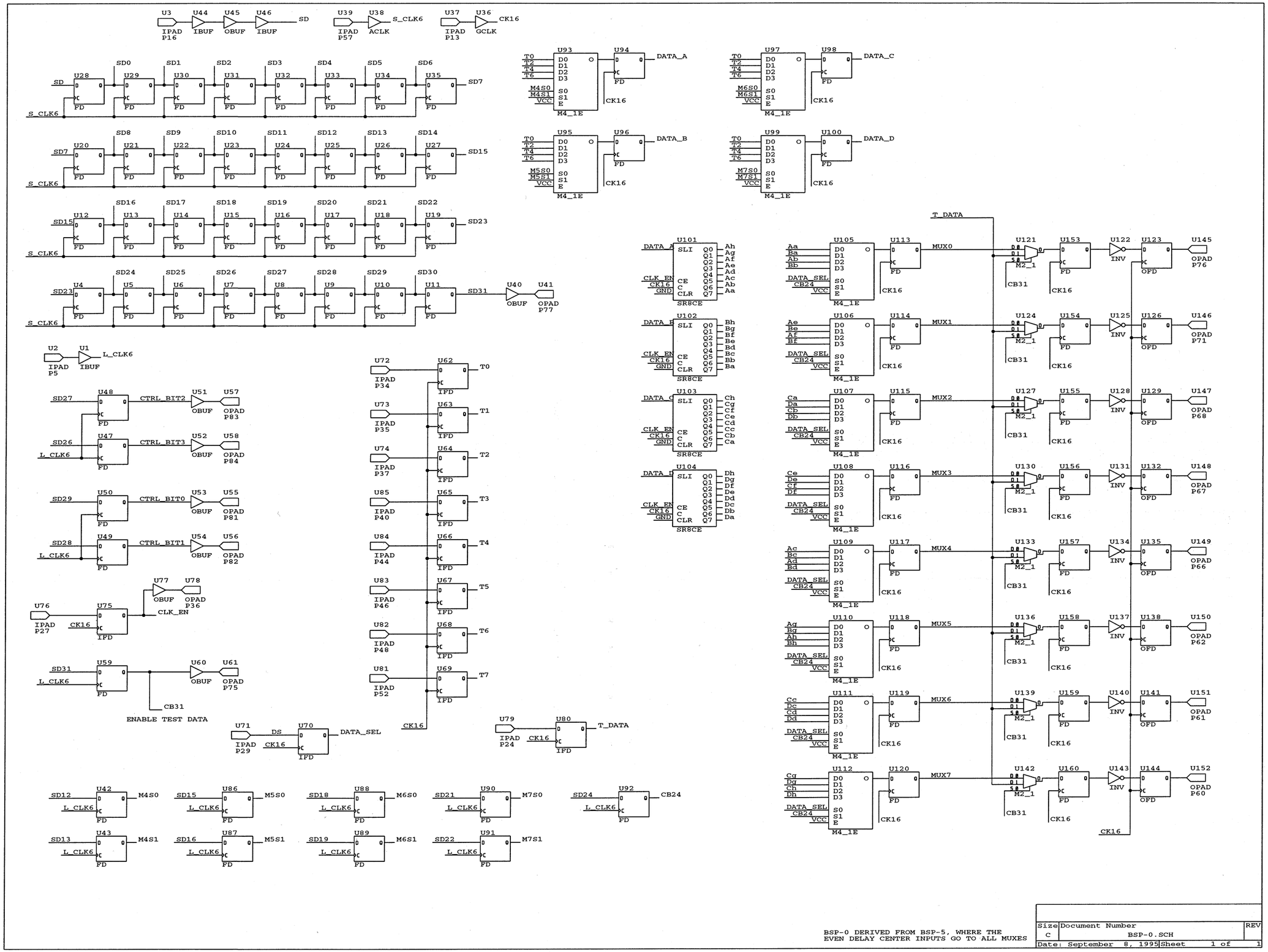
CK8

Delay counter aligns the DATA INVALID bit with the data bits.

VLBA CORRELATOR PROJECT

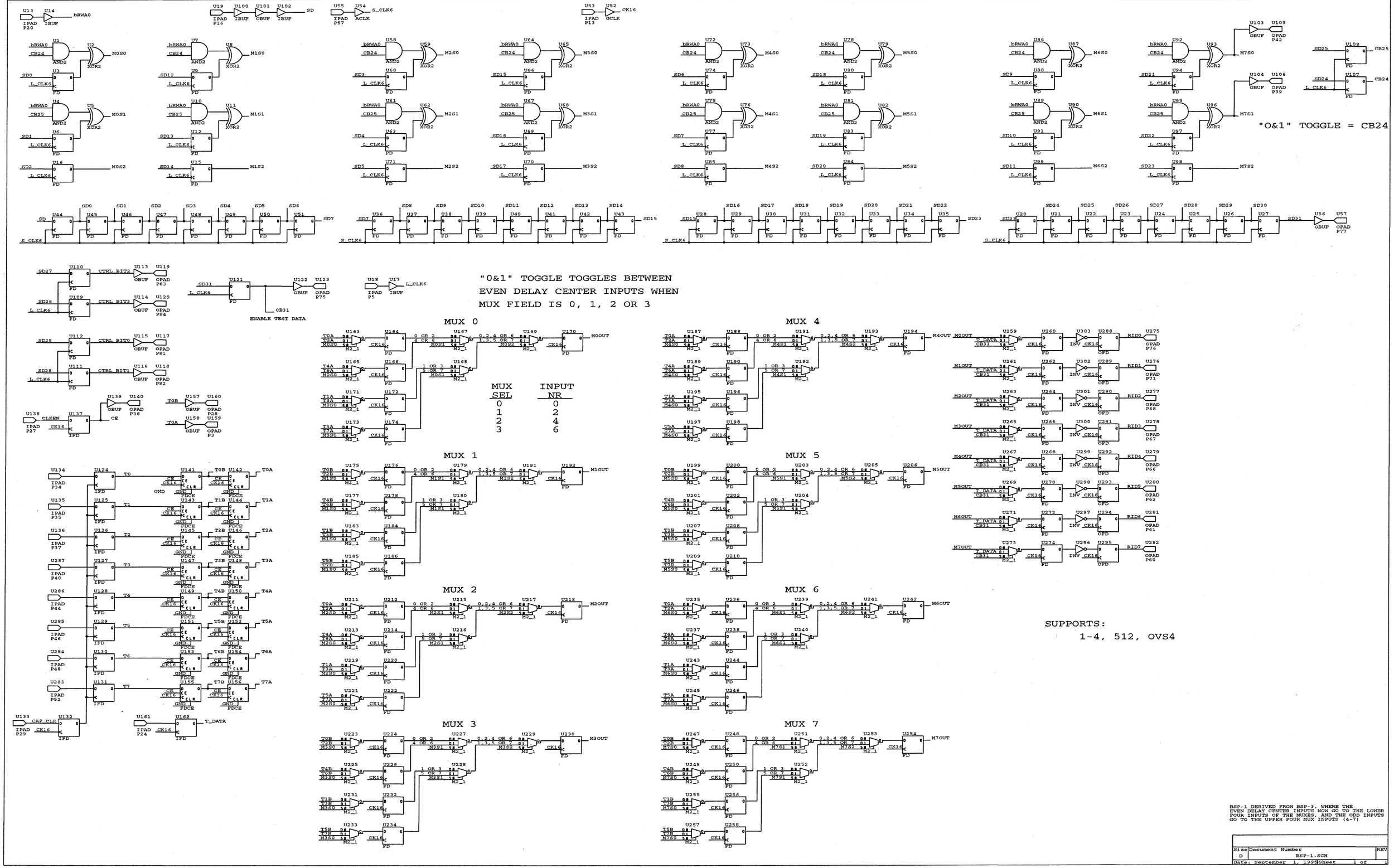
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title		
DATA INVALID DELAY		
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BSP-0 DERIVED FROM BSP-5, WHERE THE EVEN DELAY CENTER INPUTS GO TO ALL MUXES

Size	Document Number	REV
C	BSP-0.SCH	
Date: September 8, 1995	Sheet 1 of 1	


"0&1" TOGGLE = CB24
"0&1" TOGGLE TOGGLES BETWEEN
EVEN DELAY CENTER INPUTS WHEN
MUX FIELD IS 0, 1, 2 OR 3
ENABLE TEST DATA
MUX 0
MUX 1
MUX 2
MUX 3
MUX 4
MUX 5
MUX 6
MUX 7
MUX SEL
INPUT NR
0 0
1 2
2 4
3 6
SUPPORTS:
1-4, 512, OVS4
BSP-1 DERIVED FROM BSP-3, WHERE THE EVEN DELAY CENTER INPUTS NOW GO TO THE LOWER FOUR INPUTS OF THE MUXES, AND THE ODD INPUTS GO TO THE UPPER FOUR MUX INPUTS (4-7)
Size D
Document Number BSP-1.SCH
REV
Date: September 1, 1995
Sheet 1 of 1

K006D02.X02 — Shift Reg Ctrl Bits 0-5

CB24, CB25 → SEL A0, SEL A1, SEL A2

68K_SD (P16), 68K_S_CLK (P57), 68K_L_CLK (P5) → SER DATA IN → CONTROL WORD → SER DATA OUT

RWA0 (P20) Not Used

DataSel → SEL B0, SEL B1, SEL B2

CONTROL WORD → SER DATA OUT

BSP2X02.SCH

K006D11.X11 — I/O BLOCKS

P34 T0\, P35 T1\, P37 T2\, P40 T3\, P44 T4\, P46 T5\, P48 T6\, P52 T7\ → REG → T0, T1, T2, T3, T4, T5, T6, T7

P29 CapClk

P27 DataSel

BSP2X11.SCH

K006D02.X03 — Shift Reg Ctrl Bits 6-11

CB24, CB25

DataSel

SER DATA IN (68K S CLK, 68K L CLK)

SER DATA OUT

BSP2X03.SCH

K006D02.X04 — Shift Reg Ctrl bits 12-17

CB24, CB25

DataSel

SER DATA IN (68K S CLK, 68K L CLK)

SER DATA OUT

BSP2X04.SCH

K006D02.X05 — Shift Reg Ctrl Bits 18-23

CB24, CB25 → SEL A0, SEL A1, SEL A2

SER DATA IN → CONTROL WORD → SER DATA OUT

DataSel → SEL B0, SEL B1, SEL B2

CONTROL WORD → SER DATA OUT

BSP2X05.SCH

K006D02.X06 — Shift Reg Ctrl Bits 24-31

SER DATA IN (68K S CLK, 68K L CLK)

CB24, CB25, CTRL BIT3, CTRL BIT2, CTRL BIT1, CTRL BIT0, CB30 not used, CB31

SER DATA OUT → 68K SD+n P77

BSP2X06.SCH

K006D02.X07 — 8 - 1 MUX 0 (T0–T7) → RID0

K006D02.X08 — 8 - 1 MUX 1 (T0–T7) → RID1

BSP2X07.SCH

K006D02.X08 — 8 - 1 MUX 2 (T0–T7) → RID2

K006D02.X08 — 8 - 1 MUX 3 (T0–T7) → RID3

BSP2X08.SCH

K006D02.X09 — 8 - 1 MUX 4 (T0–T7) → RID4

K006D02.X09 — 8 - 1 MUX 5 (T0–T7) → RID5

BSP2X09.SCH

K006D02.X10 — 8 - 1 MUX 6 (T0–T7) → RID6

K006D02.X10 — 8 - 1 MUX 7 (T0–T7) → RID7

BSP2X10.SCH

RID0 → P76 RAM

RID1 → P71 RAM

RID2 → P68 RAM

RID3 → P67 RAM

RID4 → P66 RAM

RID5 → P62 RAM

RID6 → P61 RAM

RID7 → P60 RAM

MUX → SIGN, MAG → FFT ENGINE

TEST DATA P24

K006D02.X01 — BSP2X01.SCH — Floor Plan

BSP-2-WD.TBL (IN HCB PROTOCOL) — Ctrl word format

MODES:

1:4 — N1-4E.TIM; N1-4E.TIM, V1-4E.TIM; V1-4E.TIM, N1-4F.TIM; N1-4F.TIM, N1-4G.TIM; N1-4G.TIM

1:2 — N1-2E.TIM; N1-2E.TIM, N1-2F.TIM; N1-2F.TIM, N1-2G.TIM; N1-2G.TIM

1:1 — N1-1F.TIM; N1-1F.TIM

SHEET NAMES ARE THE ORIGINAL FILE NAMES

FILE NAMES WERE CHANGED SO THAT PREFIXES ARE ALL DISTINCT

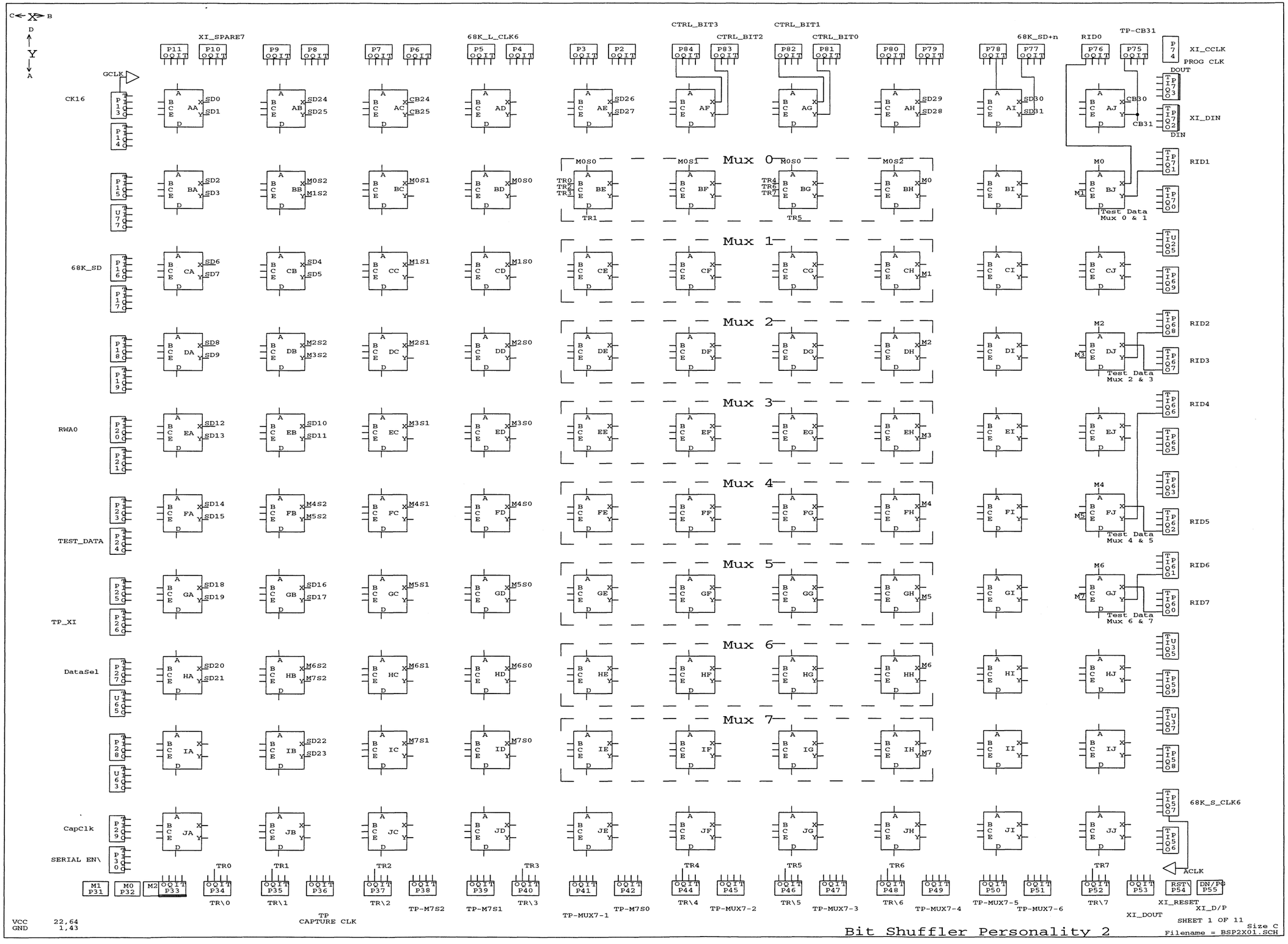
VLBA CORRELATOR PROJECT

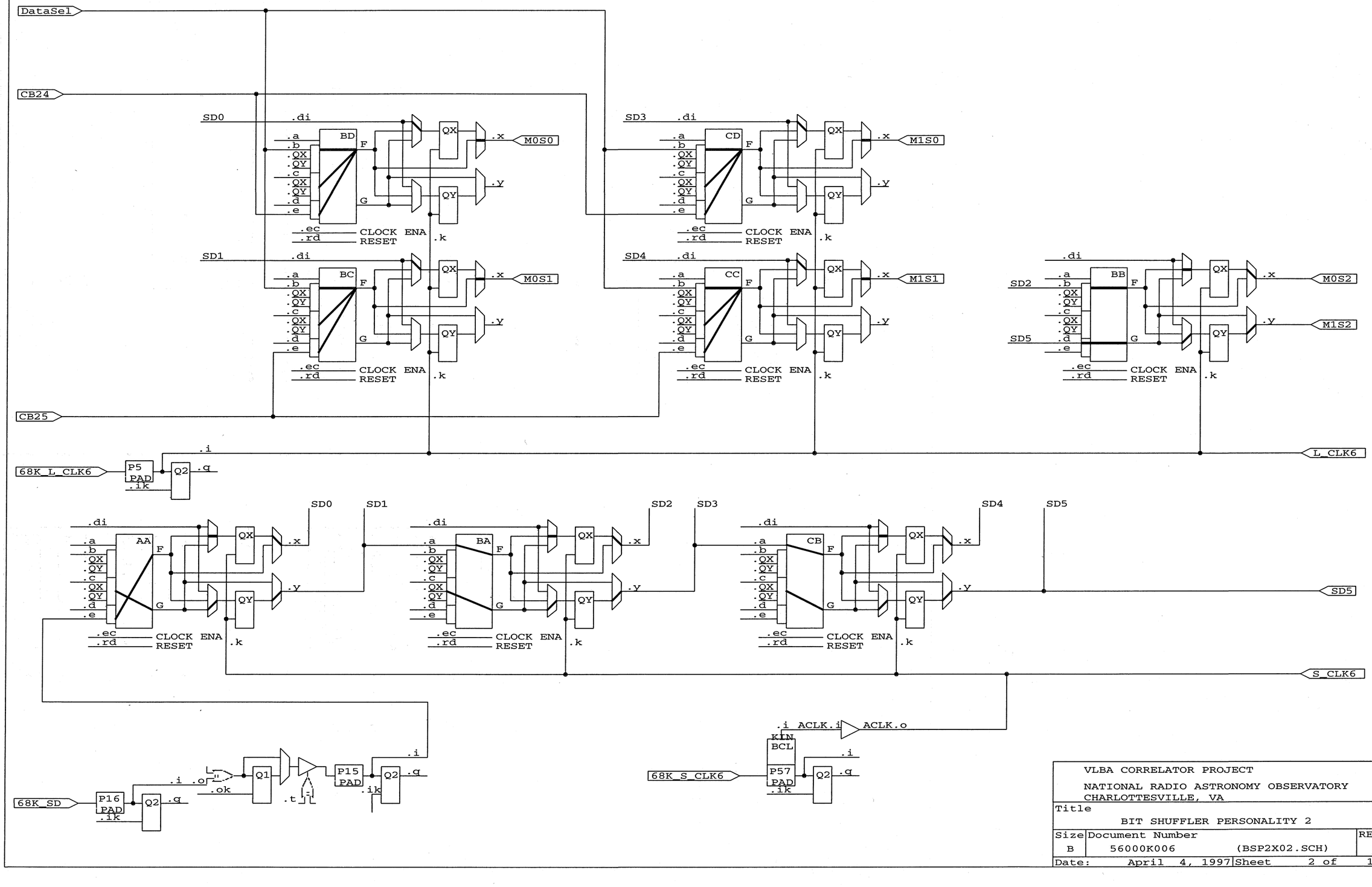
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: BIT SHUFFLER PERSONALITY 2

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E	13400K006 (BSP2BLK.SCH)	

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C B D Y A
XI_SPARE7
68K_L_CLK6
CTRL_BIT3
CTRL_BIT2
CTRL_BIT1
CTRL_BIT0
68K_SD+n
RID0
TP-CB31
XI_CCLK
PROG CLK
DOUT
XI_DIN
DIN
GCLK
CK16
68K_SD
RWA0
TEST_DATA
TP_XI
DataSel
CapClk
SERIAL EN\
Mux 0
Mux 1
Mux 2
Mux 3
Mux 4
Mux 5
Mux 6
Mux 7
RID1
RID2
RID3
RID4
RID5
RID6
RID7
Test Data Mux 0 & 1
Test Data Mux 2 & 3
Test Data Mux 4 & 5
Test Data Mux 6 & 7
68K_S_CLK6
ACLK
XI_RESET
XI_D/P
XI_DOUT
TP CAPTURE CLK
TP-M7S2
TP-M7S1
TP-MUX7-1
TP-M7S0
TP-MUX7-2
TP-MUX7-3
TP-MUX7-4
TP-MUX7-5
TP-MUX7-6
TR\0
TR\1
TR\2
TR\3
TR\4
TR\5
TR\6
TR\7
VCC 22,64
GND 1,43
Bit Shuffler Personality 2
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DataSel

CB24

CB25

L_CLK6

S_CLK6

SD5

SD6 .di — DD — F → QX → .x → M2S0; G → QY → .y

SD7 .di — DC — F → QX → .x → M2S1; G → QY → .y

SD9 .di — ED — F → QX → .x → M3S0; G → QY → .y

SD10 .di — EC — F → QX → .x → M3S1; G → QY → .y

SD8 .di — DB — F → QX → .x → M2S2; G → QY → .y → M3S2

SD11

CA: .di, .a, .b, .QX, .QY, .c, .QX, .QY, .d, .e; F, G; QX, QY; .x, .y; .ec CLOCK ENA; .rd RESET; .k

DA: .di, .a, .b, .QX, .QY, .c, .QX, .QY, .d, .e; F, G; QX, QY; .x, .y; .ec CLOCK ENA; .rd RESET; .k

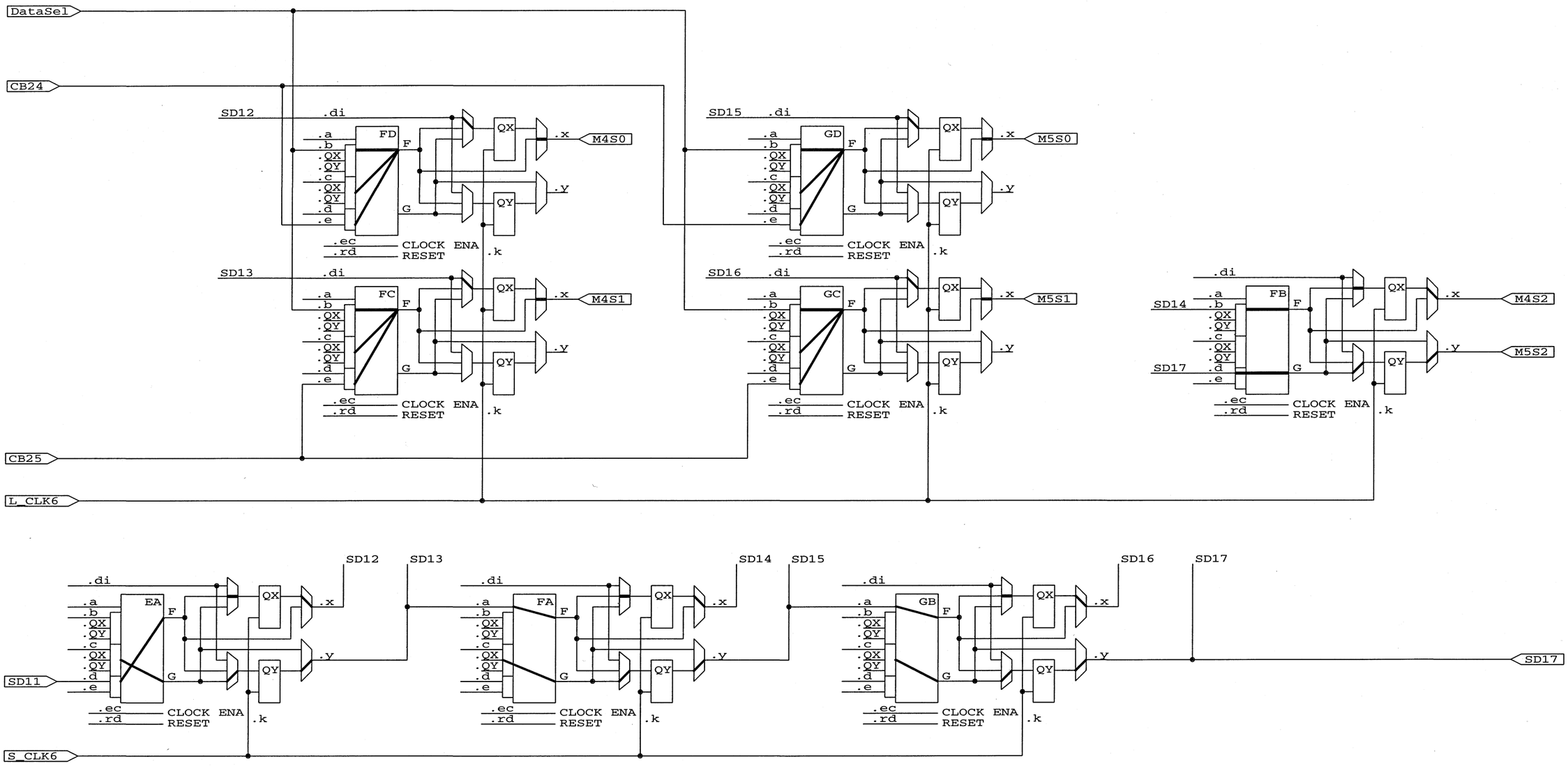
EB: .di, .a, .b, .QX, .QY, .c, .QX, .QY, .d, .e; F, G; QX, QY; .x, .y; .ec CLOCK ENA; .rd RESET; .k

SD6 SD7 SD8 SD9 SD10 SD11

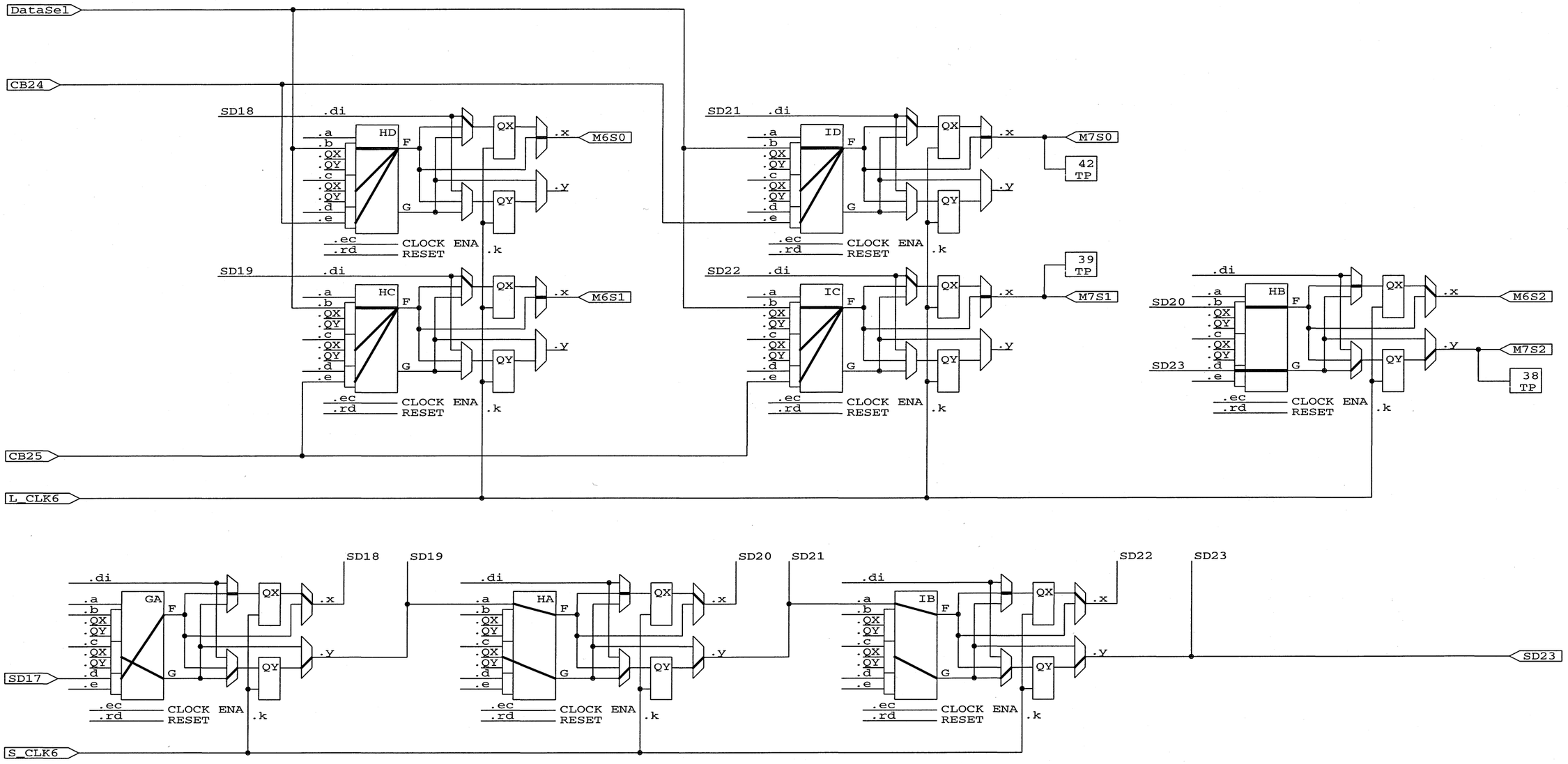
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

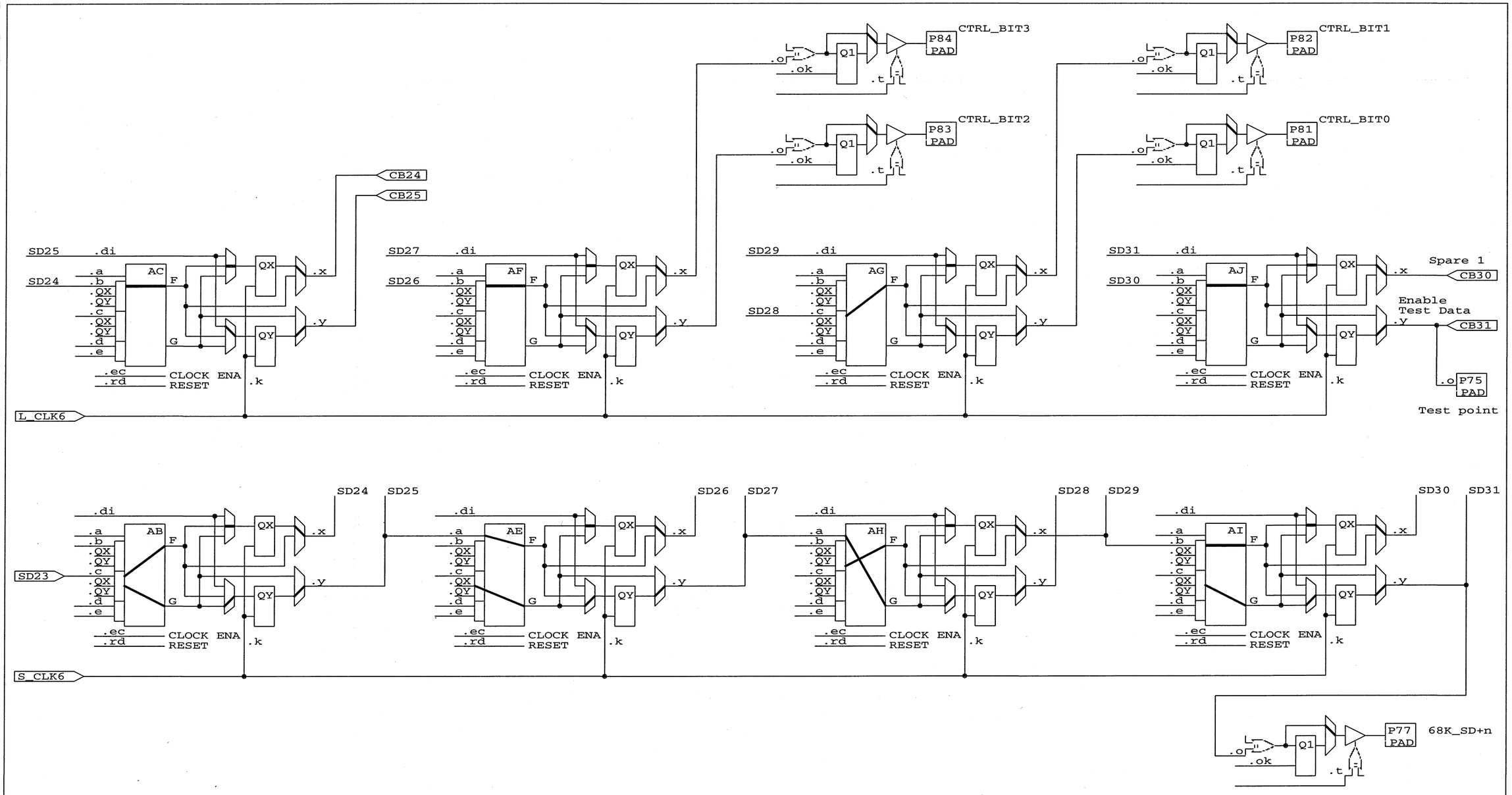
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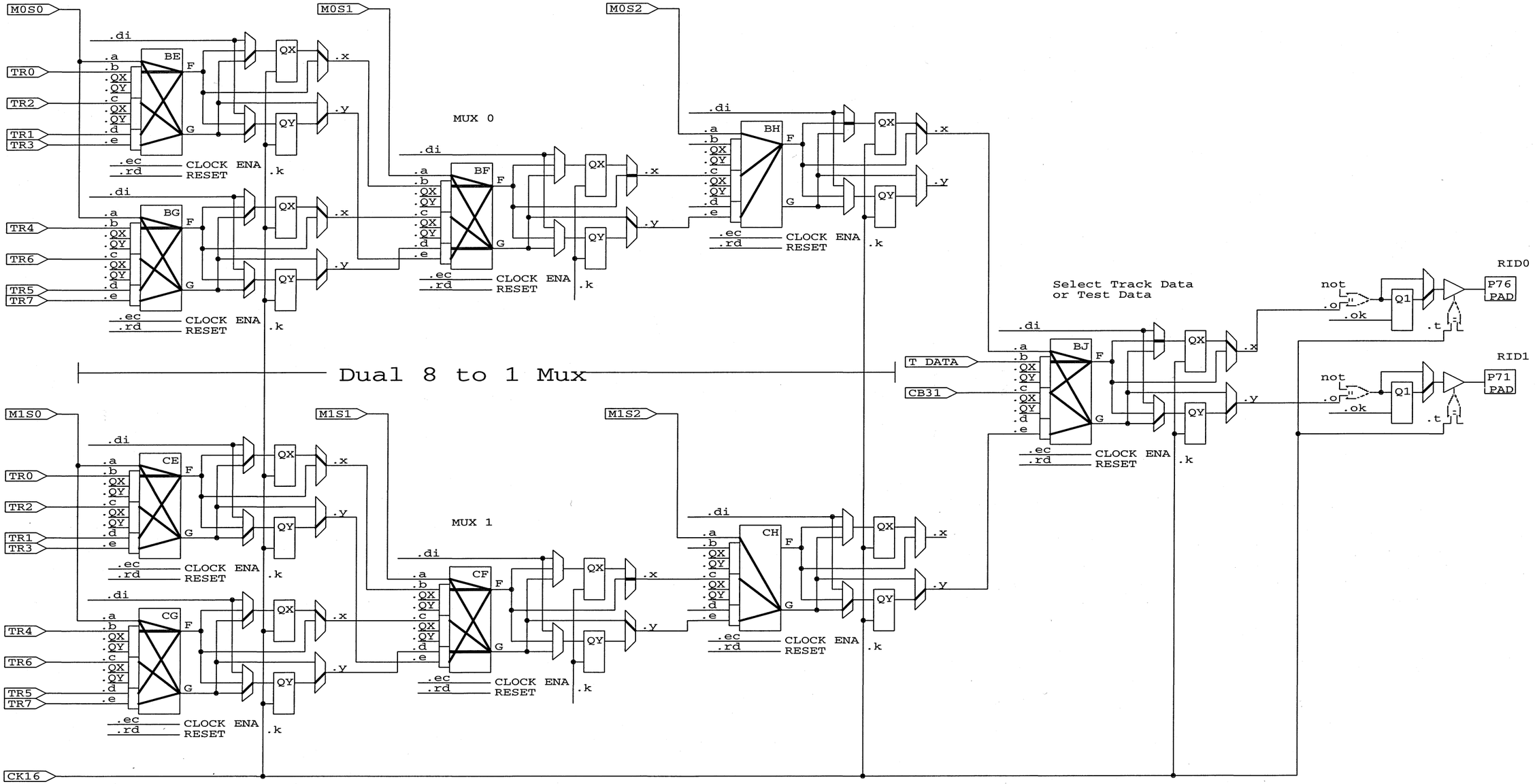
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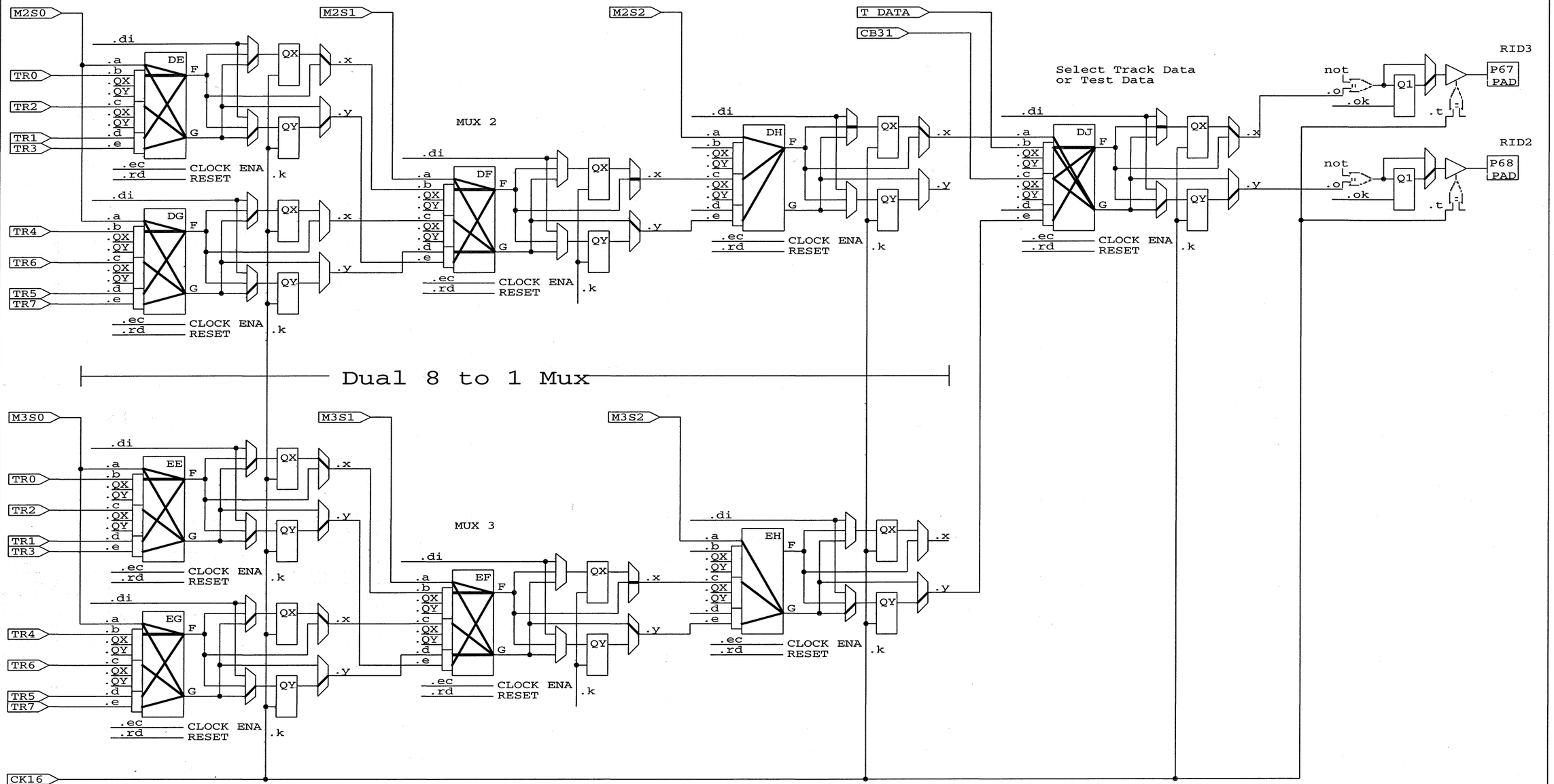
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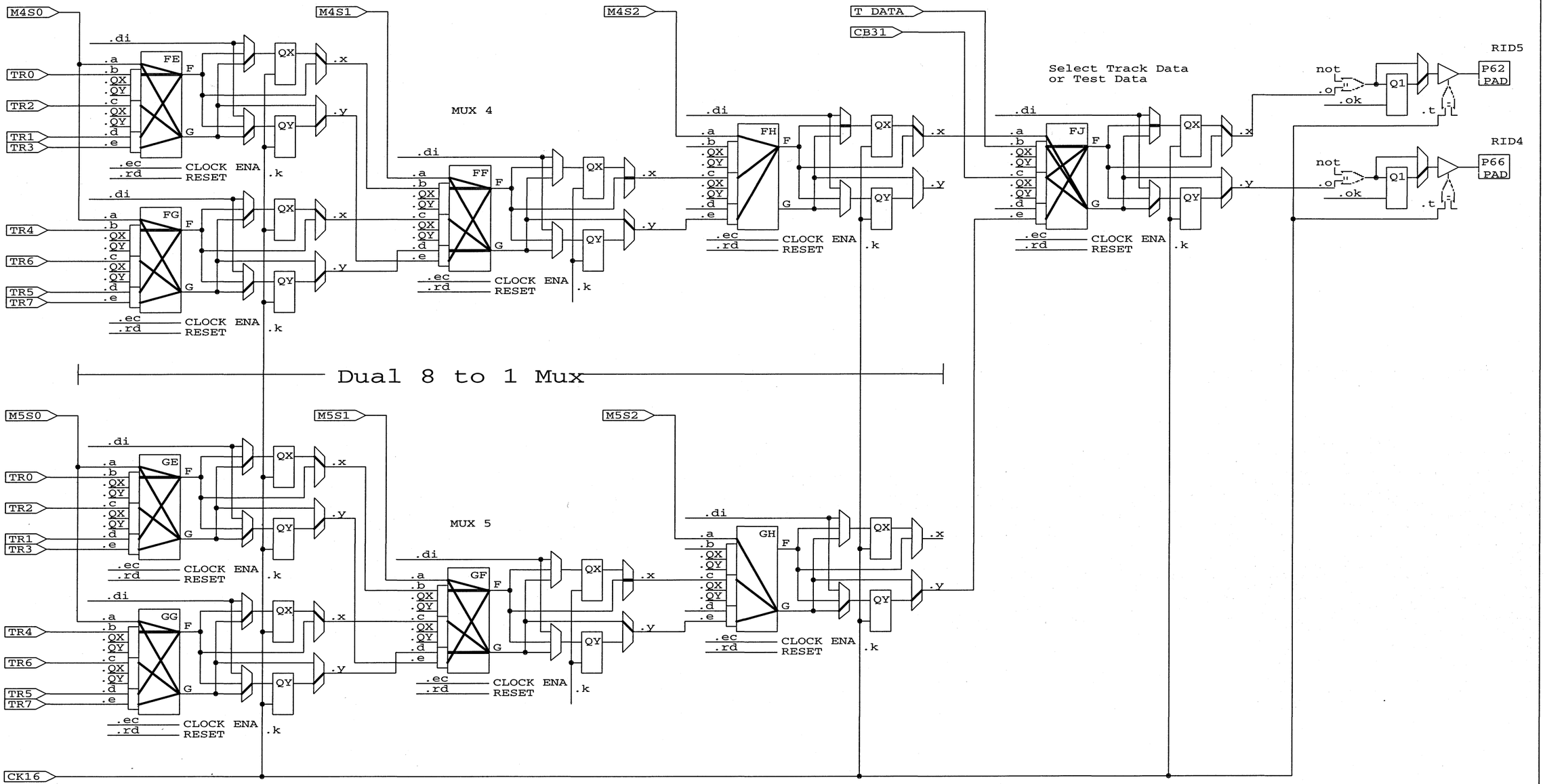


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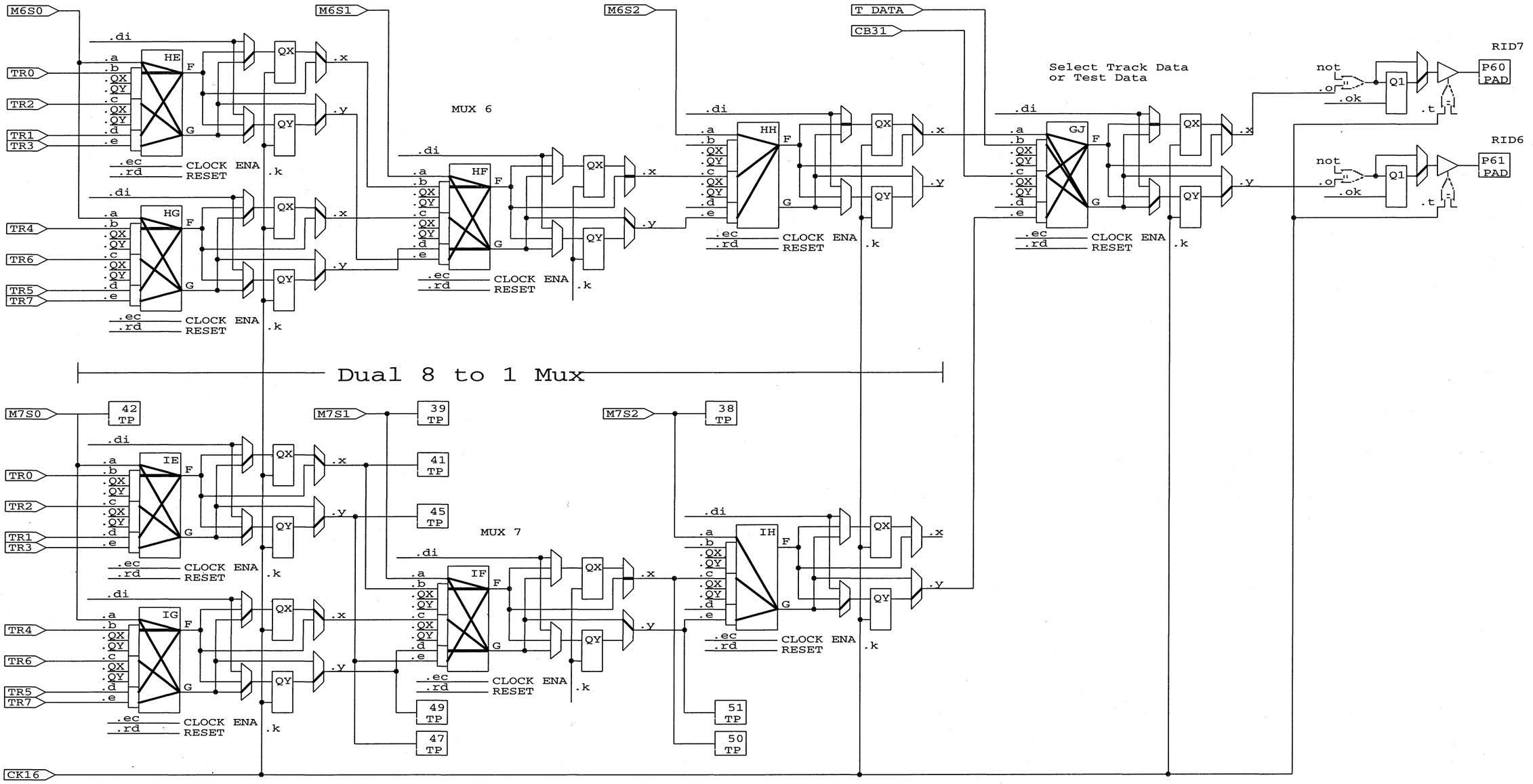
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

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BIT SHUFFLER PERSONALITY 2

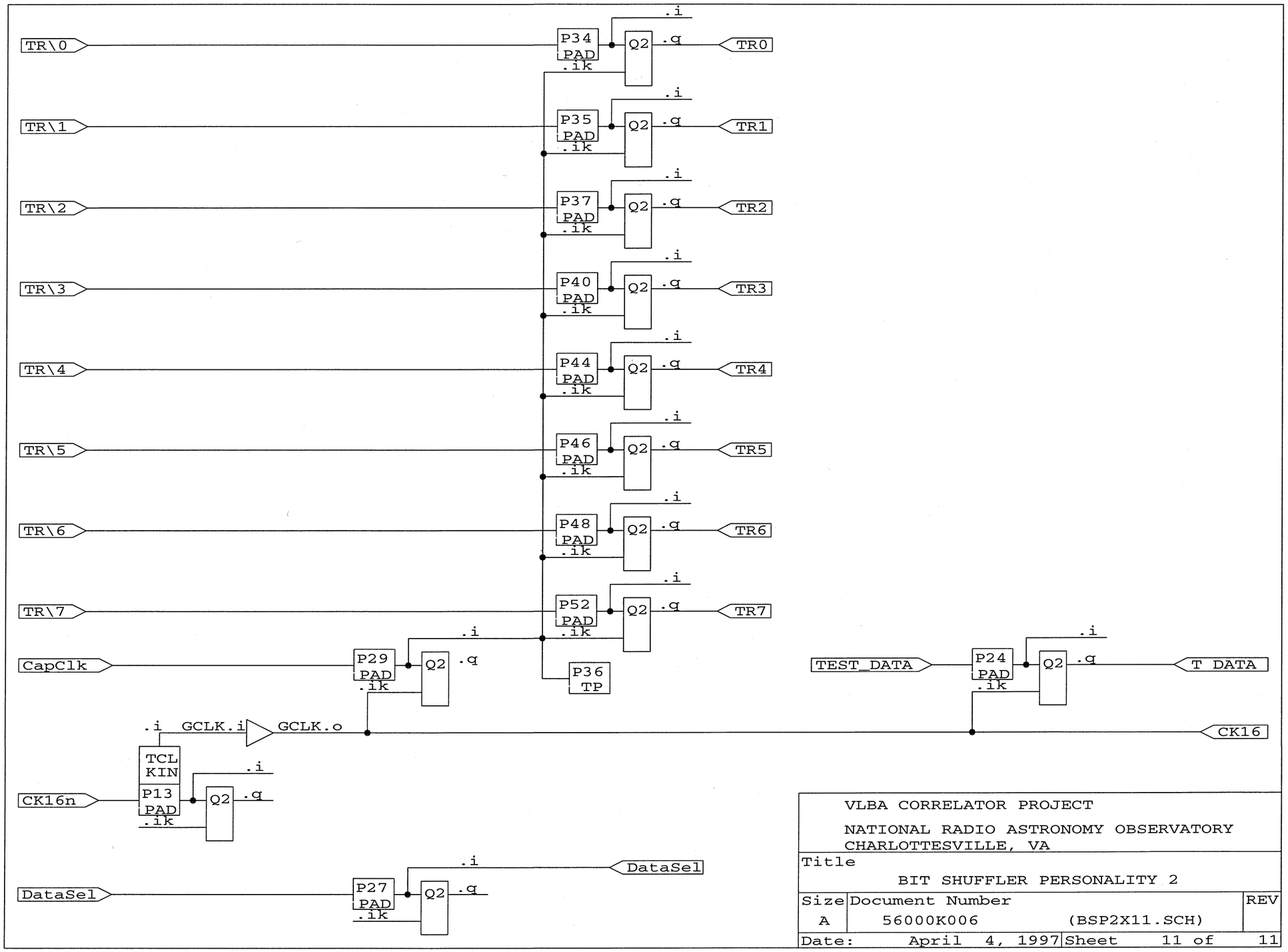
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