# VLBA Sensitivity Memo No. 35

# TEST FOR DBE FREQUENCY SYNTHESIZER BOARD

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Revision A

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The DBE Frequency Synthesizer Board has three main functions. They are the following:

- Create a 1024 MHZ clock for the Digitizer.
- Create a 20 ms wide 1PPS for the Roach Board.
- Control attenuators and switches on the ALC Board.

The following steps must be performed before the test can be done:

- Program the FPGA (chip U2) with the latest version of Synthesizer Board Firmware.
- Connect a cable between connectors J11 and J7 (or J8, J9, or J10).
- Connect a 5 MHZ sine wave to connector J1 at a level of 0 dBm.
- Connect 1PPS to connector J2. The pulse should be 400 mV high into 50 ohms. The pulse width should be at least 10 micro seconds.
- Connect the power to connector P4 and power on the board.

The last test, CHECK SPI COMMUNICATIONS TO THE SYNTHESIZER BOARD, can only be implemented if the user has a method of controlling the Synthesizer Board with another computer. This document does not cover how to accomplish this. If there is not a way to control the Synthesizer Board on the bench, then this part of the test will have to wait until the board is installed in an RDBE module with all of the necessary software to do this test.

The board must be oriented such that connector P6, the DB-25 connector, is on the right end of the board so that the descriptions below are correct.

## CHECK VARIOUS VOLTAGES ON THE BOARD

Any of the mounting holes on the board, as well as test points TP3 and TP5 may be used as a ground reference.

A. Check fuse F2 for +5 volts.
B. Check fuse F1 for +12 volts.
C. Check the right side of R40 for +7.5 volts.
D. Check the bottom side of C56 for +3.3 volts.
E. Check the left side of C3 for +3.0 volts.
F. Check the left side of C4for +1.2 volts.

## CHECK VARIOUS VOLTAGES AROUND THE SYNTHESIZER CHIP U1

The Synthesizer Chip, U1, has several regulators inside of it, whose voltages come out to some of the capacitors that surround the chip. The voltages on these capacitors should be between 2 and 3 volts, on the side of the capacitor that is closest to the chip. These exact voltages vary from one board to another. If the voltages are too low, it is possible that solder may be shorting pins together underneath the chip. It is also possible that a lack of solder is causing pins not to be connected to the board at all. The following capacitors should be checked:

A. C23 (Top Side)
B. C22 (Top Side)
C. C20 (Top Side)
D. C7 (Top Side)
E. C26 (Bottom Side)
F. C30 (Bottom Side)
G. C21 (Bottom Side)
H. C29 (Bottom Side)
I. C27 (Bottom Side)
J. C31 should be between 0 and 1.5 volts (Bottom Side)

## CHECK FOR THE 1024 MHZ CLOCK

The 1024 MHZ clock should come out of connectors J7, J8, J9, and J10 at a level of about +3 dBm.

## CHECK FOR THE DIVIDED DOWN CLOCK

Chip U10 (SY89871) divides the 1024 MHZ clock by 4. The output of this chip is differential, at LVPECL levels. This clock can be seen with an oscilloscope on the right side of resistors R22 and R23, and on the left side of resistors R24 and R25. This clock must be present in order for the 20 ms wide 1PPS pulse to be produced.

## CHECK FOR THE STATION 1PPS

The station 1PPS should be present at test point TP6 at LVTTL levels. The station 1PPS is sent to TP6 by the FPGA.

## CHECK FOR THE DELAYED 1PPS

The FPGA creates a 1PPS that starts about 20 ns after the rising edge of the station 1PPS. It is also a positive pulse, and is 20 ms in width. This pulse should be present at LVPECL levels on connectors J3, J4, J5, and J6. It is also present at LVTTL levels on pin 7 of connector P7 (this is the bottom left pin of the connector). If this pulse is present, and is delayed from the station 1PPS by about 20 ns, then all of the functions already checked on the board to this point are almost surely working properly.

## CHECK POWER-UP DEFAULT SETTINGS SENT TO THE ALC BOARD

At power-up, the Synthesizer Board sends default settings to the switches and attenuators on the ALC Board. This happens, even if the ROACH Board is not connected to the Synthesizer Board via the Ribbon Cables connected to connectors P2 and P3. Signals for the ALC board can be probed on connector P5, the DB-25. In order to accomplish this, a resistor lead that is about .030” in diameter can be inserted into the connector. Alternatively, vias on the board can be probed.

### SWITCHES 1A, 2A, 1B, AND 2B

The table below shows the test points and power-up default levels for the four switch signals. They may be probed with a volt meter.

**TEST POINTS FOR SWITCHES**

| SWITCH | CONNECTOR P5 PIN | VIA TO PROBE | POWER-UP LEVEL |
|---|---|---|---|
| 1A | 10 | CLOSE TO BOTTOM OF COMPONENT Y1 | +3.3 VOLTS |
| 2A | 23 | NEXT TO PIN 3 OF U2 | 0 VOLTS |
| 1B | 4 | BELOW RIGHT CORNER OF R83 | +3.3 VOLTS |
| 2B | 17 | RIGHT OF "Y1" SILKSCREEN | 0 VOLTS |

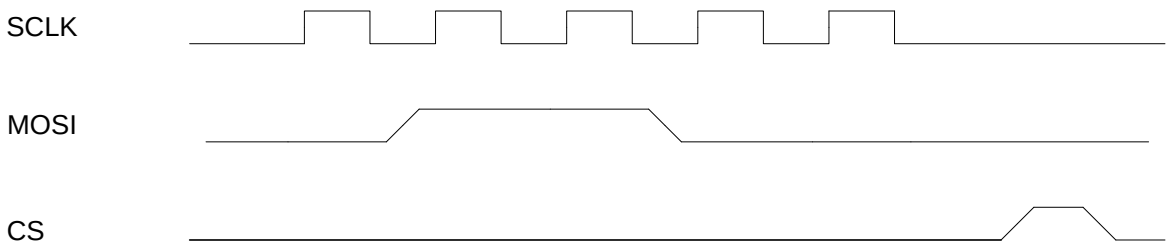
## ATTENUATORS A AND B

The Synthesizer Board controls attenuators A and B using a serial SPI interface. A 5-bit word is sent to set the attenuators. Possible values for the 5-bit word are 0 – 31, so that all 32 steps of the attenuator can be used. The power-up default value for attenuators A and B is "01100", or 12. Five clock pulses are sent on SCLK, and the pattern "01100" is sent out on MOSI, as shown below. MOSI is sampled on the rising edge of SCLK. After the five bits have been sent, CSA or CSB is raised and then lowered. This pulse occurs about 700 ns after the falling edge of the last SCLK pulse. The CSA and CSB pulses are positive going, and are about 3.4 µs wide. There is a CSA for attenuator A and CSB for attenuator B. At power-up, CSA and CSB are raised and lowered at the same time, thus causing both attenuators to be set at the same time to the value 12. These signals can be monitored easily with an oscilloscope. One period of SCLK is about 4.4 µs, so set the oscilloscope to 5 µs per division. The amplitude of the signals is about 3.3 volts. Best results are obtained by triggering on the falling edge of SCLK. If the oscilloscope is set up and connected with the power off to the synthesizer board, then it should trigger when the board is powered up. The table below shows where these SPI signals can be probed.

**TEST POINTS FOR SPI ATTENUATOR SIGNALS**

| SIGNAL NAME | CONNECTOR P5 PIN | VIA TO PROBE |
|---|---|---|
| SCLK | 7 | LEFT OF "1" ABOVE "JTAG" SILKSCREEN |
| MOSI | 20 | ABOVE AND RIGHT OF "JTAG" SILKSCREEN |
| CSA | 22 | BELOW "G" IN "JTAG" SILKSCREEN |
| CSB | 19 | RIGHT OF "P1" SILKSCREEN |

**POWER-UP SPI ATTENUATOR SIGNALS**




## CHECK SPI COMMUNICATIONS TO THE SYNTHESIZER BOARD

This part of the test can be done only if there is a way to monitor and control the Synthesizer Board using ribbon cables connected to connectors P2 and P3. In an RDBE Module, a ROACH board monitors and controls the Synthesizer Board. Alternatively, another means to monitor and control the board could be set up. Refer to the ICD for the Synthesizer Board for information about the interface between the Synthesizer Board and another computer that monitors and controls it.

### SPI COMMUNICATION WITH THE SYNTHESIZER BOARD

There is a SPI interface to the Synthesizer Board. This interface is separate from the interface from the Synthesizer Board to the ALC Board, already mentioned. As mentioned above, this

interface is described in the ICD. It is possible to monitor these signals with an oscilloscope. The table below shows where the test points are.

**TEST POINTS FOR SPI INTERFACE WITH ROACH BOARD**

| SPI SIGNAL | TEST POINT |
|---|---|
| SCLK | TP7 |
| MOSI | TP8 |
| MISO | CONNECTOR P3, PIN 3 OR FPGA PIN 110 |
| CSA | CONNECTOR P2, PIN 13 OR LEFT PAD OF RESISTOR R80 |
| CSB | CONNECTOR P2, PIN 7 OR VIA CLOSEST TO THE BOTTOM CENTER OF R24 |
| CS_FPGA | CONNECTOR P2, PIN 11 OR RIGHT PAD OF RESISTOR R82 |
| CS_EPROM | CONNECTOR P2, PIN 9 OR TOP PAD OF R83 |
| FPGA RESET | CONNECTOR P2, PIN 15 OR TOP PAD OF RESISTOR R78 |

The following tests can be done to check the SPI interface:

A. Send commands to the switches and attenuators. The protocol for these commands is in the ICD. When sending the commands, the signals can be monitored on the oscilloscope. If sending of the commands is successful, the SPI signals going from the Synthesizer Board to the ALC Board can be monitored, using the method described above for checking the power-up default settings.
B. Check the RESYNC 1PPS command. First, be sure that the 20 ms 1PPS pulse occurs about 20 ns after the station 1PPS, as described above. Then, disconnect and reconnect the 5 MHZ signal from connector J1. After this, the 20 ms 1PPS should no longer follow the station 1PPS by 20 about 20 ns. Next, send the RESYNC 1PPS command. If successful, the 20 ms 1PPS will again follow the station 1PPS by about 20 ns.
C. Check the RELOAD LMX 2531 command. This command causes the FPGA to re-initialize the synthesizer chip that creates the 1024 MHZ signal. Place a jumper between pins 1 and 2 of connector P7. This will cause the synthesizer chip to output 2048 MHZ after initialization, rather than 1024 MHZ. Next, send the RELOAD LMX2531 command. The frequency of the synthesizer clock should change from 1024 MHZ to 2048 MHZ. This is best seen with a spectrum analyzer or a frequency counter connected to connector J7, J8, J9, or J10. Remove the jumper, and send the RELOAD LMX2531 command again to set the synthesizer frequency back to 1024 MHZ.

D. Check the FPGA RESET command. This command causes the FPGA to re-initialize. Follow the same procedure as in part C, but send the FPGA RESET command instead of the RELOAD LMX2531 command. Re-initializing the FPGA will cause the synthesizer chip to re-initialize also.

E. Check the FPGA Firmware Version Number monitor. The protocol for implementing this and the other monitors is in the ICD. In a working system, this can be verified simply by doing the monitor with the control computer and checking the result. The monitor can also be observed on an oscilloscope, by monitoring the MISO signal. The latest firmware version number, in binary, should appear. It is also helpful to monitor SCLK at the same time.

F. Check the 15-bit 1PPS interval counter. Two 8-bit registers must be monitored in order to read this counter. Normally, this counter contains the number 6 or 7, corresponding to 6 or 7 clock cycles of 256 MHZ. Again, the binary number can be obtained by looking at the MISO signal on an oscilloscope. If the 20 ms 1PPS is out of sync, this number will be much larger.

G. Check the status register. As stated in the ICD, bit 0 indicates presence of the station 1PPS. Bit 1 indicates the lock status of the LMX2531 synthesizer chip. To check the 1PPS status bit, monitor the status register and verify that bit 0 is a “1”, indicating the presence of the station 1PPS. Next, disconnect the station 1PPS from connector J2. Monitor the status register again. Bit 0 should now be a “0”. Reconnect the station 1PPS to connector J2. Monitor the status register again, and bit 0 should again be a “1”. Verify that bit 1 of the status register is a “1”. This indicates that the LMX2531 synthesizer chip is locked to 5 MHZ. Now, disconnect 5 MHZ from connector J1. Monitor the status register again. Bit 1 should now be a “0”, indicating that the LMX2531 is out of lock. Reconnect the 5 MHZ signal to connector J1. Check bit 1 of the status register again, and it should be a “1”.