VLBA Sensitivity Upgrade Memo #43
A Total Power Digitizer for the VLBA RDBE

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1 Description

The VLBA Digital Back End (DBE) Automated Level Control (ALC) board will be enhanced to allow detection and digitization of the RF power level of the analog signal before it is digitized in the ROACH. This requires adding directional couplers, RF power detectors, and an Analog-to-Digital Converter (ADC) to the existing Rev A printed circuit board (PCB) design, while leaving the present functionality intact. Figure 1 shows the functional block diagram of this circuit, with the new components shaded in orange.

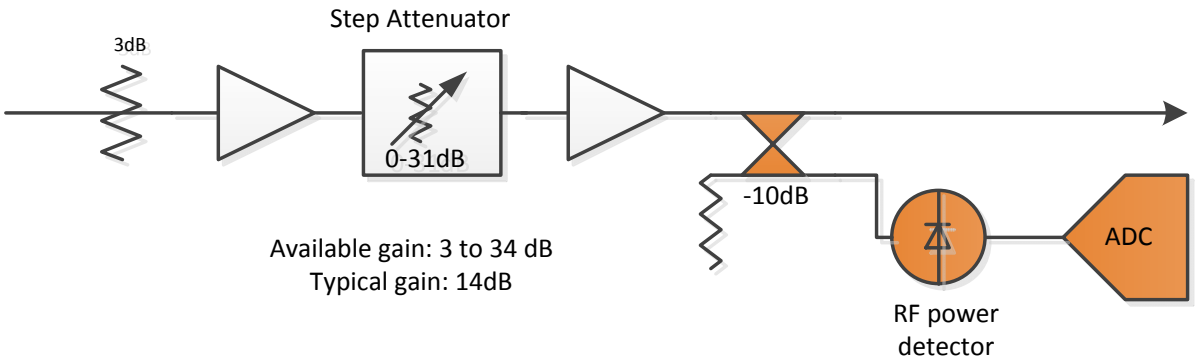

Figure 1: Functional block diagram of ALC module. The orange-shaded components – coupler, detector, and ADC -- are the new additions to the circuit

This enhancement will provide (a) a measurement of the RF power in the 512MHz VLBA IF bandwidth and (b) a measurement of the switched power ratio – the ratio of noise-diode-to-signal – before the analog RF signal is digitized. The Legacy VLBA BBC has analog monitor points in both the IF distributor and the baseband converters – total power and switched power – that are equivalent to these, and which will be eliminated when the Legacy system is retired. This leaves technical staff without a reliable analog monitor point for assessing and diagnosing system performance. While it is true that the DBE digitizer provides a measure of RMS sampled voltage, and this voltage is a proxy for IF total power, it is not an equivalent quantity, nor measured at an equivalent point in the system, to be an acceptable substitute for the legacy power measurements.

2 Theory and Background

The total power is derived by applying a laboratory-determined detector transfer function calibration formula to the detected samples. These can either be individually-calibrated, or use a universal calibration factor that is derived from the average of a sufficiently large sample of detectors, as is the case with the T450 power detector. Unfortunately, the analog-digital converter used in the T450 does not have sufficiently fine voltage steps to be able to resolve the small changes in power added by the calibration noise diode. Therefore the switched power must be measured elsewhere, in this case in the DBE analog section.

In the EVLA, a power detector is sampled by an 24-bit Σ-Δ ADC at a 1MHz rate, then demodulated to a series of 16-bit samples at a 500Hz rate; this deliberate oversampling allows adequate time resolution of the 10Hz noise diode switching signal and rejection of 60Hz interference. The MIB calculates the root-mean-square of the detected time series over one second and from this calculates the dimensionless switched power ratio *SP*.

The switched power measurement is based on a technique used in the EVLA downconverter modules that statistically approximates a true Synchronous Detection Ratio (SDR). Assuming that the switching signal is a 50% duty cycle square wave, the standard deviation of the switching signal is equal to one-half its amplitude. Therefore a statistical measure of its standard deviation can be used to derive its amplitude, which is the quantity of interest. The amplitude of this signal represents the incremental power added by the calibration noise diode in the front end, and is used to track and eliminate receiver-based gain changes from the astronomical data.

The power detector produces a voltage proportional to the log-power. In order to calculate the ratio $\frac{P_{ON}-P_{OFF}}{P_{OFF}}$ we must convert the power to linear units, which requires exponentiating. Since the expected ratio is quite small, typically 0.02 < SDR < 0.07, the technique can use the first two terms of a Taylor Series expansion of the exponential function, $e^x \approx 1 + x + \frac{x^2}{2}$ without introducing significant error. This gives the ratio $\frac{P_{ON}}{P_{OFF}}$. But because we are interested in the fractional increase in power $\frac{P_{ON}-P_{OFF}}{P_{OFF}} = \frac{P_{ON}}{P_{OFF}} - 1$ we calculate $e^x - 1 \approx x + \frac{x^2}{2}$. The data processor, whether MIB or FPGA, can calculate the switched power ratio as:

$$SP = \ln(10) * \left[\delta + \frac{\delta^2}{2}\right]$$

where

$$\delta = \frac{-2 \cdot RMS}{10} \frac{slope_1}{slope_2},$$

RMS is the root-mean-square of the 1-second time series of detected power samples and has units of ADC level per power unit,

slope$_1$ is the ADC transfer function in volts per ADC level and

slope$_2$ is the power detector transfer function in volts per power unit.

The 500Hz sample rate provides a statistically significant number of samples (50 per period of the switching waveform) for this approximation to converge on the value which a true synchronous detection method would calculate.

Figure 2 shows an example of one second of EVLA total power measurements as digitized by the AD7731, then scaled to linear power units. From linear power units we can calculate directly the quantity $\frac{P_{ON}-P_{OFF}}{P_{OFF}}$. If we take the median P_{ON} = 0.1763 and the median P_{OFF} = 0.1686, then SDR = 0.0454. The statistical approximation above yields SDR = 0.0447, or about a 1.5% error between the two methods. This is an acceptable level of accuracy for this monitor point.

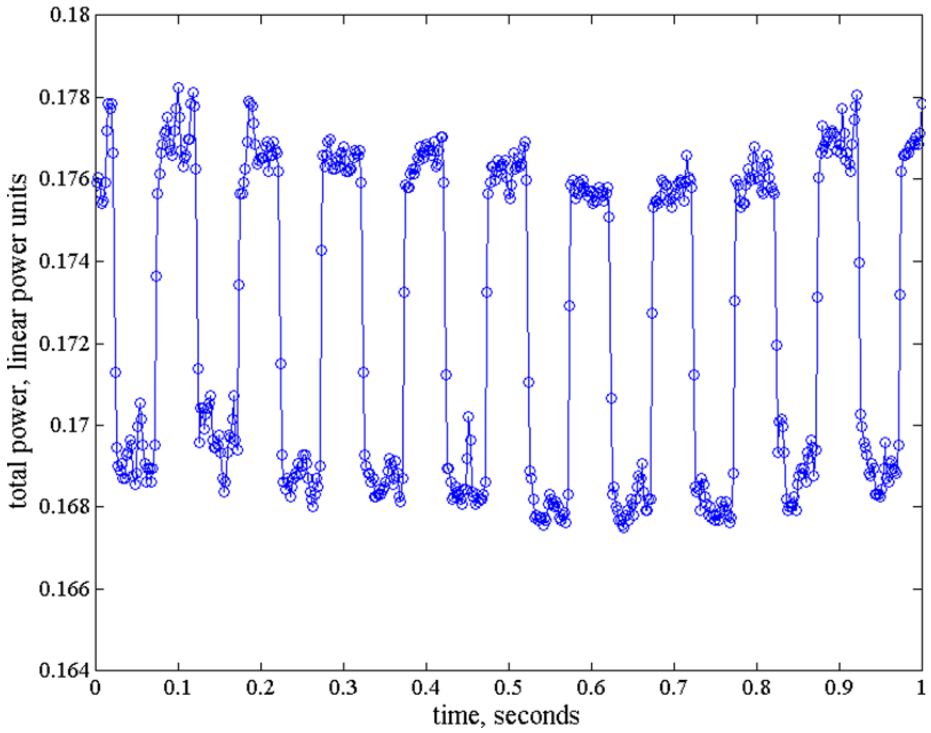

Figure 2: Total power time series from EVLA T304 total power digitizer

If we wish to match the performance of the EVLA Total Power Digitizer, then we could simply replicate the implementation from the T304, and a reasonable candidate for the ADC is the very same part used in the EVLA module – the Analog Devices AD7731 24-bit sigma-delta modulating ADC. There is sufficient stock of these parts that they can be harvested from obsolete EVLA PCB revisions to populate the entire stock of VLBA units.

In the VLBA system, the noise diode switching signal is 80Hz, compared to 10Hz in the EVLA system. In order to use the AD7731 in this application, the following options could accommodate this change in signal frequency, albeit with some unavoidable trade-offs:

1. Increase the sample rate by 8 to 4kHz. This also increases the noise bandwidth of the ADC, per Table 1. However, this increased noise is still several orders of magnitude below the power step that we seek to measure.
2. Sample at 500Hz, which will capture fewer samples within each period of the switching signal. The noise in the measurement will increase as $\sqrt{N_{Samples}}$, or about a factor of 3
3. Use a data rate intermediate to 500Hz and 4kHz, optimizing the noise added by the increased bandwidth and the noise added by the decrease number of samples.

The AD7731 rms noise voltage increases with increased output rate proportional to (data rate)^2. As long as this remains less than 39mV/dB x 0.02dB = 780μV, it does not significantly affect the measurement. We can also lower the data rate by a factor of 5 (to 800Hz) without significantly corrupting the statistics of the measurement. The loss of data results in a $\sqrt{5}$ ~ factor of 2.2 increase in noise, while the reduced output rate gives a factor of 10 decrease in noise relative to the AD7731 performance at 4000Hz.

It should be noted that the ADC-induced noise at 4kHz of 64μVRMS is lower by a factor of 12 than the 10σ requirement for resolution of the noise diode power step. Undersampling of the switching waveform corrupts the estimation of the standard deviation of the waveform faster than increased data rate raises the noise floor of the measurement. It is recommended that a data rate as close to (but not exceeding) 4kHz be used, if the digital hardware can sustain it.

3 Hardware Implementation

3.1 Power Detection

The circuit shown in Figure 1 will sample the RF power 10dB lower than the power in the main signal path. The main path power at the VLBA operating point is approximately -20dBm, so a detector at the coupled port would see approximately -30dBm. The detector should be reasonably accurate at this point +/- 10dB, at the least. The Hittite HMC909LP4 RMS power detector is sensitive to power levels as low as -50dBm, and begins to saturate around -14dBm. This detector is presently being used to measure IF power in the T450 Matrix switch, and with the most basic of calibrations is accurate to 0.5dB across the range -40dBm to -20dBm. In addition, this detector has a programmable integration time from 0.5us to 1ms, so that the detector response can be matched to the ADC sampling rate, minimizing the inherent measurement uncertainty.

The power step added by the noise diode switching signal is on the order of 2 to 7% $\left(\frac{P_{ON}-P_{OFF}}{P_{OFF}} \cong 0.02\ to\ 0.07\right)$. The resolution in dB required of the detector for 10σ confidence in

the amplitude of this switching signal is therefore on the order of 0.02dB. Interpolating from Table 1, let f_{sample} = 4000Hz. Then the noise voltage at the input of the ADC is 64µV_{RMS}. We want the resolution of the power detector to be at least ten times greater than the ADC noise floor. The minimum slope required at the power detector is therefore $\frac{0.064mV}{0.02dB} = 3.2mV/dB$. The default nominal detection slope of 39mV/dB meets this requirement. If greater resolution is desired, refer to page 11 (LOG-Slope and Intercept) of the HMC909LP4 datasheet.

The HMC909LP4 RF power detector response is shown in Figure 4. The output is linear-in-dB with a nominal slope of 39mV/dB. This slope can be adjusted to allow for "magnification" of the voltage/power response around a particular target power. In the case of the DBE ALC board, the expected operating point yields approximately -30dBm at the detector. We can maximize the power resolution in the vicinity of the operating point at the expense of losing accuracy when the power is far away from the operating point. An example of this is shown in Figure 4, where the slope has been increased to 58mV/dB, centered on -30dBm. This is almost exactly the case we will encounter, and therefore serves as a good design starting point. This allows reasonably accurate reporting of power measurements +15dB/-25dB from the nominal operating point.

Referring to Figure 3, we see that the expected error, in dB, of the detector output at 25°C is approximately +/- 0.5dB in the range -40dBm < P_{IN} < -20dBm. The error over any 0.3dB interval in the vicinity of -30dBm (the step corresponding to an SDR of 7%, the largest meaningful value we are likely to encounter) is less than 0.5dB, and nearly constant. Small absolute offset errors such as these will not affect the statistical calculation of the SDR.

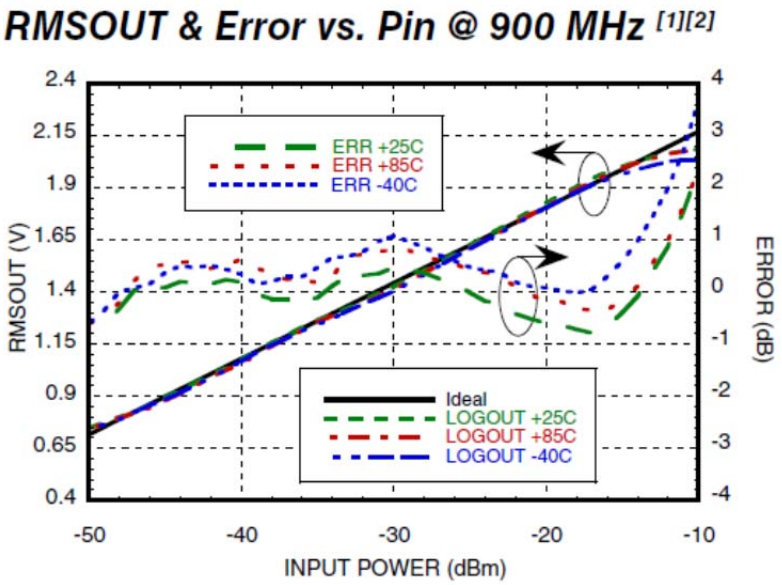

Figure 3: HMC909LP4 voltage-power response and error function for CW and noise-like signals at 900MHz. Source: Hittite Microwave

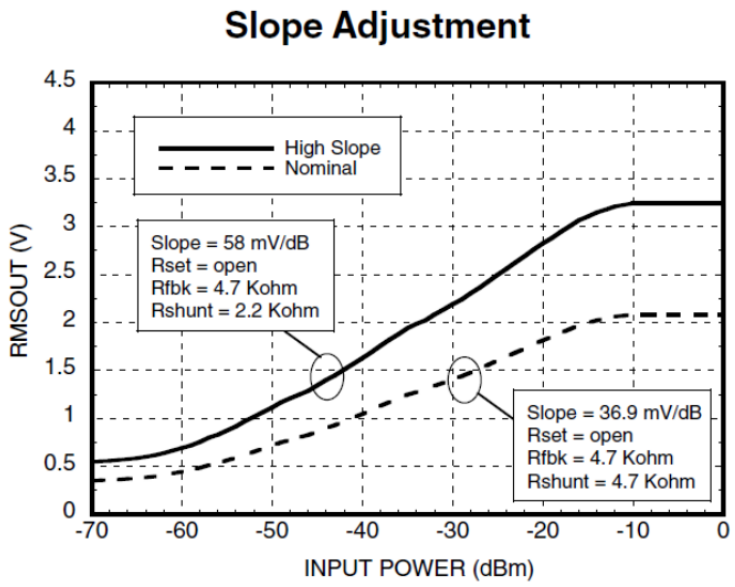

Figure 4: HMC909LP4 slope adjustment for power magnification.

3.2 Data Acquisition

The AD7731 accepts three differential or five single-ended voltage inputs, and can sustain an output data rate of up to 6.5kHz, depending on the specific FIR filter implementation. The choice of data rate is bounded on the small end by the statistical significance required in the estimation of the SDR and ADC settling time, and on the large end by the increase in input voltage noise and in the ADC, and by the maximum possible data transfer rate. Table 1 shows ADC noise voltage and settling time as a function of output data rate.

Table 1: AD7731 settling time, RMS noise, and Effective Number of Bits (ENOB) versus output data rate

Data Rate	-3dB Frequency	Settling Time	RMS Noise	ENOB
Hz	Hz	ms	uV	
400	104.8	7.5	4.2	16.5
600	157	5	5.2	16.5
800	209.6	3.75	6	16
1200	314	2.5	7.8	15.5
1600	419.2	1.87	10.9	15
2400	629	1.25	27.1	14
3200	838.4	0.94	47	13
4800	1260	0.625	99	12
6400	1676	0.47	193	11

In the EVLA implementation the 500Hz data rate realizes an effective number of bits (ENOB) of 16; the VLBA implementation will likely be equal to or smaller than this. For a data rate of $f_{switching}$*50 = 4kHz, as in the scaled-EVLA example, expect 14 effective bits of representation of

the detector signal. In practice, the number of samples per noise diode switching period could be smaller than 50 and still produce an accurate estimate of SDR.

The voltage output of the HMC909LP4 is 0.5V to 3.2V. The AD7731, configured for single-ended (pseudo-differential) inputs will accept voltages up to +/-1.28V. This requires either voltage scaling to be applied to the detector output before it is digitized, so that the positive output fits within the unipolar range of the ADC, or that the detector output be offset so that the full scale (positive voltage) range fits within the 2.56V range of the bipolar input. The scaling or offset can be removed from the digital representation of the signal.

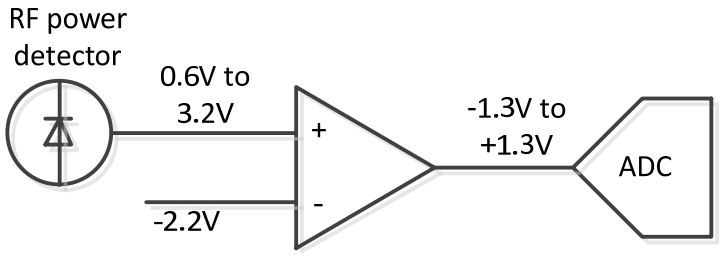

Figure 5: Voltage-offsetting circuit for detector/ADC interface

Voltage-offsetting will allow the entire detector voltage swing to fit within the ADC's +/-1.28V range, maximizing the power resolution. The HMC909 output range of 2.6Vp-p can be shifted by -2.2V to place the nominal operating point of -30dBm/2.2V at the ADC midrange. This will maximize both linearity and resolution, as shown in Figure 5. At the extreme ends of the power detector range, the ADC will be at its full-scale limits and produce nonlinear measurements. We should be willing to accept this nonlinearity and inaccuracy at the extremes of the measurement range in order to optimize the performance in the vicinity of the operating point.

The design will use one AD7731 per channel, each with its own chip select, sharing the SPI bus with the step attenuator and the serial EEPROM. Each converter can therefore maintain the proper output data rate. The chip selects will be made available by removing one (IFA-sw2 and IFB-sw2) of each complementary pair of solar attenuator control lines (see Figure 6) – the complement can be created on board from a single control line and a logic inverter. This allows the EEPROM to remain installed and connected, where it can be used to store, for example, the calibration coefficients for each ADC.

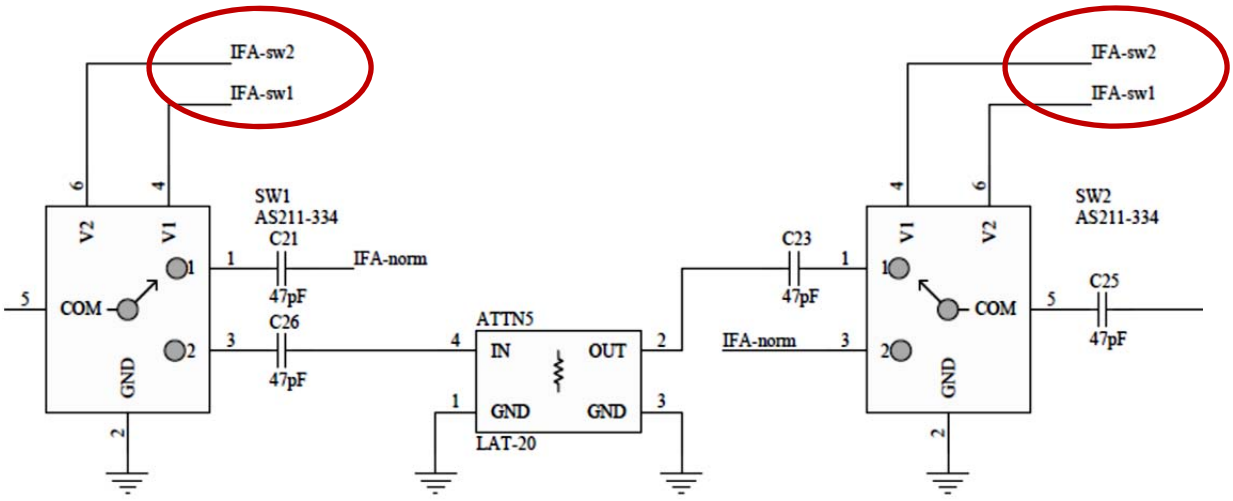

Figure 6: Schematic detail of IFA circuit, showing redundant complementary solar attenuator control line which can be reconfigured as ADC chip select signals. IFB similarly has a redundant control line.

4 Interface and Data Processing

The ALC subassembly monitor and control interface occurs through a 25-pin cable to the Clock/Synthesizer board, which relays commands from and monitor points to the PowerPC software MIB. This scheme requires that the ROACH FPGA act as an intermediate stage – in other words, two different devices must coordinate to relay information to and from the MIB and the ALC board. This enhancement project provides an opportunity to reconsider this interface. Three options present themselves:

1. Leave the interface as it is, and continue relaying data from the MIB through the two FPGAs and into the ALC board (and vice-versa). This is the least-change option, but not necessarily the most elegant
2. Redefine the interface such that the ALC board communicates directly with the MIB, such as through a high-speed serial port on the ROACH board, thereby eliminating the two intermediate FPGAs and potentially reducing firmware complexity and unnecessary dependencies
3. Retain the present M&C interface, but do some or all of the SDR processing in the Clock/Synthesizer board FPGA. This scheme would retain the dependencies and actually add to the firmware complexity, but would reduce the overall data throughput between the MIB and the ALC board.
4. Use the four unused pins on the 25-pin connector to bring the power detector output voltages and ground references out of the ALC enclosure, and mount the ADC and associated circuitry on an external circuit board. This external board may be required anyway for (2), to provide a bridge for converting the native LVDS signals to single-ended LVTTL signals. Digitizing the signals external to the ALC enclosure would simplify the circuit layout of the ALC board, but move the complexity to the external interface board.

In any of these cases, the communication and data transfer will take place over an existing SPI bus, using the two new chip select signals that result from removing the redundant complementary-command scheme for the solar attenuator switches, and keeping the existing chip select lines reserved for the serial EEPROM and step attenuators.

If all data operations were performed in an FPGA, it would require the accumulators necessary for capturing the data from the ADC (the FPGA would have sufficient memory register space to accumulate one second's worth of data: two channels of 16-bit samples at 4ksps = 128kb), plus the necessary registers to perform the root-mean square and switched power calculations. Alternatively, the FPGA could transfer the raw ADC samples to the Software MIB and the statistics can be computed there. Performing the calculations in the MIB may be preferable, since the EVLA MIB code could be ported directly to the DBE. The MIB option may involve a different interconnect scheme than is currently deployed, which may increase the complexity of the project relative to either processing the samples in the FPGA or using the FPGA chain to shuttle data to the MIB.

5 Budget and Installation Plan

The VLBA has two such units per station, plus two test rack modules, and modules for ancillary facilities such as Green Bank, Arecibo, Effelsberg, Haystack, and other observatories that use the DBE or related hardware, so a budgetary estimate of $6k is anticipated for 30 modules, or approximately $200 per module. This should give an accurate order-of-magnitude figure that can be scaled to the final production quantity.

A stock of spare enclosures will allow eight of these assemblies to be built in advance of retrofitting. These eight assemblies can be shipped to the VLBA sites to be retrofitted in place, or alternately entire spare DBE units can be built with the new assemblies and swapped by the site technicians and returned to DSOC for retrofitting.

6 Acknowledgements

The author wishes to acknowledge the contribution of Ken Sowinski who not only developed this statistical algorithm but also generously spent his time explaining its derivation and the various computational steps and assumptions to me.