

Development of SIS Mixers for ALMA Receivers

a proposal to NRAO

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1 Introduction

This proposal is for the support of work at Stony Brook in a collaborative effort with NRAO to develop and fabricate SIS mixer chips for the millimeter wave array telescope (ALMA). In this collaboration NRAO will have the primary responsibility for the mixer design and testing, while Stony Brook will have the responsibility for the fabrication of mixer chips along with the development of any needed refinement to existing niobium trilayer fabrication technology. The groups will work together to develop design and technology modifications required to optimize the mixer performance. The same basic approach as for our present contract will be used.

A development effort, including process refinement, mixer design development and testing, and barrier technology development for noise reduction, will run throughout the three year period of the proposal. In addition, during the period of months 10–24 (pre-production phase), a design and process for the production of 230GHz band mixers will be fixed. Process yields for this will be determined so that plans can be set for the final production phase (months 25–36). During the final 12 month period mixer chips for the 230 GHz band will be produced. The details of the project are listed below.

2 Detailed statement of work for the project

2.1 Continuing R&D throughout the 3-year period:

2.1.1 General goals

- 2 Improve DC testing procedures.
- 2 Improved I(V) quality – possibly explore AlN barriers.
- 2 Improve fabrication techniques.
- 2 Develop better evaluation methods

2.1.2 650 GHz mixers

Single-ended mixer

- 2 Improve design (tuning &/or I(V), etc.)
- 2 Obtain new mask set if needed.
- 2 Deliver 2 wafers.
- 2 Evaluate DC testing procedures.

2.1.3 230 GHz mixers.

Single-ended mixer

- ² Improve design (tuning &/or I(V), etc.).
- ² Obtain new mask set if needed.
- ² Deliver 2 wafers.
- ² Evaluate DC testing procedures.

Balanced sideband-separating mixer

Iteration 1

- ² Obtain new mask set.
- ² Deliver 1 wafer.

Iteration 2 – improve design (tuning &/or I(V), etc.)

- ² Obtain new mask set.
- ² Deliver 2 wafers.
- ² Evaluate DC testing procedures

2.1.4 100 GHz mixers

Single-ended mixer

Iteration 1

- ² Obtain new mask set.
- ² Deliver 1 wafer

Iteration 2 – improve design (tuning &/or I(V), etc.)

- ² Obtain new mask set.
- ² Deliver 2 wafers.
- ² Evaluate DC testing procedures

Balanced sideband-separating mixer

Iteration 1

- ² Obtain new mask set.
- ² Deliver 1 wafer.

Iteration 2 – improve design (tuning &/or I(V), etc.)

- ² Obtain new mask set.
- ² Deliver 2 wafers.
- ² Evaluate DC testing procedures

2.2 Pre-production work

2.2.1 230 GHz mixers (NRAO to make choice between single-chip and multi-chip BSSM).

- ² Deliver 4 wafers for evaluation of on-wafer and between-wafer uniformity.
- ² Decide on number of variations needed on the wafer.

2.3 Production work

2.3.1 230 GHz mixers

- ² Deliver 6 good wafers

2.4 Preproduction and production work on 100 GHz and 650 GHz mixers

Pre-production and production work on 100 and 650 GHz mixers depends on technical results, as well as other factors, during the extended development phase. Because of this uncertainty preproduction and production work on 100GHz and 650 GHz mixers is not included in this proposal. However, SUNY would be willing to increase the scope of the proposed contract to include the 100 and 650 GHz pre-production and production phases if that is approved in due course. The quantities of wafers required for each band are expected to be about the same as for 230 GHz.

2.5 Process goals

The work on the 230 GHz band will utilize trilayers with a critical current density J_c of about 8 kA/cm² and a junction area of about 1.2 μ m²; for which high quality junctions are routinely obtained. For these wafers, the process goals are:

- ² Junction area: \pm 10 % of specification.

- ² J_c : $\pm 10\%$ of specification.
- ² Subgap resistance R_{sg} (measured at 2 mV): $> 20R_n$; where R_n is the resistance measured at 4 mV.
- ² Conductor widths: $\pm 0.5 \mu m$ of design values.
- ² Resistors: $\pm 10\%$ of design values.
- ² Resonant frequency of 1/4 wave stubs: $\pm 5\%$ of design value. To accomplish this it is important to control
 - Oxide dielectric constant: $\pm 5\%$ of standard value.
 - Oxide thickness: $\pm 10\%$ of design value.
 - London penetration depth: $\pm 10\%$ of standard value.

Work on the 650 GHz band will utilize trilayers with a J_c of about 12 kA/cm^2 . For these trilayers the best R_{sg} is about $10 R_n$. Part of the development work during this project will focus on increasing this ratio to at least 20. Other than this the process goals are the same as for the 230 GHz mixers.

2.6 Testing

In addition to standard process test chips which Stony Brook will add to the mask sets, chips from the wafers to be sent to NRAO will be first tested at Stony Brook to determine junction quality, uniformity, and J_c and resonator frequency. It may also be useful to measure the low frequency junction noise, if this correlates well with mixer performance.

2.7 Process development

During this project, we see four areas in which process development is required.

1. Optimization of our process for the production of high quality junctions on quartz substrates.
2. Development of high quality, i.e. low leakage, trilayers with high J_c to permit the use of submicron junctions for the higher frequency bands.
3. Characterization of, and improvements in, the uniformity of process parameters over the 2" wafer, so that a high yield can be obtained when the work enters the production phase.

2.8 Details

2.8.1 Masks

Stony Brook will purchase the photolithographic mask sets required for this work. AutoCad files, with the mixer designs will be supplied by NRAO. Stony Brook will then make needed modifications (e.g. the addition of EBL registration marks) and add the designs for the process test sites before submitting the final mask design to the supplier.

2.8.2 Substrates

The chips will be fabricated on 2" quartz wafers. It will be Stony Brook's responsibility to obtain the wafers required for this work. The initial work will be done on 10 mil fused quartz, Dynasil 1000 or 4000 or the equivalent. Other types and/or thicknesses of quartz which are compatible with mixer operation may be tested to optimize the processing.

2.8.3 Publication

Since this is a collaborative project, it is expected that publications resulting from this work will include authors involved in the design, fabrication and testing aspects of the work.

2.8.4 Deliverables

The main deliverables under this contract will be the 23 wafers for NRAO described above. We will make out best effort to ensure compliance with the initial parameter specifications listed in Sec. 2.5 or revised specification that may be jointly developed by NRAO and Stony Brook during the project. Additional deliverables may include reports on process parameters as required to develop mixer designs. In addition, quarterly reports will be provided to NRAO summarizing each quarter's work.

3 Budget