A Revised Proposal

SIS MIXER ELEMENTS FOR ALMA

Submitted to:

National Radio Astronomy Observatory
Edgemont Road
Charlottesville, VA 22903-2475

Attention:

James L. Desmond
Associate Director, Administration

Submitted by:

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Research Associate Professor

SEAS Proposal No. EE-NRAO-1173-02
Revised June 2002

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UNIVERSITY OF VIRGINIA
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CONTRACTUAL INFORMATION

A Revised Proposal Submitted to National Radio Astronomy Observatory

Title: SIS Mixer Elements for ALMA

Proposal Number: EE-NRAO-1173-02

Date Submitted: Revised June 2002

Offeror: University of Virginia

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Duration: July 1, 2002 - June 30, 2005

Amount: $1,470,000

Approvals:

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Associate Dean for Research

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II. Proposed Development

INTRODUCTION

In the past year we continued to examine our fabrication process in light of the need for a repeatable SIS mixer fabrication process and junctions with sharp electrical characteristics. This investigation was primarily undertaken with respect to the deposition of the trilayer films and the stress of these films, and with respect to the junction fabrication process. We have also started the transfer of our technology from 30mm to 50mm wafer sizes. Finally, we have begun investigation of a quartz beam-lead process.

The film stress of Nb has been shown to play a critical role in the quality of electrical characteristics of SIS junctions[1-7]. In our laboratory, film stress on test Si wafers is obtained with a laser based tool which is used to measure the curvature of a Si wafer prior to and after film deposition. The profiles are subtracted and fit with a theoretically generated curve, from which the film stress value is extracted. We have recently discovered that ex-situ substrate cleaning and baking as well as in-situ cleaning and deposition sequencing can have a significant effect on the resulting measured film stress [8]. With these results we are better able to repeatably predict the stress of the Nb/Al-oxide/Nb (m1/Al-barrier/m2) trilayer material from which all of our SIS mixers are fabricated.

The junction fabrication process, where the m2 junction 'button' is defined, etched and insulated, is the most critical step in the entire thin fim fabrication process. If the junctions are not uniformly defined, the resulting mixer resistance will vary across the wafer. If the oxide barrier or superconducting electrodes are damaged or stressed, the electrical characteristics will have excess leakage current, and if the insulating layer(s) do not fully cover the m1 base electrode, electrical shorting will occur between the m1 base and m3 wiring electrodes. We have fabricated high quality Nb/Al-oxide/Nb Superconductor-Insulator-Superconductor (SIS) junctions using a new Ti-based quadlevel resist process[9]. The quadlevel materials have been carefully chosen to optimize the fluorine based anisotropic reactive ion etching of Nb and subsequent insulation coverage of the junctions in a self aligned process. With the use of the Ti layer, the resist feature is insured of having a top refractory metal to protect the resist, accurately and repeatably define the junction area, and to facilitate liftoff. This SIS fabrication process enables excellent control of junction size and is also compatible with both Au overlayer junction and junction anodization approaches.

We have very recently begun investigating the use of rf diode sputtered SiO_x insulation films in the junction process as an alternative to the evaporated SiO_x films currently in use. Our junction approach uses a self aligned process where the same quadlevel resist feature used to define and etch the m2 junction feature is also subsequently used to define the geometry of the insulation layer in a liftoff process. Evaporated SiO_x films are deposited in a line of site process and hence are typically much easier to liftoff. The downside of evaporated films is that they typically have more pinholes and poorer edge coverage. Sputtering has much more energy associated with the process and the resulting films have fewer pinholes and more of a conformal coverage of step heights. However, the energies associated with sputtering processes make it much more difficult to liftoff sputtered films. Our laboratory has an rf diode sputter system that is a general use system that can be utilized with a variety of targets (one at a time). We have used this system to successfully fabricate large area capacitors for the N9 mixers. Previous attempts at using the evaporative SiOx films had failed due to pinholes in the dielectric films and resulting shorts between the electrodes of the capacitor. More recently, we have worked to integrate this technology into our mixer fabrication process. It was found that smaller features (junctions and

small vias) would stay 'buried' in the dielectric and not lift off. We have adapted our quadlevel resist process (see the previous paragraph) to improve the liftoff characteristics so that the vias on the N9 mask set lift off, but typically junctions smaller than 10um still remain covered with the SiO_x. By reducing the energy and duration of the sputter cleaning step before SiO_x deposition; however, we have obtained a process that is compatible with junctions as small at 1um. The existing RF diode sputtering system uses two large L buna gaskets, is limited to a 5" target size, is used to deposit metals and insulators by a variety of users, obtains only low 10-6Torr base pressure and is over 20 years old. I propose to design and build a new system dedicated for this process in this new work.

We have recently acquired a new EVG mask aligner [10] from a DARPA grant that will allow us to transfer of our wafer processing technology from 30mm to 50mm wafer sizes. Our existing aligner can accept 50mm wafers; however, the power uniformity of the UV light deteriorates beyond 40mm. The system was recently installed, and after a recent replacement of incorrect optics we are ready to begin familiarizing ourselves with the unit and characterizing our processes for 50mm wafers.

We have also begun investigation of a quartz beam-lead process. Since thick quartz layers cannot be etched with conventional RIE, Si based beam lead processes cannot be adapted to our quartz wafers. We have developed a scheme where a 'finished' wafer is diced only 4-5mils into the wafer along the dicing 'streets'. In this scheme these dicing channels are then filled and planarized with some material. Next, a seed layer of Ti/Au is deposited over the planarized wafer and a beam lead lithography (>10um thick resist) performed to open windows in the resist for the final Au beam leads. Then 10um thick Au is plated into the resist, the resist is stripped and the seed layer removed. This leaves Au leads extending over the planarized material. The wafer is then lapped from the backside to the desired thickness (and into the planarized material in the dicing 'streets'). Finally, the planarizing material is etch out of the 'streets', leaving each mixer separated and with beam leads of Au extending from each side of the wafer. This conceptual process will be further discussed in the next section.

SIS ALMA WORK

(1) A major emphasis of our work will be maintaining and keeping within specification the fabrication technology used for the fabrication of SIS elements for ALMA mixers. Included in this work will be increasing the control over process variations and material and device characteristics.

(2) We will transfer of our wafer processing technology from 30mm to 50mm wafer sizes in the first year with our recently acquired EVG mask aligner. Our existing aligner can accept 50mm wafers; however, the power uniformity of the UV light deteriorates beyond 40mm. This system also has splitfield optics that will permit better and easier alignment of the wafers to the masks. New wafer blocks and shuttering to accommodate 50mm wafers, for optimal processing, will be also be machined for our other deposition systems.

(3) We propose to design and build a new system dedicated for SiO_x rf diode sputtering in the first year. Shown in figure 1 and 2 are focused ion beam cross sections of actual junctions that were (Fig. 1) insulated with evaporated SiO_x , and (Fig. 2) that were insulated with sputtered SiO_x.

As can be seen from these images, the coverage of the sputtered SiO_x films is superior to that of evaporated SiO_x. We have also found that the sputtered SiOx films have a much smaller pinhole

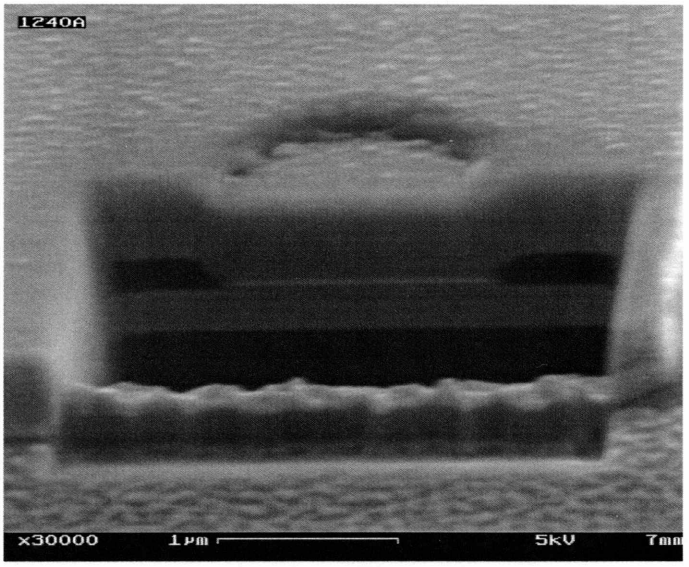

Figure 1 Cross section of an SIS junction that was insulated with evaporated SiO_x. Note how the thickness of the SiO_x decreases as it 'approaches' the perimeter of the m2 junction and how it does not fully cover the top of the exposed portion of the m2 electrode.

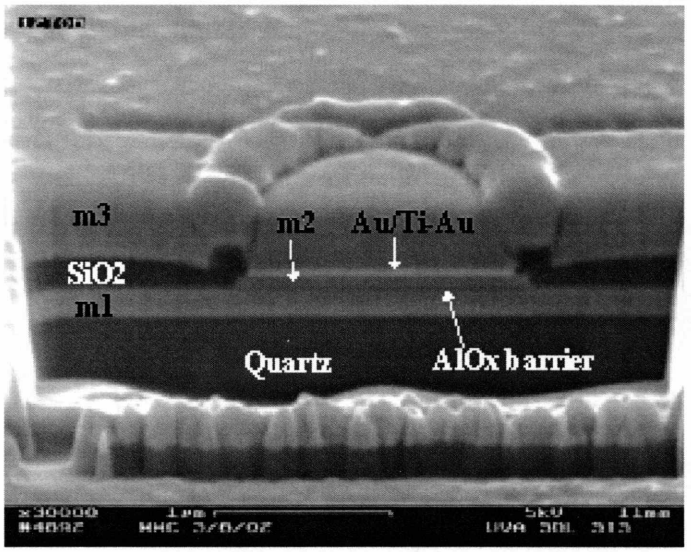

Figure 2 Cross section of an SIS junction that was insulated with sputtered SiO_x. Note how the thickness of the SiO_x fully covers the perimeter of the m2 junction as well as the top of the exposed portion of the m2 electrode.

density than the evaporated films. We previously designed and built the current Nb/Al-oxide/Nb UHV trilayer system and HV multitarget systems presently used in our research and anticipate a very quick assembly time for the proposed system due to the simplicity of the design. The existing rf diode sputtering system is not suitable for this ALMA work for a number of reasons: (a) the system is used for over ten different materials and not dedicated to SiO_x, (b) the 5" diameter target and the non symmetrical J-arm geometry of the system does not provide the film uniformity required by ALMA for 50mm wafers, and (c) the base pressure of the system is only low 10^{-6} Torr. The proposed system will utilize a larger 8" diameter target and a symmetrical unobstructed parallel plate geometry with substrate rotation for improved uniformity. The system will be all conflat with only two non UHV seals and should, from previous experience, obtain a base pressure in the 10^{-8} Torr range. This system will be dedicated for the deposition of SiO_x films and will only be operated by members of our superconducting materials and device group.

(4) We will continue our initial work on a quartz based beam lead technology. The goal of this project is to develop a robust and repeatable technology for forming "thick" Au pads that extend out beyond the edge of each individual finished chip. The chip can then be easily handled (pick them up by the beam-leads) and placed into a waveguide channel with the extended beam leads positioned in recesses on either side of the channel so that the chip is self aligned and suspended in the middle of the waveguide. Full assembly of the other half of the waveguide physically clamps

and holds the chip in place and provides electrical connection to the pads on the wafer. These pads must either be formed after the quartz wafer is diced (otherwise you will dice through the Au pads) or a backside etch process must be used where the etch separates the individual chips and stops on the Au pads. Since thick quartz layers cannot be etched with conventional RIE, a backside etch process cannot be adapted to our quartz wafers. As described previously, we have developed a scheme where a 'finished' wafer is diced only 4-5mils into the quartz along the dicing 'streets'. In this scheme these dicing channels are then filled and planarized with some material. Next, a seed layer of Ti/Au is deposited over the planarized wafer and a beam lead lithography (>10um thick resist) performed to open windows in the resist for the final Au beam leads. Then 10um thick Au is plated into the resist, the resist is stripped and the exposed seed layer removed. This leaves Au leads extending over the planarized material. The wafer is then lapped from the backside to the desired thickness (and into the planarized material in the dicing 'streets'). Finally, the planarizing material is etched out of the 'streets', leaving each mixer separated and with beam leads of Au extending from each side of the wafer.

The most difficult technical part of this process is the planarization of the 5mil (~125μm) deep by 50-100mil wide channels in the quartz with a material that is compatible with the rest of the process. Besides being able to actually planarize the material, some of the constraints on this material are: (a) it must adhere to the quartz, (b) it must not soften or reflow at temperatures above 100C, (c) it must etch in an oxygen plasma, (d) it must not etch in H_2O, ethanol, methanol trichloroethane, or photoresist stripper, (e) Ti must adhere to it, (f) it must not create excessive compressive or tensile stress on the wafer after curing or cooling or when heated, and (g) it must be fairly mechanically hard at room temperature. In addition to all these properties, some method for planarizing the wafer with the chosen material must be devised. Our initial work has centered on using spun on coatings commercially offered for planarizing deep channels. Many of these materials just could not planarize channels as deep as 125μm. All the others, though none of them planarized to better than 20um, unfortunately reflowed at temperatures well below 100C making them unusable in subsequent metallization and lithography steps.

Our current approach utilizes the pressing of the chosen planarizing material against the wafer with an optical flat. The intent of this procedure is that most of the planarization material will be squeezed out from between the crystal-flat and the wafer, leaving the dicing channels filled and a thin layer of "residual" material across the entire wafer. After etching away the optical flat, the planarization material is etched back to the wafer surface (and circuit metallization) in an oxygen plasma (any other etch chemistry would etch the SIS mixer circuits). The degree of planarization depends on the initial level of planarization after the crystal-flat is removed, the uniformity of the thin layer of "residual" material, and how uniformly the planarized material etches. We have already examined a number of possible material classes for this application- from different forms of polyethleyne to different manufacturers of bonding wax for lapping to a new beta version of a higher temperature Apiezon-W wax. Some of them have given excellent planarization results, but have failed with respect to adhesion or softening temperatures. More recently we have started an investigation of two component epoxy systems. These materials satisfy all thermal and chemical stability requirements; however work needs to be done on uniformity of oxygen etching and resulting stress on the wafer (too much stress causes the wafer, which essentially has scribed lines [the dicing avenues] across most of the wafer, to break).

(5) We will work with NRAO and HIA in continuing to develop appropriate test structures for

material evaluation. In order to obtain the desired yields from SIS mixer wafers, fewer variations of a mixer design on a single wafer can be tolerated. This strategy puts an increased demand on both knowledge of the properties of the two dielectric layers and the three Nb metallization layers and control of these properties from run to run. More compact and easily testable structures are needed to facilitate this work. Our change from evaporated SiO_x to sputtered SiO_x should also facilitate this work since some of the designs of these test structures require large area dielectric fields.

(6) We will continue to monitor the Nb film stress in our Nb/Al-oxide/Nb trilayer material and in our m3 wiring layer. We expect that with new material test structures, we will be able to correlate film stress with Nb penetration depth. It is also important to note that while all of our stress measurements are performed on Si/SiO_2 wafers, our mixers are fabricated on quartz wafers. It is not possible to measure stress with our current laser based stress measurement system since reflections from the uncoated substrate will occur at both the top and bottom surfaces, while the Nb coated quartz wafer will only have reflections at the top surface. We have recently arranged for a commercial firm to mechanically scan a set of 2" quartz wafers, have us deposit Nb and then rescan the wafer to measure the film stress. We anticipate results that correlate well with our laser based system made on alternating runs of Si/SiO2 wafers. If these results differ; however, then further work will have to be performed to determine if there is a constant offset between the measurements at different pressures or if the acquisition of a stylus based stress measurement system is needed (a Dektak Inc *6M* system [11] with the stress measurement option is $42,800).

(7) Fabrication of Band-3 and Band-6 SIS mixer element 50mm wafers for HIA and NRAO is a major emphasis of this research. It is understood that UVA intends to fabricate 17 wafers for HIA and 4 wafers for NRAO with acceptable mixer performance during the period of this proposal, the majority of these elements to be fabricated in the 2^{nd} and 3^{rd} years. It is also expected that we will interact with NRAO and HIA in the design of any new mask sets for these elements.

FACILITIES

Laboratory:

Superconducting Device Laboratory

The Superconducting Device Laboratory (SDL) operates within the Applied Electrophysics Laboratory in the Department of Electrical Engineering at the University of Virginia. The primary fabrication facility consists of a 6,000 square foot laboratory, of which roughly two-thirds is clean room space. The AEpL program involves graduate and undergraduate students, approximately forty of which are currently involved in ongoing research.

Other:

FIB facility

The Materials Science and Electrical Engineering Departments maintain an FEI-200 focused ion beam (FIB) system with a 5nm Ga+ beam size. The FIB tool (which resides in the MS dept.) is integral to the HEB research of this proposal. This facility is two minutes walking distance from the AEpL laboratory and is available for use to this research.

FIR laboratory

A cooperative research program with the Department of Physics has led to the establishment of our Far Infrared Receiver Laboratory. The FIR laboratory is fully equipped to design, assemble and evaluate millimeter and submillimeter wavelength mixers and multipliers. This facility is also only two minutes walking distance from the AEpL laboratory and is available for use to this research.

Equipment:

The AEpL is fully equipped for the investigation and fabrication of complex Nb superconductive circuits. Processing equipment includes: UHV loadlocked 3" DC magnetron dedicated trilayer system for sputtering of aluminum, niobium and gold with the option of ion cleaning, HV loadlocked 3" sources for the sputtering of Ti, Nb, Al, Au and Ge with the option of ion cleaning, single target multi use RF diode sputtering system, UV and two DUV contact aligners for photolithography with submicron resolution, Karl Zeiss 982 fieldemission scanning electron microscope, two fluorine based reactive ion etchers, loadlocked chlorine based reactive ion etcher, multisource (six) Temescal E-beam vacuum evaporator, dedicated ion milling station, Tencor surface profiler, FSM laser based thin film stress measurement system, an Allied High Tech Multitech-Prep 8 automatic wafer thinner, a Phillips Analytical xray diffraction system and a Disco wafer dicing saw.

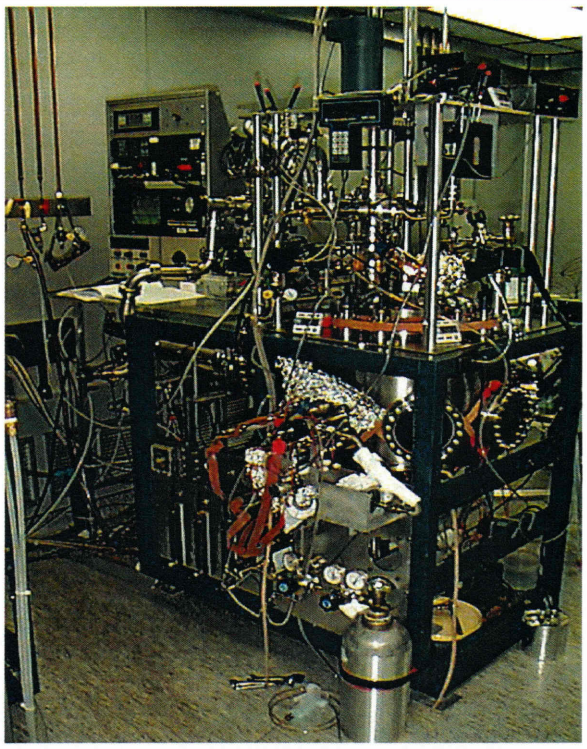

Figure 3. Loadloacked multitarget trilayer sputtering system dedicated for depositing Nb/Al-oxide/Nb films for superconducting work.

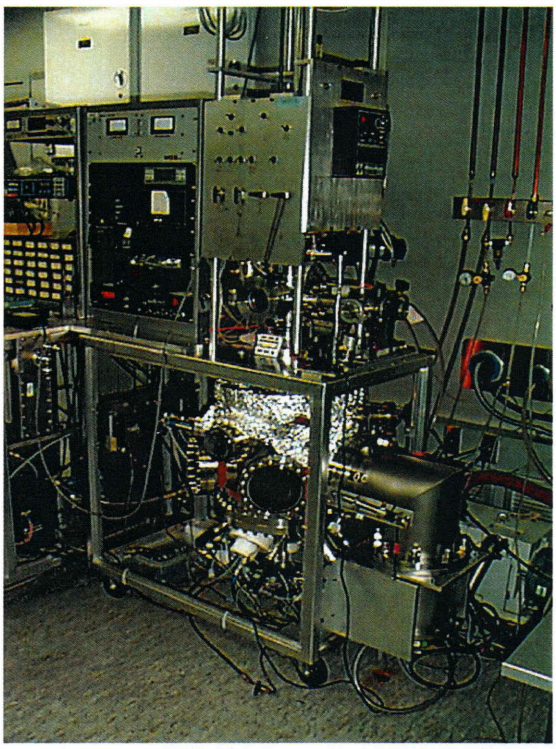

Figure 4. Loadlocked multitarget sputtering system dedicated for depositing Nb(m3), Ti, Au and PdAu films.

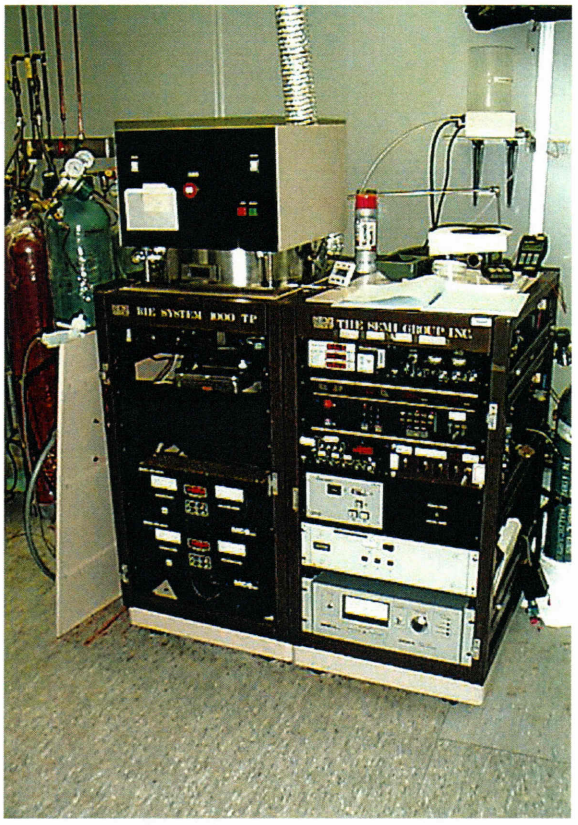

Figure 5. Semigroup RIE (one of three RIE's) available for use in this research.

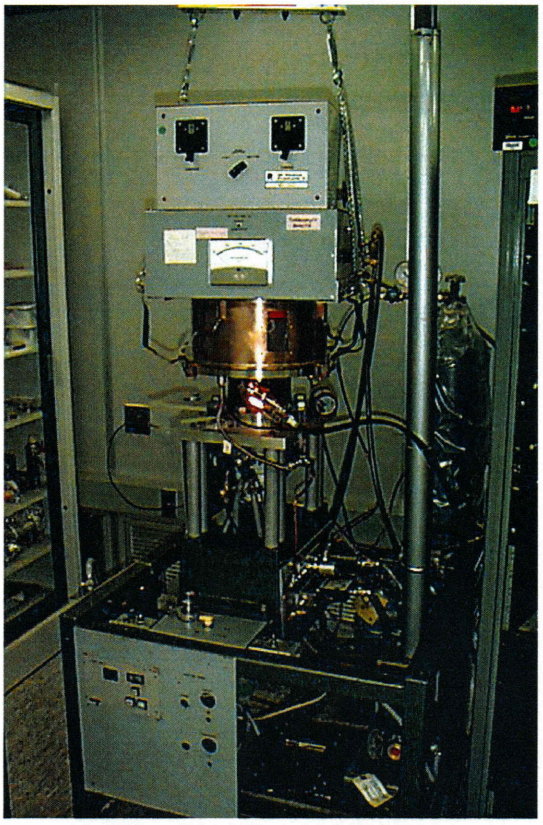

Figure 6. 20 year old, general purpose RF diode sputtering system presently used to deposit SiOx films for this research.

REFERENCES

[1] D.W. Hoffman and J.A. Thornton, "The Compressive Stress Transition in Al, V, Zr, Nb, and W Metal Films Sputtered at Low Working Pressures," Thin Solid Films, vol. 45,387-396, 1977.

[2] K. Kuroda and M. Yuda, Yuda, Niobium-stress influence on Nb/Al-oxide/Nb Josephson junctions, J. Appl. Phys. 63 (7), 2352-2357, April 1988.

[3] M. Yuda K. Kuroda and M. Yuda, Niobium-stress influence on Nb/Al-oxide/Nb Josephson junctions, J. Appl. Phys. 63 (7), 2352-2357, April 1988.

[4] T. Imamura, T. Shiota, and S. Hasuo, "Fabrication of High Quality Nb/AlOx-Al/Nb Josephson Junctions: I - Sputtered Nb Films for Junction Electrodes," IEEE Trans. On Appl. Superconductivity, vol. 2, 1, 1-14, March 1992.

[5] P. A. Booi, C.A. Livingston, and S. P. Benz, Intrinsic Stress in dc Sputtered Niobium," IEEE Trans. on Appl. Superconductivity, vol. 3, 2, 3029-3031, June 1993.

[6] R.S. Amos, P.E. Breyer, H.H. Huang, and A.W. Lichtenberger, "Stress and Source Conditions of DC Magnetron Sputtered Nb Films," IEEE Trans. on Appl. Superconductivity," vol. 5, 2326-2329, June 1995.

[7] William W. Clark IV, Joseph M. Beatrice and Arthur W. Lichtenberger, "Effects of Geometry and

Hardware on the Stress of Nb Thin Films", IEEE Trans. on Appl. Superconductivity, June 2001.
[8] R.B. Bass, L.T. Lichtenberger, and A.W. Lichtenberger, Effects of Substrate Preparation on the Stress of Nb Thin Films" Submitted to the IEEE Transactions on Applied Superconductivity 2002
[9] W. Clark, J.Z. Zhang and A.W. Lichtenberger, "Ti Quadlevel Resist Process for the Fabrication of Nb SIS Junctions" Submitted to the IEEE Transactions on Applied Superconductivity 2002
[10] EVG-620 Aligner, 3701 E. University Drive, Suite 300, Phoenix, AZ 85034,
[11] Dektak 6M Stress Measurement System, Veeco, 112 Robin Hill Rd, Santa Barbara CA, 93117

Budget Detail

	Year 1 7/1/02-6/30/03	Year 2 7/1/03-6/30/04	Year 3 7/1/04-6/30/05	Total
A. Personnel & Benefits				
1. A. W. Lichtenberger, PI				
50% effort CY @ $89,900 CY	44,950	44,950	44,950	134,850
Allowance for salary increase	787	2,159	3,572	6,518
Fringe Benefits - 23.25%	10,634	11,071	11,281	32,986
2. Research Scientist				
100% effort CY @ $45,000 CY	45,000	45,000	45,000	135,000
Allowance for salary increase	787	2,161	3,576	6,524
Fringe Benefits - 23.25%	10,646	11,083	11,294	33,023
3. L. Salinas, Lab & Res. Pract. III				
50% effort CY @ $28,566 CY (Part-Time)	14,283	14,283	14,283	42,849
Allowance for salary increase	250	686	1,135	2,071
Fringe Benefits - 10.5%	1,526	1,572	1,619	4,717
4. Graduate Research Assistant				
88 hrs. mo. x $16.10/hr. x 12 mos.	17,001	17,001	17,001	51,003
Allowance for salary increase	297	816	1,352	2,465
5. Graduate Research Assistant				
88 hrs. mo. x $16.10/hr. x 12 mos.	0	17,001	17,001	34,002
Allowance for salary increase	0	817	1,351	2,168
SUBTOTAL PERSONNEL & BENEFITS	**$146,161**	**$168,600**	**$173,415**	**$488,176**
B. Materials and Supplies				
1. Quartz, Si and other subtrates	20,000	35,000	32,000	87,000
2. Targets	20,000	20,000	20,000	60,000
3. Special Resists & Chemicals	21,500	25,500	25,500	72,500
4. Gases and Liquid N2 and He	5,000	5,000	5,000	15,000

Budget Detail

	Year 1 7/1/02-6/30/03	Year 2 7/1/03-6/30/04	Year 3 7/1/04-6/30/05	Total
C. Equipment - Sputtering System/Repair Maintenance				
1. SiOx Sputtering System	100,000	0	0	100,000
2. Replace Broken Equipment	9,000	20,000	20,000	49,000
3. Repair/Maintenance of System	9,000	25,000	25,000	59,000
4. 2 Dell Laptop Inspiron 8200	7,000	0	0	7,000
5. Dell Dimension Computer	0	2,500	0	2,500
D. Technical Services				
1. Cleanroom Fees	15,000	21,000	21,000	57,000
2. Machine Shop	10,000	10,000	10,000	30,000
E. Tuition Remission	6,350	12,700	12,700	31,750
F. Travel - Conferences	3,000	3,000	3,000	9,000
F. Other Contractual Services				
1. Publications	1,200	1,800	1,500	4,500
2. Copying, communications	470	505	680	1,655
TOTAL DIRECT COSTS	**$373,681**	**$350,605**	**$349,795**	**$1,074,081**
G. Indirect Costs - 48% MTDC	116,319	139,395	140,205	395,919
TOTAL	**$490,000**	**$490,000**	**$490,000**	**$1,470,000**

BUDGET NOTES

* Personnel - Faculty appointments are generally effective calendar year (CY/12 mos.) beginning July 1 or Academic Year (AY/9 mos.) beginning September 1.

* Graduate Research Assistants (GRAs) and Undergraduate Research Assistants (URAs) - Costs are estimated based on the minimum and maximum payments for the academic year established by the University Office of the Vice-President and Provost. All compensation in SEAS proposals are within these guidelines.

* Salary Increases - A 3% salary increase is applied to a majority of SEAS proposals, effective 11/25/02, and is accumulated annually from this date. Faculty increases are based on contributions in academic and research areas and are approved by the State of Virginia Budget Office. Staff increases are based on State of Virginia proficiency guidelines. New salaries are given as soon as they are available.

* Fringe Benefits - The University of Virginia's fringe benefits rates, as they apply to sponsored programs are proposed as follows: 23.25% for faculty and professional staff, 26.25% for classified staff, 10.5% for part-time faculty and staff and 7% for wage employees and summer effort by faculty with AY appointments. Fringe benefits apply to graduate and undergraduate research assistants if not enrolled full time (generally 12 hrs. for undergraduates and 9 hrs. for graduates).

* Materials and Supplies - Laboratory supplies for specific use in the research project (quartz, Si and other substrates, targets, special resists and chemicals, gases and liquid N2 and He). Does not include office or other general purpose supplies.

* Equipment: Sputtering System - $100,000 year 1: (1) vacuum chamber and associated flanges, access door, RF platter assembly and Ferrofluidic RF/H2O/Rotational feedthroughs, water cooled RF target assembly, and system cart-frame, (2) two RF power supplies and associated two RF matching networks, (3) pump, (4) ionguage and residual gas analyzer, (5) linear translator, (6) water chiller, and (7) Baratron pressure guage and power supply. Two Dell Laptop Inspiron 8200 computers at $3,500 each for a total of $7,000 in the FIRST YEAR Laptop computers with fast process speeds, large RAM and Harddrives are needed to allow us to store and manipulate all needed process data and images as wafers are fabricated in the cleanroom at all the different equipment locations. Replace Broken Equipment -be able to purchase new equipment when things break and can't be easily or economically repaired - $9,000 year 1 and $20,000 years 2 and 3. Repair and Maintenance of Sputtering System - $9,000 year 1 and $25,000 years 2 and 3. Dell Dimension Computer for the PI to conduct the research project - $2,500 in year 2.

* Laboratory Fees for Cleanroom Facility - The Semiconductor Device Laboratory's Cleanroom facility is provided for sponsored research programs and its operational costs must be obtained from individual research grants and contracts requiring use of this facility. Fees are based on usage of the facility in the following manner: $500 per month for those needing direct access to the cleanroom; $200 per month for those needing access only to areas outside the cleanroom.

* Central Support Services (machine shop) - Rates are established for each fiscal year by the managing unit and approved by the University Office of the Comptroller. Rates are applied equally to all University users.

* Tuition Remission - Effective September 1, 1990, it is the policy of the University of Virginia to provide tuition for graduate research assistants as partial compensation for services.

* Travel - Trips to related technical conferences, workshops, seminars, etc.

* Publications - Publications and page charges in related technical journals.

* Other Costs - Estimated project related costs for photocopying, long distance phone and FAX, etc. are based on prior SEAS research experience. The University of Virginia system, through copy cards, etc., is able to document such costs as related to the project.

* Facilities and Administrative (F&A) (Indirect/Overhead) Costs - The University of Virginia's negotiated MTDC F&A rates with DHHS per agreement of 8/21/00 are: 7/1/98 - 6/30/2002, and until further amended, 48% "on campus" and 23.6% "off-campus". (Note: The MTDC base consists of total direct costs less individual equipment items in excess of $2,000, alterations and renovations, patient care costs, stipends, tuition remission and rental costs of off-campus facilities.) Includes F&A on the first $25,000 of subcontracts.