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Subject: Correlator IPT Quarterly Report

2.6 Correlator IPT

2.6.1 Prototype correlator

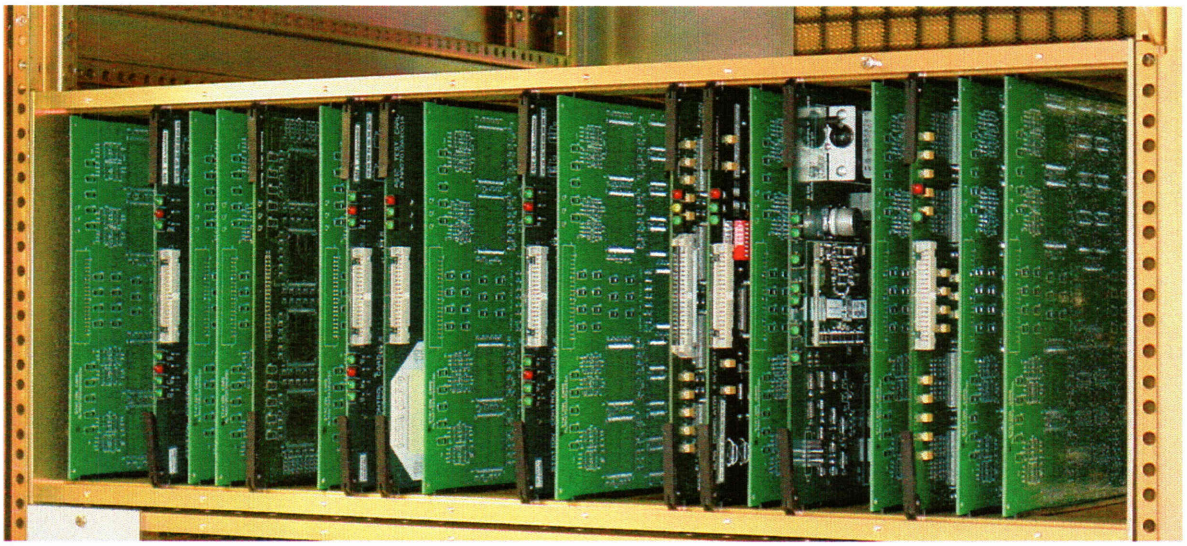
Work continued on the prototype two-antenna correlator. An agreement was reached with the Back End Subsystem group on the interface details for the optical receiver/demultiplexer card which plugs into the correlator station bin. Designs were completed for the quadrant control card, correlator motherboard, and front panel data port card. Printed circuit board layouts were completed 100% for the station motherboard, 95% for the front panel data port card, and 90% for the correlator motherboard. Modifications of the prototype designs were completed 100% for the filter card and station card, and 95% for the long term accumulator card (LTA).

Printed circuit boards were ordered and received for the filter card, station card, station interface board, station motherboard, and correlator interface board. Quotations were solicited for commercial assembly of all the boards in the prototype correlator, and some bids were received.

Assembly work began on the prototype correlator rack, and was 90% complete at the end of November (see photos).

Firmware development for advanced operation modes continued. Most of this is required in the long term accumulator card, including:

(1) Special adder tree modes required by the two-antenna prototype system;
(2) Support of LTA bin selection for subarray-based binning (e.g., use of the nutating subreflector) and baseline-based binning (e.g., sideband separation)
(3) Support of the operational environment of the two-antenna prototype system.



Partially populated prototype correlator station bin

Front (left) and rear of prototype 2-antenna correlator rack showing card cages, cards, backplanes, fans, and power supplies mounted.

2.6.2 Possible performance enhancement

A preliminary study of a possible enhancement of the baseline correlator performance resulted in ALMA Memo 441, Enhancing the Performance of the Baseline ALMA Correlator. By substituting an advanced filter card with multiple simultaneous output bands for the single-band output present filter design, it is possible to achieve much greater frequency resolution in the widest bandwidths, or to analyze several narrow bands simultaneously with even higher frequency resolution. It is likely that this could be achieved at modest cost without serious effect on the baseline correlator delivery schedule.

2.6.3 Schedule

The goals for October-November were:

(1) complete the designs for all prototype correlator cards;
(2) achieve 90% completion on remaining printed circuit board layouts;
(3) receive printed circuit boards for at least 4 newly-laid-out cards;
(4) achieve 90% completion of rack assembly.

All these goals were met.

The goals for the next quarter are:

(1) complete assembly of all printed circuit boards for the prototype correlator;
(2) begin integrated testing of cards in the rack;
(3) achieve 90% completion of integrated testing of at least 50% of the cards in the rack.

2.6.4 ALMA Second Generation Correlator (2GC)

The European team met in October to review three different FIR filter bank options -including polyphase filter- and to 'freeze' the 2GC system block diagrams.

A two-stage FIR filter architecture with a quadrature LO has been adopted. The baseband converter allows us to select a 62.5 MHz portion of the 2 GHz input baseband anywhere within the 2 GHz. The 2 GHz baseband is synthesized with partly overlapping sub-bands to achieve good control of edge effects. The 2-stage FIR filter comprises a 128-tap coarse filter and a 64-tap sharp filter equivalent to 2048-tap filtering; it is followed by a 16-bit complex-to-real output conversion stage and 3- or 4-bit requantization. Simulations have been completed and various implementations in existing FPGAs have been considered. VHDL description at different levels of the FIR filter has started.

The 2GC System Design Study document and system block diagrams have been updated. The complete set of 2GC specifications reflecting our filter bank technical choice and simulations has been issued. It will be sent to the ASAC for information and comments together with revised illustrations of spectral flexibility.

The 2GC correlator chip architecture and design is ongoing at ASTRON. Following the study of possible configurations with our serial backplane demonstrator a market survey is in progress.

In November the European team has proposed to ESO detailed Phase 2 work units and a top level planning with a first milestone in April 2003 (System Requirements Review).