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ALMA1 Production Chip Failures

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General

Introduction

This document details the failures of the ALMA1 Chips, based on the initial evaluation of five Correlator Cards. ALMA1s from the production run were used in construction. Five faulty chips were found. These have been labeled B1 through B5. Also there are problems associated with package quality.

Date Codes

All failed chips have the Date Code 21202. On the five cards, there are 237 chips with the date code 21202, and 83 chips with the date code 7204. 237/83 = 2.85 so statistically we would expect one 7204 failure for every three 21202 failures.

Coordinate Systems

A coordinate system is used to describe the location of each error.
Location (AS1 to AS64) identifies the specific ALMA1 chip on a Correlator Card.
Block (0 to 15) identifies the specific 256 lag block in an ALMA1 chip.
Lag (0 to 255) identifies the specific Lag in a Block.
Bit (0 to 15) identifies the specific Bit in an output Lag.

Test Set Up

Tests were performed using our two test fixtures, which each can hold two Correlator Cards controlled by an LTA. Cooling is provided by a fan blowing room temperature air on the cards. The errors are assumed to be not frequency sensitive, unless specifically so stated.
Temperature measurements were performed at 125 MHz, with test 506 or 516 running.
Temperature was measured by a sensor applied to the center of the package.
Temperatures of chips to the left and the right of the faulty chip are also shown.

Infant Mortality

Infant Mortality refers to a chip initially testing good, then testing bad after being burned in for an amount of time. In the table, under the Infant Mortality column, a Yes indicates that the chip met these conditions. A No indicates the chip was bad on initial testing.

Package Quality

Data Translation reported that it was necessary to turn off all component lead measurement criteria in order to place ALMA1s onto the boards. There was a 25%-40%

rejection rate of ALMA1s per tray. The measurement was performed 100% by the placement equipments visual measurement alignment system. This was based on a length-wise and cross-wise deviation of .20mm and a length-wise deformation of .25mm. These are liberal settings. Exceeding these settings runs the risk of excessive solder issues (which were experienced). When the system recognizes one lead outside of any of these parameters, the part is rejected.

Chip Failure Analysis

Chip B1

This chip is located on Correlator Card SN1, Location AS44.
The error occurs in Block 6, Lag 191.
Bit 3 is stuck low.
This showed up as an error in the NRAO tests: 503, 507, and 509.
Spray cooling did not affect the error.
This error was present on initial testing.

Chip B2

This chip is located on Correlator Card SN1, Location AS56.
The error occurs in Block 12, Lag 247.
Bit 8 is stuck high.
This showed up as an error in the NRAO tests: 511 514.
Spray cooling temporarily eliminated the error.
This error was not present on initial testing. The error appeared after 96 hours of burn-in.

Chip B3

This chip is located on Correlator Card SN1, Location AS64.
The error occurs in Block 13, Lag 213.
This shows up as an error in the NRAO tests: 60a, 605.
When the output should read 0xAAAA, it reads 0x0000.
When the output should read 0x5555, it reads 0x0001.
All other tests work fine.
The 60a and 605 tests have FULLACC turned off.
This suggests the error has something to do with the multiplexer that skips the four bits when FULLACC is turned off.
Spray cooling did not affect the error.
This error was present on initial testing.

Chip B4

This chip is located on Correlator Card SN2, Location AS29.
The error occurs in Block 11.
Bit 10 is stuck low.
NRAO test 511 and 514 have errors for a large number of lags.
The error also appeared in test 512, 513, 515, 516, 517, 518, 519, and 615 as only lag 255 having bit 10 stuck. Testing the next day had this portion of the errors gone, but the errors of test 511 and 514 remained.
Spray cooling reduced the number of lags with errors.
These errors were not present on initial testing. The errors appeared after a few hours of burn-in.

Chip B5

This chip is located on Correlator Card SN3, Location AS2.
The error occurs in Block 1, Lag 117.
The accumulation is less than what it's supposed to be by 1 to 4 counts.
Spray cooling made the count be less by a larger number of counts.
The error is speed dependent, beginning at around 125 MHz.

Summary of Chip Data

Bad Chip	DATE CODE	CC SN	Loc AS#	Block	Lag	Infant Mortality	Stuck Bit	Speed Dependent	Cooling Effect	Temperatures Deg C Left	Chip	Right
B1	21202	1	44	6	191	No	3-low	No	No	42	42	42
B2	21202	1	56	12	247	Yes	8-hi	No	Yes		46	45
B3	21202	1	64	13	213	No		No	No		42	43
B4	21202	2	29	11	Many	Yes	10-low	No	Yes	37	34	38
B5	21202	3	2	1	117	No		Yes	Yes	39	39	39

Discussion

All of these errors appear to be internal to the ALMA1 Chips as opposed to being board related or ESD handling related.

Some of the faults could be due to the test vectors not checking the failed condition logically.
Another possibility is a marginal failure condition that passed in the test vector test but fails on the card.

The failures of chip B5 being speed related clearly would not have been picked up by the test vectors.

Since chips B2 and B4 displayed infant mortality, they were probably good when the test vectors were applied. Also the fact that spray cooling affects them supports that there is something marginal.

Chips B1 and B3 were not affected by spray cooling and the errors were present on first testing. They are the best candidates for bad test vectors.

It would be of interest to retest all these chips after removal.

All the bad chips being from the same Date Code is suspicious, but this could be a coincidence.

The chips displaying infant mortality is more worrisome than bad test vectors. With bad test vectors, we may have to replace chips initially, but would then have a reliable system. If these failures are truly infant mortality, then we could have a reliable system after they are replaced. The worst case would be for chips to fail regularly in the field.

The Two Antenna Correlator used ALMA1s from our prototype run. There was one infant mortality failure in the fully populated card. The eight partially populated cards (64 chips total) have been running for about 6 months with no failures. That gives about 300,000 chip-hours versus about 25,000 chip-hours burn-in on the production chips. However these chips, being from a different run, could have different characteristics from the production run.

One prudent step might be for Innotech to delay further production of ALMA1s until this problem is resolved, in case a new run of chips is required.

We are expecting fifteen more populated Correlator Boards soon. This will allow the collecting of more data. We will also fit a test bin to allow our burning in an additional eight cards, to test for further failures.

Questions for Innotech

Questions about the Chip Failures

1. Could we get a listing for the 40,000 chips (or however many are available) of how many chips are in each date code?
2. Could we get a listing of which date codes are grouped together as coming from the same process run?
3. Was your test vector failure rate a function of date code?
4. What do the date code numbers 7204 and 21202 actually mean?
5. Would temperature cycling the chips or boards in an oven would be useful in triggering failures?
6. Can the chips be removed from the boards and still be retested?
7. Does Innotech want to do the ALMA1 removal and replacement work? If so when would you want the boards?

Questions about Package Quality

1. What is the step by step process the chips go through during packaging and subsequent testing?
2. At what point(s) in the process is the quality of the pins checked?
3. What are the names of the firms involved and where are they located?
4. Could the Pins have been damaged from rough handling in shipping?