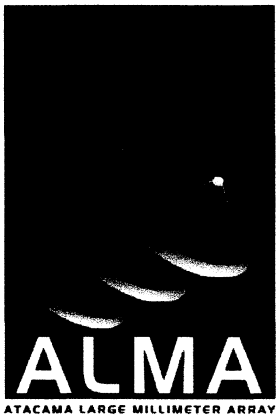

Atacama Large Millimeter Array

64 Antenna Correlator Specifications and Requirements

ALMA-60.00.00.00-001-B-SPE

Version: B

Status: *Released*

2005-05-10

Prepared By:		
Name(s) and Signature(s)	**Organization**	**Date**
Ray Escoffier and John Webber	NRAO	2005-05-10
Alain Baudry Alain Baudry	Observatoire de Bordeaux	2005-05-10
Approved By IPT Leads:		
Name and Signature	**Organization**	**Date**
John Webber John Webber Digitally signed by John Webber DN: CN = John Webber, C = US, O = NRAO, OU = ALMA Date: 2005.05.20 09:39:50 -04'00'	NRAO	
Alain Baudry Alain Baudry Signature numérique de Alain Baudry ID : cn=Alain Baudry, ou=OASU, LAAB, c=FR Date : 2005.05.19 19:19:41 +02'00'	Observatoire de Bordeaux	
Approved By System Engineering: Name and Signature	**Organization**	**Date**
Dick Sramek Richard Sramek 2005.06.01 12:30:45 -06'00'	NRAO	
Christoph Haupt Christoph Haupt 2005.06.23 00:23:15 +02'00'	ESO	
Configuration Control Board Approval:	**Organization**	**Date**
Christoph Haupt Christoph Haupt 2005.06.23 00:23:21 +02'00'	CCB Secretary	
JAO Director Release Authorization:	**Organization**	**Date**
Massimo Tarenghi A. Araya for M. Tarenghi 2005.07.06 12:55:13 -04'00'	JAO	

Table of Contents

Revision History:

1998-Sep-18: Added chapter number to section numbers. Placed specifications in table format. Added milestone summary.

1999-Apr-09: Revised milestone dates and made date format conform to adopted standard. Revised tables and some text to reflect adoption of digital FIR filter. Changed text to reflect architectural change in delay line implementation. Revised block diagram.

2000-Feb-04: Changed maximum number of antennas to 64. Changed block diagram to correspond to current thinking about system architecture.

2000-Mar-31: Revised from MMA to ALMA baseline correlator. Incorporated changes resulting from correlator and systems PDRs.

2000-Apr-12: Clarified path of digitizer development and meaning of subarrays.

2000-Dec-05: Minor revisions to a few numbers. Addition of section describing possibilities for a future correlator.

2001-Feb-07: Minor revisions to text, mostly editorial. FX correlator reference added.

2002-Jan-07: Description of sub-arraying capability modified. Revised section on future correlator.

2004-Feb-10: Major revision for version B including operating modes with tunable filter bank.

2004-July-19: Correct error in table 2 (1 filter, 31.25 MHz, 4-bit x 4-bit).

2005-Jan-28: Minor wording changes to sec 2, 3.3, 3.4, and 5.

2005-Mar-07: Added Document lists, added definitions, changes to figure 1

2005-May-10: Change font on sections 2.1 and 2.2, add dump column to tables 2, 3, and 4, and correct single error in table 2.

ALMA CORRELATOR SPECIFICATION

1 Summary

Introduction and Summary

This document describes the ALMA correlator. The ALMA correlator is a lag correlator with a digital filter bank in the input section of the system that permits it to operate as a digital hybrid correlator. The system can also be operated in a wideband time division mode.

Overall system specifications for the ALMA correlator can be seen in Table 1.

Table 1. ALMA Correlator Specifications

Item	Specification
Number of antennas	64
Number of baseband channel inputs per antenna	8
Input sample format	3 bit, 8 level at 4 GSample/s per baseband channel
Correlation sample format	2 bit, 4 level and 4 bit, 16 level; Nyquist and twice Nyquist
Maximum baseline delay range	30 km
Hardware cross-correlators per baseline*	32,768 leads + 32,768 lags
Hardware autocorrelators per antenna*	32,768
Typical performance in digital hybrid modes	8192 spectral points provided for each pair of baseband inputs**
Product pairs possible for polarization	HH, VV, HV, VH (for orthogonal H and V)

* 62.5 MHz correlators (125 MHz clock rate), divide by 32 to get number of equivalent 2 GHz correlators
** Resulting in 8192, 4096 or 2048 spectral points across the baseband spectrum, depending on polarization mode

The ALMA correlator evolved from an initial system design (described in ALMA memos 166 and 194) with a pure lag architecture incorporating simple FIR digital filter cards (described in ALMA memos 204 and 248) to a design implementing a digital hybrid correlator with the incorporation of 32-element digital filter bank cards.

The fundamental change to the original design, the replacement of the digital filter card with a tunable filter bank card, is based on the design philosophy of the proposed 2GC system (and is described in ALMA memo 476). The use of a 32-element filter bank instead of a single digital filter has the effect of increasing the performance of the system by factors of up to 32 in spectral resolution.

A single wideband time-packet or time-division mode of the original system design has been retained in the operation of the correlator to provide high time resolution where this parameter is of highest importance.

2 Applicable and Reference Documents

2.1 Applicable Documents List (ADL)

The following documents form part of this SOW. In the event of conflict between the documents referenced here and this document, this SOW shall take precedence.

No.	Document Title	Reference
AD 01	ALMA Product Assurance Requirements	ALMA-80.11.00.00-001-B-GEN
AD 02	ALMA System Electromagnetic Compatibility Requirements	ALMA-80.05.01.00-001-B-SPE
AD 03	ICD between Site and Correlator	ALMA-20.00.00.00-60.00.00.00-A-ICD
AD 04	ICD between Back-End and Correlator	ALMA-50.00.00.00-60.00.00.00-A-ICD
AD 05	ICD between Correlator and Computing Correlator Software	ALMA-60.00.00.00-70.40.00.00-A-ICD

2.2 Reference Documents List (RDL)

No.	Document Title	Reference
RD 01	ALMA Project Plan, Version II	Dated September 23rd, 2004
RD 02	ALMA Design Reviews - Definitions, Guidelines And Procedures	ALMA-80.09.00.00-001-B-PLA
RD 03	ALMA Product Tree	ALMA-80.03.00.00-001-M-LIS

2.3 Definitions, Abbreviations and Acronyms

AD	Applicable Document(s)
ADL	Applicable Documents List
ALMA	Atacama Large Millimeter Array
AOS	Array Operations Site
CCC	Correlator Control Computer
CDP	Correlator Data Processing computer
Corr	Correlator
DTS	Data Transmission System
ICD	Interface Control Document
IPT	Integrated Product Team
JAO	Joint ALMA Office
LTA	Long Term Accumulator
NTC	NRAO Technology Center
OSF	Operations Support Facility
QCC	Quadrant Control Card
RDL	Reference Document(s) List
SCC	Station Control Card
SOW	Statement of Work
TB	AOS Technical Building
TFB	Tunable Filter Bank

3 System Block Diagram

A block diagram of the ALMA correlator can be seen in Figure 1. This figure also includes some details of the ALMA digitizers, the DTS transmission system, and the real time computer and although these components of ALMA are not part of the correlator they are shown here for clarity.

The input stage of the correlator is the tunable filter bank card. This card is driven by the output of the ALMA DTS receiver/demux card which recovers the 3-bit samples generated by the ALMA digitizer and sent via optic fiber from the remote antennas over the ALMA Digital Transmission System. The filter bank card can be configured as 32 digital filters with either 62.5 or 31.25 MHz bandwidth. The center frequency of each filter is independently tunable.

The station card has several functions with the main ones being the implementation of bulk delay for geometric delay adjustment and being a router between the filter card outputs and the correlator inputs. Programming in the station cards determines how the 32 filter outputs of the filter card are processed in the correlator system.

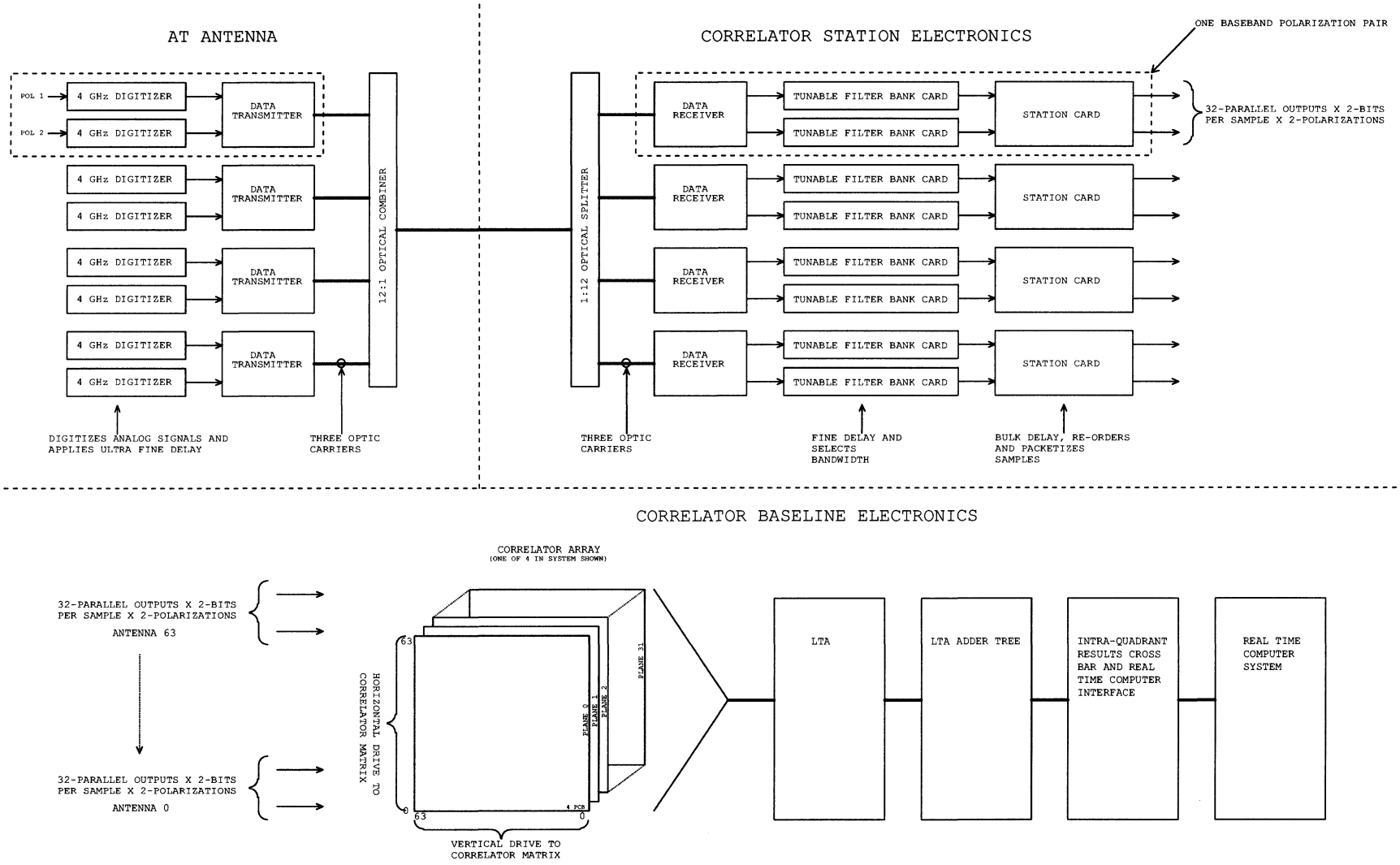

Figure 1 Correlator Block Diagram

The correlator portion of the system consists of 32 correlator planes each implementing a 64-by-64 correlation matrix. When samples from all 64 antennas in the ALMA main array drive this matrix (both axes), autocorrelations are produced on the matrix diagonal and cross correlations and produced elsewhere (with leads on one side of the diagonal and lags on the other).

The LTA (Long Term Accumulator) subsystem seen in figure 1 takes short 1 msec or 16 msec integrations output by the ALMA custom correlator chips and provides long term integration for them. The LTA also provides the interface into the real time computer system.

The ALMA correlator is designed in 4 essentially identical quadrants. Each quadrant processes the output of two of the eight baseband channel outputs of the array. For polarization observations, the two baseband channel outputs processed in a quadrant must be of opposite polarization.

4 Sub-system Description

4.1 Tunable filter bank card

Each 2 GHz IF channel input signal to a filter card consists of 32 time demultiplexed 3-bit samples, corresponding to a data flow of 4 GS/s. The basic function of the digital filter card is to develop 32 subchannels from this 2 GHz input as follows. First, the input signal is processed by a complex digital mixer driven by a digital LO to translate each subchannel frequency center to zero frequency. Second, each mixer complex output is sent to 2 parallel filters processing the real and imaginary data streams; each of these 2 parallel filters is implemented in a 2-stage architecture subsystem. The first stage is a low-pass decimation (32 tap-weight) filter. The second stage is a high performance low-pass filter synthesizing the selected subchannel band shape. After decimation and complex to real conversion the signal is 2-bit or, according to the observation schedule, 4-bit requantized. Each filter then produces streams of 2- or 4-bit samples at 125 MHz.

The 32-filter array allows us to select subchannels with a maximum bandwidth of 62.5 MHz that can be positioned anywhere within the 2 GHz IF channel. One may also

select a 31.25 MHz bandwidth with an oversampling option.

Two digital filters are implemented in one fast FPGA, and 16 FPGAs are assembled on one card called a Tunable Filter Bank card. The entire filter bank consists of 64x2 cards per correlator quadrant and there are 4x2 cards for 4 pairs per antenna.

Each filter card is interfaced to the correlator subsystem via the station bin backplane. Each filter communicates with the station bin control computer via a standard CPLD interface chip; this interface allows the system to monitor the FPGAs and to download the FPGA personalities (bandwidths and filter shapes are selected using precalculated filter tap weights).

In addition to the 16-FPGA array and to the CPLD interface, up to 3 fine delay chips are implemented in the input data stream (one for each bit) on each Tunable Filter Bank card. The fine delay increments are operated in synchronism with the bulk delay implemented in the Station Cards. The fine delay chips are also used as receiver buffers which distribute the input signal data through the filter FPGA array.

4.2 Station Card

Each Station card provides two 4 millisecond RAM buffers, one for each of two filter card outputs (that is, each buffer holds approximately 4 milliseconds of samples at the full 4 GHz sample rate of a single baseband channel output). A station card provides several basic functions in the correlator:

- Provides bulk storage of the geometric delay adjustment
- Provides a versatile cross bar function between the filter card output and the correlators
- Provides lag generation for high frequency resolution modes
- Generates time packets of samples in time division mode

The two basic modes of the station card reflect the two operation modes of the ALMA correlator. Most observations will use the high frequency resolution digital hybrid configuration. In these cases, the input to the station card from a filter card(s) consists of from 1 to 32 separate bands each with a 125 MHz clock rate (either Nyquist sampled or twice Nyquist sampled for the oversampled modes of table 2, 3, and 4).

The other operating mode of the correlator is used in high time resolution observations. In this mode, the filter cards provide a pass through function and the station

card input is the full 4 GHz clock rate output of the ALMA digitizer(s) (with samples limited to 2-bits). In this mode, each one millisecond of the full bandwidth signal at the station card input is split into 32 one millisecond packets, each with a 125 MHz clock rate, in the station card RAM buffer. The 32 packets are routed to 32 correlator planes (see below) where cross correlation occurs.

4.3 Correlators

The basic building block of the correlator system is a matrix of 64-by-64 correlator blocks referred to as a correlator "plane". A correlator plane provides a 256 lag correlator circuit at each of the intersections of the matrix (a correlator plane thus has 64X64X256 total correlator lags). Each 256 lag circuit is driven by two different polarization signals from each of two antennas and can be programmed to be a single 256-lag block, to be two 128-lag blocks, or to be four 64-lag blocks to support the various polarization options. For 256 lag blocks on the diagonal of the matrix, the two antennas are the same and these yield autocorrelation results.

The next building block of the correlator system is the correlator "array" which consists of 32 correlator planes. There is one correlator array in each correlator quadrant and this array can process the full 2 GHz bandwidth for all 64 antennas for 2 baseband channels.

In the widest bandwidth (digital hybrid) mode, each of the 32 filter card outputs is processed in one of the 32 correlator planes of a correlator array (each filter card output will typically be a 62.5 MHz band, Nyquist sampled with a clock rate of 125 MHz). For narrower bandwidth modes, some filter card outputs are not processed and the freed up correlator planes are used to develop additional lags from the active filter card outputs. Lag generation for these modes is done on the station card.

In time division observations, the 32 correlator planes in a quadrant process the 32 time bins developed by the station card. Thus each plane handles 1/32 of the samples taken by an antenna digitizer and the 32 planes correlating station card time packet outputs with a 125 MHz clock rate keeps up with the 4 GHz original sample rate.

4.4 LTA subsystem, Final Adder and Data Port Interface

The Long Term Accumulator cards provide buffers, or longer term integration, for correlator chip results. For correlator chips operating in 1 msec Correlator Accumulation Mode (CAM), results transfer from correlator chip to LTA every 1 msec. The LTA stores 16 consecutive sets of 1 msec results in separate buffers and transfers these results to the Correlator Data Processing computer (CDP) every 16 msec.

For correlator chips operating in 16 msec CAM, results transfer from correlator chip to LTA every 16 msec. The LTA provides integration of these results for integer multiples of 16 msec.

The LTA provides the first two stages of an adder tree for modes where multiple correlator planes must be added together. The final stage of the adder tree is provided by the Final Adder cards. The interface to the CDP is provided by a Data Port Interface card that is driven by the Final Adder cards.

The LTA provides the necessary multiplication (shifting) of correlator results in planes that require this operation for support of 16 level correlation.

The LTA also provides control card functions for the correlator cards, as described in the next section.

4.5 Control cards

There are three types of control cards in the correlator system.

- Station control card (SCC)
- LTA/Correlator control card (LTA/CCC)
- Quadrant control card (QCC)

Each correlator system control card has a 16-bit Infineon C167 microprocessor that communicates with the correlator control computer over a serial CAN bus. The SCC and LTA/CCC control cards each support an 8-bit bidirectional communication bus over the bin motherboard to individual logic cards in the system. This bus is used for control and monitoring functions such as initial FPGA personality loading, mode programming,

active observation support, and various monitoring responsibilities. The QCC monitors voltages and temperatures in the system and can force a power down when a danger is detected.

Software for the ALMA correlator control cards is written in C using a Keil software development system.

5 Performance

The performance of the ALMA correlator, in terms of bandwidth and frequency resolution, can be seen in the next three tables. Table 2 gives the performance of a single quadrant of the correlator in modes in which a single baseband channel of a baseband pair is processed. Table 3 gives system performance in modes in which both baseband channels of a pair are processed but no cross correlations are performed. Table 4 gives the system performance in modes in which polarization cross correlations are generated.

The sensitivity column in tables 2, 3 and 4 does not reflect the initial ALMA 3-bit digitizer contribution to sensitivity but only the correlator efficiency after the 2-bit or 4-bit requantization at the filter output. Also, optimum sampler levels are assumed.

6 Size and Power Requirements

Each quadrant of the correlator consists of eight digital racks plus one power supply rack. Four of the digital racks house DTS receiver/demux cards, filter bank cards, and station cards sufficient to process the output of two of the 8 baseband channels produced by 64 antennas of the ALMA array. The other 4 racks house a single correlator array and LTA/CCC cards.

Power requirements are expected to be about 40 kW per quadrant including the DTS receiver cards.

Table 2 Mode chart with one baseband channel per quadrant being processed

Number of sub-channel filters	Total Bandwidth	Number of Spectral Points	Spectral Resolution	Velocity resolution at 230 GHz	Correlation	Sample Factor	Minimum dump time*	Sensitivity**
32	2 GHz	8192	244 kHz	0.32 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
32	2 GHz	4096	488 kHz	0.64 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
32	2 GHz	2048	976 kHz	1.28 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
16	1 GHz	8192	122 kHz	0.16 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
16	1 GHz	4096	244 kHz	0.32 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
16	1 GHz	2048	488 kHz	0.64 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
16	1 GHz	1024	976 kHz	1.28 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
8	500 MHz	8192	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
8	500 MHz	4096	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
8	500 MHz	2048	244 kHz	0.32 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
8	500 MHz	1024	488 kHz	0.64 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
4	250 MHz	8192	30 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
4	250 MHz	4096	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
4	250 MHz	2048	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
4	250 MHz	1024	244 kHz	0.32 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
2	125 MHz	8192	15 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
2	125 MHz	4096	30 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
2	125 MHz	2048	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
2	125 MHz	1024	122 kHz	0.16 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
1	62.5 MHz	8192	7.6 kHz	0.01 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
1	62.5 MHz	4096	15 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
1	62.5 MHz	2048	30 kHz	0.04 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
1	62.5 MHz	1024	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
1	31.25 MHz	8192	3.8 kHz	0.005 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.94
1	31.25 MHz	2048	15 kHz	0.02 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.99
Time Division Mode	2 GHz	64	31.25 MHz	40.8 km/s	3-bit x 3-bit	Nyquist	16 msec	1.00

*** Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).**

*** *Multiply numbers in this column by the 0.96 sensitivity imposed by the 3-bit input digitizer.**

Table 3 Mode chart with two baseband channels per quadrant processed with no polarization cross products.

Number of sub-channel filters	Total Bandwidth	Number of Spectral Points	Spectral Resolution	Velocity resolution at 230 GHz	Correlation	Sample Factor	Minimum dump time*	Sensitivity**
32	2 GHz	4096	488 kHz	0.64 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
16	1 GHz	4096	244 kHz	0.32 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
16	1 GHz	2048	488 kHz	0.64 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
16	1 GHz	1024	976 kHz	1.28 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
8	500 MHz	4096	122 kHz	0.16 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
8	500 MHz	2048	244 kHz	0.32 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
8	500 MHz	1024	488 kHz	0.64 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
8	500 MHz	512	976 kHz	1.28 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
4	250 MHz	4096	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
4	250 MHz	2048	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
4	250 MHz	1024	244 kHz	0.32 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
4	250 MHz	512	488 kHz	0.64 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
2	125 MHz	4096	30 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
2	125 MHz	2048	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
2	125 MHz	1024	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
2	125 MHz	512	244 kHz	0.32 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
1	62.5 MHz	4096	15 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
1	62.5 MHz	2048	30 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
1	62.5 MHz	1024	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
1	62.5 MHz	512	122 kHz	0.16 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
1	31.25 MHz	4096	7.6 kHz	0.01 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.94
1	31.25 MHz	1024	30 kHz	0.04 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.99
Time Division Mode	2 GHz	128	15.6 MHz	20.4 km/s	2-bit x 2-bit	Nyquist	16 msec	0.88

*** Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).**

*** *Multiply numbers in this column by the 0.96 sensitivity imposed by the 3-bit input digitizer.**

Table 4 Mode chart with two baseband channels per quadrant processed with polarization cross products.

Number of sub-channel filters	Total Bandwidth	Number of Spectral Points	Spectral Resolution	Velocity resolution at 230 GHz	Correlation	Sample Factor	Minimum dump time*	Sensitivity**
32	2 GHz	2048	976 kHz	1.28 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
16	1 GHz	2048	488 kHz	0.64 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
16	1 GHz	1024	976 kHz	1.28 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
8	500 MHz	2048	244 kHz	0.32 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
8	500 MHz	1024	488 kHz	0.64 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
8	500 MHz	512	976 kHz	1.28 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
4	250 MHz	2048	122 kHz	0.16 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
4	250 MHz	1024	244 kHz	0.32 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
4	250 MHz	512	488 kHz	0.64 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
4	250 MHz	256	976 kHz	1.28 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
2	125 MHz	2048	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
2	125 MHz	1024	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
2	125 MHz	512	244 kHz	0.32 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
2	125 MHz	256	488 kHz	0.64 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
1	62.5 MHz	2048	30 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
1	62.5 MHz	1024	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
1	62.5 MHz	512	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
1	62.5 MHz	256	244 kHz	0.32 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
1	31.25 MHz	2048	15 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.94
1	31.25 MHz	512	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.99
Time Division Mode	2 GHz	64	31.25 MHz	40.8 km/s	2-bit x 2-bit	Nyquist	16 msec	0.88

*** Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).**

*** *Multiply numbers in this column by the 0.96 sensitivity imposed by the 3-bit input digitizer.**