ALMA Annual External Review

Draft committee feedback

12 September, 2007

- We appreciate all of the hard work that has resulted in some very key progress, and in preparing for this review
  - Amazing amount of detail to prepare (and digest)
  - Also, thank you for the hospitality and efforts to respond to our needs and questions

Overview

- ALMA is a truly exciting and impressive endeavor
  - The payoff for our collective scientific communities that will come is something for all to take pride in the collective efforts to achieve this vision
  - The partnership represents some of the best talents coming together to achieve this vision.
- Progress has been impressive
  - Program has made good strides in addressing concerns and suggestions from previously referenced reviews.
  - Re-baselined plan, control and tracking have improved over the full project
  - Significant number of risks retired, and active ongoing risk assessment and mitigation
- Very positive signs of teams working well together
  - JAO construction leadership and relationship with Execs shows strength and ownership of the program.
  - Informal involvement through some IPTs
    - includes good examples of tri-lateral involvement (computing IPT for example – there are others)
  - Longer term integration of ALMA-J into single operating Observatory
    - We encourage the more complete integration of ALMA J efforts as early as possible

ALMA is well positioned to meet the remaining challenges

Good News Highlights

- Cost appear to be well understood, tracked and under control
- Risk management is being actively and effectively pursued
- Central action item tracking is fully supported by the committee
- Applaud efforts effort taking long term view – Power issue example
  - Good range of options considered looking across construction and operations views
  - Concern that it should not drive the scope of the construction project too much. Interim plan seems good. Concerned that operations should take the lead on the longer term implementation at some point (likely now), since you have a scalable plan with off-ramps available when ever the option for the grid materializes
- Great progress with refined approach on CASA, through IPT including customers
  - Carefully consider if there are other stakeholders that should be added (if they are not already) as part of the IPT
    - Looking to stable Beta release
- Progress reported on site looks excellent – looking forward to seeing it in person
- It is very encouraging to see the antenna arriving on site
  - Vertex production getting back on track, despite first unit issues
  - Melco Production is paying off with three systems being integrated
- Development of potential back up LO by Japan is a very good future risk mitigation
  - We fully support the continued effort for this key subsystem

Key Areas of Concern and Suggestions

- Schedule slips
- Staffing
- “Perfect Storm” bottleneck coming
- Suggestions
  - Production review
  - Staffing plan
- Integration of the project

Schedule slips

- Vertex late delivery of first unit
  - Many changes reported from prototype that could increase some risk
    - We realize that these were required, but details diverge from prototype
    - Good to see their production effort catching up immediately
  - Continued use of ATF was a good decision
    - Work in Socorro in parallel to site adds to staffing pressures and risk
    - Should reduce some risks
- Production phase would benefit from additional planning
  - Divergence in arrival and need dates are a concern
  - Month for month slip in FE and BE over recent 6 months needs attention
    - Schedule diversion relative to Antenna availability for integration
  - Good work around plans discussed, but it would be better to fix disconnects
  - Difficulty of AIV activities increases with these divergences
- Impact of current contracting process in the EU is of serious concern for meeting upcoming needs
  - Advanced planning is a general solution, but concerned that events that have occurred may impact ability to respond quickly

Many near critical path systems arriving during the next year

Staffing Progress

- Some notable progress in recent hiring of key people
- We fully support early hiring of longer term staff such as Chilean hires
  - Perfect training opportunity
  - Aid in smoothing transition through coming phases to operations
- Filling JAO HR position and agreeing on single entity for local hiring - good
- Concern on ability to attract and retain staff
  - Could not assess progress versus plan very well though discussions helped
  - Process and associated time line for hiring not presented
  - Answered largely this morning with many ideas on how to improve
  - Confirming areas where transition into later activities and operations make sense earlier should help worries on retention.
  - Comprehensive HR planning that includes partner interactions to help with career planning and any related issues may help in retention.
  - If continued trouble in hiring some key managers, move out any way on anyone required to support upcoming bottlenecks
- Strategic use of contingency to hire now

Given schedule slips and wave of activity coming on site:
Change philosophy from milestone driven to aggressive strategic hiring

"Perfect Storm"

- Previous two areas of concern when combined lead to a larger concern that progress will slow substantially if bottlenecks are realized
  - Late deliveries stacking up, combined with efficient staff ramp up needs
  - Bottlenecks can stall progress suddenly
  - On the other hand, current contingency situation seems very sound
    - NA reported nearly 40% contingency on costs to go
    - We are encouraged by some examples of adding more test stations
    - Any other ideas of additional test sets or equipment bottlenecks?
    - Use more contingency to your advantage to lower further schedule risk
- Planned production review is a key upcoming step
  - to get an initial handle on what is coming and how can you drive more efficiency down the line
  - Will lead to schedule re-baseline that we believe should occur prior to seeing results of first 4-5 units, but is not a singular step
- Reverse milestone based hiring plan for key IPTs to prepare for upcoming wave of activity

Production Review, coupled with proactive hiring is key to meeting the challenge

Production Review Suggestions

- We strongly support this review in November
- Consider a working meeting/review, at least for part of it
- Bring in a few production engineering and planning types
  - Experience in working workflow, bottleneck/capacity issues, transitioning from development into smooth efficient production activities to complement your technical experts
  - Pull from partnership where this experience exists
  - Look to industrial partners that have now gotten into production phase of their items which have this experience
  - A few consultants from Lean and 6 sigma type backgrounds
- Summarize results for various management entities to review

Integration of the partnership

- Moving toward fully integrated teams from all partners that moves you towards a single Observatory
- Benefits could be reaped now as you prepare for the AIV through handoff to operations
- Formal partners have come together very well from originally separate efforts
- Would encourage further integration of ALMA-J as you go forward
- Encouraged by a few 'seamless IPTs' that include a good cross section from all partners

Seamless approach to some IPTs is working well
Propagate this throughout

Review Format and Process feedback – Future improvement suggestions

- Use more material readily available to educate committee ahead of time
  - More references to previous review results
  - Note: we are particularly interested in outcome of production review or workshop
- Tailor presentation to hone in on current picture
  - Avoid slides that you will be 'explaining away' and focus on the best concise picture of what is happening
    - Staffing status did not seem to represent progress against current plan – in most areas, this was explained verbally
- Provide access to committee as progress is made to review at their leisure between yearly review
  - Use this to focus yearly review on updates and critical issues
    - Not necessarily involve all program if there are no issues
    - Assumes some level of committee consistency
      - Work with Execs to clarify longer term plan for this review
- Some concern on potentially overlapping charters of some committees and reviews will hamper rather than help the program
  - Role of this committee – does it overlap with AMAC in any way that should be clarified?
  - Role of AMAC with respect to internal program audit function of PA/QA
    - Auditing of reviews for example
  - Work to rationalize review structure to maximize benefit to project while satisfying exec need for oversight

Band3 Wafer Fabrication Discussion 1-30-08

TERMS:

trilayer, m1, m2
Trilayer is the superconductor-insulator-superconductor (SIS) material from which we make the SIS junctions. The trilayer for this project is wafer/Nb/Al-oxide/Nb/Au (where our process uses a Au overlayer). Our notation for this is m1/barrier/m2/Au... where m1 is metal one

liftoff trilayer
The Nb/Al-oxide/Nb/Au is deposited in-situ in a UHV vacuum magnetron sputter deposition tool dedicated to SIS work. There are two methods for obtaining distinct patterns ("base electrode" patterns) of trilayer on the wafer. The liftoff method is to define an organic pattern on the wafer before trilayer deposition, deposit the trilayer, and then put the wafer into a liquid solution that dissolved the organic pattern and (hopefully) removes the organic- lifting off the trilayer that was on top of it. We use this liftoff method with a multilayer 'trilevel resist' organic feature (wafer/polyimide/Nb... well actually it is wafer/nfr/polyimde/Nb but we still call it trilevel). Note, liftoff is a messier process as any unwanted organic debris will leave pinholes in the trilayer, and the liftoff process can leave 'wings' on the perimeter of the trilayer and debris on the wafer.

RIE trilayer
The other method to define trilayer patterns is to deposit the trilayer onto a clean and un-patterned wafer and to later define a (single layer) resist pattern and etch the trilayer. One of the difficulties in such a process is that the Al-oxide layer will not etch in a fluorine chemistry (fluorine is the customary chemistry for RIEs). Early on we used a wet etch to define the trilayer, however we could not accurately define patterns and could not define small linewidths with a wet etch process. More recently, for the band8/10 work, we have investigate an RIE process that uses a chlorine chemistry which is much more corrosive than fluorine. This process now works very well and is able to define small trilayer features accurately and with abrupt sidewalls. All of our use of this RIE process, except for some recent band3 wafers, has been with Nb/Al-AlN/m2 trilayer.

Stress
There have been a number of papers on stress (we have written three) in SIS junctions. Thin films can have intrinsic stress depending on whether there are more atoms per volume than 'ideal/bulk' (compressive) or fewer (tensile). The superconducting properties of films fall off as they become more tensile, beyond a modest level of tensile stress. The superconducting properties of compressive films are generally good, even for fairly large stress. The impact of 'good' Nb films with stress are reported to come into play on how the stress impacts the barrier (Al-oxide) layer. The thesis is that when a film with stress is etched, the built up stress across the film is released, and is most pronounced the closer one is to the edge of the trilayer.

Imagine an island of trilayer where we have defined a button of resist for an SIS junction. When we etch the m2 counter electrode layer, the stress in that film is released at the perimeter of the junction. That stress can damage the Al-oxide barrier and hence negatively impact the electrical characteristics (I-V) of the junction. The more stress in the film, the more stress to be relieved and the larger the effect on the junction. Junction size also plays a role. The larger the junction, the smaller the importance of the junction perimeter (which is where the stress is primarily relieved) and hence the smaller the effect. Most folks perform their studies with 1um junctions, however I found a paper which showed stress effects for junctions 4um and smaller in size.

Now envision a wafer which is defined by RIE trilayer. If the films are stressed (and it is unlikely that there is no stress in the trilayer), then after the RIE definition there is now stress release at the perimeter of the trilayer than extends into the trilayer- even before the junction etch! So you can already have damage to the Al-oxide barrier. Others have reported how, with RIE trilayer, the IVs deteriorate the closer one positions the junction near the trilayer perimeter. Another factor is the thickness of the m1 and m2 layers. The thicker the layer, the more stress to be relieved, and the greater the effect.

It is also widely reported that if one uses a liftoff of the trilayer, the stress effects can be generally circumvented. The explanation is that since large expanses of trilayer never existed, there is not a large component of built up stress that would be relieved during the junction etch, and hence little or no damage to the Al-oxide barrier. This is one reason why we have used liftoff trilayer (along with not having chlorine RIE until relatively recently). NOTE, we have not seen any stress effects in our trilayer RIE wafers for Nb/Al-AlN/m2 SIS materials. We tentatively believe that the AlN barrier 'holds up' better to any stress effects.

pogo strip
Each wafer has a set of SIS junction elements that are connected to large pads that I can easily connect to with a pogo pin jig and dip test in helium. Each 'chip' of these junction elements is call a 'pogo strip'. We also call these junction elements pogo junctions.

mixer-test element
On each pogo strip are different testable pogo junctions, one element array (N=1, N=2, or N=4) per pogo pad. There are generally two kinds of element arrays. The "mixer-test element" is a mixer chip that has been slightly shortened in length to fit on the pogo strip chip, but retains every important features of a real mixer chip. Note that that in the mixer-test layout, the trilayer pads on which the four junctions 'sit' are two small (as small as our process permits and still be able to align the junctions on the trilayer islands and also define an interconnection "m3" wiring layer) trilayer islands where the junctions are positioned on these islands as close to the edge of the trilayer as our alignment capabilities permit without having a junction overhand the edge. These two trilayer islands have a 2um 'moat' of no trilayer and then is surrounded by a region of trilayer.

uva-test element
The "uva-test element" is a very simple layout of junctions on rectangular trilayer pads. Note that the trilayer pads on the uva-test element are a good bit larger than the trilayer pads for the mixer-test element. Also note that the junctions on the uva-test element are positioned further from

NEW Band3 MASK

t3-262 11-07 First Wafer with new mask set
Wafer had RIE trilayer... because our Semigroup RIE had 'died'... and we had no way to form trilevel liftoff features. We had also discussed, with HIA, our wanting to try our new process RIE and pentalevel resist) on some band3 wafer. I-Vs were ones I have never seen before. They had the four SIS signatures (sharp turn ons), at the correct gap voltage, but they were 'sitting' ontop of ~150 microamps or so of DC current (we are calling this the 'Table Current'). So envision the zero voltage Josephson current rising ~150um higher than expected, and then the expected I-V curves happening on top of that current. For the N=1 (ie, single junction) case, the I-Vs were fine!

Our Explanation: Ti-line effect, due to the more abrupt trilayer with the m3 circling the trilayer moat... Need less abrupt trilayer, or longer m3 etch than customary to avoid this effect. Note, our Al-AlN results with RIE trilayer have all been for N=1 junctions (N=1 only on the test mask set)

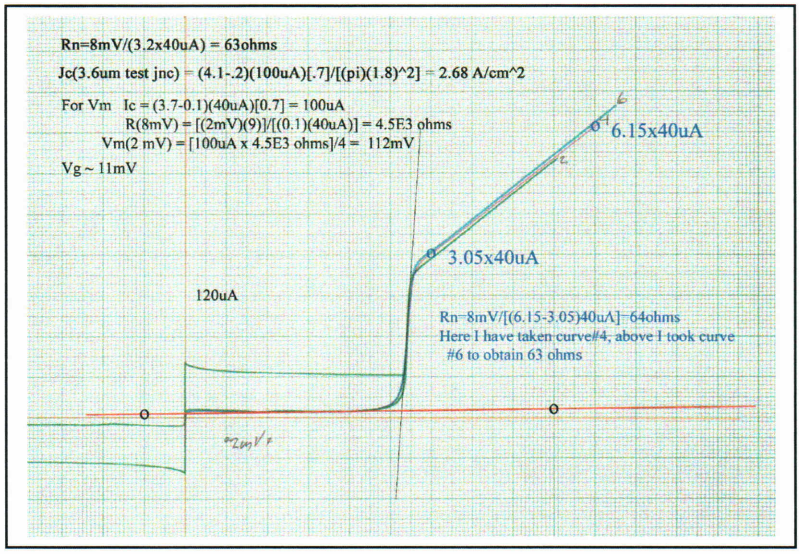
T3-272 12-07
Second Wafer with new mask set (oops, was RIE not liftoff)
We finished the Band3 and Band6 wafers. Band3 I-Vs (~80ohms), though uniform, have some extra leakage about about half gap and a wider turn on, while the Band6 wafer looks pretty good. The deficiencies in the Band3 I-Vs are not the same sort of problems that we have been seeing in the past (some junctions good, others terrible for any given N=4 mixer). The I-Vs on the other pogos are consistent with these. So, I can make the argument that what we are seeing is not the old problem. Since the Band6 wafer that run just a bit before the Band3 has nice I-Vs, I would argue that something else went just a bit awry in the Band3 run (could be the RIE starting to have its troubles that eventually made the tool inoperable, or could be the junction insulation just not quite doing its job). OR STRESS

T3-~~296~~ 269 01-07
Third Wafer with new mask set (RIE trilayer)
Uva-test pogo are GOOD, mixer-test are not... St

Our explanation: Stress...

edge of the trilayer. I have been using the same uva-test element layout since the N8 mask set (well before band6 and band3). The junctions are placed further inside the trilayer perimeter so as to make alignment easier.

Wafer History, looking at I-V quality:



t2-1388 11-03 good pogo IVs

t2-1389 03-04 good pogo IVs

t2-1394 07-04 good pogo IVs

t2-1406 09-04 good pogo IVs

best t2-1485 03-05 good pogo IVs

Next best t2-1493 09-05 good pogo IVs

IV compliant, RF not so good

t2-1644 02-06 good pogo IVs

some with 1 blown junction

t2-1659 03-06 good pogo IVs

t2-1665 07-06 good pogo IVs (mixed nrc mixer chip IVs, resistance spread)

a few good chips

t2-1622 08-06 good pogo IVs (mixed nrc mixer chip IVs, resistance spread)

t2-1664 01-07 mixed pogo IVs

t2-1666 01-07 mixed pogo IVs

t3-113 01-07 mixed pogo IVs

t3-115 -1-07 mixed pogo IVs

out of the array of 4 – 1 or 2 shorted junctions

During ~1665-1662, when NRC was measuring some mixers with good IVs, but others where only 3 out of 4 or 2 out of 4 junctions had good IVs, UVA and NRC had extensive discussions about what could be going awry, and UVA took full inventory of their process.

During this time period t2-1665 to t3-115 and beyond, UVA has fabricated two good Band6 wafers (which have a lot of similarities wrt geometry), three good KWL2 wafers – both which use Nb/Al-oxide/Nb trilayer, as well as over ten good Nb/Al-AlN/m2 wafers.

Eventually UVA became convinced that the problem with the 1665-t3-115 wafer sets had to do with the mask set itself degrading… with the degradation seen, with SEM, to be more advanced for the mixers chip junctions than the pogo chips.