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31 January

John Webber
Ray Escoffier
NRAO, Charlottesville

Dear John and Ray,

Let me use for this time the 'old' air mail way … there is no rush.

The Progres Report I send you covers the year 2000. Sorry if this is not an engineer report, it was mainly intended for the Europe-ALMA Management and for some of our Directors. It will tell you where we stand now.

Any comments/criticisms would be most welcome.

We plan to go the foundry by May with a full 7 comparator design although we may not have yet a first return from the STM foundry.

Apart from the high speed bipolar BiCMOS design we have now a small group in Florence which has just started to work on an GaAs solution.

We are in contact with the Japanese but their OKI GaAs chips are not commercially available.

In the Progress Report as well as in my revised contribution for the Project Book we have addressed the question of the interfacing of an n-bit high speed digitizer to the Fiber Optic transmitter. We are exploring various solutions. (I believe also that analysis of measurements on the Test Interferometer will help in the design of the Demux stage.)

Best wishes,

Alain

Alain Baudry

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Baudry

Progress Report on
ALMA High Speed Sampler Prototype and Tests

Alain Baudry, editor (baudry@observ.u-bordeaux.fr)

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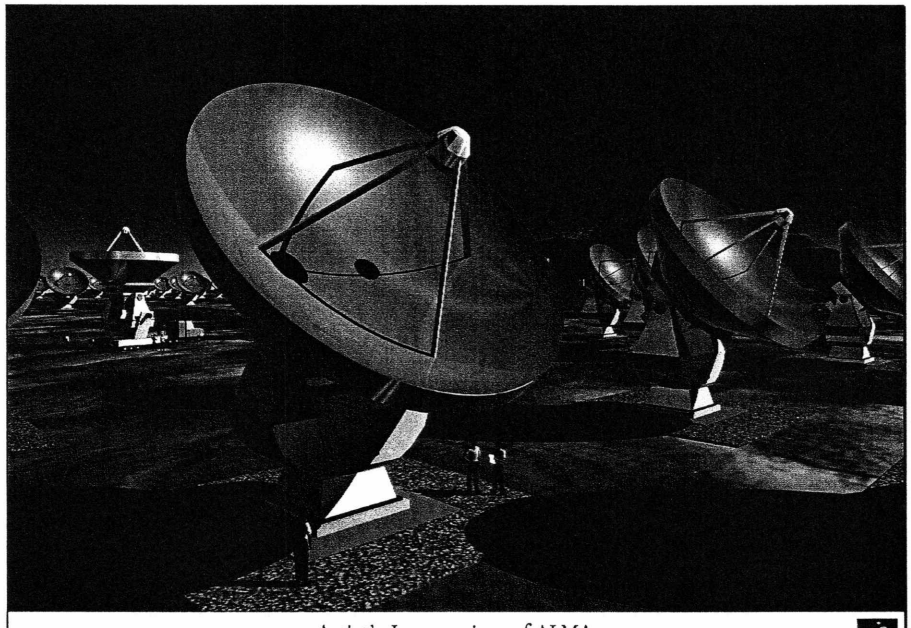


ESO PR Photo 24a/99 (8 June 1999) Artist's Impression of ALMA (Atacama Large Millimetre Array)

Preamble

This study was supported by the *"Agreement for the High Speed Sampler Prototype and Tests concerning the ALMA Backend and correlator Subsystems"* between ESO, a Consortium of Laboratories and INSU-CNRS.

The work outlined in this report is a contribution to the European ALMA Backend Electronics Team.

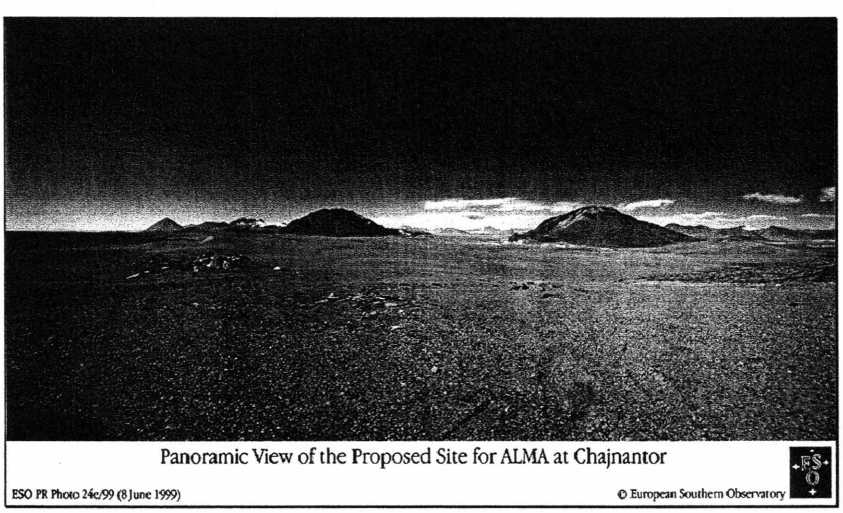
Apart from the contributors to this Progress Report, several other people at IXL (Bordeaux), IRAM (Grenoble), and CESR (Toulouse) have contributed or helped in defining specifications and technical choices. We especially thank P. Fouillat, Y. Deval at IXL, J.Y. Mayvial at IRAM and D. Lagrange at CESR.

Document History

Creation: November 2000
Final edition: 25 January 2001

Summary

Top level specifications and a general view of the ALMA digitizer requiring 7 comparators clocked at 4 GHz are given in Chapter 1. Some details on the building blocks, simulations and ASIC layout of a first 2-bit digitizer based on fast SiGe technology are given in Chapter 2. Possible solutions to the interfacing of the high speed sampler to the fiber optic data transmission system are briefly suggested in Chapter 3. Details of the test bench fabricated to characterize the sampler prototypes are presented in Chapter 4.



Panoramic View of the Proposed Site for ALMA at Chajnantor

ESO PR Photo 24e/99 (8 June 1999) © European Southern Observatory

Chapter 1. ALMA Digitizers: Overview

1.1 Introduction, Top Level Specifications

The analog-to-digital converters, or digitizers, installed in each of the 64 antennas of the ALMA system (with eight digitizers associated to eight 2 GHz sub-bands per antenna) provide the flexibility required by the fiber optic transmission of the IF toward the correlator. Digital conversion is of course indispensable to the correlator in order to derive the correlation function as a function of digital lags for spectroscopy. The digitizers are thus crucial and single-point-failure elements in the system. The ALMA system incorporates 3-bit digitizers thus improving the overall sensitivity compared to the classical 2-bit case. The goal specifications are given in Table 1.1 below.

Table1.1 ALMA top level specifications

Input BW 2-4 GHz
Sample clock 4 GHz (250 ps)
Bit resolution 3 bits
Quantization levels 8
Aperture time ~ 50 ps
Jitter ~ a few ps
Small indecision region
Output demultiplexing factor 1/16
PLL Clock distribution 4 GHz, 250 MHz (125 MHz system clock)
Fine delay command
Low power consumption

A survey of tens of Web sites for commercial samplers or track/hold amplifiers with conversion rates above 1 Gsps show that the product required for ALMA does not exist off the shelf. Some commercial products go as high as 1-2 Gsps, one goes up to 4 Gsps but no digitizer has an input bandwidth up to 4 GHz . They are multi-application products with more bits than actually required for radio astronomy (and thus with high power consumption ~ 4 to 7 W).

1.2 Digitizer Overview

The block diagram of the ALMA digitizer is given in Figure 1.1. It includes several fundamental elements briefly described below. The input adapter amplifier, the comparators and associated latches and encoding are implemented in a single ASIC. The fast demultiplexing unit is separated from the ASIC to diminish any coupling of the digital output with the analog signal input. The ASIC and the demultiplexing unit form the digitizer proper.

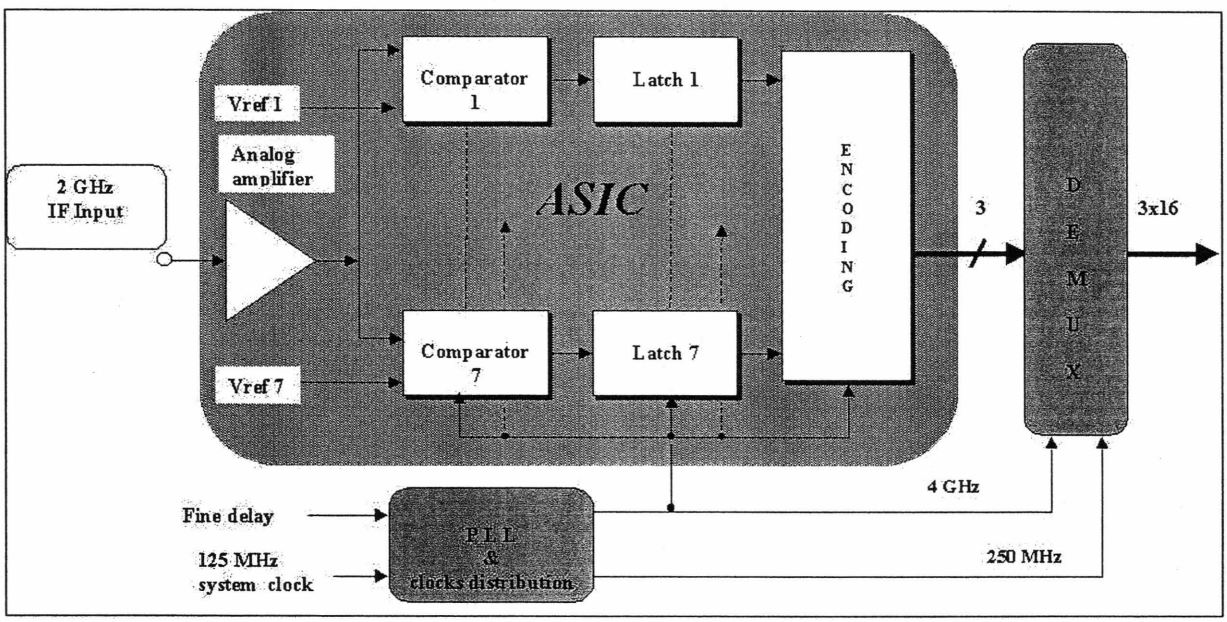


Figure 1.1 Digitizer block diagram

The PLL box produces and distributes the sinusoidal 4 GHz sampling clock signal and the 250 MHz signal required by the demultiplexing unit. This is another separate unit which will be common to at least one digitizer pair. Fine delay setting may be obtained by controlling the sample phase in the PLL box.

1.3 The Digitizers

1.3.1 Input Adapter Amplifier.

The input analog signal is delivered from one of the four outputs (50 ohms impedance) of the IF down-converter module in the range 2 to 4 GHz. It is random with Gaussian statistics. The

response of this amplifier is flat within +/- 0.5 dB over 2 GHz bandwidth and linear up to about +15 dB above the r.m.s. input signal voltage. The voltage supply required for the adopted ASIC technology is +/-1.25 V.

The digitizer input level is controlled in the IF downconverter with +/- 0.25 dB attenuator steps placed in the 2-4 GHz output paths of each IF downconverter. This allows us to minimize platforming effects and to keep the quantization thresholds constant and at their optimum level for maximum quantizing efficiency.

1.3.2 Comparators and Quantization Thresholds

The sampling function is performed in the comparators which include two latches operated in a master-slave configuration and clocked at 4 GHz. The 4 GHz clock signal is equally distributed to 7 comparators. It is shaped internally in a dedicated amplifier driven by the external 4 GHz sinusoidal signal. The seven thresholds comprise a zero reference voltage and are set around +/- 0.5 σ, 1 σ and 1.5 σ where σ is the r.m.s. voltage at the common input of the 7 comparators; these levels are kept constant and their exact value is tuned with an accurate division voltage chain so as to minimize the quantization losses. First simulations of SiGe digitizers indicate that the sampler indecision region is small and at the level of 1% of the smallest comparison threshold.

1.3.3 Encoding

The digitizer encoding is not yet finally adopted. It is not dictated by the correlator specifications because the digital FIR filters have look-up tables to translate between the digitizer code and the 4-level correlator chip code. However, the encoding should minimize the power consumption and should permit easy identification of the digitized signal sign (Walsh demodulation). We plan to deliver SCFL differential logic levels.

1.3.4 Adopted Technology

At the moment, the adopted technology is based on high speed SiGe bipolar transistors from ST-Microelectronics. In order to check the technology performances, the layout of an experimental ASIC comprising an input amplifier, two comparator-latches, two output buffers and clock distribution has been prepared with design tools and verification software from ST-Microelectronics. Simulations are encouraging and a fully verified layout will soon be sent to the foundry. Some details are given in Chapter 2. In a near future the technology will evolve from BiCMOS6G to BiCMOS7G all designs being made with 2.5 V DC supply voltage.

1.3.5 Digitizer Test Bench

Thorough tests of the digitizer prototypes will be undertaken with a dedicated test bench described in Chapter 4. This bench comprises a broad band input noise source with low/bandpass filters. The 3-bit output data from the sampler ASIC are sent to a Fast Demultiplexing Unit whose data are then processed in a simplified (16 lags) low frequency correlator based on FPGAs.

Chapter 2. Design and Simulations of a First 4 GHz, 2-bit SiGe Sampler

2.1 Introduction

The general architecture of the ALMA digitizer is described in Chapter 1 and in Figure 1.1. Two blocks remain outside the digitizer chip: the 4 GHz & 125/250 MHz clock generator and the demultiplexing unit. This design choice and careful shielding should minimize cross-talks and digital feedback to the sampler input.

The main characteristics of the digitizer chip are an input bandwidth from 2 GHz up to 4 GHz, 3 bits output data at 4 GHz clock, 7 quantization levels and a threshold indecision region as low as possible. The predictable main critical parts of this chip are the input amplifier and the comparators.

After having investigated in the literature some topologies used in state of the art high speed samplers, the IXL Laboratory began the design of innovative structures for signal amplification followed by two comparators. Such a design was performed with 0.25 µm CMOS technology from STMicroelectronics. This circuit will return from the foundry by the end of January 2001. Nevertheless, simulations have shown that this technology is not well suited to the high speed required for the ALMA project.

Therefore, we have decided around mid-2000 to take advantage of a new technology used in our laboratory : SiGe BiCMOS 0.35 µm from STMicroelectronics. This process allows us the design of very high speed building blocks.

Our first SiGe prototype is a complete digitizer (excluding the encoding part which we do not need now since we have integrated two comparators only in the chip). This first chip is thus a 2-bit, 3-quantization level digitizer which we will use to validate the concept and topology of adopted sub-systems.

2.2 SiGe digitizer

In this section we describe the various parts of the digitizer, and we present the main characteristics of the chip based on simulations.

The first step was to refine the comparator specifications especially its hysteresis range which in turn imposes the minimum input signal to be compared, and thus the first threshold voltage.

2.2.1 Comparator-Latch

The operating supply voltage range is specified, in the used SiGe 0.35 μm technology, to be within 2.5 V. We have adopted a symmetrical ±1.25 V. The signal level at the common input of the two comparators is called σ. This is a Gaussian "white noise" signal on a 2 GHz bandwidth. The comparator hysteresis determines the minimum input level σ, and the comparator supply voltage limits its maximum level. Such a Gaussian signal has the following characteristics: σ is the signal level obtained for 68% of the time, and 3 and 5 x σ are achieved during 1% and 0.001‰ of the time respectively. For 2 GHz bandwidth we will thus obtain 2000 steps at 5σ every second; our design must account for this dynamic range.

In order to settle on a σ value, we have to evaluate the hysteresis of the comparator which determines the sampler indecision region. Based on simulation results and know-how of such a design, the adopted topology (see below) exhibits an hysteresis in the10 μV range. We thus expect, once the chip has been fabricated, a measured indecision level roughly between some hundreds of microvolts and one millivolt.

Adopting for the hysteresis a maximum value of 1 mV and fixing this value to around or below 1% of the input signal σ, we find σ ≈ 100 mV. The future ALMA digitizers will require 3 bits and eight comparison levels. The seven thresholds have been chosen to be 0 V, ± 0.5 σ, ± σ and ± 1.5 σ. Therefore, the maximum voltage at the input of the comparators (namely the maximum output voltage of the amplifier) will reach 500 mV (5 σ). The topology of the comparator and associated latches is shown in Figure 2.1. The input signal is coming from the amplifier, and the reference input is one of the seven threshold voltages. The comparator includes two cells, in order to minimize the hysteresis (one subtracts the two input signals, and the other amplifies this difference). It is followed by two latches achieving a sampling and storing process in a master/slave configuration. They are clocked at 4 GHz.

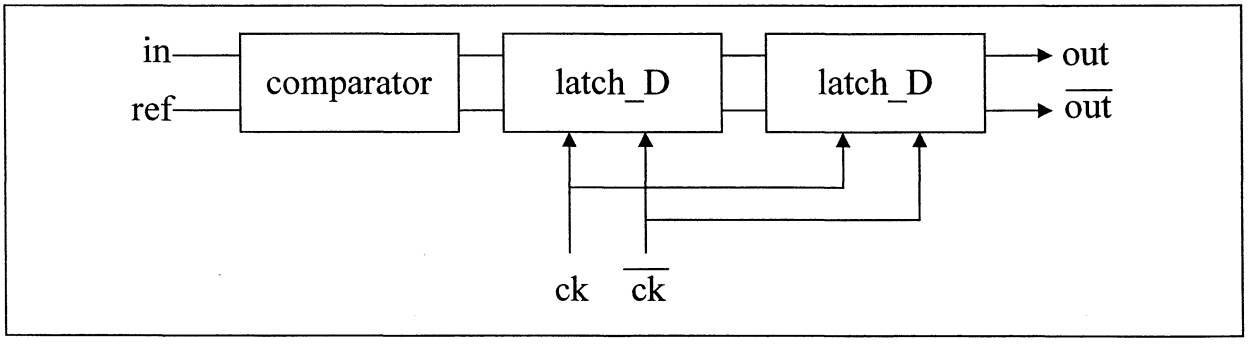


Figure 2.1 Sampler topology

2.2.2 Amplifier

The input adapter/amplifier specifications are given in Chapter 1. The amplifier output stage must be able to provide a signal larger than ± 1.5 σ, the maximum threshold voltage, at the input of the comparators. Furthermore, we have to include a common-mode feedback loop in order to lock the mean value of the amplifier output voltage to the zero volt center threshold. The amplifier gain is not critical in our design. However, its response must remain linear and the ripple over 2-4 GHz bandwidth should not exceed ±0.5 dB.

Simulations show good agreement with specifications. The amplifier response at 0.5 dB goes up to 4.5 GHz with 9 dB voltage gain. According to previous specifications, the maximum input signal level under 50 Ω is then around 180 mV r.m.s.

2.2.3 Clock distribution

In order to deliver the 4 GHz clock signal to the sampler, we have integrated a dedicated amplifier with 800 mV differential output levels well suited to the latch inputs. The input signal under 50 Ω is 200 mV at 4 GHz.

2.2.4 *Digitizer prototype*

In order to validate our previous assumptions concerning selected topologies of the building blocks, we have designed a 2-bit, 3-level digitizer prototype comprising one amplifier, one clock buffer and two comparators. The output signals of this prototype have to match the logical levels 0 V and -900 mV for tests on the simplified autocorrelator designed by IRAM.

Full simulations including all parasitic elements have been performed (see Figure 2.2). Our specifications are met, except for the output level. These simulations have been made with input signal and clock frequencies equal to 2 GHz and 4 GHz respectively. The output signals v_{s1} and v_{s2} are in a high logic level ("1") when the input is greater than the low and high thresholds respectively.

Figure 2.3 shows a complete view of the layout design just before it goes to the foundry. One sees 32 I/Os dedicated to the: power supply (21 inputs), reference voltage (3 inputs), input differential signal and clock (4 inputs), and output signals (4 outputs). The chip area is 6.75 square mm, and the total power consumption under ± 1.25 V is 520 mW. This consumption will be optimized in future designs.

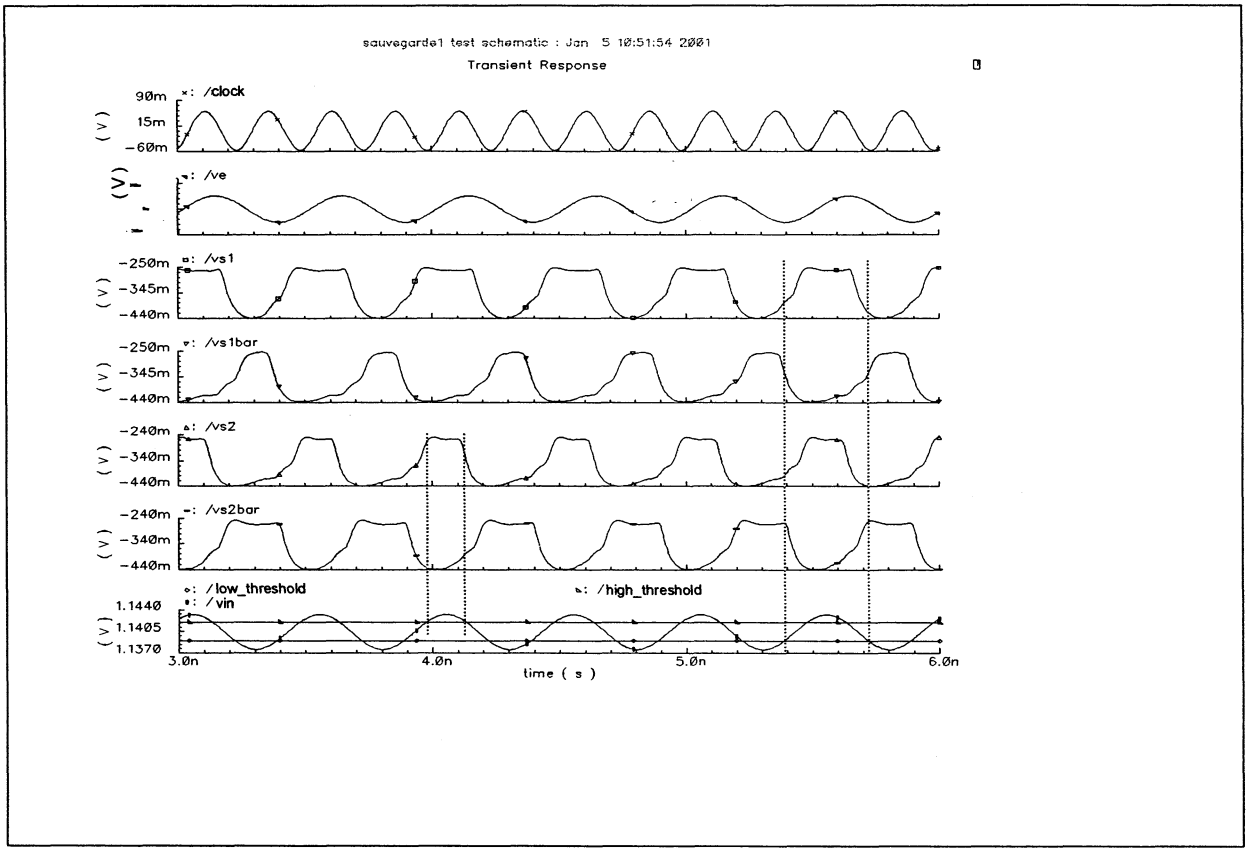


Figure 2.2 Digitizer prototype: simulation results

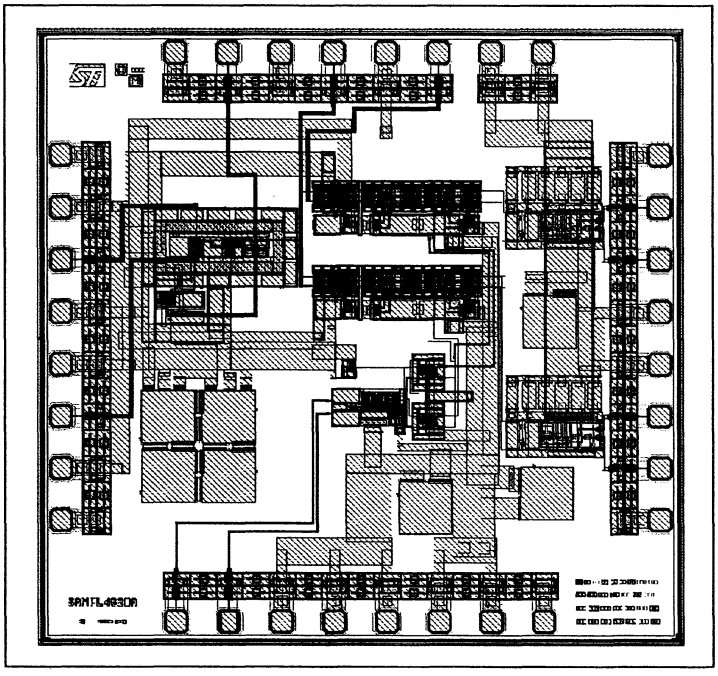


Figure 2.3 Layout view of the digitizer prototype

Chapter 3. ALMA High Speed Sampler Demultiplexing

3.1 Introduction

Various solutions can be considered to handle the sampler ASIC output data rate before transmission to the Fiber Optic System link. This is a difficult question which will be fully addressed during the second year of the Phase 1 Study.

The n-bit output data from the sampler ASIC are sent to a Fast Demultiplexing Unit (FDU) (DEMUX box in Figure 1.1). In the ALMA system the demultiplexed output is interfaced to the Virtual Parallel Bus (VPB) transmitter. It delivers 16 times 3 bits or 48 lines at 250 Mbps consistent with the 12 Gbps output data flow from each sampler ASIC, and consistent with the input of the VPB digital serializer and optical combiner needed for the IF/FO downlink to the ALMA correlator.

3.2 Test Bench Fast Demultiplexing Unit

IRAM designs an FDU for the digitizer test bench described in Chapter 4. This FDU is made up of three single bit demultiplexing boards (Figure 3.1). Each board comprises a 1:16 demultiplexer and a synchronizer allowing multi-bit demultiplexing operation. The 1:16 demultiplexer consists of several logic layers the first one using commercial high speed GaAs ICs. The synchronizer can be seen as a PLL stage detecting whether the (equivalent) 1:16 logic counters of two chained demultiplexers operate in the same phase state or not.

3.3 ALMA High Speed Sampler Data Flow Reduction

Designing for the ALMA system a series-reproducible version of the test bench FDU poses a significant problem because there are no commercial demultiplexers phasing 3 bit signals at high rates. We envisage three main possibilities: a) synchronize the three single bit commercial demultiplexers as performed in the test bench; b) use commercial high speed gate arrays, if available; c) develop a new ASIC. While option b) needs to be investigated carefully, we do not know at the moment whether it will be reliably possible with option a) to go to the production stage for hundreds of units.

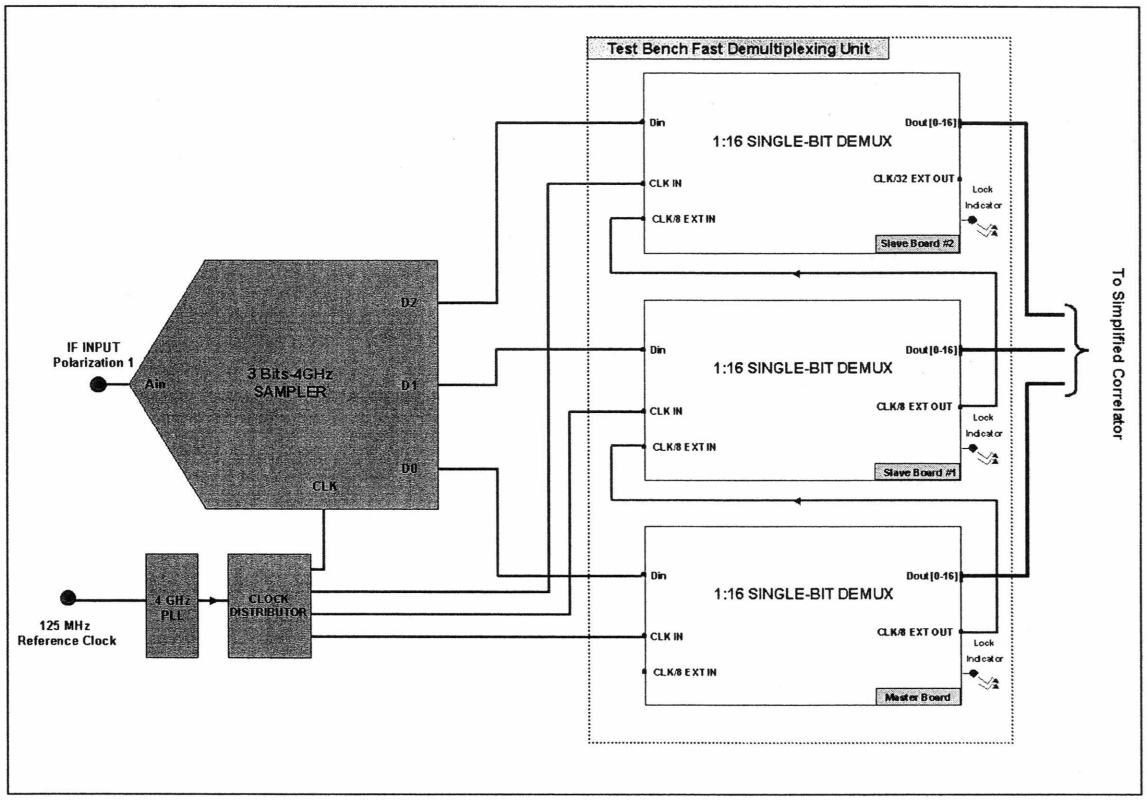


Figure 3.1 Test Bench Fast Demultiplexing Unit (FDU) Block Diagram

Chapter 4. Digitizer Test Bench: Principles and Status

4.1 Test Bench Overview

The test bench described here will provide dynamic characterization of the sampler ASIC, hence feedback to the ASIC design group for further chip runs.

4.1.1 Tests to be performed

Probability density function. Measurement of the statistical distribution of the input signal samples will make possible to extract real thresholds from each of the 7 comparators and to compare them to their nominal values defined in Section 2.2.1.
Time stability. The autocorrelation sequence zeroth lag is an image of the signal power. Its time stability is of prime importance as data integration time may vary up to several hours. It can be estimated according to the Allan variance of the sampled data.
Sampler frequency response. The input signal being a white noise, the autocorrelation FFT should be flat. In practice, one will obtain a low-pass response including ripple within the passband (due to input buffer mismatch for instance). In fact, the computed FFT corresponds to the frequency response of the ASIC analog input stages and will underline excessive frequency distortion of this stages.

4.1.2 Physical architecture

The test bench (Figure 4.1) is made up of both commercial instruments (clock generator, power splitter, power supply, VME sized CPU board, display unit) and home made units (noise source, fast demultiplexing unit, simplified correlator board, IRAM correlator unit).

The clock generator will deliver a working frequency up to 1.3 time the nominal sampling frequency (4GHz). The noise source is flat over the input frequency range and will be able to deliver an output level of -3dBm over a 2GHz bandwith. The sampler ASIC will be powered thanks to an adjustable power supply to measure the input stage gain stability vs power supply. Cable lengths will be carefully chosen in order to overcome signal timing between sampler test board and the demux unit.

The autocorrelation number of lags is set to 16 which represents a good compromise between complexity and performance. Thus, the fast demultiplexing unit (FDU) acquires a set of 16

consecutive samples at a rate of 4 GS/s. Once samples have been captured, they are distributed at a lower rate to be processed off-line by the simplified correlator board.

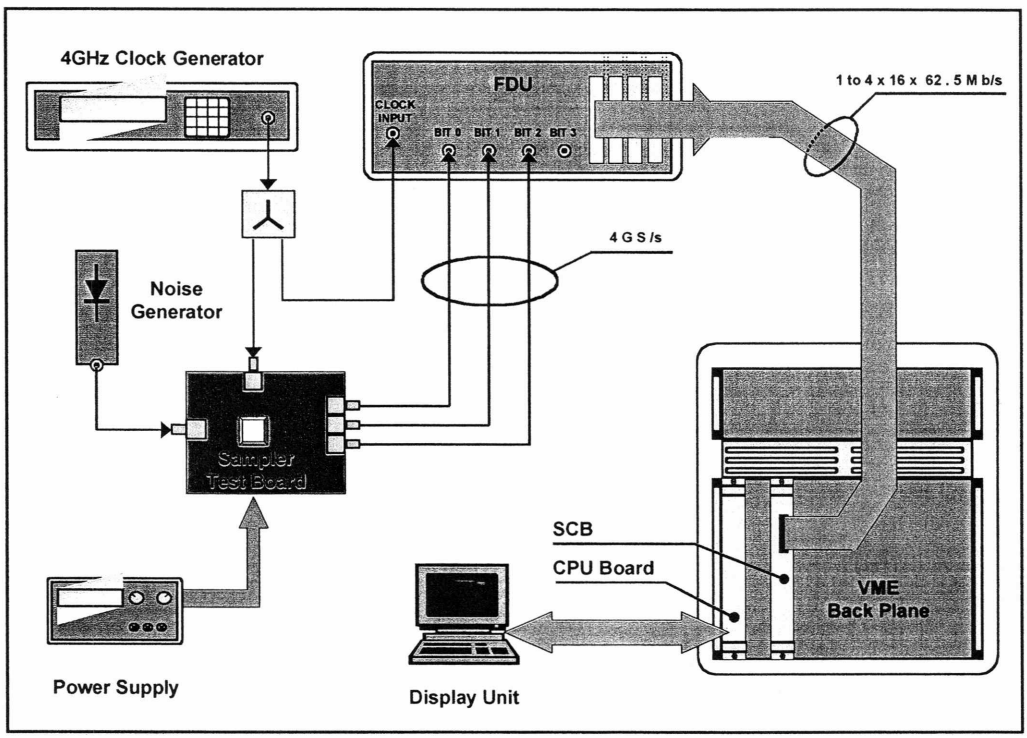


Figure 4.1: Test Bench Physical Architecture

The simplified correlator board (SCB) is in charge of the 16 lags autocorrelation calculation as well as of the probability density function measurement. At the present time, these two functionalities will not be avalaible simultaneously on the board for practical design reasons. Regarding the wanted test, the corresponding FPGA configuration EPROM should be set on board.

Once calculations are finished (according to the wanted accuracy), the final result is sent out of the SCB trough the VME bus to an OEM CPU board. The latter supports the test software which computes the Van Vleck correction then the FFT and displays results. In order to be able to instantaneously observe the effect of whatever change (on-board adjustement, temperature step, etc.), an FFT display refreshing rate of once per second will be implemented.

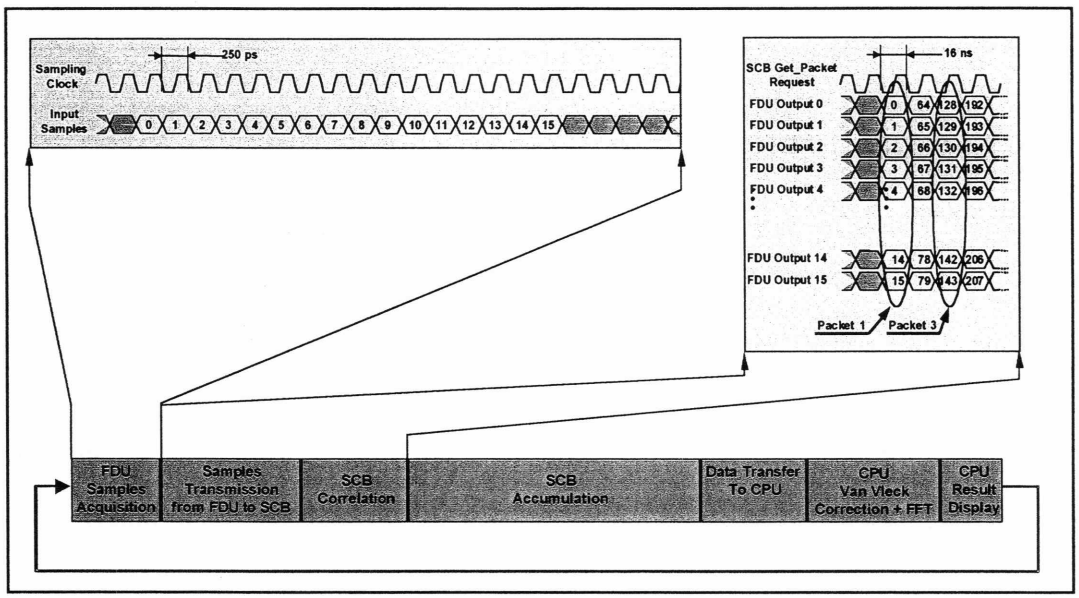


Figure 4.2: System time sequence

4.2 Hardware Implementation

4.2.1 System block diagram

Samples acquisition and processing are performed by the FDU and the SCB respectively (Figure 4.3). Following an acquisition request from the SCB, the16 samples packet is parallely transmitted toward the SCB. This asynchronous transmission between FDU and SCB offers the great advantage of being able to run the FDU at a sampling frequency independent of the SCB processing speed. During qualification tests this possibility is of prime importance and will permit to run various circuits.

4.2.2 FDU

Because the sampler resolution could change and because ultra-high frequency is involved in this unit, a one board per bit architecture is adopted. A single demultiplexer board is composed of an off-the-shelf GaAs 1:8 demux as a first layer. Its 500Mb/s output rate is downconverted to 62.5Mb/s thanks to a second layer made up of a set of two 8-bits register alternatively latched. This final rate is based on the maximum input rate accepted by the correlator FPGA. Once the 16-bit packet has been captured, it is transmitted to the SCB thanks to line buffers.

Up to four boards may be chained (1 Master, 3 Slaves) allowing us to test sampler chips having resolutions as high as 4 bits.

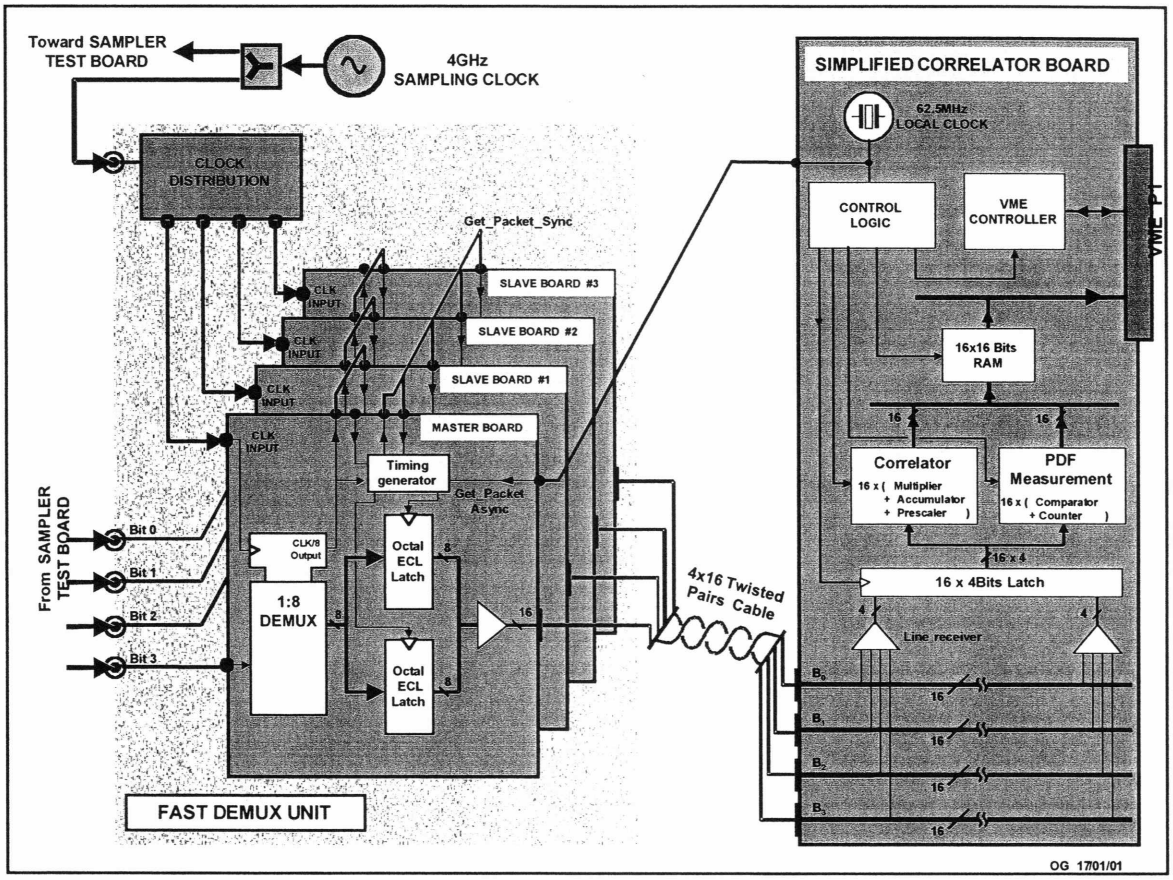


Figure 4.3 System block diagram

4.2.3 SCB

Autocorrelation and probability density function (PDF) measurements are physically computed thanks to the same digital circuits. In particular, multiplications and comparisons are performed thanks to look-up tables (LUTs). The only difference between these two operations lies in the LUT contents. When using the circuit to compute the autocorrelation, LUTs are downloaded with the optimal multiplication table, whereas using the circuit to measure the PDF, LUTs are downloaded such as they can be seen as a set of 16 comparators (we may test up to 4-bit samplers), each dedicated to the occurrence count of a specific level. In a first analysis, all operations will be implemented thanks to two FPGAs together with miscellaneous standard digital circuits. This leads to an SCB size of one VME board.

4.2.4 Noise generator

The selected noise source delivers a white noise over the 100 MHz to 4 GHz frequency range. Depending on the sampler ASIC performance, the output spectral density shape could be either of the lowpass or bandpass type. This will be selected thanks to an external filter. Whichever the chosen spectral density shape, the output voltage should be limited to 160 mV r.m.s. This will be achieved thanks to the 1dB step precision attenuator.

Output power stability will be optimised thanks to regulated power supplies and by controling the noise source temperature. An OEM temperature controller coupled to the noise source socket will ensure a constant working temperature whatever the external temperature variations.

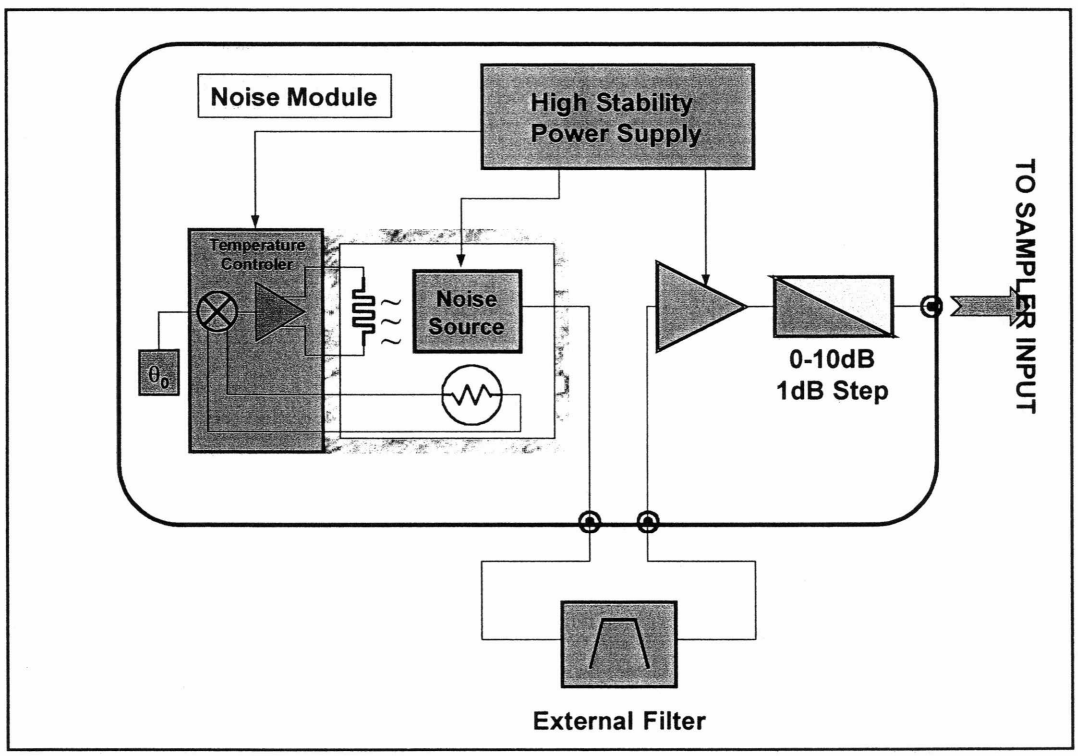


Figure 4.4 Noise generator block diagram

4.3 Test Bench Development Status

The status of the digitizer test bench at the end of 2000 is described in the table below.

Table 4.1 Development status

	FDU	SCB	Noise Generator
Schematic	Done	To Be Done	Done
Parts Purchase	Done	To Be Done	Done
Board layout	In Progress	To Be Done	Not Applicable
Board Assembly	To Be Done	To Be Done	Not Applicable
Mechanical Housing	To Be Done	To Be Done	In Progress
Qualification Tests	To Be Done	To Be Done	To Be Done

APPENDIX

ALMA High Speed Sampler Prototype and Tests

Documents Produced from December 1999 to December 2000

- *"A review of high speed samplers: commercial modules and Observatory fabrications"*
D. Deschans, A. Baudry, Internal ALMA memo, December 1999

- *"Digitizer development plan"*
A. Baudry, 28 February 2000, ALMA System Revierw, ESO Garching

- *"ASIC échantillonneur pour le grand réseau d'antennes mm/submm ALMA"*
A. Baudry, P. Fouillat, J.B. Begueret, Y. Deval, D. Deschans, 26 Juillet 2000, Document soumis à STMicroelectronics

- *"Spécification Technique du Besoin"*
Groupe de travail réalisation d'un ASIC échantillonneur pour le projet ALMA (révisé Août 2000)

- *"Design of a simplified correlator to test new samplers for ALMA"*
O. Gentaz, June 2000 (IRAM backend group homepage)

- *"High Speed Sampler Data Flow"*
O. Gentaz, November 2000, Internal ALMA memo

- *Minutes editing* of internal high speed sampler meetings and reviews: eight issues

- Contribution to the *ALMA Project Book, Chapter 9, IF Processing and Signal Transmission*