10-20-98

Virtex™ 2.5 V Field Programmable Gate Arrays

October 20, 1998 (Version 1.0) — Advance Product Specification

Features

- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 50k to 1M system gates
  - System performance up to 150 MHz
  - 66-MHz PCI Compliant
  - Hot-swappable for Compact PCI
- Multi-standard SelectIO™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM™ devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierachical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.25-µm five-layer metal process
- 100% factory tested

Description

The Virtex FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.25-µm CMOS process. These advances make Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the nine members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

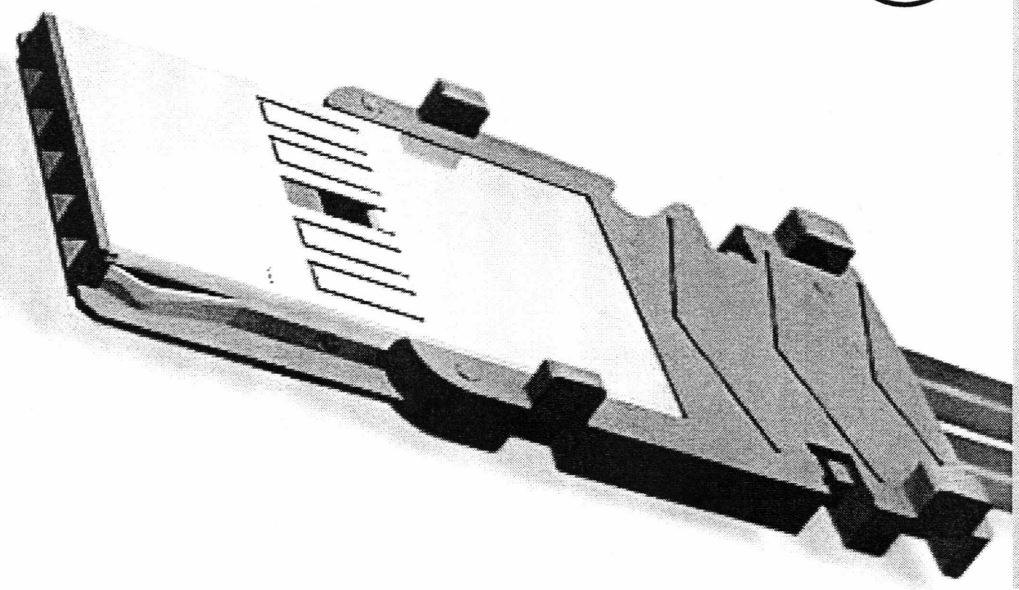
Table 1: Virtex Field-Programmable Gate Array Family Members.

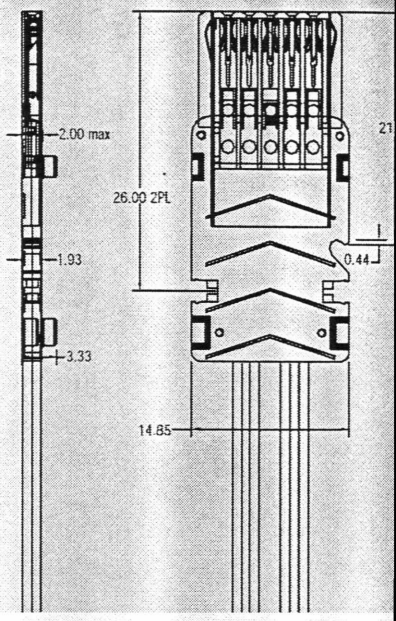
Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	BlockRAM Bits	Max Select RAM Bits
XCV50	57,906	16x24	1,728	180	32,768	24,576
XCV100	108,904	20x30	2,700	180	40,960	38,400
XCV150	164,674	24x36	3,888	260	49,152	55,296
XCV200	236,666	28x42	5,292	260	57,344	75,264
XCV300	322,970	32x48	6,912	316	65,536	98,304
XCV400	468,252	40x60	10,800	404	81,920	153,600
XCV600	661,111	48x72	15,552	404	98,304	221,184
XCV800	888,439	56x84	21,168	404	114,688	301,056
XCV1000	1,124,022	64x96	27,648	404	131,072	393,216

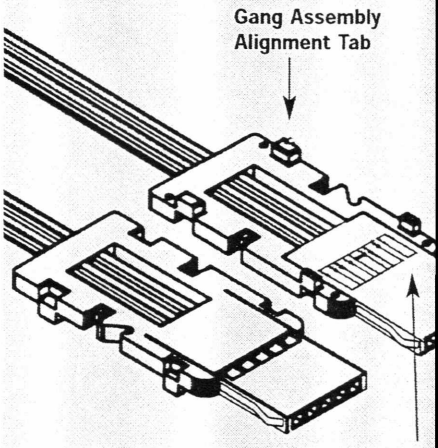
2MM HIGH-SPEED CABLE INTERCONNECT-TO-BACKPLANE SYSTEM

HM

ISO 9001 CERTIFIED







Controlled Impedance Shielding 1X5 -Top and Bottom View

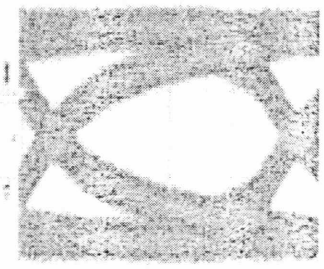
Offering Exceptional Performance and Flexibility for Today's Leading-Edge Circuit Designs

The Tensolite HM Interconnect System is designed and manufactured in compliance with global standard IEC 1076-4-101. A high-density, high-speed system for high-frequency applications, it was developed in response to the demands of the data processing, industrial process controls, medical systems, avionics, instrumentation, and telecommunications markets. It is a complete modular system, board-to-board and cable-to-board, with minimum crosstalk and exceptionally fast signal rise times measured in picoseconds.

At the heart of the HM system are modular cable connectors with a 2mm signal contact pitch, whose pins are arranged in stackable 1 X 5 wafers for optimum performance. Latch shrouds are available, along with a complete line of complementary accessories.

Cable available for use with the Tensolite HM Interconnect System are 26, 28 and 30 AWG single-ended, 50-ohm, high-speed miniature coaxial; and differential pair, 100-ohm twin-ax.

SPICE models are available to enable the designer to simulate the complete signal path.

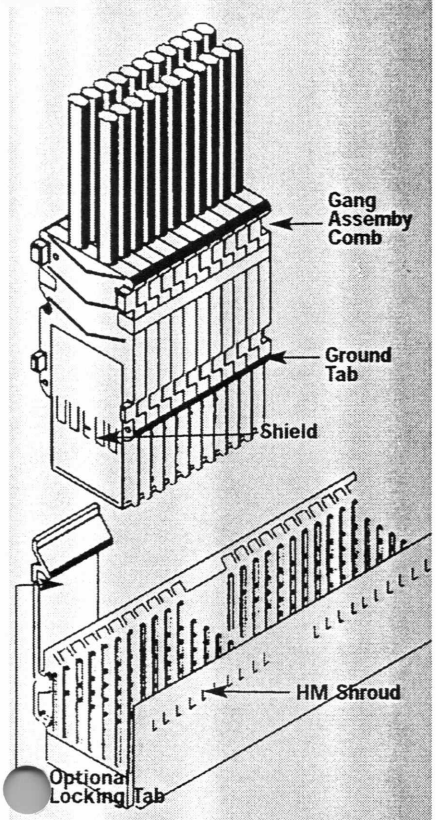


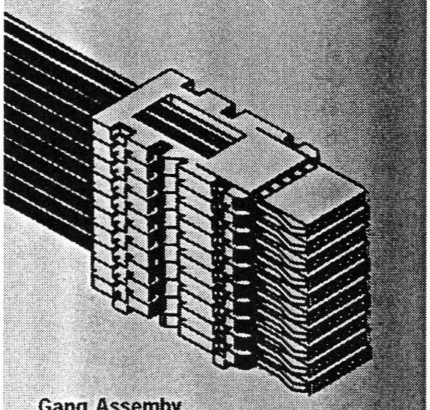
OPEN EYE PATTERNS at up to 1 Gigabit per sec. – Actual test data illustrating logic levels 1 and 0 for a 20-ft. cable length of differentially-driven 28-AWG balanced line at 500 Megabits per second, 1.0 Volt peak-to-peak.

Tensolite
Interconnect Systems
A Company

HM

HIGH-DENSITY METRIC CABLE ASSEMBLIES





Gang Assemby
5X10

MECHANICAL

On-Center Spacing	2 mm
Mating Pin Length	4 to 6 mm
Mating Pin Dimensions	0.35 mm X 0.45 mm
Insertion Force, Per Contact	0.75 N, max.
Withdrawal Force, Per Contact	0.15 N, min.
Normal Force, Per Contact	0.70 N
Cable Retention Force	22 N, min.
Durability (Insertions / Withdrawals)	250 cycles

ELECTRICAL

Insulation Resistance	100 MΩ, min.
Dielectric Withstanding Voltage	500 V
Voltage Rating	250 VAC
Current Rating, @ 70°C, Per Contact	1.0 A
Contact Resistance	20 mΩ, max.

MATERIALS

Shield	Beryllium Copper
Contacts	Beryllium Copper
Dielectric, per UL 94V-0	Glass-Filled LCP

PLATINGS

Shield 95/5 Tin Lead all over		1.27 µm, min.
Contacts	Ni all over	1.27 µm, min.
	Au all over	1.27 µm.

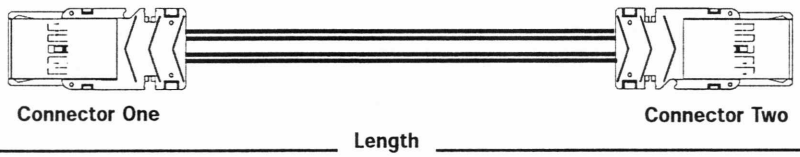


TABLE 1 - AVAILABLE PINOUT SEQUENCES

WAFER POSITION	A	B	C	D	E	F	G	H	I	J	K	L
1	S	S	-	S	G	S	-	G	-	S	S	-
2	S	S	-	G	S	G	-	S	-	S	S	-
3	G	G	G	-	-	-	-	-	-	-	-	-
4	S	-	S	S	G	-	S	-	G	S	-	S
5	S	-	S	G	S	-	G	-	S	S	-	S

S=SIGNAL G=GROUND

CONFIGURATION INFORMATION

Connector One	Pinout Sequence	Cable Style	Assembly Length	No. of Wafers in Assembly	Pinout Sequence	Connector Two
HM □	□	□□	□□□.□	□□	□	□
U= Unshielded S= Shielded	A to L (Table 1)	01 to 12 (Table 2, Gatefold)	Inches	1 to 24	A to L (Table 1)	U= Unshielded S= Shielded

Tensolite

Represented By

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A Company

Preliminary
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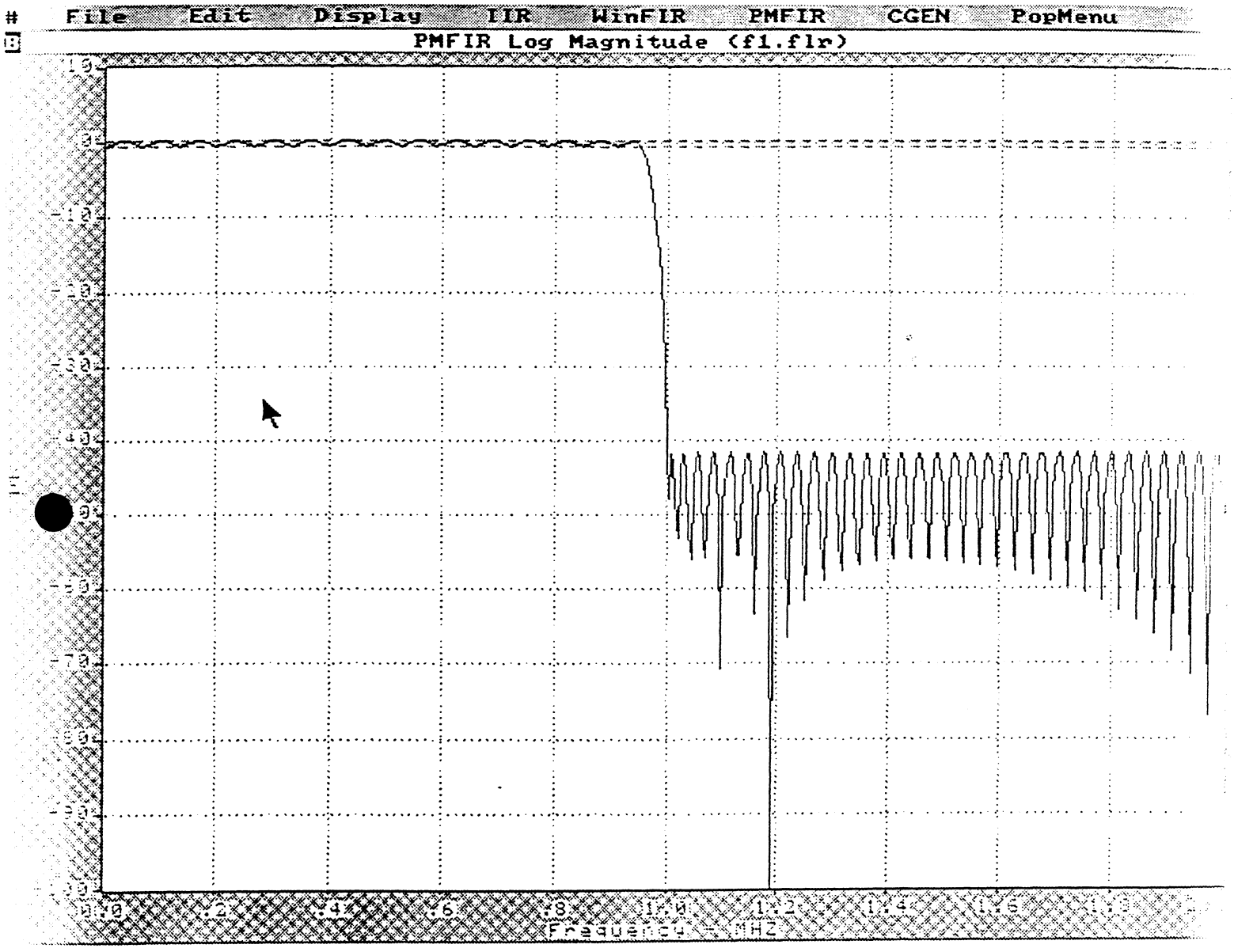
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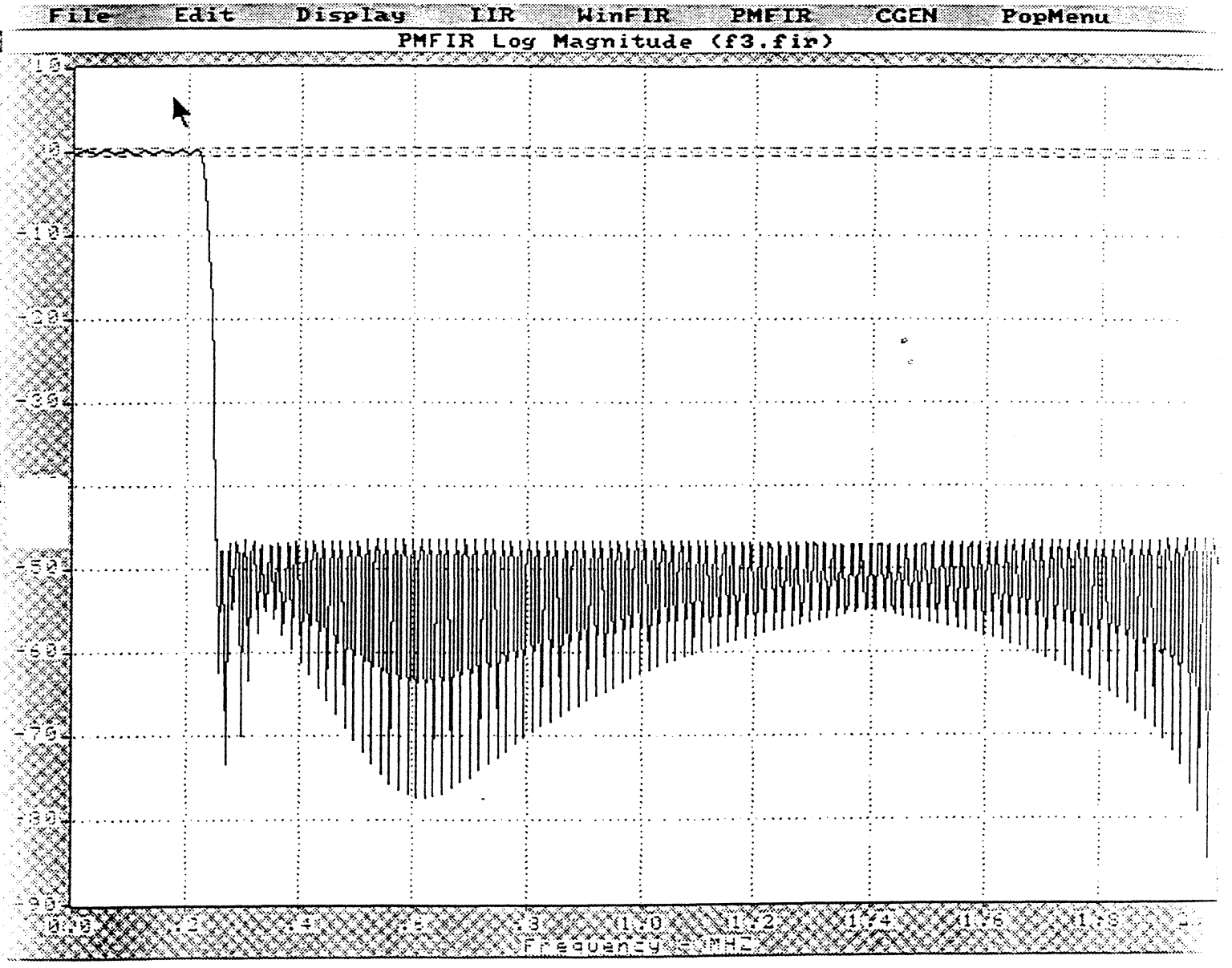
PMFIR Log Magnitude (f1.flr)
Frequency MHz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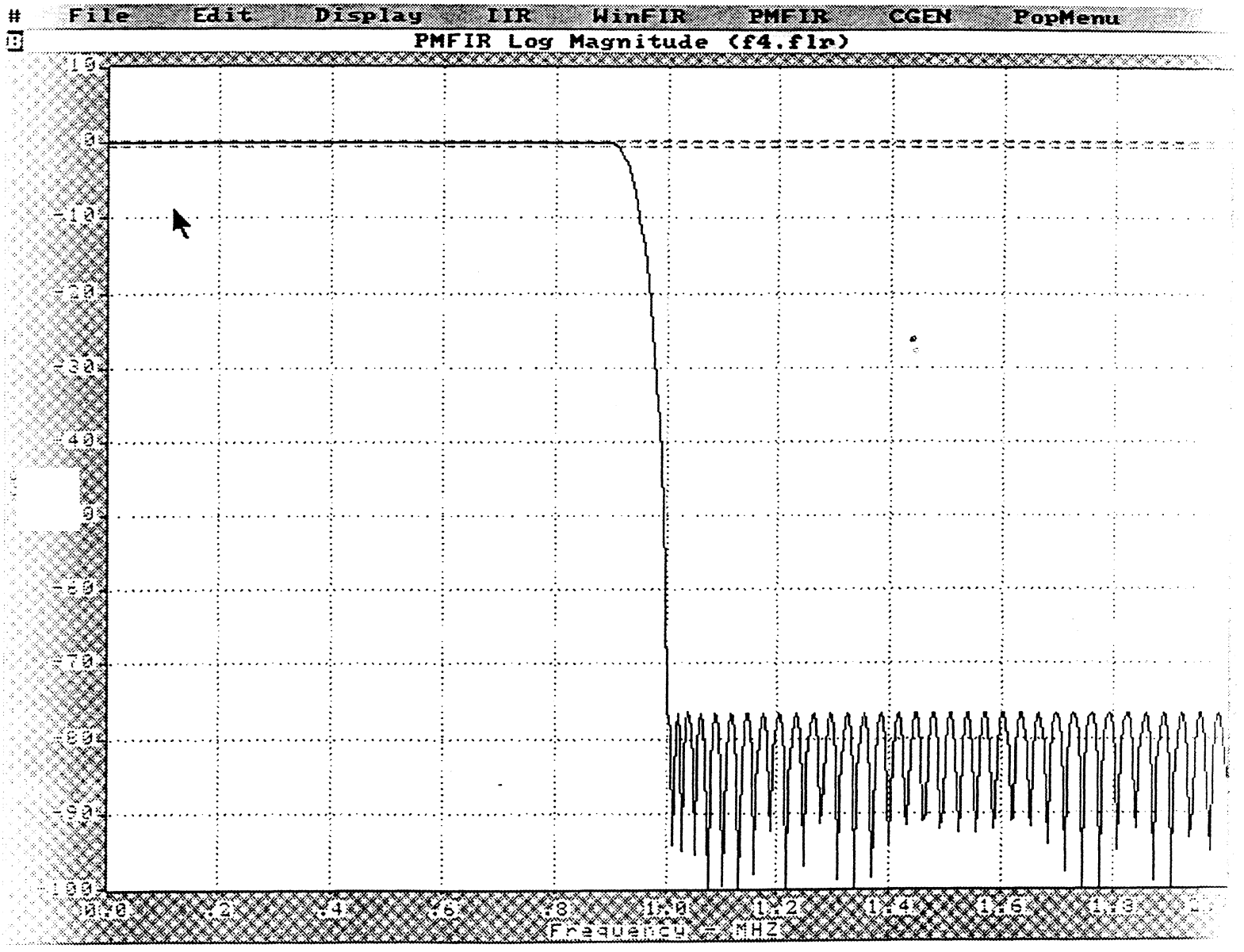
PMFIR Log Magnitude (f3.fir)
Frequency - MHz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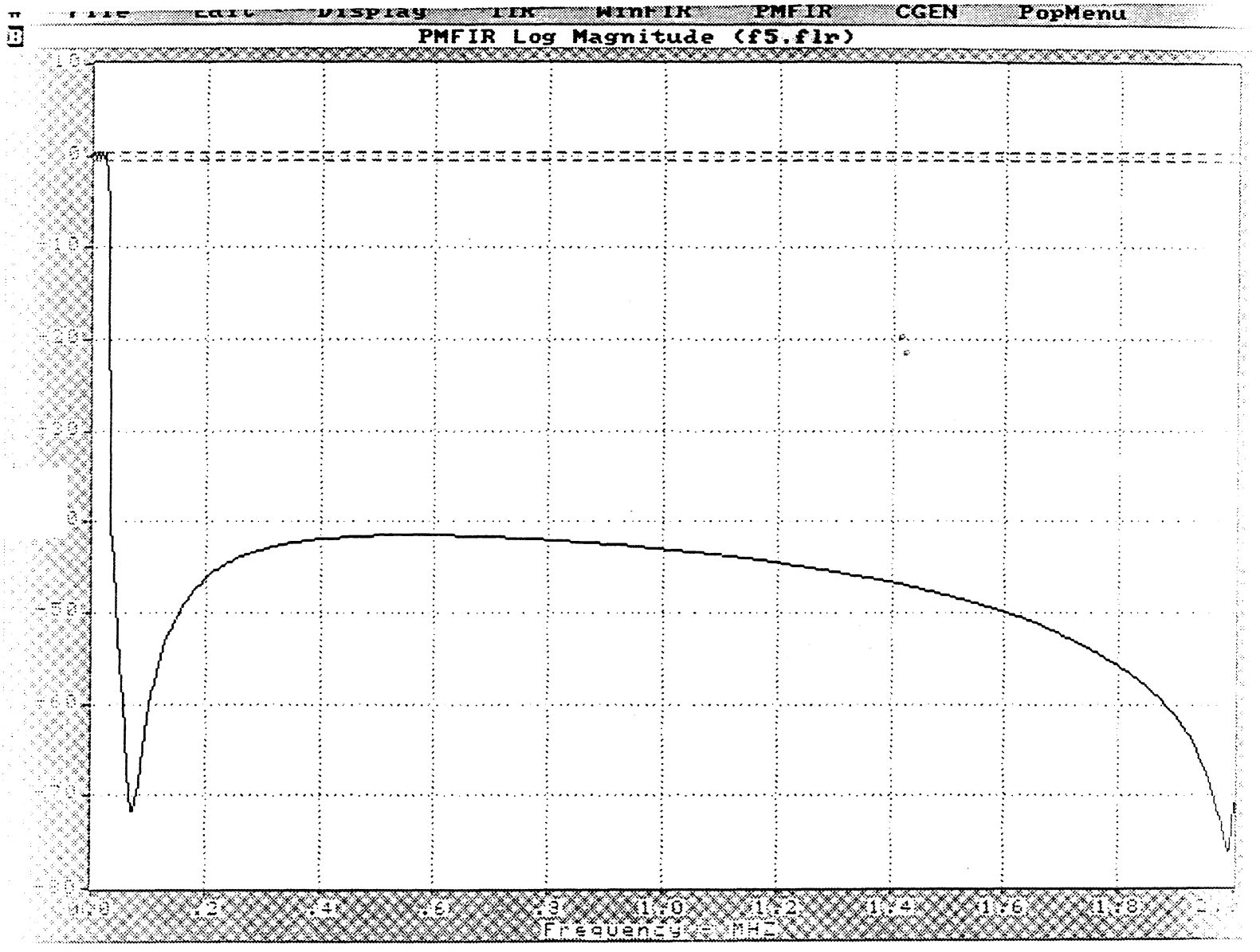
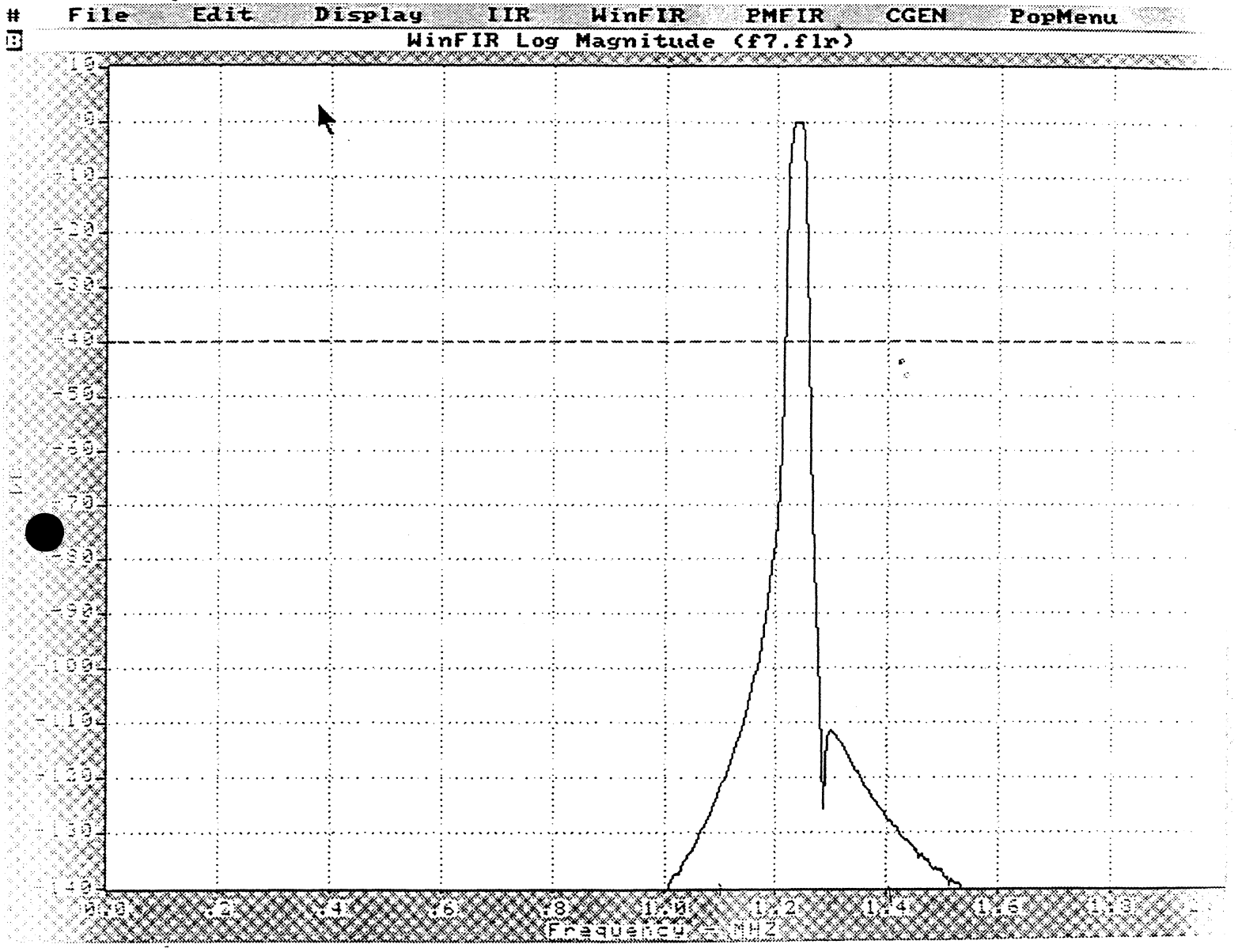
PMFIR Log Magnitude (f4.flr)
Frequency - MHZ


File Edit Display FIR WinFIR PMFIR CGEN PopMenu
PMFIR Log Magnitude (f5.flr)
.2
.4
.6
.8
1.0
1.2
1.4
1.6
1.8
Frequency = MHz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WinFIR Log Magnitude (f7.flr)
Frequency in MHZ