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MMA Correlator ASIC Specification

1.0) Introduction

This specification gives the requirements for the 4096-lag correlator ASIC to be used in the MMA correlator. This chip runs on a 125 MHz clock. The chip operating voltage will be 3.3 VDC or less (the final chip supply requirement will be determined later). The chip package will be a surface mount, cavity down, industry standard package.

Each individual lag of the correlator chip consists of a 2-bit, 4-level, times 2-bit, 4-level, multiplier whose output is summed in a 25-bit accumulator. Each accumulator has secondary storage for the 16 most significant bits. All 25 bits of the accumulator can be asynchronously cleared before an integration. A single synchronous blanking signal input to the chip can be used to stop correlation on all correlator circuits.

The MMA correlator chip has many modes of operation. A 96-bit serial program word on the chip provides the configuration information for the chip. The serial program word register on the chip must be loaded by a microprocessor external to the chip before operation can begin. The program word register has a secondary storage register to prevent the chip from seeing the serial program word shift-through.

2.0) Block diagram

Figures 1 and 3 give a complete block diagram of the MMA correlator chip. This chip is a 4-by-4 matrix of correlator blocks in which each block consists of 256 multiplier/accumulator/secondary storage circuits (referred to as lags). Each of the correlator blocks can be used as a single 256-lag correlator, as two 128-lag correlators or as four 64-lag correlators as programmed using the chip serial program word. Each 256-lag block is thus comprised of four 64-lag sub-blocks and there are a total of 64 of the 64-lag sub-blocks on the chip.

Figure 3 shows the 4-by-4 array of correlators being driven by samples from 4 antennas on each axis of the matrix (shown in the figure as antennas Y, Y+1, Y+2, and Y+3 on the vertical axis of the matrix and antennas X, X+1, X+2, and X+3 on the horizontal axis). Each antenna supplies 2-bit samples from each of two samplers (samplers M0 and M1 as seen in figure 1 and 3).

The correlator chip thus requires eight 2-bit driving signals for the vertical axis of the internal 4-by-4 matrix and eight 2-bit driving signals on the horizontal axis. The vertical axis as seen in figure 1 is always driven from the bottom of the page. The horizontal axis, as seen in figure 1, has 3 modes of drive: drive from the input pins at the bottom of figure 1, drive from the right I/O pins, or drive from the left I/O pins of figure 1. Tri-state drivers, controlled by bits of the serial program word, determine the mode of operation. When the horizontal axis of the correlator matrix is driven from the vertical axis signals, these signals also drive both the right and left I/O pins out of the chip using the tri-state drivers seen in figure 1.

Readout of the 16-bit accumulator secondary storage registers is over a 16-bit tri-state bus. Any of the 64 64-lag sub-blocks may be selected for results readout with the application of a 6-bit sub-block code plus two permissive (card X and Y axis) output enable signals. The 64-lag results shift out in lag order, zero lag first, lag one next, lag two next, etc. Any number from 1 to all 64 lags may be read from each sub-block at a time (the exact number of results read-out is determined by the duration of the shift-out gate signal).

The results readout rate is programmed by 3 bits in the chip serial program word and can be from 125 MHz to 125/8 MHz. Results shiftout always occurs on a

125 MHz chip clock rising edge. The phase of the 125/N MHz shiftout (N = 1 to 8) is controlled by the BLANKING chip input as the rising edge of this signal initializes the divide by N counter controlling results shiftout (see Figure 7).

2.1) Data input-output

Figure 2 shows data (samples) into and out of the correlator chip. The chip is meant to be connected in a matrix configuration on the correlator card in the MMA application. The chip supports the horizontal and vertical matrix structure of the card.

Figure 2 illustrates one of 16 input signals to the correlator chip. Control of the data flow is as seen via two bits of the serial program word (labeled MODE0 and MODE1 on figure 2) which control the state of the tri-state drivers internal to the chip. All 16 of the data paths in the chip are to be programmed using the same two program bits.

The vertical axis signals into the actual correlator matrix must be applied through adjustable delay lines. A delay of from zero to 31 bits is required to compensate for the position of the correlator chip in the correlator card chip matrix (all delay lines seen on Figure 1 will be programmed for the same delay).

Anti bus contention on the tri-state drivers of the chip-to-chip horizontal data axis is supplied by adjacent chips exchanging handshake signals as shown. Since all signals on the horizontal axis of the card flow in the same direction, 4 anti contention I/O pins are required on the chip, one input and one output pin on each side (right and left) on the chip (labels on Figure 2 are LEFT-OE, LEFT-OE-IN, RIGHT-OE, and RIGHT-OE-IN).

2.2) The basic correlator

Figure 6 shows one of the 4096 correlator circuits on the correlator chip. A correlator consists of a 2-bit, 4-level, by 2-bit 4-level, multiplier, using the multiplier table shown, whose output is summed in a 25-bit accumulator at the 125 MHz chip clock rate (that is, one multiplication and summation into the accumulator occurs on each clock transition). The 25-bit accumulator consists of a 5-bit synchronous stage, a 4-bit ripple-through pre-scalar, and a 16-bit ripple through counter.

The accumulator has two modes of operation depending on the state of 4 program word bits (one program bit for each row of the 256-lag blocks). In one mode, the 4-bit pre-scalar is bypassed and the accumulator acts as a 21-bit accumulator. In this mode, the pre-scaler is held static to reduce the power consumption of the chip. In the second mode, the pre-scalar is used in a normal way and the correlator has the full 25-bit accumulator for integration.

A 16-bit secondary storage register is supplied for the 16 most significant bits of the accumulator. During read-out, the 16-bit secondary storage registers shift broadside off the chip. All 64 lags from a lag sub-block connect as a 16-bit wide 64-bit deep broadside shift register.

In normal operation, the blanking signal to the chip will be high (inhibiting correlation/integration) for 256 clock cycles every 1.048 milli-seconds. Occasional blanking cycles will be marked, via an externally generated dump enable signal (an input pin to the chip), for dumping to secondary storage of all 16 upper accumulator values. Two signals, the jam load signal to the secondary storage register and the accumulator clear, will be generated from the rising edge of the marked blanking signal (see section 2.6).

2.3) 64-lag correlator sub-block

Figure 5 shows how 64 of the basic correlator circuits are connected together to build a 64-lag correlator sub-block. All 64 2-bit P (prompt) inputs to the 64 correlators are connected in parallel while the 64 2-bit D (delayed) inputs are connected to the correlators using a 64 stage (1 bit or 2 bit) lag generator (shown as a shift register on the bottom of Figure 5). The output of the sub-block lag generator connects to an adjacent 64-lag correlator sub-block input multiplexor.

The lag generating shift register has two modes of operation. In the normal mode, there is one stage of shift register between each correlator of the 64-lag correlator sub-block (for each bit of the 2-bit D signal). When the input signal is twice Nyquist sampled, the lag generator supplies two stages of shift register per signal bit between each correlator. A bit from the serial program register determines the one-or-two bit operation of lag generators for one row of correlators (4 bits for the entire chip).

2.4) 256-lag correlator block

Figure 4 shows how four 64-lag sub-blocks interconnect to make a 256-lag correlator block. Each 256-lag correlator block is driven by four 2-bit sampler signals. The exact mode of operation is controlled by 8 multiplexor stages that are programmed by 16 bits from the program word register. Each row of 256-lag correlator blocks in the 4-by-4 chip matrix receives the same 16 program word bits and, hence, a total of 64 program word bits are used to control all multiplexors on the chip.

A 16-bit 4-to-1 output multiplexor is used to allow selection of any of the four 64-lag correlator sub-blocks for read-out. The two bits to control these multiplexors come from chip inputs.

2.5) Results read-out

Figure 7 shows the final 16-bit 16-to-1 multiplexor stages required for results read-out. Sixteen bit broadside outputs from each of the sixteen 256 correlator blocks come together in these multiplexors where one 16-bit result may be selected for shift out. The shift-out control logic block of figure 7 decodes the 6-bit correlator select lines (two correlator sub-block select bits and 4 block select bits), the x- and y-axis select bits, and the shift-out enable line to develop 64 shift-out clocks, one for each 64-lag sub-block.

Results shift-out is done on the system 125 MHz clock divided by N, where N goes from 1 to 8 as selected by the serial program word. Capture of the SHIFT OUT GATE signal is done on an internally generated 125/N MHz signal synchronized to the blanking input to the chip (that is, the rising edge of the blanking signal is used to set the phase of the 125/N MHz shift-out clock). Since the exact timing of the blanking signal will vary depending on the position of the chip in the card matrix, an adjustable delay line with a 64-bit adjustment range and programmed by 6 bits from the serial program word is required (this delay is independent of the delays seen on Figure 1).

2.6) Control logic

Figure 8 shows the control logic required for the correlator chip.

A 96-bit serial in program register can be programmed from an external source to set the mode of operation for the chip. The interface to this program register is one data input pin and one clock input pin. The serial clock is buffered and output from the chip while data from the last stage of the shift register is also output from the chip so correlator chips on the correlator

card may be connected in series. Maximum shift in/out rate of the program word is 20 MHz.

The program register has a secondary register so all program bits to the chip can be made to change at once. The secondary storage register is loaded with a single strobe input to the chip. This strobe input is also buffered and driven off the chip.

The 125 MHz clock for the chip comes in on a single pin and is buffered and drives out on 4 output pins for drive to other chips on the correlator card.

The blanking signal into the chip and the dump enable signal into the chip control the correlators and correlator accumulator secondary storage registers. A logic high on the blanking term will synchronously stop all correlators on the chip (that is, all correlators will hold unchanged for the duration of the blanking term assertion).

Dump of the correlator accumulator results into the correlator secondary storage will occur about 8 clock transitions after the assertion of the blanking signal if the dump enable signal is high.

A second way for dump to storage to occur is if the diagonal program bit from the serial program register is high. Autocorrelators (correlators on the diagonal of the array correlator matrix) will be required to dump to storage every 1 msec blanking cycle. For chips on the correlator card matrix, dump will occur on 4 of the eight 256 lag correlator blocks (correlator blocks on the diagonal of the chip) after every blanking time.

All accumulators that are dumped into secondary storage will be reset by a signal generated in the control logic (about) 8 clocks after dump to storage occurs.

3.0) Input-Output pins

Below is a list of the package pins for the correlator chip;

signal name	in/out	# pins	description
C125	input	1	125 MHz clock
CLK0 thru CLK3	output	4	125 MHz clock output signals
DB0 thru DB15	inputs	16	input data signals
DT0 thru DT15	outputs	16	output data signals
DL0 thru DL15	I/O	16	left chip input/tri-state output
DR0 thru DR15	I/O	16	right chip input/tri-state output
BLANKING	input	1	blanking
BLANK OUT	output	1	blanking out
DUMP ENA	input	1	dump enable
DUMP OUT	output	1	dump enable out
PDATA	input	1	program data in
PCLK	input	1	program clock in
PSTB	input	1	program data strobe in
PDATA OUT	output	1	program data out
PCLK OUT	output	1	program clock out
PSTB OUT	output	1	program data strobe out
LAG0 THRU LAG15	tri-state	16	results read-out bus
X OE	input	1	horz output enable
Y OE	input	1	vert output enable
LAG GATE	input	1	shift-out gate
GOUT0 THRU GOUT3	output	4	gate0 thru gate3

SEL0 THRU SEL5	input	6	sel0 thru sel5
RIGHT-OE	output	1	anti bus contention signal
RIGHT-OE-IN	input	1	anti bus contention signal
LEFT-OE	output	1	anti bus contention signal
LEFT-OE-IN	input	1	anti bus contention signal
VSS	power	10?	chip power
VDD	power	10?	chip power
	total	132	

4.0) Serial program word

The 96-bit serial program word must provide control bits for the following functions:

bit name	# pins	description
DLY0 thru DLY4	5	program delay lines in DB0 thru DB15 and blanking
DLY10 thru DLY14	5	program delay lines in blanking shift out path
MODE0 AND MODE1	2	program internal tri-state drivers
R0MUX0 thru R0MUX15	16	program row 0 correlator multiplexors
R0MUX1 thru R1MUX15	16	program row 1 correlator multiplexors
R0MUX2 thru R2MUX15	16	program row 2 correlator multiplexors
R0MUX3 thru R3MUX15	16	program row 3 correlator multiplexors
R0MODE	1	row 0 21 bit/25 bit accumulator bit
R1MODE	1	row 1 21 bit/25 bit accumulator bit
R2MODE	1	row 2 21 bit/25 bit accumulator bit
R3MODE	1	row 3 21 bit/25 bit accumulator bit
R0OVERSAMP	1	row 0 over sample program bit
R1OVERSAMP	1	row 1 over sample program bit
R2OVERSAMP	1	row 2 over sample program bit
R3OVERSAMP	1	row 3 over sample program bit
DIAGONAL	1	chip diagonal program bit
SMODE0 thru SMODE2	3	shift-out rate program bits
total	88 (8 spare bits)	