3-26-99

Gary Maki - MRC

Technical questions on draft spec:
- Asynchronous clear
- Clock drive

Things might change slightly as design progresses
MRC designers are very busy.
Ray: how long would it take? A: Cadaris' estimate is OK; need full custom.
National Semiconductor - expect we might use 0.18μm process - would be OK for small volume; MOSIS & AMI possible
1 engineer would be able to do everything up to layout in 1.5 years
Might consider defining standard cells - 20 or so - and then use mostly automatic place & route; this would greatly reduce layout time at expense of some chip area and a little power consumption.
Might get use ultra low power designs - 0.35μm and 1 volt
Warner Miller 301 286 8183 - correlators & Goddard

Pressure from NASA could reorganize priorities
NSA has hired National Semiconductor - might get low cost - also Lincoln Lab is a possibility - don't know about cost