The ALMA Correlator LTA (Long Term Accumulator) Function

1 Introduction **** PRELIMINARY****

We will provide a Long Term Accumulation (LTA) function on the ALMA Correlator Cards, with a minimum of 1 msec integration for SELF products and a minimum of 16 msec for CROSS products. Additionally, we will provide the capability of high speed readout, with every result read out every 1 msec, where no Long Term Accumulation function is provided. This is intended to be an option for possible use at a later time.

All references to 1 msec specifically refer to 1.048576 msec, the fundamental blanking cycle in the system, and 16 msec is 16 times 1.048576 msec. The blanking cycle is 131,072 system clock cycles (8 nsec per cycle), of which 256 clock cycles are blanked and 130,816 cycles perform correlation.

The approximate maximum data rate available from one correlator array (see below) is 308 MByte/sec in the system proposed in these notes (1.2 GByte/sec from the total of four arrays).

The following discussion is based on a 64 antenna ALMA system.

2 Correlator Arrays

The ALMA correlator will contain four arrays of correlator cards, one array per baseband pair. Each array consists of 32 planes, and each plane consists of 4 correlator cards, as shown below (one of four arrays shown, 128 cards per array). Each plane correlates contiguous blocks of samples, provided by the memory cards. There are 32 parallel planes in order to handle the 32 parallel output paths from the sampler. The memory cards re-package the samples to drive the correlator planes.

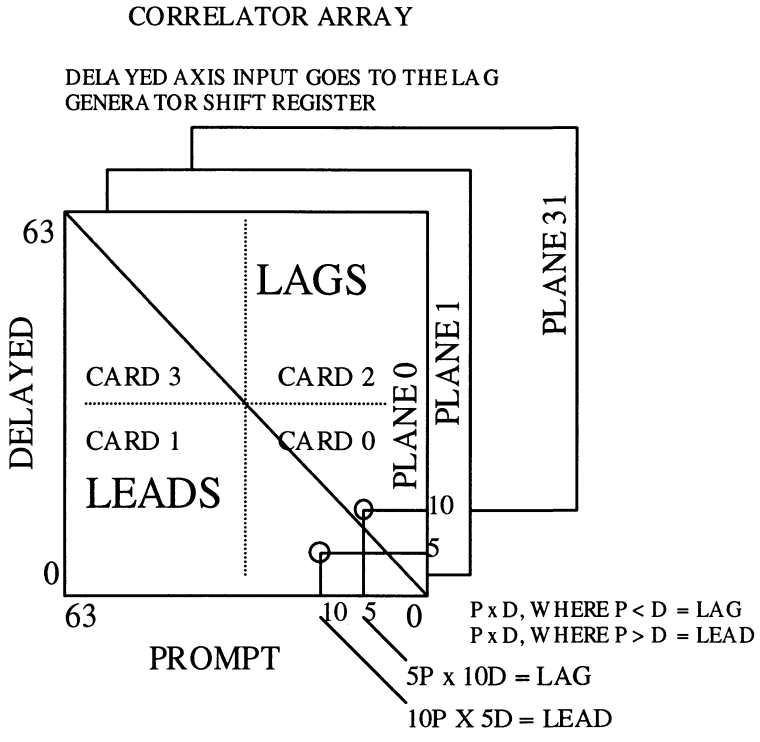

Figure 1, MMA Correlator Array

Each individual correlator card has 1,024 correlator blocks (32 x 32), and each block produces 256 sixteen bit wide results every integration period. This is a total of 262,144 results per card. These correlator blocks will be referred to as hardware baselines or just as baselines. On the diagonal cards (0 and 3), there are 32 x 256 = 8,192 self product results on each card. This leaves 253,952 non-self products on each of these cards, where half (126,976) are LEADs and the other half are LAGs.

There are a total of 16,384 self products, 516,096 LEADs and 516,096 LAGs per plane. The total number of results in one card, one plane, one array and in the complete system of four arrays are:

PRODUCT	ONE NON-DIAG CARD	ONE DIAG CARD	ONE PLANE	ONE ARRAY	FOUR ARRAYS
SELF	0	8,192	16,384	524,288	2,097,152
CROSS	262,144	253,952	1,032,192	33,030,144	132,120,576
TOTAL	262,144	262,144	1,048,576	33,554,432	134,217,728

(Total ram storage for 134,217,728 results at 4 bytes per result = 536,870,912 bytes; if double buffered, this produces a total of 1,073,741,824 bytes = 1 Gbyte total.)

2.1 Correlator Plane

Figure 2, One Correlator Plane , shows a set of four correlator cards, forming a single plane (1 of 32) of a correlator array, with the diagonal correlator chips highlighted. Each chip contains 16 baselines (a baseline produces 256 product results), and in each diagonal chip four of the baselines are SELF products (the baselines on the chip diagonal). Each card contains 64 chips, labeled 0-63 in the figure.

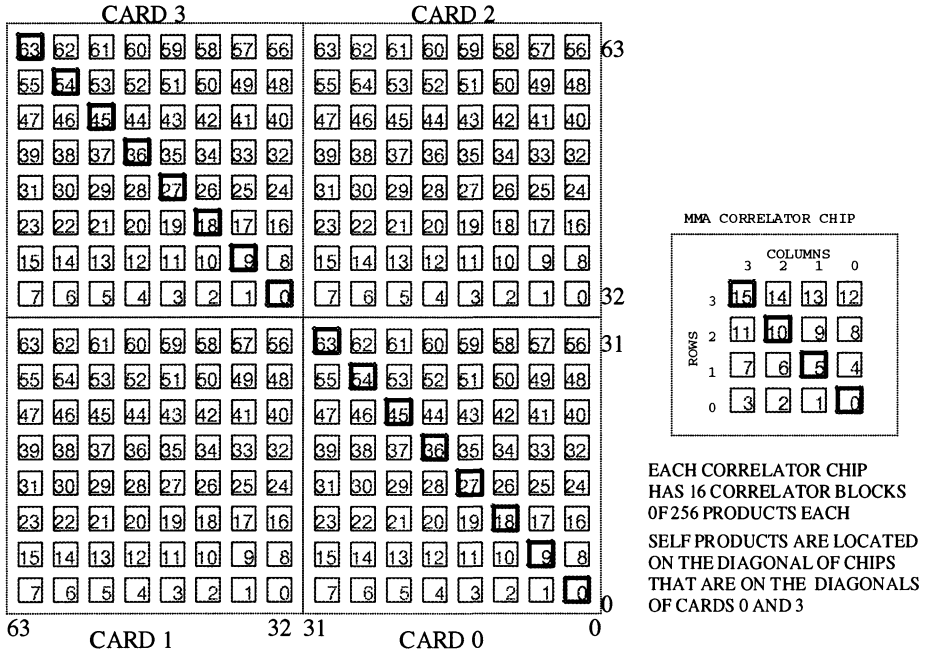

Figure 2, One Correlator Plane

The defined numbering order for hardware baselines in a correlator plane is given in Appendix I, Baseline Map.

3 Initial LTA Goals

Two basic operating modes for the correlator card are planned:

1) Low Speed Mode: Read correlator chip SELF products every 1 msec, and CROSS products every 16 msec. Provide Long Term Accumulation locally (on the Correlator card) in multiples of 1 msec for SELF and multiples of 16 msec for CROSS results.

   All results are transferred out of the correlator card on a single output data link, at a rate of 32 nsec per result. Results are 32 bit unsigned integers.

2) High Speed Mode: Read all correlator chip products (SELF and CROSS), every 1 msec. No Long Term Accumulation is provided. Results are transferred out of the correlator card on 8 parallel output data links, at a rate of 16 nsec per result on each of the 8 links. Results are 16 bit unsigned integers.

3.1 LTA Implementation

There are 64 correlator chips on a correlator card. The chips are grouped in 8 groups of eight. Each group of 8 chips connects to a LTA. In Low Speed Mode, results from four LTA are multiplexed together, producing two output streams that are further multiplexed into one final output data link at the card output. In High Speed Mode, each group of 8 chips drives a separate output data link.

Within each group of 8 chips, pairs of chips are tri-stated together, so there are four tri-state buses feeding each LTA. Each bus is 16 bits wide. The tri-state buses are restricted to being driven by only two chips in order to accommodate the High Speed Mode, where each chip access must be completed in 64 nsec. This is on the conservative side. All 8 chips on one tri-state bus would require 16 nsec accesses in High Speed Mode. Four chips per bus would probably be reasonable, but this still requires two 16 bit buses into the LTA, and pin counts will probably require that we use a separate CPLD to multiplex the chip buses into a single 16 pin bus to the LTA. The LTA will consist of a 240 pin plastic quad flat pack FPGA and a static ram. A 144 pin PQFP CPLD will be used to multiplex the four chip buses into the FPGA.

The output data links will pass data that is 16 bits wide. The 32 bit data width from the LTA will be passed in two 16 bit words. Present plans call for investigating the use of the National or TI LVDS serial links, using the serializers that handle 21 bits of parallel data. The link requires 4 twisted pairs. Present plans also call for investigating the use of 2 mm Hard Metric connectors, where a single backplane cable connector consists of a wafer with two twinaxial differential pairs, so a cable assembly of two cable wafers is required for the Low Speed Mode output data link.

The High Speed Mode output links will require 8 output cable assemblies, or a total of 16 cable wafers.

The two modes will not co-exist. Different FPGA personalities will be required for the two modes. High Speed Mode will require a completely different LTA path, external to the correlator card. No further consideration will be given to this mode in the following discussion.

The on card LTA functions will be followed by subsequent LTA stages, to further combine results from individual planes as necessary.

4 Readout Cycle

A single correlator chip can be considered to contain 16 baselines of 256 results each. For purposes of reading results from the chips, we do not need to know what the 256 results represent. (The results could be four sets of 64 lags from polarization pairs for example.) Most chips in the system will be producing only CROSS products, while some chips will produce both CROSS and SELF products. The chip will do dump to storage for the SELF products every blanking cycle (the 1.048576 msec cycle), and dump to storage for the CROSS products every 16 blanking cycles.

The LTA must read all SELF products every 1 msec and all CROSS products every 16 msec. Thus it is required that on average, we read all the SELF products and 1/16 of the CROSS products every 1 msec.

The readout of SELF products will require 0.262144 msec (1/4 of the blanking cycle). This will be referred to as TIME SLOT 0. Readout of CROSS products will require 0.524288 msec (1/2 of the blanking cycle). This will be referred to as TIME SLOT 1. The final ¼ of the blanking cycle provides time for housekeeping chores if needed.

5 Data Rates

Looking at the maximum data rate available from a single plane of one correlator array, we have 16,384 SELF results per 1 msec or 15,600,000 results per second, plus 1,032,192 CROSS results per 16 msec or 61,523,437 results per second. This is a total of approximately 77 million results per second. At four bytes per result, this is 308 MByte/sec data rate capacity from a single plane, 9.9 GByte /sec total from one array of 32 planes, and 39.4 GByte/sec total from all four arrays.

On a per card basis, there are 262,144 CROSS results per 16 msec from a non-diagonal card, and 253,952 CROSS results from a diagonal card, plus 8192 SELF results per 1 msec from a diagonal card. The data rate from a non-diagonal card is thus 15,625,000 results per second, or 62.5 MByte/sec. From a diagonal card the rate is 91.8 MByte/sec. The total for the four cards in one plane is thus approximately 308 MByte/sec. (These are the rates if all results are transferred from the cards using the shortest accumulation times of 1 msec for SELF and 16 msec for CROSS.)

We need to determine how we will throttle back on the data in the subsequent stages of the LTA (the stages that follow the correlator card LTA). The scheme proposed below will cut the maximum data rate by a factor of 32, so that the 308 MByte/sec from each of 32 planes in an array is cut back to 308 MByte/sec total from one array.

We presently propose to use a pipelined adder tree following the 32 planes of a correlator array. At one extreme (2 GHz bandwidth), this adder tree will add together the results from 32 planes. At the other extreme (2 GHz/32 bandwidth), the adder tree will provide a path by which the results from 32 planes are multiplexed out to the final link to the VME system.

At full bandwidth (2 GHz), all 32 planes can be summed together, producing 256 spectral channel results per baseline in each of the four arrays, with minimum integration times of 1 msec and 16 msec for SELF and CROSS results respectively. At minimum bandwidth (62.5 MHz), all 32 planes contain distinct lags, producing 8192 spectral channel results per baseline in each of the four arrays. But in order to multiplex all 32 planes to the output instead of adding the 32 planes, the minimum integration time must be increased by a factor of 32.

Table 1, Integration Times, tabulates the total number of spectral channels produced across all four arrays, for each bandwidth from 2 GHz to 62.5 MHz, where the minimum integration times are increased by factors of 2 for each factor of 2 increase in the number of available spectral channels. The number of spectral channels from each array could be for a single baseband, or split between the two basebands in a pair, or split into full polarization mode (RR, RL, LR, LL).

BANDWIDTH EACH BB	SPEC CHANS EACH ARRAY	SPEC CHANS TOTAL	MIN SELF INT	MIN CROSS INT
2 GHz	256	1024	1 msec	16 msec
1 GHz	512	2048	2 msec	32 msec
500 MHz	1024	4096	4 msec	64 msec
250 MHz	2048	8192	8 msec	128 msec
125 MHz	4096	16384	16 msec	256 msec
62.5 MHz	8192	32768	32 msec	512 msec

Table 1, Integration Times

Table 1, Integration Times, presents integration times for cases where maximum spectral resolution is required at each bandwidth. It should be possible to trade spectral resolution for integration time. At the more narrow bandwidths, if it is not required to retain the full spectral resolution, then the integration times can be decreased proportional to the decrease in resolution. If we discard the additional spectral resolution, so that we develop only 1024 spectral channels (across all 4 arrays), then the minimum integration times remain at 1 msec for SELF and 16 msec for CROSS.

A possible tradeoff to consider providing is a mode where we take the signals from one baseband pair and process them through the four baseband pair paths of the correlator. In this case, the data could be gated in each array, where only one array is gated on at a time. Each array integrates for ¼ of the available time. As an example, at a bandwidth of 500 MHz, we have the capacity to produce 1024 spectral channels in each array, or 4096 spectral channels total, and each array integrates for 4 msec / 64 msec for SELF/CROSS products. The results that are read out of each array every 4 msec / 64 msec contain integrations that actually represent only 1 msec / 16 msec actual integration time due to the gating.

6 Data Readout

Appendix II provides details of the data paths on the correlator card, and gives an example of which chip baselines might be read out in each time slot during a set of sixteen 1 msec intervals, in a set of two LTA. Results are not double buffered in the LTA functions. This requires that the off card adder tree is capable of accepting data when it is presented, rather than being able to request data from the correlator card. Additionally, if the LTA is accumulating for multiple integration times (e.g. four 16 msec intervals), at the end of 64 msec the results will be transferred out of the correlator card in a single 16 msec interval instead of being spread out over a 64 msec interval. Double buffering will be provided at the output of the adder tree, so that the VME system is not forced to take bursts of data in this manner. For example, if the LTA accumulation time is 64 msec, each dump of data will be available for the whole 64 msec interval.

Re-iterating, SELF results always dump from correlator chip to on card LTA every 1 msec. CROSS results always dump from correlator chip to on card LTA every 16 msec. The LTA then accumulates SELF results for multiples of 1 msec and CROSS results for multiples of 16 msec. But the accumulated results dump from the LTA to the adder tree in 1 msec bursts for SELF and 16 msec bursts for CROSS.

LTA accumulation time is controlled on a baseline basis. For every baseline being processed by the LTA, it is necessary to specify if it is time to Clear Accumulator and to transfer the previous accumulated result to the adder tree. When processing SELF products, a LTA reads two baselines at a time, 256 results per baseline, 256 nsec per result, for a total of 65 usec. The LTA thus must be updated every 65 usec with the Clear Accumulator state for two baselines. For CROSS products, the LTA must be updated every 262 usec, with the state for four baselines.

7 Ram Storage Requirements

Each local LTA provides storage for 8 correlator chips times 16 baselines times 256 results each = 32,768 results. Each storage location is 4 bytes wide, so this is 128K Bytes total ram per LTA. The total storage on one correlator card is thus 8 times 128K or 1 M Byte total, and the total storage in one correlator plane is 4 M Byte. Thus the first stage of the adder tree must provide 4 M Byte per plane for each of 32 planes, or 128 M Byte total ram storage for one array. Subsequent stages of the adder tree require half as much storage at each stage, with a double buffered output stage, for a total of 256 M Byte storage in the adder tree for one array.

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1 2 OF BASELINES DISTRIBUTED ACROSS 4 CORRELATOR CARDS IN ONE PLANE OF A MMA CORRELATOR ARRAY

LAG BASELINES ABOVE DIAGONAL

CARD 3 CARD 2

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
2079 2078 2076 2073 2069 2064 2058 2051 2043 2034 2024 2013 2001 1988 1974 1959 1943 1926 1908 1889 1869 1848 1826 1803 1779 1754 1728 1701 1673 1644 1614 1583	1551 1518 1484 1449 1413 1376 1338 1299 1259 1218 1176 1133 1089 1044 998 951 903 854 804 753 701 648 594 539 483 426 368 309 249 188 126 63	
2078 **2077** 2075 2072 2068 2063 2057 2050 2042 2033 2023 2012 2000 1987 1973 1958 1942 1925 1907 1888 1868 1847 1825 1802 1778 1753 1727 1700 1672 1643 1613 1582	1550 1517 1483 1448 1412 1375 1337 1298 1258 1217 1175 1132 1088 1043 997 950 902 853 803 752 700 647 593 538 482 425 367 308 248 187 125 62	7
2076 2075 **2074** 2071 2067 2062 2056 2049 2041 2032 2022 2011 1999 1986 1972 1957 1941 1924 1906 1887 1867 1846 1824 1801 1777 1752 1726 1699 1671 1642 1612 1581	1549 1516 1482 1447 1411 1374 1336 1297 1257 1216 1174 1131 1087 1042 996 949 901 852 802 751 699 646 592 537 481 424 366 307 247 186 124 61	
2073 2072 2071 **2070** 2066 2061 2055 2048 2040 2031 2021 2010 1998 1985 1971 1956 1940 1923 1905 1886 1866 1845 1823 1800 1776 1751 1725 1698 1670 1641 1611 1580	1548 1515 1481 1446 1410 1373 1335 1296 1256 1215 1173 1130 1086 1041 995 948 900 851 801 750 698 645 591 536 480 423 365 306 246 185 123 60	__
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413 1412 1411 1410 1409 1408 1407 1406 1405 1404 1403 1402 1401 1400 1399 1398 1397 1396 1395 1394 1393 1392 1391 1390 1389 1388 1387 1386 1385 1384 1383 1382	1381 1380 1379 1378 **1377** 1340 1302 1263 1223 1182 1140 1097 1053 1008 962 915 867 818 768 717 665 612 558 503 447 390 332 273 213 152 90 27	
1376 1375 1374 1373 1372 1371 1370 1369 1368 1367 1366 1365 1364 1363 1362 1361 1360 1359 1358 1357 1356 1355 1354 1353 1352 1351 1350 1349 1348 1347 1346 1345	1344 1343 1342 1341 1340 **1339** 1301 1262 1222 1181 1139 1096 1052 1007 961 914 866 817 767 716 664 611 557 502 446 389 331 272 212 151 89 26	6
1338 1337 1336 1335 1334 1333 1332 1331 1330 1329 1328 1327 1326 1325 1324 1323 1322 1321 1320 1319 1318 1317 1316 1315 1314 1313 1312 1311 1310 1309 1308 1307	1306 1305 1304 1303 1302 **1301** **1300** 1261 1221 1180 1138 1095 1051 1006 960 913 865 816 766 715 663 610 556 501 445 388 330 271 211 150 88 25	
1299 1298 1297 1296 1295 1294 1293 1292 1291 1290 1289 1288 1287 1286 1285 1284 1283 1282 1281 1280 1279 1278 1277 1276 1275 1274 1273 1272 1271 1270 1269 1268	1267 1266 1265 1264 1263 1262 1261 **1260** 1220 1179 1137 1094 1050 1005 959 912 864 815 765 714 662 609 555 500 444 387 329 270 210 149 87 24	__
1259 1258 1257 1256 1255 1254 1253 1252 1251 1250 1249 1248 1247 1246 1245 1244 1243 1242 1241 1240 1239 1238 1237 1236 1235 1234 1233 1232 1231 1230 1229 1228	1227 1226 1225 1224 1223 1222 1221 **1220** **1219** 1178 1136 1093 1049 1004 958 911 863 814 764 713 661 608 554 499 443 386 328 269 209 148 86 23	
1218 1217 1216 1215 1214 1213 1212 1211 1210 1209 1208 1207 1206 1205 1204 1203 1202 1201 1200 1199 1198 1197 1196 1195 1194 1193 1192 1191 1190 1189 1188 1187	1186 1185 1184 1183 1182 1181 1180 1179 **1178** **1177** 1135 1092 1048 1003 957 910 862 813 763 712 660 607 553 498 442 385 327 268 208 147 85 22	5
1176 1175 1174 1173 1172 1171 1170 1169 1168 1167 1166 1165 1164 1163 1162 1161 1160 1159 1158 1157 1156 1155 1154 1153 1152 1151 1150 1149 1148 1147 1146 1145	1144 1143 1142 1141 1140 1139 1138 1137 1136 **1135** **1134** 1091 1047 1002 956 909 861 812 762 711 659 606 552 497 441 384 326 267 207 146 84 21	
1133 1132 1131 1130 1129 1128 1127 1126 1125 1124 1123 1122 1121 1120 1119 1118 1117 1116 1115 1114 1113 1112 1111 1110 1109 1108 1107 1106 1105 1104 1103 1102	1101 1100 1099 1098 1097 1096 1095 1094 1093 1092 **1091** **1090** 1046 1001 955 908 860 811 761 710 658 605 551 496 440 383 325 266 206 145 83 20	__
1089 1088 1087 1086 1085 1084 1083 1082 1081 1080 1079 1078 1077 1076 1075 1074 1073 1072 1071 1070 1069 1068 1067 1066 1065 1064 1063 1062 1061 1060 1059 1058	1057 1056 1055 1054 1053 1052 1051 1050 1049 1048 1047 **1046** **1045** 1000 954 907 859 810 760 709 657 604 550 495 439 382 324 265 205 144 82 19	
1044 1043 1042 1041 1040 1039 1038 1037 1036 1035 1034 1033 1032 1031 1030 1029 1028 1027 1026 1025 1024 1023 1022 1021 1020 1019 1018 1017 1016 1015 1014 1013	1012 1011 1010 1009 1008 1007 1006 1005 1004 1003 1002 1001 **1000** **999** 953 906 858 809 759 708 656 603 549 494 438 381 323 264 204 143 81 18	4
998 997 996 995 994 993 992 991 990 989 988 987 986 985 984 983 982 981 980 979 978 977 976 975 974 973 972 971 970 969 968 967	966 965 964 963 962 961 960 959 958 957 956 955 954 **953** **952** 905 857 808 758 707 655 602 548 493 437 380 322 263 203 142 80 17	
951 950 949 948 947 946 945 944 943 942 941 940 939 938 937 936 935 934 933 932 931 930 929 928 927 926 925 924 923 922 921 920	919 918 917 916 915 914 913 912 911 910 909 908 907 906 905 **904** 856 807 757 706 654 601 547 492 436 379 321 262 202 141 79 16	__
903 902 901 900 899 898 897 896 895 894 893 892 891 890 889 888 887 886 885 884 883 882 881 880 879 878 877 876 875 874 873 872	871 870 869 868 867 866 865 864 863 862 861 860 859 858 857 **856** **855** 806 756 705 653 600 546 491 435 378 320 261 201 140 78 15	
854 853 852 851 850 849 848 847 846 845 844 843 842 841 840 839 838 837 836 835 834 833 832 831 830 829 828 827 826 825 824 823	822 821 820 819 818 817 816 815 814 813 812 811 810 809 808 807 806 **805** 755 704 652 599 545 490 434 377 319 260 200 139 77 14	3
804 803 802 801 800 799 798 797 796 795 794 793 792 791 790 789 788 787 786 785 784 783 782 781 780 779 778 777 776 775 774 773	772 771 770 769 768 767 766 765 764 763 762 761 760 759 758 757 756 755 **754** 703 651 598 544 489 433 376 318 259 199 138 76 13	
753 752 751 750 749 748 747 746 745 744 743 742 741 740 739 738 737 736 735 734 733 732 731 730 729 728 727 726 725 724 723 722	721 720 719 718 717 716 715 714 713 712 711 710 709 708 707 706 705 704 **703** **702** 650 597 543 488 432 375 317 258 198 137 75 12	__
701 700 699 698 697 696 695 694 693 692 691 690 689 688 687 686 685 684 683 682 681 680 679 678 677 676 675 674 673 672 671 670	669 668 667 666 665 664 663 662 661 660 659 658 657 656 655 654 653 652 651 650 **649** 596 542 487 431 374 316 257 197 136 74 11	
648 647 646 645 644 643 642 641 640 639 638 637 636 635 634 633 632 631 630 629 628 627 626 625 624 623 622 621 620 619 618 617	616 615 614 613 612 611 610 609 608 607 606 605 604 603 602 601 600 599 598 597 596 **595** 541 486 430 373 *315* 256 196 135 73 10	2
594 593 592 591 590 589 588 587 586 585 584 583 582 581 580 579 578 577 576 575 574 573 572 571 570 569 568 567 566 565 564 563	562 561 560 559 558 557 556 555 554 553 552 551 550 549 548 547 546 545 544 543 542 541 **540** 485 429 372 *314* 255 195 134 72 9	
539 538 537 536 535 534 533 532 531 530 529 528 527 526 525 524 523 522 521 520 519 518 517 516 515 514 513 512 511 510 509 508	507 506 505 504 503 502 501 500 499 498 497 496 495 494 493 492 491 490 489 488 487 486 485 **484** 428 371 313 254 194 133 71 8	__
483 482 481 480 479 478 477 476 475 474 473 472 471 470 469 468 467 466 465 464 463 462 461 460 459 458 457 456 455 454 453 452	451 450 449 448 447 446 445 444 443 442 441 440 439 438 437 436 435 434 433 432 431 430 429 **428** **427** 370 312 253 193 132 70 7	
426 425 424 423 422 421 420 419 418 417 416 415 414 413 412 411 410 409 408 407 406 405 404 403 402 401 400 399 398 397 396 395	394 393 392 391 390 389 388 387 386 385 384 383 382 381 380 379 378 377 376 375 374 373 372 371 370 **369** 311 252 192 131 69 6	1
368 367 366 365 364 363 362 361 360 359 358 357 356 355 354 353 352 351 350 349 348 347 346 345 344 343 342 341 340 339 338 337	336 335 334 333 332 331 330 329 328 327 326 325 324 323 322 321 320 319 318 317 316 *315* 314 313 312 311 **310** 251 191 130 68 5	
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188 187 186 185 184 183 182 181 180 179 178 177 176 175 174 173 172 171 170 169 168 167 166 165 164 163 162 161 160 159 158 157	156 155 154 153 152 151 150 149 148 147 146 145 144 143 142 141 140 139 138 137 136 135 134 133 132 131 130 129 128 **127** 65 2	0
126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 110 109 108 107 106 105 104 103 102 101 100 99 98 97 96 95	94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 **64** 1	
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 **0**	

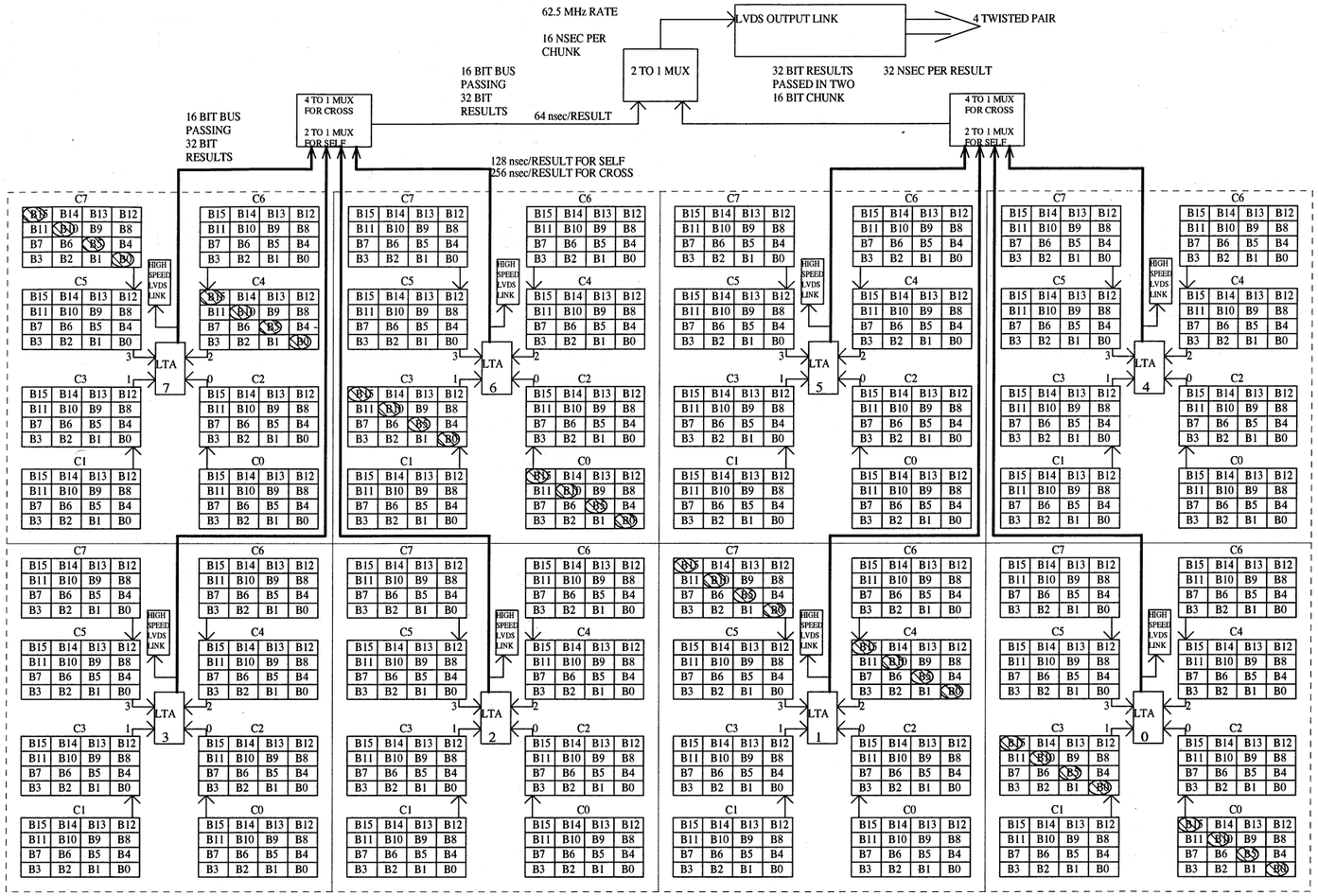
CARD 1 PROMPT AXIS CARD 0

LEAD BASELINES BELOW DIAGONAL

|__ 16 baselines all in one chip
8 x 8 matrix of correlator chips per card
64 correlator chips per card
Each baseline = 256, 16 bit results

|__BSLINE 315 LEAD
10 PROMPT x 5 DLYD

|__BSLINE 315 LAG
5 PROMPT x 10 DLYD



CORRELATOR CARD
(INCLUDES LTA)

SELF AND CROSS ON CARD

"REPRESENTATIVE" READOUT SEQUENCE FOR ONE COLUMN PAIR

1 MSEC NR	TIME SLOT	LTA 0 CHIP BUS 0 CHIP	LTA 0 CHIP BUS 0 BSLINES	LTA 0 CHIP BUS 1 CHIP	LTA 0 CHIP BUS 1 BSLINES	LTA 0 CHIP BUS 2 CHIP	LTA 0 CHIP BUS 2 BSLINES	LTA 0 CHIP BUS 3 CHIP	LTA 0 CHIP BUS 3 BSLINES	LTA 4 CHIP BUS 0 CHIP	LTA 4 CHIP BUS 0 BSLINES	LTA 4 CHIP BUS 1 CHIP	LTA 4 CHIP BUS 1 BSLINES	LTA 4 CHIP BUS 2 CHIP	LTA 4 CHIP BUS 2 BSLINES	LTA 4 CHIP BUS 3 CHIP	LTA 4 CHIP BUS 3 BSLINES
0	SLOT0	0	0,5,10,15	3	0,5,10,15												
1	SLOT0	0	0,5,10,15	3	0,5,10,15												
2	SLOT0	0	0,5,10,15	3	0,5,10,15												
3	SLOT0	0	0,5,10,15	3	0,5,10,15												
4	SLOT0	0	0,5,10,15	3	0,5,10,15												
5	SLOT0	0	0,5,10,15	3	0,5,10,15												
6	SLOT0	0	0,5,10,15	3	0,5,10,15												
7	SLOT0	0	0,5,10,15	3	0,5,10,15												
8	SLOT0	0	0,5,10,15	3	0,5,10,15												
9	SLOT0	0	0,5,10,15	3	0,5,10,15												
10	SLOT0	0	0,5,10,15	3	0,5,10,15												
11	SLOT0	0	0,5,10,15	3	0,5,10,15												
12	SLOT0	0	0,5,10,15	3	0,5,10,15												
13	SLOT0	0	0,5,10,15	3	0,5,10,15												
14	SLOT0	0	0,5,10,15	3	0,5,10,15												
15	SLOT0	0	0,5,10,15	3	0,5,10,15												

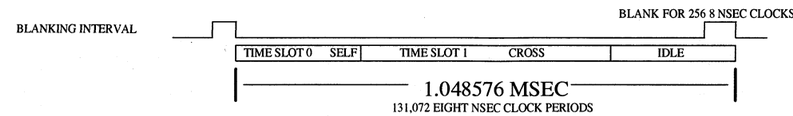
NO RESULTS READ FROM THESE CHIP BUSES DURING TIME SLOT 0

NO RESULTS READ FROM THESE CHIP BUSES DURING TIME SLOT 0

TIME SLOT 0 = SELF

TIME SLOT 1 = CROSS

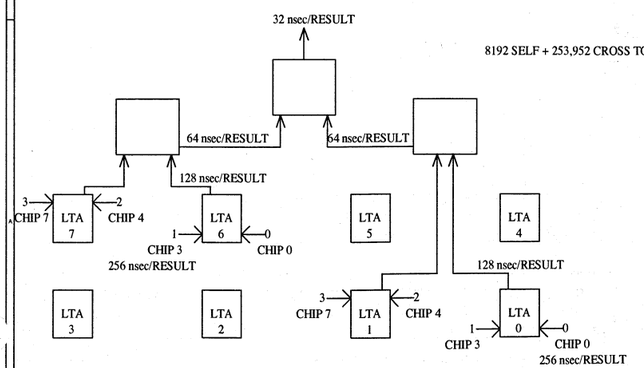
1 MSEC NR	TIME SLOT	CHIP BUS 0 CHIP	CHIP BUS 0 BSLINES	CHIP BUS 1 CHIP	CHIP BUS 1 BSLINES	CHIP BUS 2 CHIP	CHIP BUS 2 BSLINES	CHIP BUS 3 CHIP	CHIP BUS 3 BSLINES	CHIP BUS 0 CHIP	CHIP BUS 0 BSLINES	CHIP BUS 1 CHIP	CHIP BUS 1 BSLINES	CHIP BUS 2 CHIP	CHIP BUS 2 BSLINES	CHIP BUS 3 CHIP	CHIP BUS 3 BSLINES
0	SLOT1	2	0,1	1	0,1	6	0,1	5	0,1	2	0,1	1	0,1	6	0,1	5	0,1
1	SLOT1	2	2,3	1	2,3	6	2,3	5	2,3	2	2,3	1	2,3	6	2,3	5	2,3
2	SLOT1	2	4,5	1	4,5	6	4,5	5	4,5	2	4,5	1	4,5	6	4,5	5	4,5
3	SLOT1	2	6,7	1	6,7	6	6,7	5	6,7	2	6,7	1	6,7	6	6,7	5	6,7
4	SLOT1	2	8,9	1	8,9	6	8,9	5	8,9	2	8,9	1	8,9	6	8,9	5	8,9
5	SLOT1	2	10,11	1	10,11	6	10,11	5	10,11	2	10,11	1	10,11	6	10,11	5	10,11
6	SLOT1	2	12,13	1	12,13	6	12,13	5	12,13	2	12,13	1	12,13	6	12,13	5	12,13
7	SLOT1	2	14,15	1	14,15	6	14,15	5	14,15	2	14,15	1	14,15	6	14,15	5	14,15
8	SLOT1	0	1,2	3	1,2	4	1,2	7	1,2	0	1,2	3	1,2	4	1,2	7	1,2
9	SLOT1	0	3,4	3	3,4	4	3,4	7	3,4	0	3,4	3	3,4	4	3,4	7	3,4
10	SLOT1	0	6,7	3	6,7	4	6,7	7	6,7	0	6,7	3	6,7	4	6,7	7	6,7
11	SLOT1	0	8,9	3	8,9	4	8,9	7	8,9	0	8,9	3	8,9	4	8,9	7	8,9
12	SLOT1	0	11,12	3	11,12	4	11,12	7	11,12	0	11,12	3	11,12	4	11,12	7	11,12
13	SLOT1	0	13,14	3	13,14	4	13,14	7	13,14	0	13,14	3	13,14	4	13,14	7	13,14
14	SLOT1	NO RESULTS READ HERE				4	0,5	7	0,5	0	0,5	3	0,5	4	0,5	7	0,5
15	SLOT1					4	10,15	7	10,15	0	10,15	3	10,15	4	10,15	7	10,15



LOW SPEED MODE: 1 MSEC MIN SELF 16 MSEC MIN CROSS

TIME SLOT 0 TOTAL TIME = 0.262144 msec (1/4 OF THE BLANKING INTERVAL)

32 SELF BASELINES, 8192 SELF RESULTS TOTAL READ OUT EACH BLANKING INTERVAL



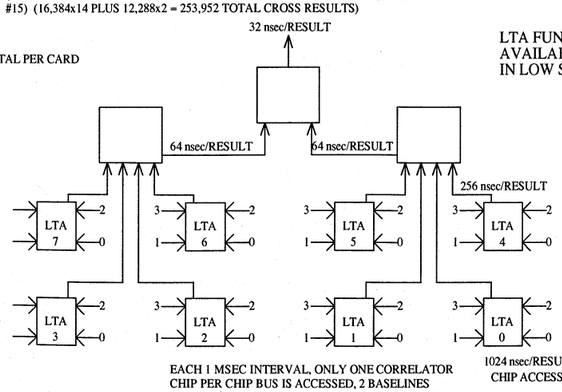
EACH 1 MSEC INTERVAL, ONLY ONE CORRELATOR CHIP PER CHIP BUS IS ACCESSED, 4 BASELINES PER ACCESSED CHIP, 256 RESULTS PER BASELINE

1024 SELFS IN ONE CHIP TIMES 256 nsec EACH EQUALS 262.144 usec EACH 1.048576 msec

8192 SELF + 253,952 CROSS TOTAL PER CARD

TIME SLOT 1 TOTAL TIME = 0.524288 msec (1/2 OF THE BLANKING INTERVAL)

64 CROSS BASELINES, 16,384 CROSS RESULTS TOTAL READ OUT EACH BLANKING INTERVAL (TRUE FOR 1 MSEC # 0 - 13; ONLY 48 CROSS BASELINES, 12,288 CROSS RESULTS IN #14 AND #15) (16,384x14 PLUS 12,288x2 = 253,952 TOTAL CROSS RESULTS)



EACH 1 MSEC INTERVAL, ONLY ONE CORRELATOR CHIP PER CHIP BUS IS ACCESSED, 2 BASELINES PER CHIP READ OUT, 256 RESULTS PER BASELINE, 512 RESULTS TIMES 1.024 usec = 524.288 usec

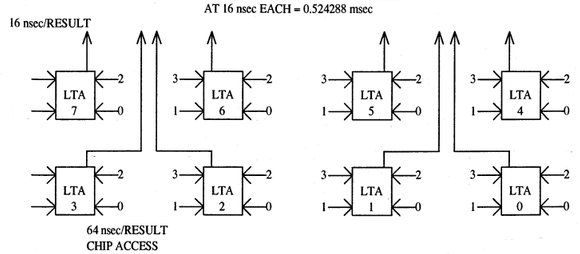
LTA FUNCTION ONLY AVAILABLE IN LOW SPEED MODE

HIGH SPEED MODE: 1MSEC FOR SELF AND CROSS

CARD DRAINED IN 1/2 THE BLANKING INTERVAL

8 LVDS OUTPUT BUSES
EACH BUS PASSES 16 BIT RESULTS
62.5 MHz PARALLEL RATE INTO LVDS SERIALIZERS;

EACH BUS OUTPUTS 32,768 RESULTS, AT 16 nsec EACH = 0.524288 msec

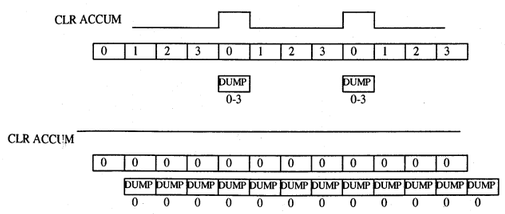


MAX OF TWO CORRELATOR CHIPS PER CHIP BUS IN ORDER TO SUPPORT THE HIGH SPEED READOUT OPTION

SELF RESULTS ARE ACCUMULATED IN THE LTA IN MULTIPLES OF 1 MSEC

CROSS RESULTS ARE ACCUMULATED IN THE LTA IN MULTIPLES OF 16 MSEC

SELF RESULTS ARE DUMPED IN 1 MSEC
CROSS RESULTS ARE DUMPED IN 16 MSEC
NO MATTER WHAT THE LTA ACCUMULATION TIME IS SET FOR



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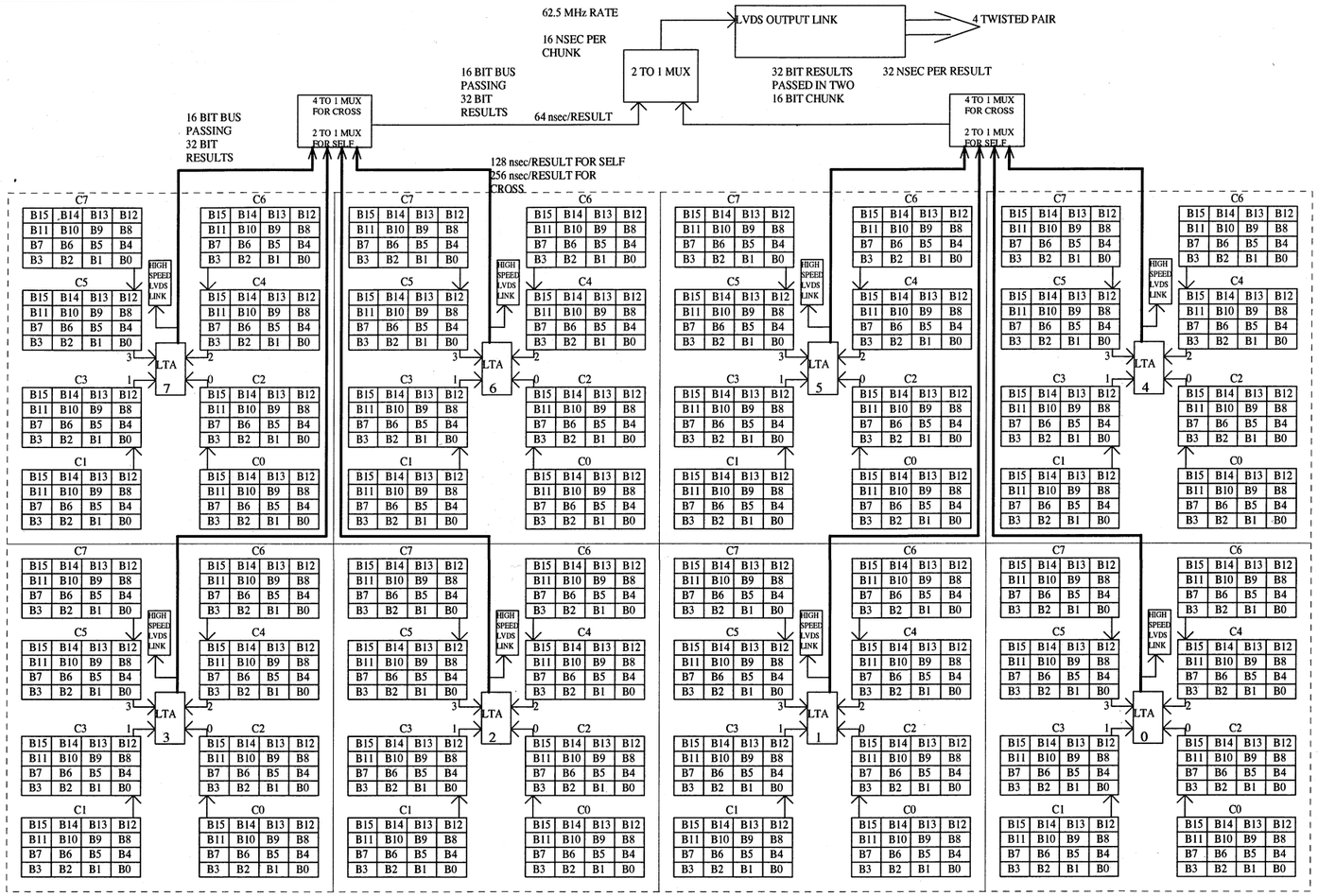
Date: Friday, May 28, 1999	Sheet 1 of 1	



CORRELATOR CARD (INCLUDES LTA)

NO SELFS ON CARD

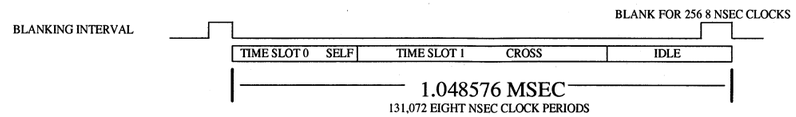
"REPRESENTATIVE" READOUT SEQUENCE FOR ONE COLUMN PAIR

1 MSEC NR	TIME SLOT	LTA 0 CHIP BUS 0 CHIP	LTA 0 CHIP BUS 0 BSLINES	LTA 0 CHIP BUS 1 CHIP	LTA 0 CHIP BUS 1 BSLINES	LTA 0 CHIP BUS 2 CHIP	LTA 0 CHIP BUS 2 BSLINES	LTA 0 CHIP BUS 3 CHIP	LTA 0 CHIP BUS 3 BSLINES	LTA 4 CHIP BUS 0 CHIP	LTA 4 CHIP BUS 0 BSLINES	LTA 4 CHIP BUS 1 CHIP	LTA 4 CHIP BUS 1 BSLINES	LTA 4 CHIP BUS 2 CHIP	LTA 4 CHIP BUS 2 BSLINES	LTA 4 CHIP BUS 3 CHIP	LTA 4 CHIP BUS 3 BSLINES
0	SLOT0																
1	SLOT0																
2	SLOT0																
3	SLOT0	NO RESULTS READ FROM THESE CHIP BUSES DURING TIME SLOT 0								NO RESULTS READ FROM THESE CHIP BUSES DURING TIME SLOT 0							
4	SLOT0																
5	SLOT0																
6	SLOT0																
7	SLOT0																
8	SLOT0																
9	SLOT0																
10	SLOT0																
11	SLOT0																
12	SLOT0																
13	SLOT0																
14	SLOT0																
15	SLOT0																

TIME SLOT 0 = SELF

TIME SLOT 1 = CROSS

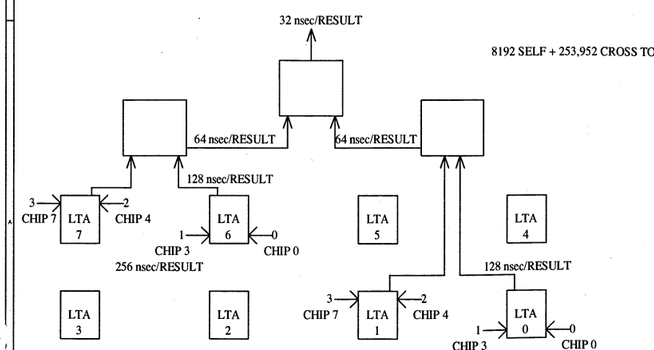
1 MSEC NR	TIME SLOT	CHIP BUS 0 CHIP	CHIP BUS 0 BSLINES	CHIP BUS 1 CHIP	CHIP BUS 1 BSLINES	CHIP BUS 2 CHIP	CHIP BUS 2 BSLINES	CHIP BUS 3 CHIP	CHIP BUS 3 BSLINES	CHIP BUS 0 CHIP	CHIP BUS 0 BSLINES	CHIP BUS 1 CHIP	CHIP BUS 1 BSLINES	CHIP BUS 2 CHIP	CHIP BUS 2 BSLINES	CHIP BUS 3 CHIP	CHIP BUS 3 BSLINES
0	SLOT1	2	0,1	1	0,1	6	0,1	5	0,1	2	0,1	1	0,1	6	0,1	5	0,1
1	SLOT1	2	2,3	1	2,3	6	2,3	5	2,3	2	2,3	1	2,3	6	2,3	5	2,3
2	SLOT1	2	4,5	1	4,5	6	4,5	5	4,5	2	4,5	1	4,5	6	4,5	5	4,5
3	SLOT1	2	6,7	1	6,7	6	6,7	5	6,7	2	6,7	1	6,7	6	6,7	5	6,7
4	SLOT1	2	8,9	1	8,9	6	8,9	5	8,9	2	8,9	1	8,9	6	8,9	5	8,9
5	SLOT1	2	10,11	1	10,11	6	10,11	5	10,11	2	10,11	1	10,11	6	10,11	5	10,11
6	SLOT1	2	12,13	1	12,13	6	12,13	5	12,13	2	12,13	1	12,13	6	12,13	5	12,13
7	SLOT1	2	14,15	1	14,15	6	14,15	5	14,15	2	14,15	1	14,15	6	14,15	5	14,15
8	SLOT1	0	1,2	3	1,2	4	1,2	7	1,2	0	1,2	3	1,2	4	1,2	7	1,2
9	SLOT1	0	3,4	3	3,4	4	3,4	7	3,4	0	3,4	3	3,4	4	3,4	7	3,4
10	SLOT1	0	6,7	3	6,7	4	6,7	7	6,7	0	6,7	3	6,7	4	6,7	7	6,7
11	SLOT1	0	8,9	3	8,9	4	8,9	7	8,9	0	8,9	3	8,9	4	8,9	7	8,9
12	SLOT1	0	11,12	3	11,12	4	11,12	7	11,12	0	11,12	3	11,12	4	11,12	7	11,12
13	SLOT1	0	13,14	3	13,14	4	13,14	7	13,14	0	13,14	3	13,14	4	13,14	7	13,14
14	SLOT1	0	0,5	3	0,5	4	0,5	7	0,5	0	0,5	3	0,5	4	0,5	7	0,5
15	SLOT1	0	10,15	3	10,15	4	10,15	7	10,15	0	10,15	3	10,15	4	10,15	7	10,15



LOW SPEED MODE: 1 MSEC MIN SELF 16 MSEC MIN CROSS

TIME SLOT 0 TOTAL TIME = 0.262144 msec (1/4 OF THE BLANKING INTERVAL)

32 SELF BASELINES, 8192 SELF RESULTS TOTAL
READ OUT EACH BLANKING INTERVAL



8192 SELF + 253,952 CROSS TOTAL PER CARD

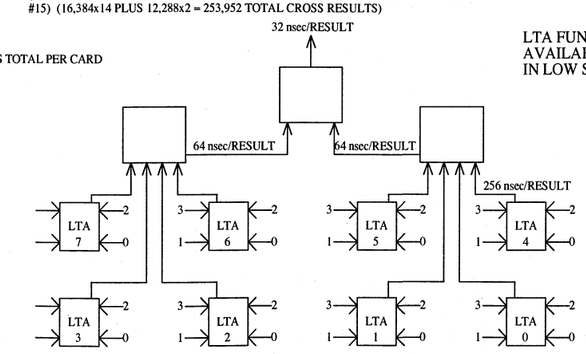
EACH 1 MSEC INTERVAL, ONLY ONE CORRELATOR CHIP PER CHIP BUS IS ACCESSED, 4 BASELINES PER ACCESSED CHIP, 256 RESULTS PER BASELINE

1024 SELFS IN ONE CHIP TIMES 256 nsec EACH EQUALS 262.144 usec EACH 1.048576 msec

256 nsec/RESULT CHIP ACCESS

TIME SLOT 1 TOTAL TIME = 0.524288 msec (1/2 OF THE BLANKING INTERVAL)

64 CROSS BASELINES, 16,384 CROSS RESULTS TOTAL READ OUT EACH BLANKING INTERVAL (TRUE FOR 1 MSEC # 0 - 13; ONLY 48 CROSS BASELINES, 12,288 CROSS RESULTS IN #14 AND #15) (16,384x14 PLUS 12,288x2 = 253,952 TOTAL CROSS RESULTS)



EACH 1 MSEC INTERVAL, ONLY ONE CORRELATOR CHIP PER CHIP BUS IS ACCESSED, 2 BASELINES PER CHIP READ OUT, 256 RESULTS PER BASELINE, 512 RESULTS TIMES 1.024 usec = 524.288 usec

1024 nsec/RESULT CHIP ACCESS

LTA FUNCTION ONLY AVAILABLE IN LOW SPEED MODE

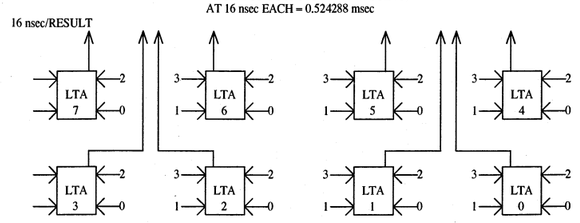
HIGH SPEED MODE: 1MSEC FOR SELF AND CROSS

CARD DRAINED IN 1/2 THE BLANKING INTERVAL

8 LVDS OUTPUT BUSES
EACH BUS PASSES 16 BIT RESULTS
62.5 MHz PARALLEL RATE INTO LVDS SERIALIZERS;

EACH BUS OUTPUTS 32,768 RESULTS, AT 16 nsec EACH = 0.524288 msec

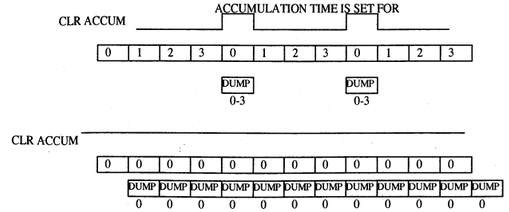
MAX OF TWO CORRELATOR CHIPS PER CHIP BUS IN ORDER TO SUPPORT THE HIGH SPEED READOUT OPTION



SELF RESULTS ARE ACCUMULATED IN THE LTA IN MULTIPLES OF 1 MSEC

CROSS RESULTS ARE ACCUMULATED IN THE LTA IN MULTIPLES OF 16 MSEC

SELF RESULTS ARE DUMPED IN 1 MSEC
CROSS RESULTS ARE DUMPED IN 16 MSEC
NO MATTER WHAT THE LTA ACCUMULATION TIME IS SET FOR



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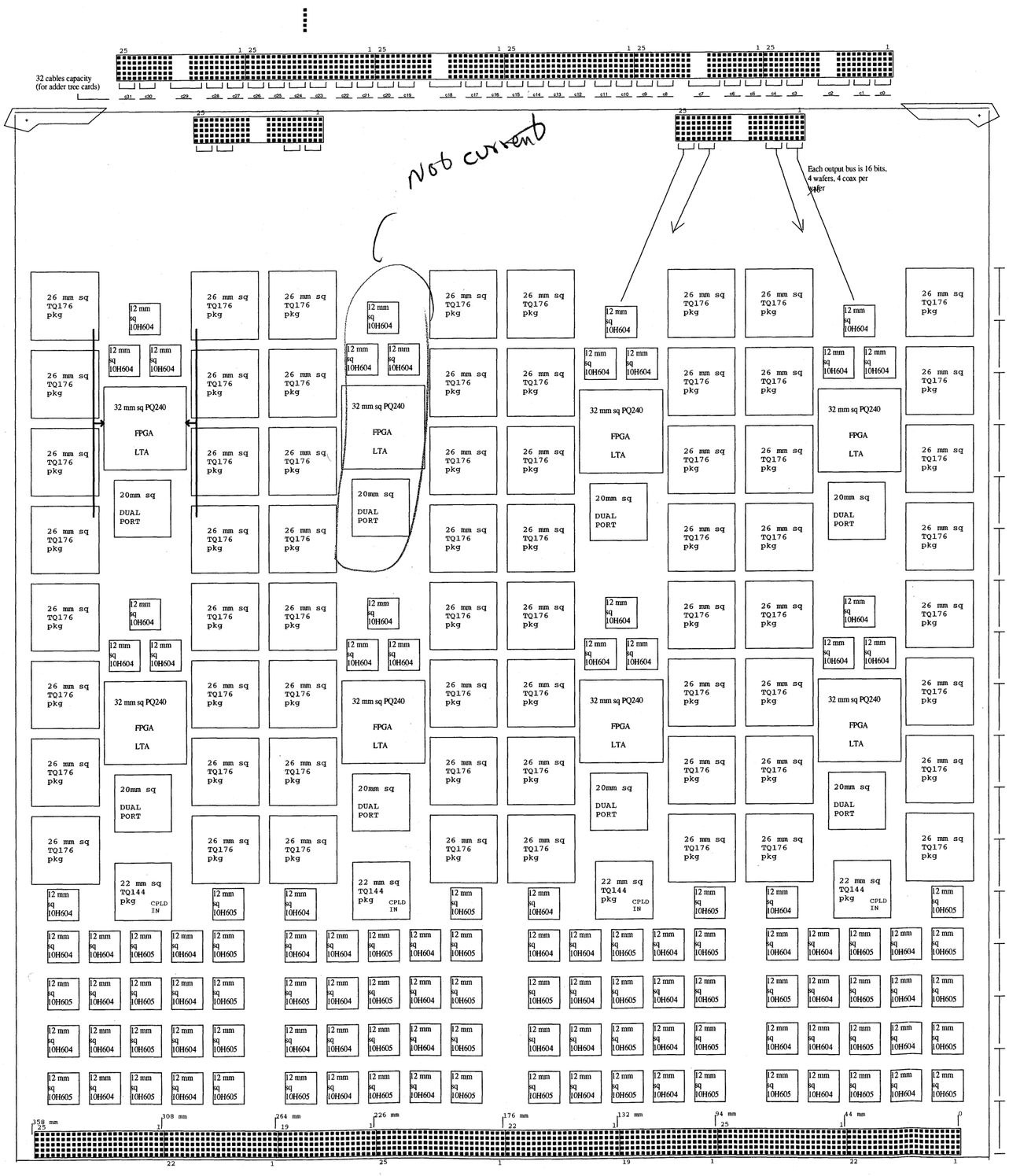
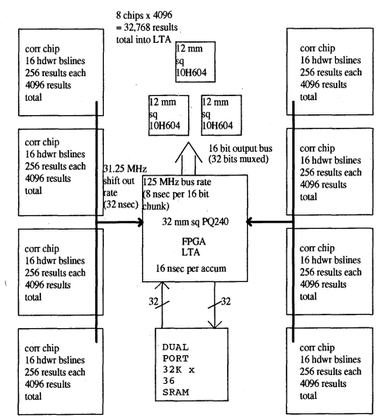
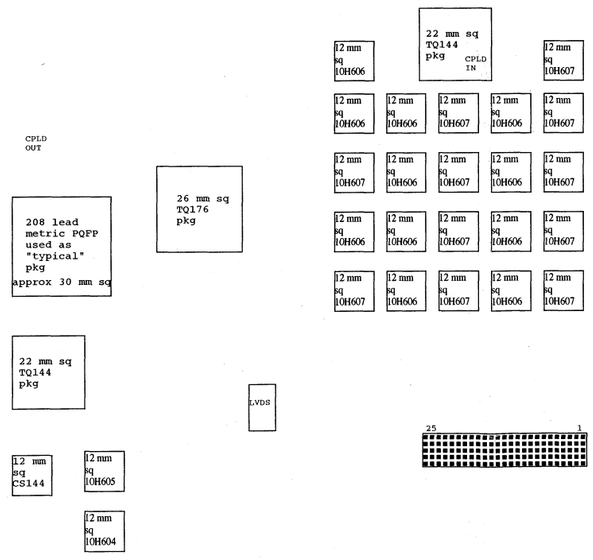




Corr chip may be more than 144 pins???

Joe estimates approx 164 pins at present



There are 2 bits from each of 2 memory cards for each of 4 ants, and both the MAIN and AUX sets of ants = 2x2x4x2=32 signals per column, 64 signals for a pair of columns

64 divided by 6 = 11 pairs of HEX rcvr/driver IC packages for a pair of columns

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