

MMA Correlator Chip Consulting Proposal

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1 Summary

The MMA correlator chip is obviously a major component of the MMA signal processing system, with the cost of the design and manufacture of the chip being the largest contributor to the system budget. The power consumption of the chip is also a major concern due to the difficulty in cooling the system at the high altitude of the MMA site. The proposed MMA correlator chip will be the largest single chip correlator ever implemented. It is estimated that the chip will have 3.5-4.0 times the number of transistors as the 1024 lag GBT correlator chip. [1, 2]

All of the above factors, as well as the required 125 MHz clock rate, make the successful design of the MMA chip a non-trivial task. Although the feature sizes of current CMOS process technologies make it feasible to consider a 4 million transistor chip, careful consideration of logic, circuit and layout design are required to actually make the design both possible and cost effective. Modern CMOS processes also bring with them an inherent reduction in power dissipation due to lowered supply voltages and smaller internal parasitic capacitances. However, it is possible to negate these reductions through poor circuit or layout design practices.

The equivalent gate count of the GBT correlator chip was about 850,000 gates. The estimated gate count of the MMA correlator chip is approximately 3.5 million equivalent gates. It is unlikely that a cell based design approach would provide an affordable die, especially if the design is synthesized from a high level design language, such as Verilog or VHDL, with no attention given to physical layout considerations. Due to the small die size/low cost, low power and high performance requirements of the MMA correlator chip, a custom approach to the chip design is proposed here.

2 Proposed Design Methodology

The die size, packing density, high performance and low power requirements of the MMA correlator chip require a structured custom design methodology in which the logic and circuit design allow for the use of individual transistors rather than pre-existing circuit modules taken from a library. The ability to design at the transistor level provides the flexibility required to minimize the transistor count while meeting the performance specifications of the chip. In addition, the ability to design at the transistor level allows for circuit elements to be created which do not consume excess power. This approach also provides the most flexibility in designing for layout considerations such as routing and module aspect ratios. The structured part of this methodology is in the hierarchical creation of circuit and layout

modules which provide regularity in the design. This structured modularity brings with it the reduction in complexity necessary to make a design of this magnitude possible. A structured custom approach does, however, require extensive VLSI logic, circuit and layout design experience to be successful.

3 Previous Correlator Design Experience

Dr. John Canaris has 17 years of VLSI design experience and is the designer of 3 correlator chips. Two of these chips have become standards for radio observatories world wide.

3.1 JPL Correlator

The JPL correlator was designed at about the same time as the famous Bos chip. This correlator, designed for a space borne spectrometer is a 32 lag/25 MHz device, which consumes less than 10mW/lag, at 5 volts. It implements the same 2 bit, 4 level multiplier/accumulator as the proposed MMA correlator. This processor was delivered to JPL and is working in a balloon borne digital spectrometer system. [3]

3.2 ESTAR Correlator

A feasibility study undertaken for the ESTAR correlator chip showed that the integration of large numbers of correlator lags was possible. The proposed ESTAR chip would have integrated 1600 independent correlators operating at a sample clock rate of 60 MHz. This study led to the design of the 1024 lag GBT correlator. [4]

3.3 1024 Lag Correlator

The 1024 lag correlator chip, also known as the GBT chip, is a high speed device which implements many of the features required by the MMA chip, including the additional registers necessary for over-sampling. This device is installed, or is being installed in correlator systems world wide, including the GBT, Arecibo and the Max Plank Institute for Radio Astronomy. [5]

3.4 MIT-Haystack Correlator

This is an extremely complex device which integrates eight 64 lag correlator sections with the necessary multiplexing and configuration registers to implement the functionality required by the MIT-Haystack MkIV correlator. In addition, it contains 8 arithmetic/control units for phase rotation and data manipulation necessary for processing data read from tape. The MMA correlator will use a subset of the internal multiplexing implemented in the Haystack chip. This device is also being installed world wide, most recently in the JIVE correlator located in the Netherlands.

3.5 Consulting

In 1995 Dr. Canaris had a contract with Aerojet Corporation to attend design reviews for a 1024 lag correlator. This contract paid \$100.00/hour + reimbursable expenses.

4 Proposed Work

The design of the MMA correlator chip can be broken down into 5 phases, three of which are covered by the proposed work. Additionally, these three tasks will be broken down into 2 separate contracts.

1. Logic design. During this phase all logic elements required to meet the functional specification of the chip are designed and simulated.
2. Circuit design. During this phase all transistor sizes are assigned and speed paths are simulated to ensure that the timing specification will be met. In addition critical elements, such as flip-flops, are simulated to ensure correct functionality. This phase requires SPICE models from the target foundry.
3. Layout design. All physical layout design required to create the mask set needed for fabrication is performed during this phase. Design rule checks and layout to schematic checks are performed. This phase requires layout design rules from the targeted foundry.
4. Manufacture and testing of prototype devices. Mask sets are generated and wafers are processed during this phase. After wafer fabrication devices are packaged and tested for correct operation.
5. Manufacture and testing of production devices. Manufacture, packaging and testing of final production devices occurs at this stage.

The work proposed here covers the first 3 items, which would leave the design ready for manufacturing prototypes. The proposed work will be completed in two phases, under separate contracts. The first phase will cover logic and circuit design. The second phase will cover the physical layout design portion of the project. The schedule dates given here are dependent upon the start date of the contract.

5 Schedule and Major Milestones

Logic Design	320 hours	completed by 12/31/1999
Circuit Design	160 hours	completed by 2/28/2000
Layout Design	960 hours	completed by 12/31/2000
Total	1440 hours	

6 Deliverables

1. Phase One: Complete netlist of the chip design in the BOLT language This netlist will contain timing information and device sizes so that it is ready for layout to begin in Phase 2.
2. Phase Two: Complete electronic data base of physical design ready for transfer to the targeted silicon foundry. Updated netlist which reflects any changes made during Phase 1 of the project.

7 Rates

Wages	\$88.00/hour
Fringe @ 24%	\$21.10/hour
Overhead @ 10%	\$10.90/hour
Total	\$120.00/hour

8 Targeted Technology and Foundry

Due to rapid change in CMOS manufacturing technologies it is desirable to postpone selection of the process technology and foundry as long as possible. This will provide the benefit of the greater packing densities and lower supply voltages which come with new generations of processes. At this time the most likely candidate is a $0.35\mu\text{m}$ process available at American Microsystems, Inc.

The final selection of a process/foundry must be carefully coordinated with the chip delivery schedule and budget. With a custom design methodology the physical layout is somewhat more dependent on the targeted process design rules than is a library based methodology. Once layout commences it could, in the worst case, require a complete rework of the layout design as well as redoing a portion of the circuit design. At some point it is best to choose a technology and stick with it, rather than holding out for something better.

Using a structured approach to the custom design reduces the amount of rework which might occur, as only a fraction of the layout is actually unique. Most of the layout consists of instances of the basic modules.

9 Accelerated Schedule/Schedule Slip Contingency Plan

If it is desired to accelerate the schedule, or if unforeseen difficulties arise which cause the schedule to be jeopardized, Dr. Canaris personally knows many excellent engineers and layout designers he could call on for assistance. If additional resources are required the work would be performed under Dr. Canaris' supervision and not as an "over the wall" subcontract.

10 Conflict of Interest

There are no prohibitions in Dr. Canaris' current employment agreement which preclude him from consulting on a project of this nature.

11 Resources required from NRAO

Dr. Canaris would require the loan of a computer system, either a Hewlett-Packard workstation or a state-of-the-art PC. If the system is a PC it must be capable of running the Linux operating system as well as Microsoft Windows. The layout portion of the project will require the purchase of a software package costing approximately \$15,000. Additionally, a local connection to the Internet would facilitate the transfer of information between Dr. Canaris and NRAO. Assistance from NRAO in the development of logic simulation test cases, produced from real observation data, would increase the chances of first pass success.

References

- [1] A. R. Thompson, et. al., "MMA Memo 142: MMA Systems Working Group Report", Report of the Systems Working Group of the MMA Development Consortium, September 1995.
- [2] R. Escoffier, "MMA Memo 166: The MMA Correlator", April 1997.
- [3] J. Canaris and S. Whitaker, "A Low Power CMOS Correlator ", First Great Lakes Symposium on VLSI, Kalamazoo, Michigan, March 1991, pp. 122-127.
- [4] J. Canaris, "VLSI Processor Architecture for a Synthetic Aperture Radio Antenna", Study Phase Final Report, Contract G5-NAG-5-1635, Goddard Space Flight Center, March 1992.
- [5] J. Canaris, "NASA SERC Digital Correlator Projects", Proceedings of the 4th NASA Symposium on VLSI Design, Moscow, Idaho, October 1992, pp. 4.2.1-4.2.3.