Correlator group meeting

Ray: can easily make memory cycle exactly 1 msec. Just throw away a tiny fraction of memory.
Result of investigation: can't do delays as previously conceived—have to do it elsewhere.
Part of delay was at digitizer, part at correlator—now have moved all delays to antenna.
Greenberg will investigate commercial chip sources.
We will take no action on the digitizer until after URSI.

→ All the stuff (24 cards) must go on one backplane—may not fit even in a 30-inch rack—system question.

Need one quadrant to do all IF's for 1/4 of antennas.
For 64-antenna system, one quadrant = 8 racks

Review process: each board will be reviewed in detail by one other engineer

→ Present design with 1-msec dumps does not recirculate—is this important?

Can probably accomodate an 8K chip with no extra cost or dump time implications. Broadwell still looking at details.

→ Test interferometer: go first to digital, or start analog & move digitizer later?