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founded 9 yrs ago
design for Phillips

INNOTECH SYSTEMS INC.

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Joe Greenberg
National Radio Astronomy Observatory (NRAO)
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Charlottesville,VA 22903
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July 28, 1999

Dear Mr. Greenburg:

This quote is for engineering services and production units for the ALMA 4096 Lag Correlator ASIC. Included in this proposal are ASIC development, test plan, engineering service charges, production pricing and schedule. A 0.35um or 0.25um process is recommended and quoted herein. Pricing currently reflects a 0.35um process.

We've done some preliminary SPICe simulations to tie down the power dissipation issue (see "Power" note below). Please let me know if the assumptions about your control of the system ambient conditions are acceptable. Likewise for the delivery schedule.

Should *Innotech Systems, Inc.* fail to properly execute any of these design steps, that work will be corrected free of any additional charge. Additional fees will be required for any circuit or specification changes after Design Start.

All billings are net 30 days. This is a budgetary quote and is subject to engineering availability. Thank you for this opportunity to participate in the ALMA project.

Sincerely,

Louis J. Morales

STATEMENT OF WORK

DESIGN STEP	RESPONSIBILITY	CRITICAL PATH +
DESIGN START Agreement on specification, design approach, and schedule. Initial design review. Work begins.	Customer/ISI	1 week
CIRCUIT DESIGN Design logic from existing schemaitcs and specification. Custom multiply/add/accumuate block is designed. Add test logic. Begin initial simulations.	ISI	3 weeks
ASIC CIRCUIT SIMULATION Circuit is simulated to verify functionality. Logic simulations are done. Begin floorplanning for layout.	ISI	3 weeks
INITIAL SIGN-OFF REVIEW Pre-route ASIC design review. Customer approves all work done to date.	Customer/ISI	½ week
ASIC LAYOUT Cells are completed. ASIC routing is done. Actual capacitances are extracted and used for final SPICE simulations. Layout is checked against design rules and schematic connectivity using CAE software.	ISI	7 weeks
POST-LAYOUT SIMULATION Circuit timing is verified using actual capacitance loading from layout results. Circuit improvements are made. Final DRC and LVS checks are completed.	ISI	1 week
FINAL SIGN-OFF REVIEW Final design review. Customer approves all design work prior to ASIC prototype build. ASIC prototypes are started.	Joint	½ week
TEST DEVELOPMENT Simulation vectors are converted to test program. Test hardware is implemented and checked.	ISI	-
PROTOTYPES Delivery of 10 commercial ASIC prototypes.	ISI	7 weeks

Description of Solution:

Design Methodology: Complete turnkey ASIC development for ALMA 4096 Lag Correlator ASIC, based on existing schematics and specification.

NRAO's Responsibilities: Finalize spec, review and sign-off approval of simulation results, test plan approval, and prototype approval.

ISI's Responsibilities: Circuit development, schematic entry, circuit simulation, ASIC design, development, test plan, test generation, masks, prototype and production foundry.

Notes:

8192 Lag Correlator ASIC would require 0.25um CMOS. This would be OK, but the you will need a somewhat exotic package (<6°C/W for heat dissipation) and the die size will be getting a bit large. I bleive the price differential will be 2-3X for piece price (more expensive process/package & larger die size) and +$140K for non-recurring lot charges. If price is not the main issue, we can re-visit this option.

Card clock delays can probably be managed with a single clock generator/PLL per board and judicious routing of the clock and data paths. On the ASIC plan on about 3ns clock to output delay and 0ns hold time.

Power is a serious issue. We will customize the layout for the multiplier, accumuator, and adder to minimize power at 125MHz operation. Also, I believe you will need to control the ambient temperature to below 40°C at about 1000CFM air flow, although we may be able to do better on power dissipation with further work on the circuit/layout.

Test pins and partial scan logic will be added to access the internal logic for good test coverage within a reasonable number of tester cycles.

Questions:

Ambient temperature range required?

Over what period of time do you want to take delivery of parts? I think you will want a full board's worth of chips ASAP after prototype approval, with the remainder produced after initial board debug.

How many pins would be needed for the 8192 Lag Correlator ASIC option?

ASIC Overview:

Circuit Description: ALMA 4096 Lag Correlator ASIC
Process: 0.35um or 0.25um CMOS
Package: 240 MQFP
Special requirements: none

Engineering Services Pricing:

Item	Description	Unit Price	Qty	Total
1	Design Start			$52600.
2	Initial Sign-off Review			$26300.
3	Final Sign-off Review			$107500.
4	Test development			$7100.
5	Prototype Approval (within 45 days)			$26300.
		TOTAL		$212700.

OPTIONAL:

Item	Description	Unit Price	Qty	Total
7	Additional engineering time	$95/hour		

Production Pricing:

ALMA 4096 Lag Correlator ASIC in 240 MQFP:
39322 units $45/unit one time buy in 2 shipments (scheduled within 8 mo)
delivery 16 weeks ARO

80 die/wafer in .35μm

$65 each for .25μm – depends on delivery schedule