8-2-99

Date:	Mon, 02 Aug 1999 14:45:54 -0400
From:	Joe Greenberg <jgreenbe@NRAO.EDU>
To:	"Louis J. Morales" <loum@innotechsystems.com>, rescoffi@NRAO.EDU, cbroadwe@NRAO.EDU, jwebber@NRAO.EDU
CC:	Joe Greenberg <jgreenbe@NRAO.EDU>
Subject:	Wednesday Conference Call

Louis called me today. I have set up a conference call for 9AM Wed, in the main conference room, to discuss ASIC design issues. We will call him at 617 695 2700.

Louis also said that the Prototype development/mask/product cost was about 100K of the 213K quote. That was for 10 prototypes in .35 micron technology.

+50K to 100K for .25 μm

prototype lot ~800 good parts

"Louis J. Morales" wrote:

>
> Joe,
>

- Regarding the power numbers I gave you. I agree that 0.25um may be a better choice for 2001. At this point, 0.2um or 0.18um processes will be hard to get scheduled and are much more expensive for masks and wafers. This issue can be revisited when you get close to producing the prototype lot.

>

- Here are answers to your questions:

>

- >Does the cost quoted include the prototype masks and production?
- Yes.
- Prototype and production masks should be the same, assuming we all do our
- parts correctly. If there are changes to the design after the prototype lot, another mask and prototype lot charge will be incurred.

>

- >When would the additional $95/hr charge kick in?
- If the design specs don't change after Design Start, additional engineering won't
- be needed. You may want additional engineering work before design start to nail down power issues in various processes, for example.

>

- >We would like to schedule a conference call to discuss issues.
- I'll be in the office through Thursday of this week except for Tuesday morning.
- I'll give you a call this afternoon.

>
> >
>

- At 10:10 AM 7/30/99 -0400, Joe Greenberg wrote:
- >Some immediate observations are:

> >

- >The 10 Watts for .35 micron is definitely unacceptable.

> >

- >The 5 Watts for .25 micron is higher than we would like. We are
- >shooting for 2 watts, due to the additional cooling constraints of
- >placing the chip at high altitude.

> >

- >We would also like to investigate .18 micron, since we don't need
- >prototypes until 7/2001.

> >

- >In response to your questions:

> >

- >Ambient temperature range is sufficient. We would be using cooled
- >forced air.
- >We would like a full boards worth (64) for prototype evaluation. If
- >that is excessively expensive, we could take a smaller number first. We
- >would want production quantities in mid 2002.

> >

- >The 8192 lag option would have identical pinout to the 4096 lag option.
- >The only change is the 64 lag sub blocks changing to 128 lags.

> >

- >We have the questions:

> >

- >Does the cost quoted include the prototype masks and production?

> >

- >When would the additional $95/hr charge kick in?

> >

- >We would like to schedule a conference call to discuss issues.

> >

> >Thanks,

- >Joe

> >

- >"Louis J. Morales" wrote:

> >>

> >> Joe,

> >>

- >> We've reviewed your specs and schematics in detail and completed a
- >> budgetary quote for your review. Please look this over and let me know if
- >> you'd like to take this further.

> >>

> >>

> >> ----------

- >> Louis J. Morales
- >> Innotech Systems, Inc.
- >> loum@innotechsystems.com
- >> (617)695-2700
- >> (617)423-0466 Fax

> >

> >

ALMA U.S. Task and Resource planning

Filter: All Tasks

WBS (f)	Task	Start	Finish	Duration	Work
8	**Correlator**	**1998-06-01**	**2007-03-30**	**461w**	**484.59w**

Notes
The MMA correlator will accept multiple baseband analog signals from the IF system, digitize them, and calculate the cross-correlation functions on a pairwise basis.

8.1	**Specifications**	**1998-06-01**	**1998-11-13**	**24w**	**18w**

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	75%	18w	0w	1998-06-01	1998-11-13

Notes
The specifications are detailed in MMA Memo 166. They include a total of 16 GHz of signal from each antenna, a maximum bandwidth of 2 GHz per spectrum chunk, 2-bit 4-level quantization, 1024 spectral channels over a single 2 GHz bandwidth, and full polarization capability in various modes. These preliminary specifications will be further examined and revised as required during the design process.

8.1.1	**Capabilities**	**1998-06-01**	**1998-08-21**	**12w**	**0w**

Notes
The capabilities are outlined in MMA Memo 194. They include various combinations of total bandwidth, polarization capability, and spectral resolution. These items will be further examined and revised as required during the design process.

8.1.2	**Configurations**	**1998-08-24**	**1998-11-13**	**12w**	**0w**

Notes
Various configurations are given in MMA Memos 166 and 194. They include various combinations of total bandwidth, polarization capability, and spectral resolution. These items will be further examined and revised as required during the design process.

8.2	**Test Correlator**	**1998-07-20**	**2000-03-31**	**89w**	**45w**

ID	Resource Name	Units	Work	Delay	Start	Finish
12	Correlator Programmer	15%	13w	0w	1998-07-20	2000-03-31
15	Engineer Correlator	9%	8w	0w	1998-07-20	2000-03-31
16	Technician Correlator	27%	24w	0w	1998-07-20	2000-03-31

Notes
The first MMA prototype antennas will be delivered to the test site before the prototype MMA correlator is ready. In order to evaluate antenna performance, a test correlator capable of producing both auto- and cross-correlations is required. Such a correlator will be built and tested using the designs of the GBT spectrometer which has already been completed (similar systems have been built for MPIfR, UMass, and the NRAO 12-m antenna). The work will consist of fabricating and testing circuit boards, an equipment rack, and the firmware needed for MMA test modes, followed by delivery to the test site for integration.

8.2.1	**Specifications**	**1998-07-20**	**1998-08-14**	**4w**	**0w**

Notes
The test correlator will be capable of producing either auto-correlation spectra (one antenna) or cross-correlation spectra (two antennas). Its working modes will be adaptations of the modes of the GBT design. These specifications will be determined and documented.

8.2.2	**Adapt GBT design**	**1998-08-17**	**1998-09-11**	**4w**	**0w**

Notes
The limitations of the GBT spectrometer design for cross-correlation impose certain restrictions on operating modes, including a slight loss of SNR if both auto-correlation and cross-correlation spectra are to be calculated simultaneously. These details will be determined and documented.

8.2.3	**Order parts**	**1998-09-14**	**1998-11-06**	**8w**	**0w**

Notes
Sufficient "Quaint" chips are available for the test correlator. The list of parts for the circuit boards, rack, cages, interconnects, etc. will be determined and the parts procured or fabricated.

8.2.4	**Assemble**	**1999-04-01**	**1999-08-18**	**20w**	**0w**

Notes
The various parts and subassemblies will be fabricated in-house and by outside contractors.

8.2.5	**Test**	**1999-08-19**	**2000-01-05**	**20w**	**0w**

Notes
The correlator boards will be tested individually in specialized test fixtures. Firmware defining the operating modes and software to operate the system will be written. The system will be tested in the laboratory prior to delivery to the test site.

8.2.6	***Deliver Test Correlator to VLA site***	***2000-03-31***	***2000-03-31***	***0d***	***0w***

8.3	**Preliminary Design**	**1998-09-15**	**1999-09-01**	**50.4w**	**40.54w**

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	57%	28.49w	0w	1998-09-15	1999-09-01
16	Technician Correlator	24%	12.05w	0w	1998-09-15	1999-09-01

Notes
The MMA correlator will consist of equipment racks, power supplies, interconnecting cables, samplers, a control computer, and a number of different printed circuit cards performing the various functions of sample sorting, cross-correlation, accumulation, post-processing, and control. During 1998-99, all design work performed under this item will consist of computer designs and simulations of the various elements of the correlator. During 2000, some parts of the system including test fixtures and prototype cards will be fabricated and tested. Some firmware will be written and tested. Fabrication of prototype correlator cards will occur in 2001, when the first correlator chips become available.

WBS (f)	Task	Start	Finish	Duration	Work
8.3.1	**Evaluate overall architecture**	1998-09-15	1999-03-01	24w	0w

Notes

The present conceptual design assigns a particular set of time slices of the data from all antennas for a particular IF band to a single correlator board. Other boards receive similar data from interleaved time slices or other IF bands. The assignment of data is performed by a memory board which may also serve as a delay element. After cross-correlation, the results from many correlator boards are combined in a long term accumulator board. The data are then passed to the next stage of processing, which may be a general purpose computer or a dedicated array of digital signal processing chips. The timing of the whole process is set by control boards which work under a controlling computer. The implications of this architecture will be further examined and changes to the conceptual design will be made when necessary.

8.3.2	**Define board functionality**	1999-03-02	1999-03-29	4w	0w

Notes

The present conceptual design assigns different tasks to specific modules. These assignments will be examined in detail and changed as required to reach a realizable design.

8.3.3	**Straw man system layout**	1999-03-30	1999-05-31	9w	0w

Notes

The layout of the correlator includes the questions of which modules are mounted where, how they are interconnected for data and control flow, and how they are powered. This in turn defines how the racks must be arranged. These questions will be examined in sufficient detail to yield a realizable design.

8.3.4	**Evaluate thermal and power characteristics**	1999-06-01	1999-08-02	9w	0w

Notes

Once the board functionality and preliminary layout are done, it will be possible to determine the power consumption, the location of heat generation, and the power requirements. An analysis will be performed to verify that the preliminary design is possible to build without significant heat dissipation problems in the low atmospheric pressure environment of the high site.

8.3.5	***PDR: Correlator***	*1999-09-01*	*1999-09-01*	*0d*	*0w*
8.4	**Sampler**	1999-04-12	2001-07-06	117w	13.27w

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	11%	13.27w	0w	1999-04-12	2001-07-06

Notes

The sampler is a high performance analog-to-digital converter. There will be 8 IF signals from each antenna, each of 2 GHz maximum bandwidth, so 8 samplers will be required for each antenna.

8.4.1	**Specifications**	1999-04-12	1999-09-24	24w	0w

Notes

The preliminary specifications for the sampler include operation with a 4 GHz clock rate and an output data stream demultiplexed into 32 channels of data at a clock rate of 125 GHz. Details of such specifications as input signal level, hysteresis, sampling level stability, sampling epoch jitter, and thermally induced drift will be determined and documented. The specifications for the sampler chip will also be determined.

8.4.2	**Circuit design**	1999-09-27	1999-12-24	13w	0w

Notes

A digital circuit which operates at 4 GHz clock rate requires special design considerations. The circuit, modeled on existing designs which work up to ~2 GHz, will be designed and evaluated in detail prior to fabrication.

8.4.3	**Chip design**	1999-12-27	2000-06-23	26w	0w

Notes

It is likely that a custom chip will be required to meet the sampler specifications and that it will require the use of gallium arsenide technology. The design will be performed by outside contractors working closely with the correlator design engineers.

8.4.4	**PC board layout**	1999-12-27	2000-03-24	13w	0w

Notes

The PC board which holds the samplers, demultiplexers, and supporting circuitry will be designed and laid out.

8.4.5	**Mechanical design**	2000-03-27	2000-04-21	4w	0w

Notes

The circuit boards will likely be mounted in RF-tight boxes, which in turn will be mounted in VLA-like modules of a design to be defined by the systems group. The details of the sampler module, which will probably handle two independent data streams simultaneously, will be determined.

8.4.6	**Chip fabrication**	2000-06-26	2000-09-22	13w	0w

Notes

The sampler chip will be fabricated by an outside contractor.

8.4.7	**PC board fabrication**	2000-04-24	2000-07-21	13w	0w

Notes

The PC boards will be fabricated and populated with sampler and supporting chips.

8.4.8	**Test fixture**	2000-06-26	2000-09-01	10w	0w

Notes

The sampler will require a test fixture which supplies an analog signal and permits examination of the output results. This fixture will be designed and fabricated.

8.4.8.1	**Design**	2000-06-26	2000-07-28	5w	0w
8.4.8.2	**Assemble**	2000-07-31	2000-09-01	5w	0w

WBS (f)	Task	Start	Finish	Duration	Work
8.4.9	**Prototype assembly**	2000-09-25	2000-10-20	4w	0w
	Notes: Prototype sampler modules (PC boards, boxes, modules) will be assembled.				
8.4.10	**Prototype test**	2000-10-23	2000-12-15	8w	0w
	Notes: The prototype modules will be tested with the test fixture. More detailed testing will involve use of the correlator itself as part of the test apparatus.				
8.4.11	**Design modifications**	2000-12-18	2001-02-09	8w	0w
	Notes: It is likely that, as a result of the design, fabrication, and test effort for the sampler, some design modifications will be found necessary. These will be implemented in a design revision as required.				
8.4.12	**Fabricate, assemble and test with design mods**	2001-02-12	2001-07-06	21w	0w
	Notes: After one round of testing and redesign, the revised version of the sampler will be built and the final design verified.				
8.5	**Finite Impulse Response Filter**	1998-07-03	2000-12-01	126.2w	7w
	ID 15 — Resource Name: Engineer Correlator — Units: 6% — Work: 7w — Delay: 0w — Start: 1998-07-03 — Finish: 2000-12-01				
	Notes: A digital FIR filter has been chosen for baseband filtering instead of a traditional analog filter approach. This filter will always work at a 4 GHz sample rate and provide any filter bandwidth required. This will reduce cost and greatly improve stability of the system by avoiding systematic errors which are always present in an analog system. In turn, this will decrease closure errors and improve the dynamic range and fidelity of images.				
8.5.1	**Target specifications**	1998-07-03	1998-11-19	20w	0w
	Notes: The detailed specifications for the performance required of the FIR filter will be determined and documented.				
8.5.2	**Computer simulation**	1998-07-03	1998-12-31	26w	0w
	Notes: The performance of the FIR filter will be simulated in detail and the results evaluated. Numerical simulation will permit evaluation of the number of taps required and the accuracy of the arithmetic operations needed to give good performance.				
8.5.3	**Implementation decision**	1998-12-04	1999-02-18	10.8w	0w
	Notes: The results of the computer simulations will be compared with an analysis of the cost and performance of an entirely analog filter system. The decision between the two will then be made. The decision to use the digital filter has been made.				
8.5.3.1	**Evaluate cost/performance of FIR filter**	1998-12-04	1998-12-17	2w	0w
8.5.3.2	**Evaluate cost/performance of analog filters**	1998-12-18	1998-12-31	2w	0w
8.5.3.3	***Decision: FIR Filter or Analog BBC***	*1999-02-18*	*1999-02-18*	*0d*	*0w*
	Notes: Division Heads Face-to-Face Meeting 1999-Feb-18 Attendees AOC: Brooks, Brundage, Glendenning, Stauffer CV: Brown, Simon, Sramek, Webber, White, Wootten Tuc: Emerson, Gordon, Radford Digital Filter Decision Webber and Emerson sent out the memo on their recommendation to use the digital filtering system. The DHs, sitting as a control board, agreed with their recommendation. The digital filter is now the MMA project baseline.				
8.5.4	**Circuit design**	1999-02-16	1999-04-12	8w	0w
	Notes: The circuit required to support an FIR chip will be designed.				
8.5.5	**Chip design**	1999-04-13	1999-07-12	13w	0w
	Notes: It may be possible to implement the FIR filter in an FPGA of modern design which has sufficient logic elements. This will be determined, and if it appears possible, then the firmware will be written for such an operation. If this approach appears unfeasible, then a custom chip design will be undertaken, using an outside contractor as for the correlator chip. 1999-Mar-22: It has been determined that the FIR filter can be implemented in an FPGA at the required processing rate and at reasonable cost. This saves the expense of a custom chip design and allows for much greater flexibility. The FPGA chip programming substitutes for designing a custom chip.				
8.5.6	**PC board layout**	1999-04-13	1999-05-10	4w	0w
	Notes: A simple PC board to hold the FIR chips and supporting elements will be designed.				
8.5.7	**Mechanical design**	1999-05-19	1999-06-01	2w	0w
	Notes: It will be decided how the FIR filter fits into the system (it must come after the sampler, which will always run at 4 GHz). The module to hold one or more filters will be designed.				

WBS (f)	Task	Start	Finish	Duration	Work
8.5.8	*CDR: Finite Impulse Response Filter*	*2000-02-28*	*2000-02-28*	*0d*	*0w*
8.5.10	**PC board fabrication**	**1999-07-12**	**1999-10-01**	**12w**	**0w**
	Notes The PC board will be fabricated.				
8.5.11	**Test fixture**	**1999-06-02**	**1999-10-01**	**17.6w**	**0w**
	Notes The FIR filter will require a test fixture which supplies digital test signals and permits examination of the output results. It may be made compatible with the output of a sampler module. This fixture will be designed and fabricated.				
8.5.11.1	**Design**	**1999-06-02**	**1999-06-29**	**4w**	**0w**
8.5.11.2	**Assemble**	**1999-09-06**	**1999-10-01**	**4w**	**0w**
8.5.12	**Prototype assembly**	**1999-11-04**	**1999-12-01**	**4w**	**0w**
	Notes A complete FIR chassis will be assembled and at least partially populated with FIR boards.				
8.5.13	**Prototype test**	**1999-12-22**	**2000-02-01**	**6w**	**0w**
	Notes The complete FIR chassis will be tested with simulated and sampled data.				
8.5.14	**Design modifications**	**2000-03-07**	**2000-05-01**	**8w**	**0w**
	Notes It is possible that, as a result of the design, fabrication, and test effort for the FIR filter, some design modifications will be found necessary. These will be implemented in a design revision as required.				
8.5.15	**Fabricate, assemble and test with design mods**	**2000-05-02**	**2000-08-21**	**16w**	**0w**
	Notes After one round of testing and redesign, the revised version of the FIR filter will be built and the final design verified.				
8.5.16	*Deliver FIR Filter for Test Interferometer*	*2000-12-01*	*2000-12-01*	*0d*	*0w*
8.6	**Custom Boards**	**1999-09-02**	**2002-01-11**	**123.4w**	**198.29w**
	Notes The correlator will require several custom PC boards similar to those in the GBT spectrometer.				
8.6.1	**Memory Board**	**1999-09-02**	**2000-08-02**	**48w**	**50w**

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	90%	43w	0w	1999-09-02	2000-08-02
16	Technician Correlator	15%	7w	0w	1999-09-02	2000-08-02

Notes
The memory board which accepts the demultiplexed output of the sampler will be designed to store and re-order samples for time-slice cross-correlation. This will involve design, analysis, and possibly simulation to a degree. The delay necessary for interferometer operation may be incorporated into this board. Prototypes and test fixtures will be built and tested.

8.6.1.1	**Circuit design**	**1999-09-02**	**1999-11-24**	**12w**	**0w**
8.6.1.2	**Circuit simulation**	**1999-11-25**	**1999-12-22**	**4w**	**0w**
8.6.1.3	**PC board layout**	**1999-12-23**	**2000-01-05**	**2w**	**0w**
8.6.1.4	**PC board fabrication**	**2000-01-06**	**2000-01-19**	**2w**	**0w**
8.6.1.5	**Test fixture**	**2000-01-06**	**2000-02-16**	**6w**	**0w**
8.6.1.5.1	**Design**	**2000-01-06**	**2000-01-19**	**2w**	**0w**
8.6.1.5.2	**Assemble**	**2000-01-20**	**2000-02-16**	**4w**	**0w**
8.6.1.6	**Prototype assembly**	**2000-01-20**	**2000-02-16**	**4w**	**0w**
8.6.1.7	**Write microcode**	**1999-12-23**	**2000-02-16**	**8w**	**0w**
8.6.1.8	**Prototype test**	**2000-02-17**	**2000-04-12**	**8w**	**0w**
8.6.1.9	**Design modifications**	**2000-04-13**	**2000-05-10**	**4w**	**0w**
8.6.1.10	**Fabricate, assemble & test with design mods**	**2000-05-11**	**2000-08-02**	**12w**	**0w**
8.6.2	**Correlator Board**	**1999-09-02**	**2002-01-11**	**123.4w**	**48.29w**

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	34%	41.52w	0w	1999-09-02	2002-01-11
16	Technician Correlator	5%	6.76w	0w	1999-09-02	2002-01-11

Notes
The correlator board which does the cross-correlation function calculation will be designed, analyzed, and possibly simulated to a degree. Prototypes and test

WBS (f)	Task	Start	Finish	Duration	Work
"Correlator Board" continued					
	Notes fixtures will be built and tested.				
8.6.2.1	Circuit design	1999-09-02	1999-11-24	12w	0w
8.6.2.2	Circuit simulation	1999-11-25	1999-12-22	4w	0w
8.6.2.3	PC board layout	1999-12-23	2000-01-05	2w	0w
8.6.2.4	PC board fabrication	2000-01-06	2000-01-19	2w	0w
8.6.2.5	Test fixture	2000-01-06	2000-02-16	6w	0w
8.6.2.5.1	Design	2000-01-06	2000-01-19	2w	0w
8.6.2.5.2	Assemble	2000-01-20	2000-02-16	4w	0w
8.6.2.6	Prototype assembly	2001-07-02	2001-07-27	4w	0w
8.6.2.7	Write microcode	1999-12-23	2000-02-16	8w	0w
8.6.2.8	Prototype test	2001-07-30	2001-09-21	8w	0w
8.6.2.9	Design modifications	2001-09-24	2001-10-19	4w	0w
8.6.2.10	Fabricate, assemble and test with design mods	2001-10-22	2002-01-11	12w	0w
8.6.3	Long-Term Accumulator Board	1999-09-02	2000-08-02	48w	50w
	ID Resource Name Units Work Delay Start Finish 15 Engineer Correlator 90% 43w 0w 1999-09-02 2000-08-02 16 Technician Correlator 15% 7w 0w 1999-09-02 2000-08-02				
	Notes The accumulator board which accepts the results of 32 correlator cards (each responsible for a single time-slice) will be designed, analyzed, and possibly simulated to a degree. Prototypes and test fixture will be built and tested.				
8.6.3.1	Circuit design	1999-09-02	1999-11-24	12w	0w
8.6.3.2	Circuit simulation	1999-11-25	1999-12-22	4w	0w
8.6.3.3	PC board layout	1999-12-23	2000-01-05	2w	0w
8.6.3.4	PC board fabrication	2000-01-06	2000-01-19	2w	0w
8.6.3.5	Test fixture	2000-01-06	2000-02-16	6w	0w
8.6.3.5.1	Design	2000-01-06	2000-01-19	2w	0w
8.6.3.5.2	Assemble	2000-01-20	2000-02-16	4w	0w
8.6.3.6	Prototype assembly	2000-01-20	2000-02-16	4w	0w
8.6.3.7	Write microcode	1999-12-23	2000-02-16	8w	0w
8.6.3.8	Prototype test	2000-02-17	2000-04-12	8w	0w
8.6.3.9	Design modifications	2000-04-13	2000-05-10	4w	0w
8.6.3.15	Fabricate, assemble & test with design mods	2000-05-11	2000-08-02	12w	0w
8.6.4	System Control Boards	1999-09-02	2000-08-02	48w	50w
	ID Resource Name Units Work Delay Start Finish 15 Engineer Correlator 90% 43w 0w 1999-09-02 2000-08-02 16 Technician Correlator 15% 7w 0w 1999-09-02 2000-08-02				
	Notes The timing, configuration, data flow, and other parameters will be controlled by system control boards which will be designed, analyzed, and possibly simulated to a degree. Prototypes and test fixture will be built and tested.				
8.6.4.1	Circuit design	1999-09-02	1999-11-24	12w	0w
8.6.4.2	Circuit simulation	1999-11-25	1999-12-22	4w	0w
8.6.4.3	PC board layout	1999-12-23	2000-01-05	2w	0w
8.6.4.4	PC board fabrication	2000-01-06	2000-01-19	2w	0w
8.6.4.5	Test fixture	2000-01-06	2000-02-16	6w	0w
8.6.4.5.1	Design	2000-01-06	2000-01-19	2w	0w
8.6.4.5.2	Assemble	2000-01-20	2000-02-16	4w	0w
8.6.4.6	Prototype assembly	2000-01-20	2000-02-16	4w	0w

WBS (f)	Task	Start	Finish	Duration	Work
8.6.4.7	**Write microcode**	1999-12-23	2000-02-16	8w	0w
8.6.4.8	**Prototype test**	2000-02-17	2000-04-12	8w	0w
8.6.4.9	**Design modifications**	2000-04-13	2000-05-10	4w	0w
8.6.4.10	**Fabricate, assemble & test with design mods**	2000-05-11	2000-08-02	12w	0w
8.7	**Correlator Chip**	1999-01-04	2002-07-05	183w	43w

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	24%	43w	0w	1999-01-04	2002-07-05

Notes

The MMA correlator will require a new correlator chip incorporating 4096 cross-multipliers and accumulators plus the internal switching and control circuitry needed by the correlator design. The work performed under this item in 1999 and 2000 will consist of computer design and simulation of the correlator chip. Fabrication of prototypes will occur in 2001.

8.7.1	**Specifications**	1999-01-04	1999-02-26	8w	0w

Notes

The detailed correlator chip specifications will be determined and documented.

8.7.2	**Select vendor**	1999-03-01	1999-06-25	17w	0w

Notes

Quotations from potential vendors of the correlator chip will be obtained and compared. As the result of a competitive process, a vendor will be selected to design the chip and ultimately be responsible for its fabrication.

8.7.3	**Chip design**	1999-06-28	2000-09-22	65w	0w

Notes

The correlator chip will be designed by the selected vendor, working closely with the correlator engineers.

8.7.4	**Prototype chip fabrication**	2001-01-08	2001-07-01	25w	0w

Notes

A small batch of prototype correlator chips will be fabricated by the selected vendor.

8.7.5	**Prototype chip test**	2001-07-02	2001-08-24	8w	0w

Notes

The prototype correlator chips will be evaluated in test fixtures and on prototype correlator boards. The results will determine the suitability of the chip for production.

8.7.6	**Design modifications**	2001-09-24	2002-01-11	16w	0w

Notes

It is likely that, as a result of the design, fabrication, and test effort for the correlator chip, some design modifications will be found necessary. These will be implemented in a design revision as required.

8.7.7	**Fabricate and test design mods**	2002-01-14	2002-04-12	13w	0w

Notes

The revised version of the correlator chip will be fabricated and the design modifications verified.

8.7.8	**Fabricate production run**	2002-04-15	2002-07-05	12w	0w

Notes

An initial production run of the revised design will be made. This will provide enough correlator chips to build the prototype correlator.

8.8	**Racks**	2000-08-03	2001-07-16	49.6w	39.5w

ID	Resource Name	Units	Work	Delay	Start	Finish
15	Engineer Correlator	13%	6.43w	0w	2000-08-03	2001-07-16
16	Technician Correlator	67%	33.07w	0w	2000-08-03	2001-07-16

Notes

The correlator will be housed in many racks with multiple interconnections.

8.8.1	**Design mechanical layout**	2000-08-03	2000-08-30	4w	0w

Notes

The mechanical layout of various card cages, cables, etc. will be designed.

8.8.2	**Design power distribution**	2000-08-31	2000-09-27	4w	0w

Notes

The power supplies, their location, and their connection to the card cages will be designed. The thermal properties will be considered and air flow designed to dissipate heat adequately in the thin air of the high site.

8.8.3	**Select control computer**	2000-12-05	2001-01-01	4w	0w

Notes

The requirements for the control computer(s) which operate the correlator on an intimate level will be determined by analysis. A computing capability and suitable operating system will be chosen. Possible expansion or upgrade paths will be considered.

WBS (f)	Task	Start	Finish	Duration	Work
8.8.4	**Design control wiring**	2001-01-02	2001-01-29	4w	0w
	Notes: The control wiring, including flow of setup information and timing signals, will be designed and evaluated based on the experience with the GBT spectrometer.				
8.8.5	**Design signal wiring**	2001-01-30	2001-02-26	4w	0w
	Notes: The largest part of the correlator wiring, namely the signal interconnections, will be designed and evaluated in detail.				
8.8.6	**Order parts**	2001-02-27	2001-04-23	8w	0w
	Notes: The racks, cables, card cages, hardware, etc. will be determined and ordered.				
8.8.7	**Assemble prototypes**	2001-04-24	2001-07-16	12w	0w
	Notes: Prototype racks which are fully wired to accommodate correlator circuit boards will be assembled and tested.				
8.9	**Post-Correlation Processor**	1999-05-05	2000-12-01	82.6w	14w
	ID 12 Correlator Programmer, Units 8%, Work 7w, Delay 0w, Start 1999-05-05, Finish 2000-12-01				
	ID 15 Engineer Correlator, Units 8%, Work 7w, Delay 0w, Start 1999-05-05, Finish 2000-12-01				
	Notes: Because of the high volume of output data from the correlator, it may be necessary to design and build a custom post-correlation processor which employs large numbers of DSP chips. This will be designed to perform well-defined functions such as the application of real-time calibration data and Fourier transforms to the spectral domain before the data is passed to a general-purpose computer.				
8.9.1	**Specifications**	1999-05-05	1999-06-01	4w	0w
	Notes: The requirements for the post-processor will be written, including which tasks it will perform, and the speed requirements.				
8.9.2	**Select data processing hardware**	1999-06-07	1999-10-01	17w	0w
	Notes: A selection of particular DSP's will be made. A decision about building custom processor boards or using commercially available boards will be made on the basis of performance and cost.				
8.9.3	**Design rack**	1999-10-04	2000-01-01	13w	0w
	Notes: A custom rack of card cages containing the post-processor will be designed.				
8.9.4	**Order parts**	2000-01-05	2000-02-01	4w	0w
	Notes: The DSP's, PC boards to hold them, card cages, racks, power supplies, etc. will be ordered.				
8.9.5	**Assemble**	2000-02-04	2000-06-01	17w	0w
	Notes: The post-processor will be assembled.				
8.9.6	**Test**	2000-06-05	2000-12-01	26w	0w
	Notes: The post-processor will be tested with simulated and real data.				
8.10	*CDR: Prototype Correlator*	*2000-07-31*	*2000-07-31*	*0d*	*0w*
8.11	**Software**	1999-02-01	2003-05-30	226w	66w
	ID 12 Correlator Programmer, Units 29%, Work 66w, Delay 0w, Start 1999-02-01, Finish 2003-05-30				
	Notes: Software at many levels will be written and debugged in conjunction with board and system checkout. This includes microprocessor code on individual boards, FPGA code, and software within the correlator computer. The software within the array control computer and data interface computer will also be written.				
8.12	**Prototype Correlator Production**	1999-09-02	2003-05-30	195.4w	0w
	Notes: A prototype correlator which is sufficiently populated as to permit cross-correlation of at least a dual-polarization 2 GHz bandwidth signal from 2 antennas will be built and tested.				
8.12.1	**Determine configuration**	1999-09-02	1999-10-27	8w	0w
	Notes: The detailed configuration of the prototype correlator to be used with the test array will be determined.				
8.12.2	**Order parts**	2002-03-07	2002-05-01	8w	0w
	Notes: The parts for the boards and racks for the prototype correlator will be ordered.				

WBS (f)	Task	Start	Finish	Duration	Work
8.12.3	**Assemble**	2002-07-08	2002-11-08	18w	0w
	Notes: The prototype correlator will be assembled.				
8.12.4	**Test**	2002-11-11	2003-03-28	20w	0w
	Notes: The prototype correlator will be tested.				
8.12.5	*Deliver Prototype Correlator to VLA site*	*2003-05-30*	*2003-05-30*	*0d*	*0w*
8.13	**Site Correlator Production**	2002-11-11	2006-10-06	204w	0w
	Notes: The correlator to be used at the high site will be fabricated, tested, and delivered to the MMA. This may be done in several builds.				
8.13.1	**First 1/4 correlator**	2002-11-11	2004-06-18	84w	0w
8.13.1.1	**Determine configuration**	2002-11-11	2002-12-06	4w	0w
	Notes: Any required final adjustments to the configuration will be determined and applied.				
8.13.1.2	**Order parts**	2002-12-09	2003-02-28	12w	0w
	Notes: All parts for the correlator including correlator chips will be ordered.				
8.13.1.3	**Assemble**	2003-03-03	2003-09-12	28w	0w
	Notes: The correlator will be assembled.				
8.13.1.4	**Test**	2003-09-15	2004-06-18	40w	0w
	Notes: The correlator will be tested in the laboratory.				
8.13.1.5	*Deliver 1/4 Correlator to MMA site*	*2004-06-18*	*2004-06-18*	*0d*	*0w*
8.13.2	**Second 1/4 correlator**	2003-09-15	2005-03-25	80w	0w
8.13.2.1	**Order parts**	2003-09-15	2003-12-05	12w	0w
	Notes: All parts for the correlator including correlator chips will be ordered.				
8.13.2.2	**Assemble**	2003-12-08	2004-06-18	28w	0w
	Notes: The correlator will be assembled.				
8.13.2.3	**Test**	2004-06-21	2005-03-25	40w	0w
	Notes: The correlator will be tested in the laboratory.				
8.13.2.4	*Deliver 1/4 Correlator to MMA site*	*2005-03-25*	*2005-03-25*	*0d*	*0w*
8.13.3	**Third 1/4 correlator**	2004-06-21	2005-12-30	80w	0w
8.13.3.1	**Order parts**	2004-06-21	2004-09-10	12w	0w
	Notes: All parts for the correlator including correlator chips will be ordered.				
8.13.3.2	**Assemble**	2004-09-13	2005-03-25	28w	0w
	Notes: The correlator will be assembled.				
8.13.3.3	**Test**	2005-03-28	2005-12-30	40w	0w
	Notes: The correlator will be tested in the laboratory.				
8.13.3.4	*Deliver 1/4 Correlator to MMA site*	*2005-12-30*	*2005-12-30*	*0d*	*0w*
8.13.4	**Fourth 1/4 correlator**	2005-03-28	2006-10-06	80w	0w
8.13.4.1	**Order parts**	2005-03-28	2005-06-17	12w	0w
	Notes: All parts for the correlator including correlator chips will be ordered.				

WBS (f)	Task	Start	Finish	Duration	Work
8.13.4.2	**Assemble**	2005-06-20	2005-12-30	28w	0w
	Notes The correlator will be assembled.				
8.13.4.3	**Test**	2006-01-02	2006-10-06	40w	0w
	Notes The correlator will be tested in the laboratory.				
8.13.4.4	***Deliver 1/4 Correlator to MMA site***	*2006-10-06*	*2006-10-06*	*0d*	*0w*
8.14	**Continued Support**	2003-06-02	2007-03-30	200w	0w
	Notes The engineers and technicians responsible for the correlator will provide continued support to site personnel as the correlator is brought on line along with the other parts of the MMA.				