8-24-99

INNOTECH SYSTEMS INC.

320 MAIN STREET PORT JEFFERSON N.Y. 11777 516 928-6888 FAX 473-5259

Joe Greenberg
National Radio Astronomy Observatory (NRAO)
2015 Ivy Road, Suite 219
Charlottesville,VA 22903
804-296-0355
jgreenbe@nrao.edu

August 24, 1999

Dear Mr. Greenburg:

Thank you for visiting us last Monday. This is our modified proposal for engineering services and production units for the ALMA 4096 Lag Correlator ASIC based on our discussions. Included in this proposal are ASIC development, test plan, engineering service charges, production pricing and schedule. This quote has been modified to reflect a staged development, improved power estimation and for using 0.25um or smaller technology since our proposal of July 28.

Two options have been added as well. Additional costs and production pricing for the 8192 version of the ASIC have been added. Also, an option for a multi-project wafer run of a reduced function version of the ASIC is offered. The multi-project wafer may be desirable for increased confidence that the ASIC circuitry conforms to your system requirements.

Should *Innotech Systems, Inc.* fail to properly execute any of these design steps, that work will be corrected free of any additional charge. Additional fees will be required for any circuit or specification changes after Design Start or for changes in technology selection after Physical Design has started.

All billings are net 30 days. This quote and is subject to engineering availability. Manufacturing Phase pricing is budgetary. Thank you for this opportunity to participate in the ALMA project.

Sincerely,

Louis J. Morales
V.P. of Engineering

STATEMENT OF WORK

DESIGN STEP	RESPONSIBILITY	CRITICAL PATH +
INITIAL DESIGN PHASE: Q4'99 estimated start		
DESIGN START Agreement on specification, design approach, and schedule. Initial design review. Work begins.	Customer/ISI	1 week
CIRCUIT DESIGN Design logic from existing schematics and specification. Custom multiply/add/accumulate block is designed. Add test logic. Begin initial simulations.	ISI	4 weeks
PRELIMINARY ASIC CIRCUIT SIMULATION Circuit is simulated to verify functionality. Logic simulations are done using representative process information.	ISI	4 weeks
INITIAL SIGN-OFF REVIEW Pre-route ASIC design review. Customer approves all work done to date.	Customer/ISI	½ week
FINAL TECHNOLOGY SELECTION PHASE: Q3'00 estimated start		
PHYSICAL DESIGN Design technology and foundry are chosen. Tech files and cell libraries needed to support the chosen process are received and installed at ISI. Circuits completed to date are resized/redesigned to accommodate process and available cell libraries. Floorplanning begins.	ISI	6 weeks
ASIC LAYOUT Cells are completed. ASIC routing is done. Actual resistances and capacitances are extracted and used for final SPICE simulations. Layout is checked against design rules and schematic connectivity using CAE software.	ISI	8 weeks
POST-LAYOUT SIMULATION Circuit timing is verified using actual capacitance loading from layout results. Circuit improvements are made. Final DRC and LVS checks are completed. Layout database is ready for manufacturing.	ISI	2 weeks
MPW RUN (OPTIONAL) Generate layout for a 64 X 2 lag version of the complete chip. Prototype with an appropriate multi-project wafer run house depending on schedule wafer starts and process choices (wafer starts are generally every 2 months for new processes, e.g. 0.25um)	ISI	TBD
Deliver 10 packaged and tested prototypes	ISI	TBD
MANUFACTURING PHASE: Q1'01 estimated start		
FINAL SIGN-OFF REVIEW Final design review. Customer approves all design work prior to ASIC prototype build. ASIC prototype lots are scheduled and started.	Joint	½ week
TEST DEVELOPMENT Simulation vectors are converted to test program. Test hardware is implemented and checked.	ISI	-
PROTOTYPES Delivery of 100 commercial ASIC prototypes.	ISI	9 weeks

Description of Solution:

Design Methodology: Complete turnkey ASIC development for ALMA 4096 Lag Correlator ASIC, based on existing schematics and specification. Design and production work will be split into 3 phases: initial design, technology specific, and manufacturing.

NRAO's Responsibilities: Finalize spec, generic circuit design, review and sign-off approval of simulation results, test plan approval, and prototype approval.

ISI's Responsibilities: ASIC specific circuit development, schematic entry, circuit simulation, ASIC design, development, test plan, test generation, masks, prototype and production foundry.

Notes:

8192 Lag Correlator ASIC The price differential will be ~2X for piece price (more expensive package & larger die size) and +$57K for non-recurring charges. Power dissipation would be about 1.6X the 4096 version. If price is not the main issue, we can re-visit this option.

Power - We will customize the layout for the multiplier, accumuator, and adder to minimize power at 125MHz operation. With ambient temperature to below 30°C at about 1000CFM air flow (at ~55% air density) there should be no problem with power given our current estimates.

Test pins and partial scan logic will be added to access the internal logic for good test coverage within a reasonable number of tester cycles.

ASIC Overview:
Circuit Description: ALMA 4096 Lag Correlator ASIC (8192 lag version is optional)
Process: 0.25um CMOS
Package: 240 PQFP
Additional requirements: boundary scan & TAP controller

Engineering Services Pricing: Each phase specified may be committed to independently. The Manufacturing Phase charges will vary depending on our technology choice at that time. It is expected that pricing will decrease for 0.25um production by 2001.

Item	Description	Unit Price	Qty	Total
1	Design Start			$52600.
2	Initial Sign-off Review			$26300.
	INITIAL DESIGN TOTAL			$78900.
3	Physical Design			$29400.
	FINAL TECHNOLOGY SELECTION TOTAL			$29400.
4	Final Sign-off Review			$131000.
5	Test development			$7000.
6	Prototype units	$140.	100	$14000.
7	Prototype Approval (within 45 days)			$26000.
	MANUFACTURING TOTAL			$178000.

OPTIONAL:

Item	Description	Unit Price	Qty	Total
8	MPW prototype run			$32000.
9	MPW prototypes	$200	10	$2000.
10	Additional engineering time	$95/hour		
	Additional for ALMA 8192 version:			
3A	ALMA 8192 additional physical design (over 4096)			+ $10000.
4A	ALMA 8192 additional FS review			+ $25000.
4B	ALMA 8192 custom leadframe			+ $20000.
5A	ALMA 8192 additional Test Development			+ $2000.

Production Pricing:

ALMA 4096 Lag Correlator ASIC in 240 PQFP:
10000 units (minimum) $70/unit one time buy in 2 shipments (scheduled within 8 mo)
39322 units $45/unit " " " " " "

ALMA 8192 Lag Correlator ASIC in 240 PQFP:
10000 units (minimum) $130/unit one time buy in 2 shipments (scheduled within 8 mo)
39322 units $84/unit " " " " " "
delivery 18 weeks ARO