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HOT ELECTRON CHARGING EFFECTS

The following is a synopsis of the effect put together by one of my guys. The degradation due to this effect is increasing with newer technologies. As a data point, Chartered Semi announced their hot carrier lifetime degradation for 0.18um process as follows: 10% reduction in Idsat w/ Vds=1.1*Vdd, Vdd=1.8v, L=0.18um, 2.7 years (NMOS device). This effect is dramatically improved with reduction in Vdd.

SUBSTRATE CURRENT:

The electric field near the drain can reach extraordinarily large values with moderate voltages in short-channel devices. As a consequence, carriers can acquire enough energy between scattering events to cause impact ionization upon their next collision. Impact ionization by these "hot" carriers creates electron-hole pairs. The generated electrons tend to be swept to the drain and generated holes swept into the substrate in an NMOS device. The resulting substrate current is a sensitive function of the drain voltage, and this represents an additional conductance term shunting the drain to ground. This effect is of greatest concern when one is seeking the minimum output conductance at high drain-source voltage.

GATE CURRENT:

Some of the "hot" electrons can be attracted to the oxide due to the electric field induced by a positive gate voltage. If the electrons have energies on the order of 1.5 eV, they may be able to tunnel into the oxide; or in some cases they may be able to overcome the silicon-oxide potential barrier and produce a gate current which may exist for a long time. The charge comprising this gate current can become trapped in the oxide, causing upward threshold shifts in NMOS devices and threshold reduction in PMOS devices.

MEASURES:

The hot electron charging effects are continuous processes so the device degrades over a period of time, and may tend to limit the useful life of the device. To reduce the peak channel field and thereby mitigate high-field effects, a lightly doped drain (LDD) structure is used in modern devices. In such a transistor, the doping in the drain region is arranged to have a spatial variation, progressing from relatively heavy near the drain contact to lighter somewhere in the channel. The peak electric field is also a function of the curvature of the n+ drain region. The electric field in the conventional device peaks approximately at the metallurgical junction and drops quickly to zero in the drain since no field can exist in the highly conductive n+ region. On the other hand, the electric field in the LDD device extends across the lightly doped n- region before dropping to zero at the drain.

References:

T.H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits", pp. 73-77, Cambridge University Press, 1998.

D.A. Neamen, "Semiconductor Physics And Devices", pp. 593-600, Richard D. Irwin, INC., 1992