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Subject: WBS for joint phase 1
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Dear John,

Nice to see you are registered at the Washington meeting. There will be some opportunity to discuss further the WBS for Joint Phase 1 and other questions.

I definitely prefer the revised WBS for the Joint Phase where we see a progression from the baseline to the future correlator; this is in the spirit of closer cooperation.

I have questions/comments:

Task 7.2 Test Interferometer Correlator: I know that you are 'cloning' the GBT correlator for 800 and 100 MHz band operation. In relation to this it would be great to generate a system block diagram for the test interferometer (who is doing that?) -agreed by the US and Europe- to see where we could offer help.

Task 7.3 Baseline Correlator Development: Items 7.3.1 to 7.3.8 mean a lot of achievements for which you are working hard but I need to know whether there is room for sharing tasks.

- 7.3.1 Sampler: do you proceed according to your own strategy? As you know we passed to Larry some comments/critcisms on his 'MMA Digitizer Chip: Draft Spec.' document, but I am unsure about your decisions on this question. Or do we believe that commercial samplers for the Baseline Correlator can do the job? This is highly risky I believe.
We have a team here (Bordeaux/Toulouse) working on samplers and we hope that by the end of 2001 we could produce prototype ASICs for high speed sampling; 2-bit 4-levels but probably not 3-bits.

-7.3.2 FIR Filter: You mean Filter for test interferometer? How does this fit with the idea (which I like much) to have all delays at the antenna? You include fine delay in the FIR filter card or do you see this as a further development specific to the Baseline correlator?
Following your MMA Memo 204 there has been a lot of interest here again, and in Arcetri (Comoretto): simulations, and work on fpga (rapid) chips from Altera. Ther is still a long way to go to an ASIC

- 7.3.3 Custom Boards: I presume the correlator board will not be finished at the end of Phase 1. I understand you wish to start this task quickly.

- 7.3.4 Correlator Chip: The chip designer has been selected I presume? and you intend to start production during Phase 1. The overall production process may last much longer.

I'd like to add

7.4 Future Correlator

to the revised WBS sent by Dick Kurz. Our team in Europe is not yet complete but we foresee a Feasibility Study during 2000, and a Preliminary Design Phase with final report and hopefully review of PDP at the end of 2001. I'd like to inform you about all this in Washington (including our work on samplers and FIRs).

Do you agree in adding a 7.4?

Hoping there will be enough time in Washington I'd also like:

a- to discuss with you in general terms about the ALMA correlator block-diagram: functionalities, relation to the overall system concept;

b- to inform you about the study areas proposed at Jodrell about the fibre work for ALMA.

I'd appreciate your answers and/or reactions before the meeting next week. I'm leaving on tuesday 5 and not much available on 4 afternoon.

Best wishes, Alain

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