Correlator chip – IMEC

1. Distance problem. Work mostly ~~in Europe~~ in English, have worked with US companies electronically. They figure 2 face-to-face meetings required.
2. Large company – they have resources to keep schedule.
3. IMEC is separate from Europractice [redacted] = project name within IMEC, service offered by a consortium. Have 4 partners who use Europractice for prototyping. Would be a small effort. Contract with IMEC only.
4. Usual thing? Frequently do same sort of thing. Consider this of moderate complexity. Size? have gone up to 300k gates, but done more complex circuits. Have right tools.
5. Why use UMC instead of IMEC foundry? Not set up to do production – process research only. UMC 100% capacity – brief problems due to Taiwan earthquake. For volume, would contract with IMEC only – they would handle wafer production, test, and packaging.
6. Responsibility for proper functioning? Agree to a process for testing which determines that chip has correct functionality. Done at end of layout using approved test vectors. Have never [redacted] gotten silicon which does not work.
7. Why 6 metal layers? Interconnect issues. 95% use of silicon in core – chip would grow with fewer layers. Have typically used 5 or 6 layers. Might try layout with as few as 4 layers for this chip – but would have to look carefully at timing. Save NRE for masks – not much

IMEC, cont.

difference in production volume

8. Use 240-pin instead of 208-pin plastic package? Would be only a small difference in price.
9. Standard cells? Virtual Silicon standard cells, used at many foundries. Qualified library. ~250 standard cells, ~100 I/O cells, memory generators. Have not done a full power analysis. due to short bid cycle. For full custom, lots of extra cost. Library has several versions of each cell, with various levels of drive capability and power consumption.
10. Lifetime? Will operate @ 2.5V, gives good lifetime - have not checked with foundry. Interacts with performance margin.
11. What is ESTEC? Technical center of ESA.
12. How many custom designs per year? 10-15.
13. Speed? Doing 0.7μm with 560Mhz clock. 125Mhz is slow for 0.25μm
14. Have beta release of 0.18μm library. By April 2000, 1.8V, will have some circuits designed. Available as multi-project in mid-2000. Guess prototype run would cost X2. Dedicated run of ~5 wafers. Guess production cost for 4K log chip will go down (based on previous experience with migration to smaller features). Could start with VHDL first; technology commitment comes about 2 months after start. Design & layout costs would be the same. Might be a little more effort to get the timing right.

Correlator chip - XENTEC

1. How was per-chip price determined? Would go through an ASIC house who would contract with UMC. Xentec would be out of the loop. Quote came from the ASIC company.
2. What experience? Complexity is at the lower end, gate count on high end. Have done 5X-10X complexity chip with 350K gates. Have done memory design. Always right the first silicon. Xentec in last 18 months: 6 chips, 4 from spec. Have done full custom. First cut at our chip was to do full custom in 0.18μm - much more expensive, a little more risky not to use standard cells. Would be ~30% less silicon, much less power - looked at 8k chip.
3. Standard cells. Could go to 0.18μm, could go partial or full custom. Price would be 40% less in volume, but considerably more NRE, could get 8k with <2W. Artisan library, could be MITEL [redacted] or Globalcad for 0.18μm library.
4. Power. Did an analysis. With 100% running, Artisan low-power flipflop assumed. Got ~2.3-2.5W using 0.25μm and 2.5V. Assumed short external runs. Xentec strong in analog design, know what tricks to play.
5. 6 layers of metal? Think 3 is too few, expect 4-5; 4 may be optimum. Masks are only ~$1500 each. Would be hard to meet 125 MHz speed with only 3 layers.

6. 240-pin vs. 208-pin? Only pennies difference – maybe <$1 more per chip. Packages 1-2¢ per pin. Mostly done in Taiwan, Korea etc.
7. Lifetime. Doesn't think it's a problem. Talked to the foundry. Would design for 135 MHz and worst-case commercial; expect it would work to 140-150 MHz.
8. Structure of company? 10 engineers, Sun/HP workstations. 8 are MSEE, 2 BSEE. Half booked by a company in Minneapolis. Most customers in US, some Europe & Canada.
9. Test vectors. Expect 100% verification of digital. Don't know if they will use a PLL for clock distribution. Factory tests typically run at 5-10 MHz. Suggests characterizing 100 chips over freq, temp, power.
10. 0.18 μm? Say, start 1 Dec.; in March decide for 0.18 μm – would have to resimulate – some extra NRE. Expect ~~the~~ 60-70% increase in NRE going to 8k lgs. Expect $49 each for prototypes. Don't quite know if 0.25 μm can reach 125 MHz at 1.8V – would be pushing it, would probably need 5 layers.
11. Accuracy of power prediction depends on vendors. E.g. LSI Logic – estimates were 40% high. Xentec has always been 10-20% lower in silicon than in simulation.
12. Comment: designing in 0.18 μm is about 50% different from designing in 0.25 μm. Don't do schematic capture – use VHDL or Verilog which can generate schematics.