INNOTECH SYSTEMS INC.
41 WINTER STREET SUITE 53 BOSTON MA 02108 (617)695-2700 FAX 423-0466

DESIGN START REVIEW

Date of meeting: January 11, 2000
Design Name: ALMA Lag Correlator
NRAO Part Number: TBD
Foundry Part Number: TBD

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Reviewed at meeting:

Spec review: circuit function, timing requirements, and chip function. Chip development is started based on the schematics and specification.

NRAO is satisfied with the basis of Design Start and authorizes ISI to proceed with the chip development.

AGREED BY NRAO:	ACCEPTED BY INNOTECH SYSTEMS:
John C Webber	
Name	Name
1-18-00	1/14/00
Date	Date

INNOTECH SYSTEMS INC.
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Recipient:	Acct Payable	Sent By:	Lou Morales
Company:	NRAO	Company:	Innotech Systems Inc.
Fax Number:	91(505)835-7030	Fax Number:	617-423-0466
Voice Number:	(505)835-7000	Voice Number:	617-695-2700

Date: 1/14/00

Time: 6:46:02 PM

Total No. Pages: 4

Subject: ALMA ASIC Design Start

Message:

Here's our bill for the Design Start milestone completion. Also attached is the Design Start Sign-off form and an estimated working schedule.

Please return the Sign-off form at your convenience.

INNOTECH SYSTEMS INC.
320 MAIN STREET PORT JEFFERSON N.Y. 11777 516 928-6888 FAX 473-5259

ISI INVOICE NUMBER:
M00101

CUSTOMER PURCHASE ORDER NUMBER:	ORDER DATE:	PRINTED ON:	PAGE
57514	**December 6, 1999**	**January 14, 2000**	**1**

QUOTE NUMBER:	CONTRACT NUMBER:	FREIGHT TERMS:
BA092999	**n/a**	**n/a**

METHOD OF SHIPMENT:
Design start completed 1/11/00 with Ray Escoffier

SALES TERMS:
Net 30

SHIP TO:

Associated Universities Inc.
NRAO
2015 Ivy Road
Suite 219
Charlottsville, VA 22903

BILL TO:

Associated Universities Inc.
NRAO
PO Box 0
Socorro, NM 87801-0000
Attn: Accounts Payable

SHIP TO CUSTOMER NUMBER: **CB0020**

BILL TO CUSTOMER NUMBER: **CB0020**

ITEM	PART NUMBER	DESCRIPTION	PRICE	QUANTITY	TOTAL
1	DS-0001	Design Start for ALMA Lag Correlator ASIC development	$52600.	1	$52600.

TOTAL DUE: $52600.

January 14, 2000

NRAO ALMA ASIC DEVELOPMENT INITIAL SCHEDULE

DESIGN START	(1/11/00)
Choose 0.18um foundry/update pricing	1/28/00
Get fabs library, technology, and model files	2/11/00
CIRCUIT DESIGN / CIRCUIT SIMULATION	
Design add/accumulate complete; start layout	2/25/00
Design 1 lag complete; finish add/acc sims and lifetime est.	3/10/00
Layout add/accumulate complete; start preliminary lag1 layout	3/17/00
Design lag64/128 complete; preliminary lag1 layout complete; start work on test methods	3/24/00
Complete report on power dissipation and cost implications of 4K/8K ASIC version	3/31/00
Decide on 4K/8K ASIC version	4/5/00
Design 256/512 lag block and top level circuitry complete, including expected test logic required	5/5/00
TEST DEVELOPMENT	
Production test vectors are written and simulated.	6/2/00

< at this point, we may want to wait a month or more, especially since funding for the next step is not likely until January 2001. This would reduce the amount of rework needed if a technology or logic change is needed >

INITIAL SIGN-OFF REVIEW	
Pre-route ASIC design review	6/12/00+
ASIC LAYOUT	7/14/00+
POST-LAYOUT SIMULATION / VERIFICATION	8/4/00+
DATABASE SIGN-OFF REVIEW	8/9/00+