1-20-00 Webber

# ALMA Correlator PDR

# Introduction, Schedule, and Budget

John Webber

January 20, 2000

# ALMA Correlator PDR Agenda

## January 20

| | | | |
|---|---|---|---|
| Coffee etc. | 0800 | | |
| Introduction | 0830 | 15m | John Webber |
| Science requirements | 0845 | 15m | Al Wootten |
| System overview | 0900 | 30m | Ray Escoffier |
| Digitizer requirements | 0930 | 10m | Larry D'Addario |
| Digitizer plans | 0940 | 20m | Alain Baudry |
| BREAK | 1000 | 20m | |
| Signal interfaces | 1020 | 20m | Ray Escoffier |
| FIR filter | 1040 | 40m | Ray Escoffier |
| Station cards | 1120 | 40m | Ray Escoffier |
| LUNCH | 1200 | 60m | |
| Fiber optics | 1300 | 30m | Jim Jackson |
| Correlator card & chip | 1330 | 60m | Joe Greenberg |
| Long term accumulator | 1430 | 30m | Chuck Broadwell |
| BREAK | 1500 | 20m | |
| Computer interface | 1520 | 20m | Chuck Broadwell |
| Software issues | 1540 | 20m | Jim Pisano |
| Schedule & budget | 1600 | 30m | John Webber |
| Open discussion | 1630 | 60m | |
| ADJOURN | 1730 | | |
| | | | |
| DINNER-cocktails | 1830 | | Rococo's |
| -food | 1900 | | |

Particular issues to discuss:

- Filters at the antenna or the correlator?
- Interfaces with fiber optic cards
- Chip: 0.18 micron technology? 8K/4K lags?
- Monitor and control
- Control card/local microprocessor issues and programming language

January 21

| | | | |
|---|---|---|---|
| Coffee etc. | 0800 | | |
| European plans | 0830 | 120m | Baudry, Torres, Bos |
| BREAK | 1030 | 30m | |
| Discussion | 1100 | 30m | |
| Closed committee session | 1130 | 60m | |
| LUNCH | 1230 | 60m | |
| Lab tours, dispersal | 1330 | | |

# Procedures

Presentations by the correlator group will detail the design goals, design principles, progress to date, and plan for further development.

Committee and invited participants are expected to:

> Ask questions and comment at any time.
>
> Write up issues requiring a response beyond that given in the course of the review and submit them to the chairman.
>
> At the conclusion of the meeting, provide answers to the guideline questions.

Following the review, any unresolved issues submitted will be studied and a response provided within one month; the MMA Project Manager will determine if any further action is required.

# MMA PDR Guidelines

(1) Are the top level performance requirements for the subsystem complete and adequate?

Has ? ~~adequate~~ OK

(2) Have ~~the~~ ~~correct~~ design solutions been selected for study and development during the MMA D&D Phase? Are there important alternate solutions that are not being studied?

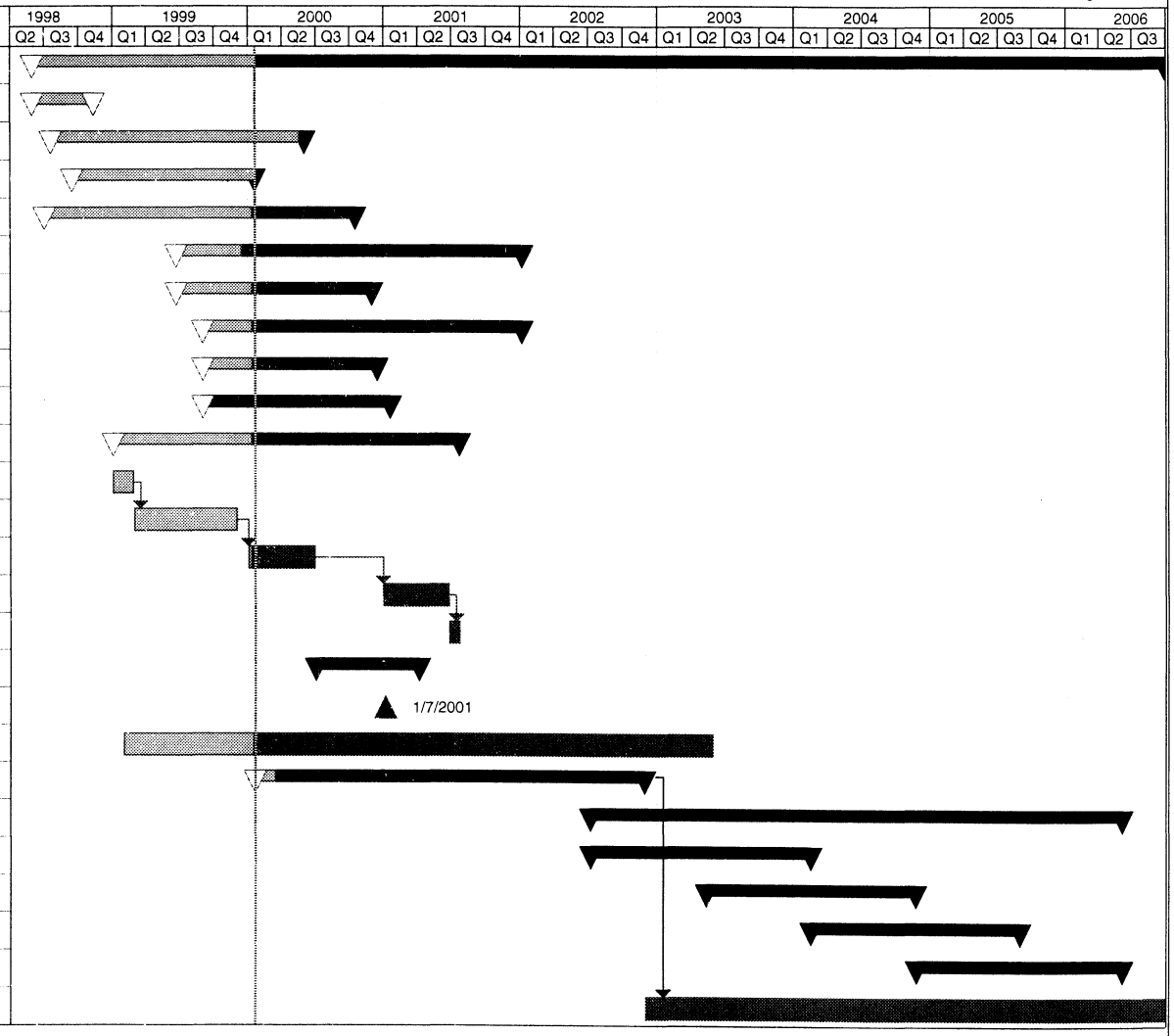
(3) If a major procurement is required for the subsystem during the MMA D&D Phase, is the procurement plan correct?

# ALMA U.S. Task Scheduling

**8 Correlator Tasks selected**

File: Correlator plan 2000-Jan-18.mpp
View: Clean Gantt View
Printed: 1:48 PM 1/18/00


| WBS ( | Task | Start | Finish |
|---|---|---|---|
| 8 | **Correlator** | 6/1/1998 | 9/29/2006 |
| 8.1 | Specifications | 6/1/1998 | 11/13/1998 |
| 8.2 | Test Correlator | 7/20/1998 | 6/1/2000 |
| 8.3 | Preliminary Design | 9/15/1998 | 1/20/2000 |
| 8.5 | Finite Impulse Response Filter | 7/3/1998 | 10/18/2000 |
| 8.6 | Custom Boards | 6/23/1999 | 1/7/2002 |
| 8.6.1 | Station Card | 6/23/1999 | 12/1/2000 |
| 8.6.2 | Correlator Card | 9/2/1999 | 1/7/2002 |
| 8.6.3 | Long-Term Accumulator | 9/2/1999 | 12/15/2000 |
| 8.6.4 | System Control Card | 9/2/1999 | 1/19/2001 |
| 8.7 | Correlator Chip | 1/4/1999 | 7/23/2001 |
| 8.7.1 | Specifications | 1/4/1999 | 2/26/1999 |
| 8.7.2 | Select vendor | 3/1/1999 | 12/3/1999 |
| 8.7.3 | Chip design | 1/3/2000 | 6/29/2000 |
| 8.7.4 | Prototype chip fabrication | 1/2/2001 | 6/25/2001 |
| 8.7.5 | Prototype chip test | 6/26/2001 | 7/23/2001 |
| 8.8 | Racks | 7/3/2000 | 4/6/2001 |
| 8.10 | CDR: Prototype Correlator | 1/7/2001 | 1/7/2001 |
| 8.11 | Software | 2/1/1999 | 5/30/2003 |
| 8.12 | Prototype Correlator Production | 1/21/2000 | 11/29/2002 |
| 8.13 | Site Correlator Production | 7/9/2002 | 6/5/2006 |
| 8.13.1 | First 1/4 correlator | 7/9/2002 | 2/16/2004 |
| 8.13.2 | Second 1/4 correlator | 5/13/2003 | 11/22/2004 |
| 8.13.3 | Third 1/4 correlator | 2/17/2004 | 8/29/2005 |
| 8.13.4 | Fourth 1/4 correlator | 11/23/2004 | 6/5/2006 |
| 8.14 | Continued Support | 12/2/2002 | 9/29/2006 |




Milestones: **bold type**
Summary Tasks: **underline**

Task | Split | Progress | Milestone | Completed Mlstn | Summary | Summary Progress

# ALMA Correlator Status

- Station card: 90% of design done, waiting on I/O tests
- FIR filter: 90% of design done, waiting on I/O tests
- Correlator card: 20% of design done
- LTA: 40% of design done
- Control card: concept done, awaiting completion of requirements of other cards
- Test fixtures:
  - Station card/filter testing: 30% of design done
  - Correlator card testing: not started
  - Plan minimal card count complete correlator for debugging

# ALMA Correlator Cost

Planned expenditures to end of 2000: $ 1,245,765

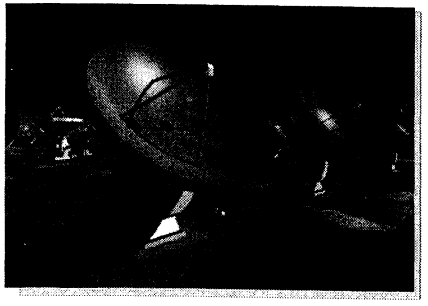
| Baseline Plan, 4K chip, 0.25 micron process: 2001-2006 expenditures, 1999 Kdollars | | | | |
|---|---|---|---|---|
| Item | Labor | Parts | Contingency | Item Total |
| FIR Filter | 30 | 10 | 8 | 48 |
| Station Card | 67 | 7 | 15 | 89 |
| Correlator Card | 67 | 7 | 15 | 89 |
| Long-Term Accumulator | 67 | 7 | 15 | 89 |
| System Control Card | 34 | 4 | 7 | 45 |
| Correlator Chip | 44 | 2302 | 610 | 2956 |
| Racks | 45 | 28 | 15 | 88 |
| Prototype Correlator | 500 | 193 | 194 | 887 |
| First Quadrant | 536 | 1485 | 566 | 2587 |
| Second Quadrant | 536 | 1485 | 566 | 2587 |
| Third Quadrant | 536 | 1485 | 566 | 2587 |
| Fourth Quadrant | 536 | 1485 | 566 | 2587 |
| TOTALS | 2998 | 8498 | 3143 | 14639 |

New plan, 4K chip, 0.18 micron technology $13838 K (-801 K)
Big plan, 8K chip, 0.18 micron technology $14967 K (+328 K)

Using 0.18 micron technology, cost of doubling correlator size is about $1.1M, or about 8% of the correlator cost.

Contingency is about 27% of total.

Totals are F.O.B. Charlottesville.



Atacama
Large
Millimeter
Array

# ALMA Prototype Correlator Control Computer Design

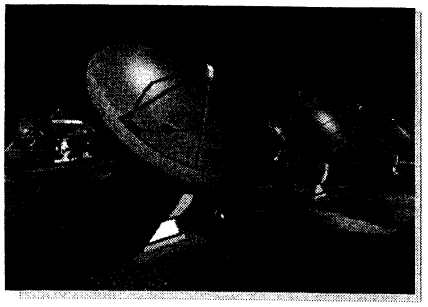

Jim Pisano

NRAO


January 20, 2000



1-20-00



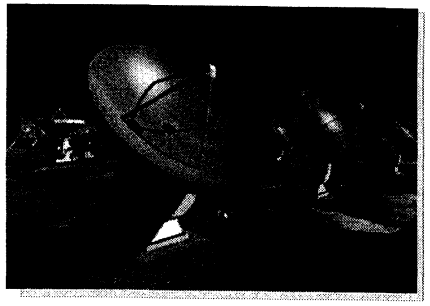


# Computer Hardware Design

- Correlator Control Computer
- Data Processing Computer

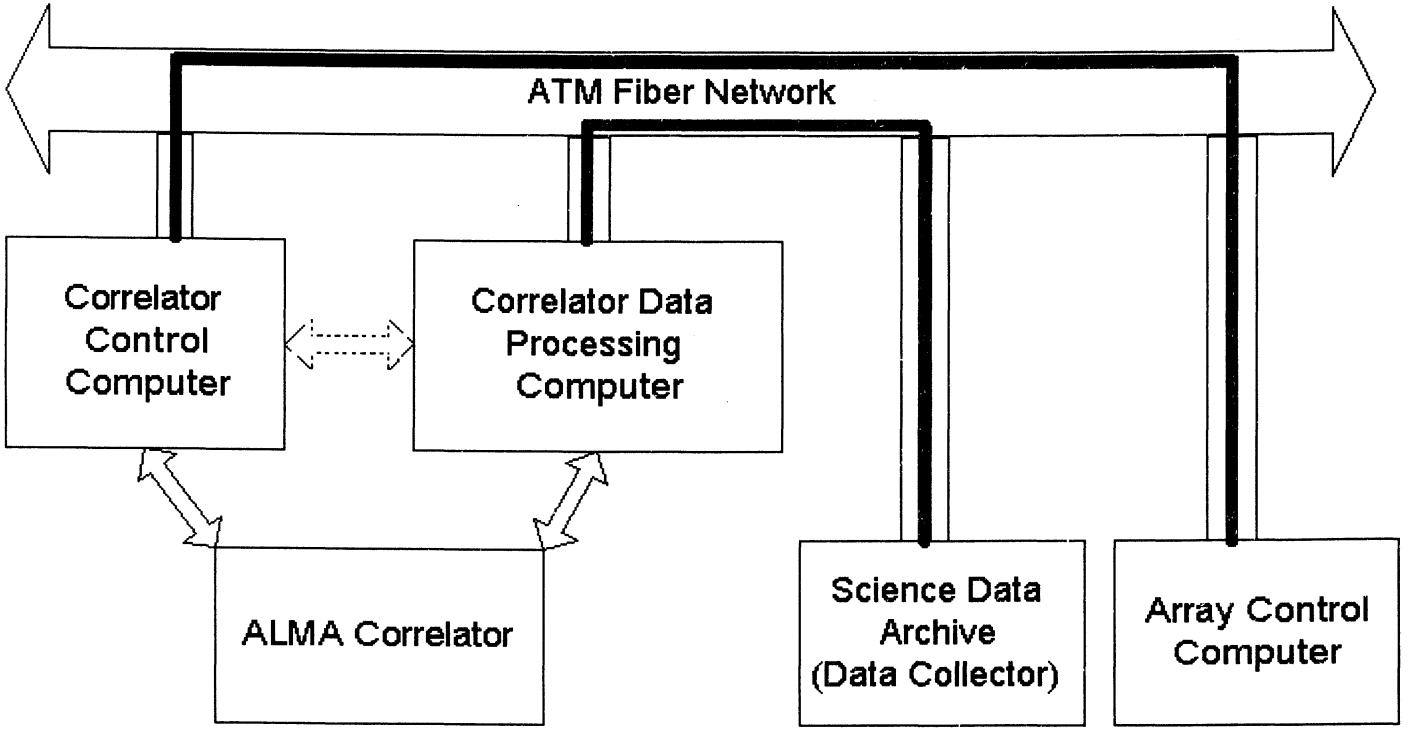
# Computer Software Design

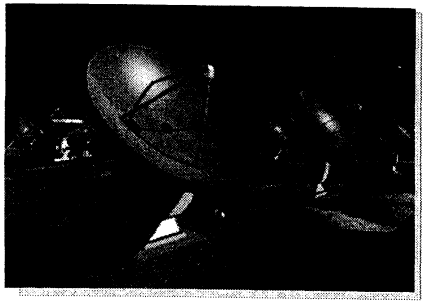
- Correlator Control Software
- Data Processing Software



**Atacama Large Millimeter Array**

# Computer Overview

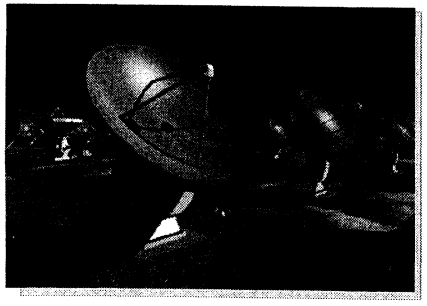






# Correlator Control Computer

- 1-2 PowerPC CPUs, VME bus
- CAN (Controller Area Network) Protocol
- CAN Network Master
- ATM node(s) in array-wide computer network



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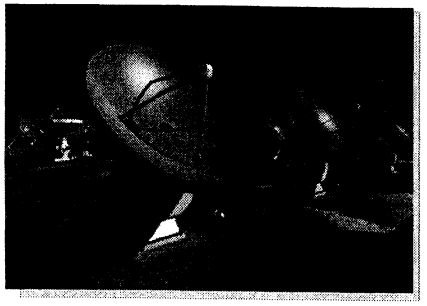
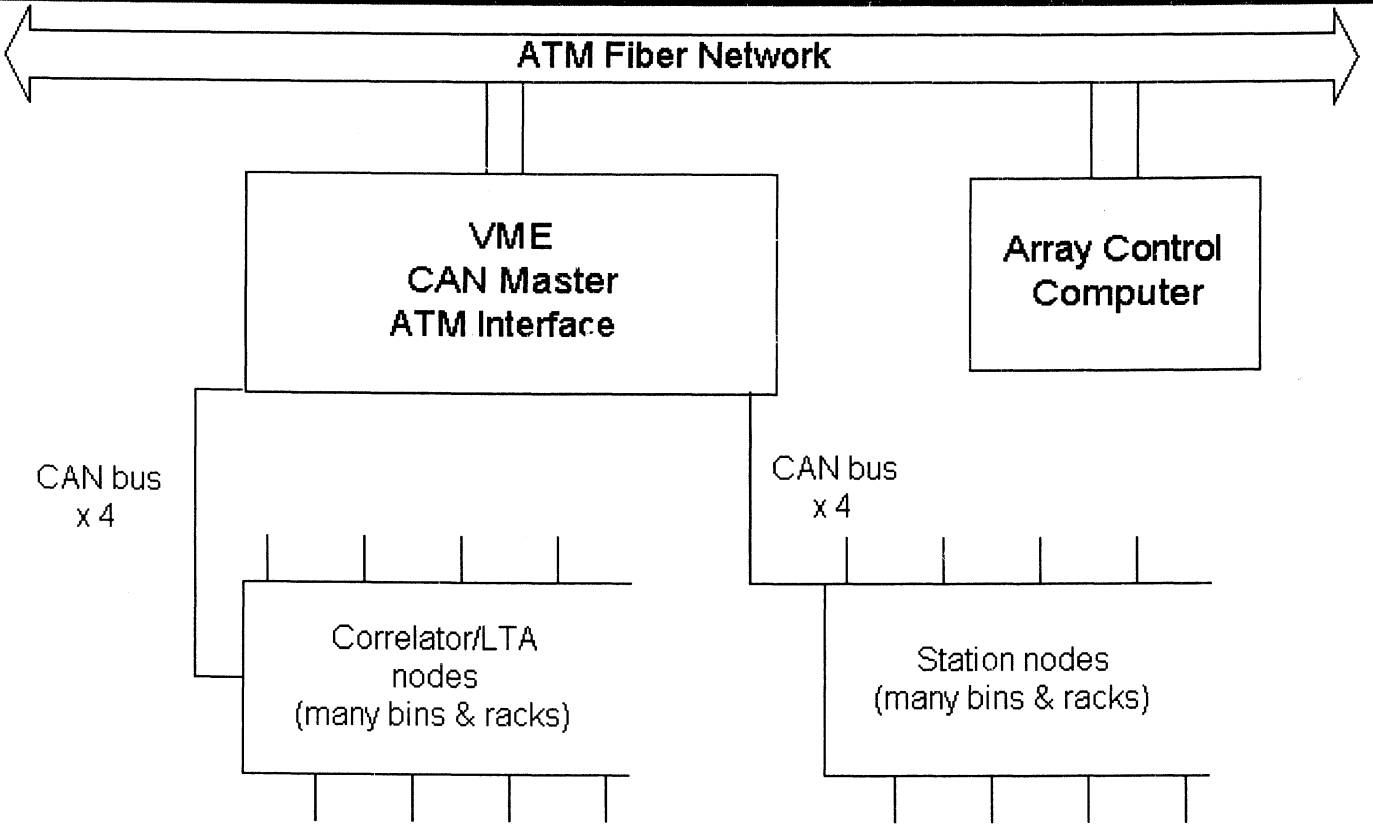
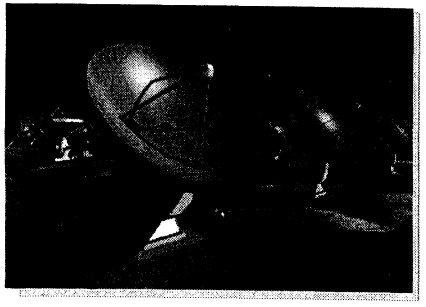
# Correlator Monitor & Control

- ALMA M&C bus uses CAN protocol defined in ***ALMA Monitor and Control Bus Draft Specification***
- Master/Slave mode with broadcasting
- 1 Mbit/sec, 40 meters, ~ 6K msgs./sec max.
- Maximum of 64 nodes - 1-2 CAN networks per baseband pair



# Atacama Large Millimeter Array







# Data Processing Computer

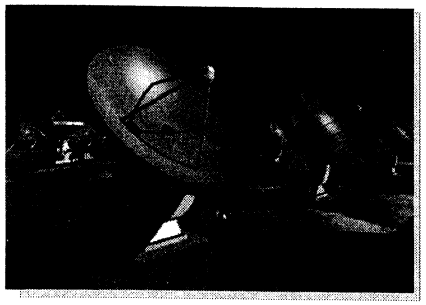
- Multiple CPUs
- VME plus high-speed bus, e.g, SkyChannel, RACEway/RACE++, InfiniBand
- FPDP (Front Panel Data Port) interface to LTA
- ATM node(s) in array-wide computer network

**Atacama Large Millimeter Array**

# LTA Data Output & Processing Rates

| Antennas | Total Results Quantity | Total Results per second | Number of 1024 lags/sec |
|---|---|---|---|
| 2 | 2,048 | 128,000 | 125 |
| 4 | 8,192 | 512,000 | 500 |
| 8 | 32,768 | 2,048,000 | 2,000 |
| 16 | 131,072 | 8,192,000 | 8,000 |
| 32 | 524,288 | 32,768,000 | 32,000 |
| 64 | 2,097,152 | 131,072,000 | 128,000 |

| | FFT (MIT FTW) FLOPS 26,492 | VanVleck Correction 22,572 | Hanning Windowing 3,072 | Total MFLOPS | Total MFLOPS for 8 GHz Bandwidth |
|---|---|---|---|---|---|
| 2 | 3,311,500 | 2,821,500 | 384,000 | 7 | 26 |
| 4 | 13,246,000 | 11,286,000 | 1,536,000 | 26 | 104 |
| 8 | 52,984,000 | 45,144,000 | 6,144,000 | 104 | 417 |
| 16 | 211,936,000 | 180,576,000 | 24,576,000 | 417 | 1,668 |
| 32 | 847,744,000 | 722,304,000 | 98,304,000 | 1,668 | 6,673 |
| 64 | 3,390,976,000 | 2,889,216,000 | 393,216,000 | 6,673 | 26,694 |



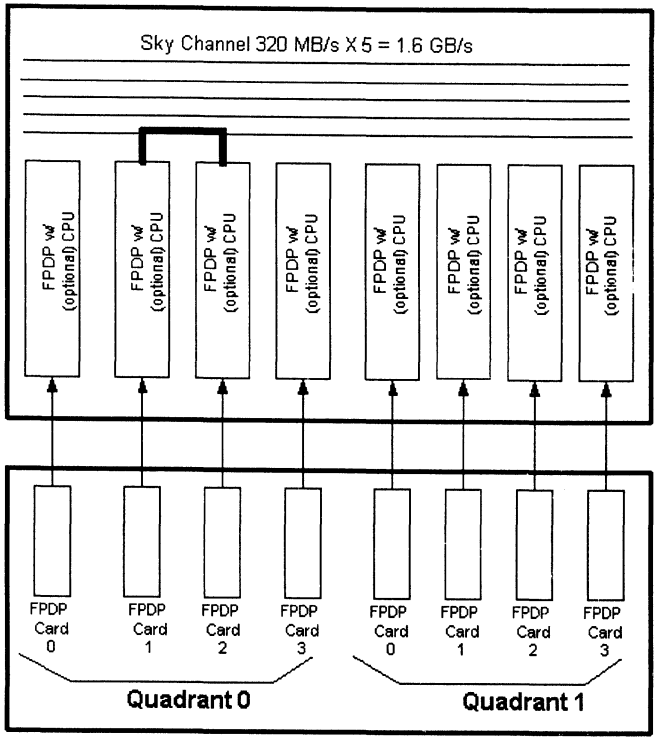


# Data Processor Computer

- 16 - 32 PowerPC 7400 (G4) @ 2.6 GFLOPS each
- 16 FPDPs capable of 160 MB/s each
- SkyChannel packet-switched network w/ 320 MB/s capacity
- 800 MB/sec total input rate spread over 4 quadrants - 200 MB/sec per quadrant

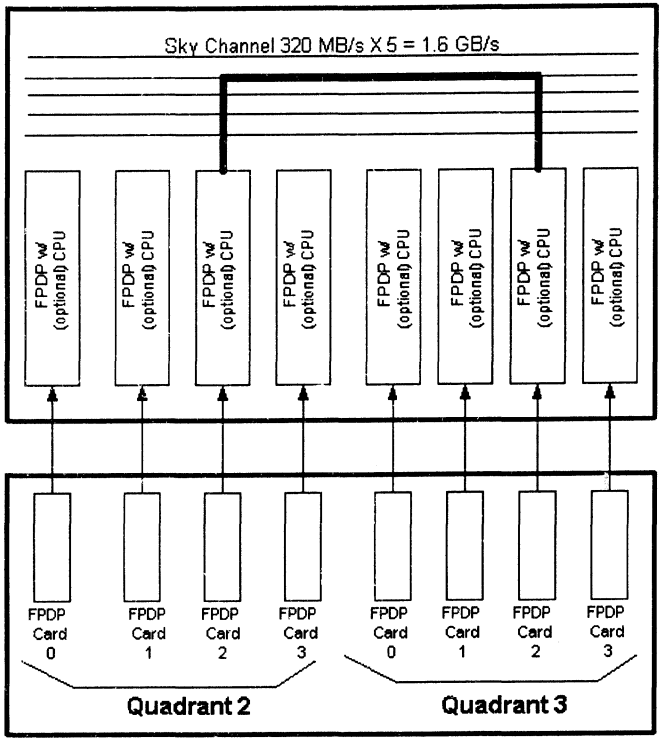
# Atacama Large Millimeter Array

VME Crate

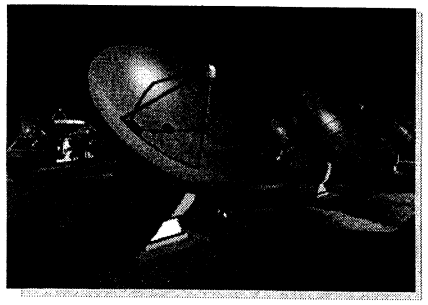



Correlator crate same rack as VME crate

VME Crate



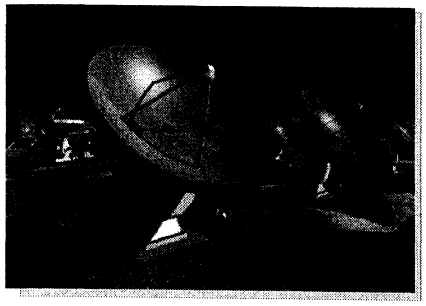

Correlator crate same rack as VME crate



Atacama Large Millimeter Array

# Software Overview

- Development Environment
  - C++/C
  - VxWorks RTOS
  - SKYvec Software Development Environment, i.e., compilers, libraries, RTOS, etc.
  - NRAO-supplied libraries, e.g., CAN drivers, data processing routines.



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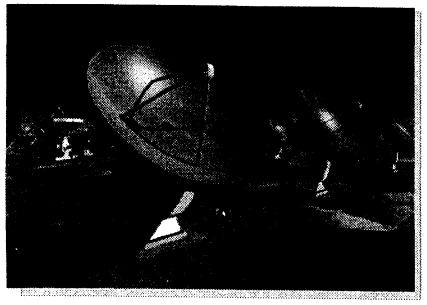
# Software Design Defining Items

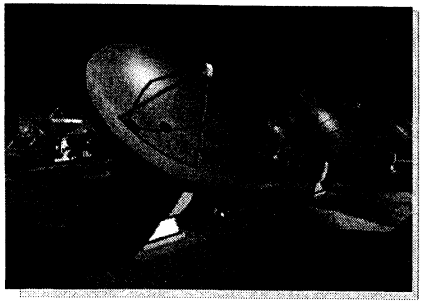
- Distributed software environment
- Inter-processor, inter-task communication
- Strong timing constraints
- Concurrent correlator configure/run model
- 3MB/sec sustained, 30MB/sec burst output





# Software Design Items (2)

- Support most correlator hardware capabilities
- Support expansion of computer hardware as correlator grows
- Reuse existing GBT clone correlator design





# Other Considerations

- Trading basebands for resolution
- Software requirements changing
- Hardware upgrades
- Software maintenance/upgrades

# The ALMA Correlator Computer Interface

## Correlator Results (High Data Rate Interface)

- LVDS interfaces from correlator racks to VME rack(s)
  (capable of full 128 MByte/sec rate out of LTA/Adder Tree)

  Total of 16 interfaces in full system (2 GByte/sec capacity)

- Front Panel Data Port (FPDP) Interface into VME bin

  Basic FPDP specifications:

  - 32 bit parallel interface
  - 40 MHz transfers (160 MByte/sec)
  - Cable length up to 5 meters

  Plan to limit cable length to 2 meters

  Plan to limit transfer rate to 25 MHz (100 MByte/sec max)
  (capacity of one result every 40 nsec, throttle back as required)

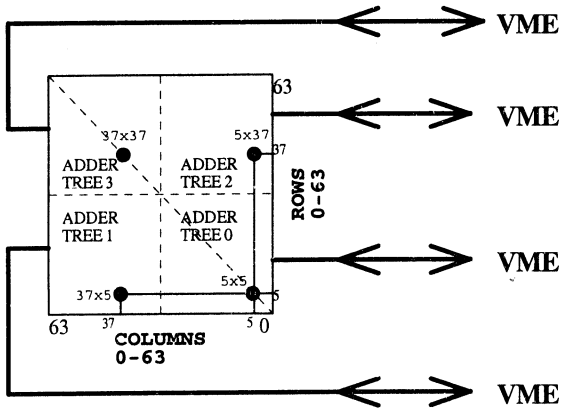
  Present plans suggest 80 nsec / result max utilization
  (50 MByte/sec)

Reasons for selecting FPDP:

- Ubiquitous
- Relatively simple
- 160 MByte/sec matches planned 128 MByte/sec output capacity of each stream

# THE ALMA CORRELATOR COMPUTER INTERFACE

(CORRELATOR RESULTS)




| ROW | | | | | | COLUMN | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | 0 | 5 | 4 | 3 | 2 | 1 | 0 |
| CARD MSB | | | | | | CARD LSB | | | | | |

**REQUEST PROTOCOL FOR EACH INTERFACE**

| BITS 15-10 | BITS 9-5 | BITS 4-0 |
|---|---|---|
| MASK NR (0-62) | ROW NR (0-31) | COLUMN NR (0-31) |

ONE OF 63 MASKS THAT SPECIFY WHICH PLANES ARE TO BE ADDED TOGETHER

- HOW MANY FPDP REQUIRED PER QUADRANT?

  MINIMUM:

  FOUR BI-DIRECTIONAL FPDP INTERFACES

  COULD CONSIDER:

  4 VME TO CORR FOR REQUESTS
  4 CORR TO VME FOR RESULTS

  OR

  4 VME TO CORR FOR REQUESTS
  8 CORR TO VME FOR RESULTS

- REQUEST PROTOCOL SUGGESTION:

  MAXIMUM REQUEST LIST IS 1024 REQUESTS (for 16 msec)

  2 BYTES PER REQUEST = 2048 BYTES IN 16 MSEC

  = 128 KBYTE/SEC

  MAY USE 5 Mbit/sec SYNCHRONOUS SERIAL INTERFACE INTERNALLY TO DISTRIBUTE THE REQUEST LIST TO THE LTA CARDS

# The ALMA Correlator Computer Interface

## Correlator Control (Low Data Rate Interface)

- Infineon (Siemens) C167 embedded processors

  All embedded code written in C (our goal anyway)

- CAN bus

  2000-6000 transactions per second (8 bytes each = 16-48 KByte/sec)
  64 Nodes max per bus

- Flash storage of FPGA images, C167 code etc.

  Large data blocks downloaded during "maintenance" time blocks

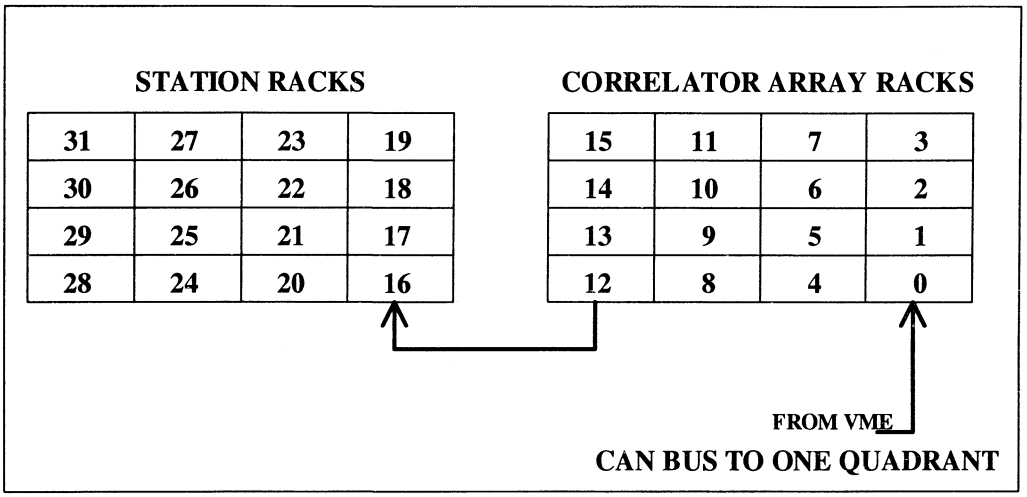
- No FPGA image changes as a function of mode

  This is the goal for at least all "normal" modes

- Local generation of mode based program words

# The ALMA Correlator Computer Interface

## Correlator Control (Low Data Rate Interface)




- LTA / Correlator Control Card "example"

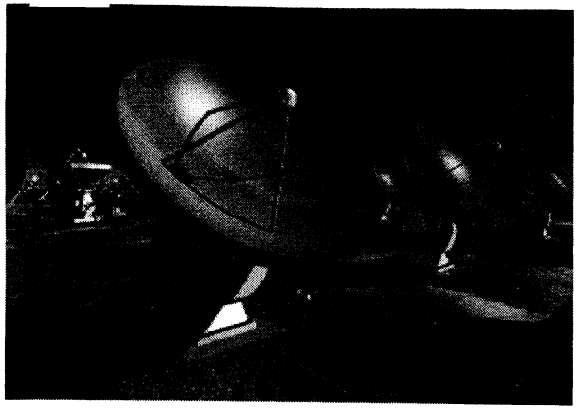
| Parameter | | Corr | LTA |
|---|---|---|---|
| Correlation mode: | CROSS or AUTO | X | X |
| Accumulation time: | number of 1 msec multiples | | X |
| Over sample mode: | over sampled or not | X | |
| Polarization mode: | V, H, V+H or Full | X | |

All 16 cards require identical copies of the above parameters for each of 64 antennas -------- > CAN Broadcast mode?

Assume one CAN 8 byte transaction per antenna for the above parameters:

64 of the 2000 per second would then be required to totally re-configure the cards, if broadcast mode is viable, (1024 if not)

Webber



# ALMA Correlator PDR

## Science Requirements

20 January 2000

A. Wootten

Drawn from science documents from 1995 Tucson meetings, MAC submm supplements, white paper by Rupen, Shepherd and Wright, MMA Memo Series, and comments from S. Myers and others.



1-20-00

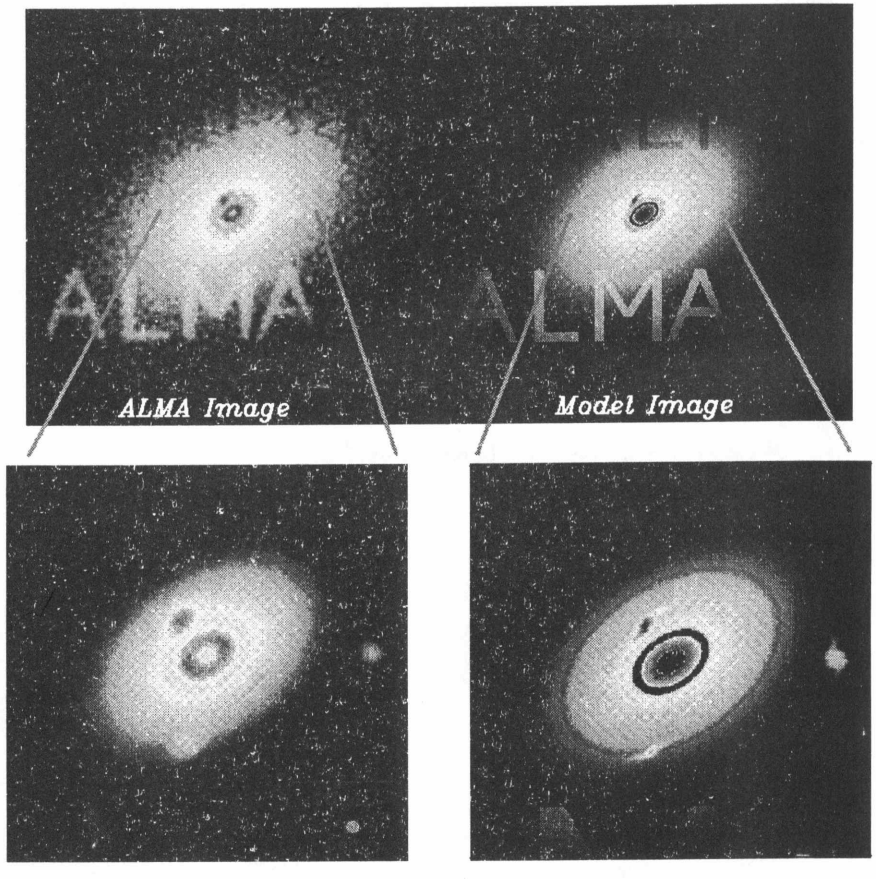
# Maximum Total Interferometric Bandwidth

- Continuum sensitivity
  - Massive protoplanets in other Solar Systems
  - Detailed views of protoplanets and protoplanetary disks
  - Emission from high-redshift galaxiew and protogalaxies
- Spectral line benefits
  - Pressure-broadened planetary lines - 3 Ghz
  - Outflows from young stars - 2GHz at highest frequencies
  - Recombination lines
    - Active Galactic Nuclei - 5 Ghz (1500 km/s at 850 GHz)
    - Solar 1-2 Ghz
    - H II regions 2 Ghz
  - Milky Way gas - 0.7 Ghz
  - 'Redshift machine' as much as possible--two 8 Ghz windows in opposite sidebands
  - Spectral line surveys as much as possible

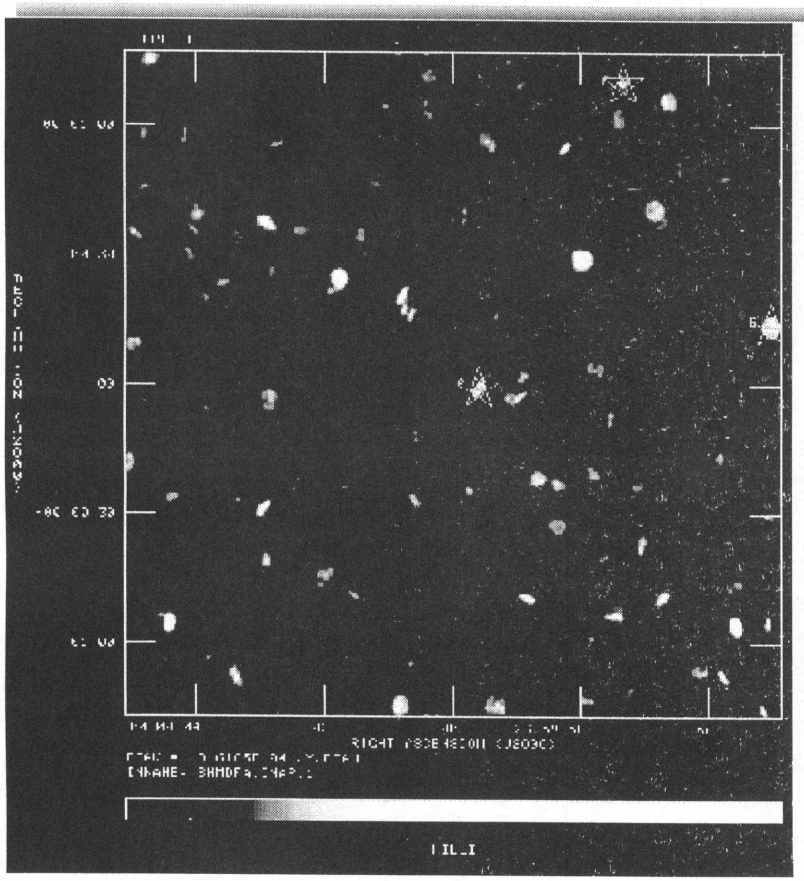
# Protoplanetary disks

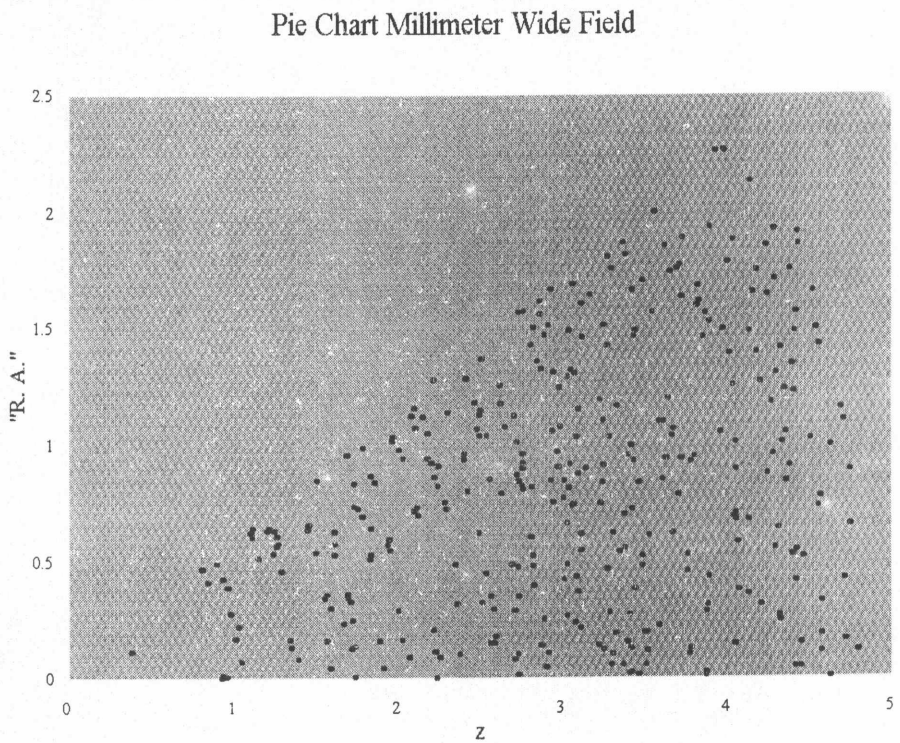
ALMA can detect and image protoplanets in nearby systems. Weak emission requires great sensitivity and bandwidth.

In some systems, spectral signatures of an atmosphere should be measureable in the reddening-free submillimeter, while optical or infrared spectroscopy remains confused by dust obscuration in a particle rich accretion environment.



# Redshift Machine mode





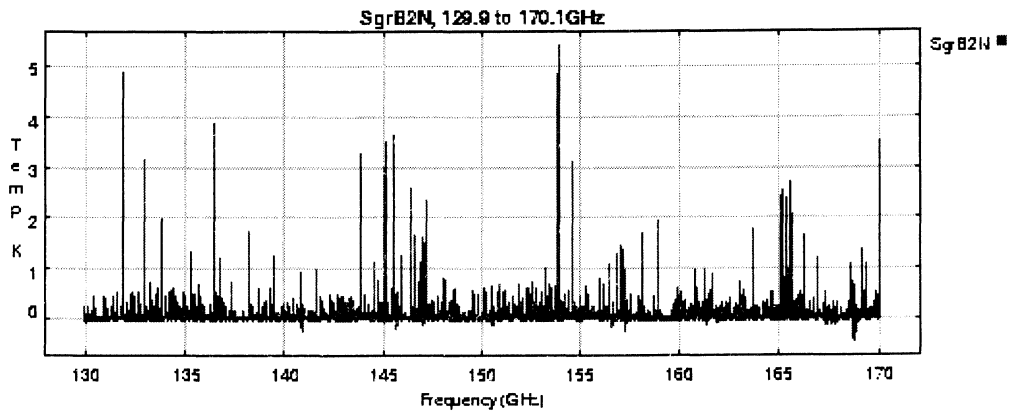

- Hundreds to thousands of galaxies in HDF-size fields; ~20% with measureable CO require the broadest band possible for identification and redshift measurement. This gives
- ALMA an ability to image in three dimensions, a capability beyond HST.

# Spectral Resolution

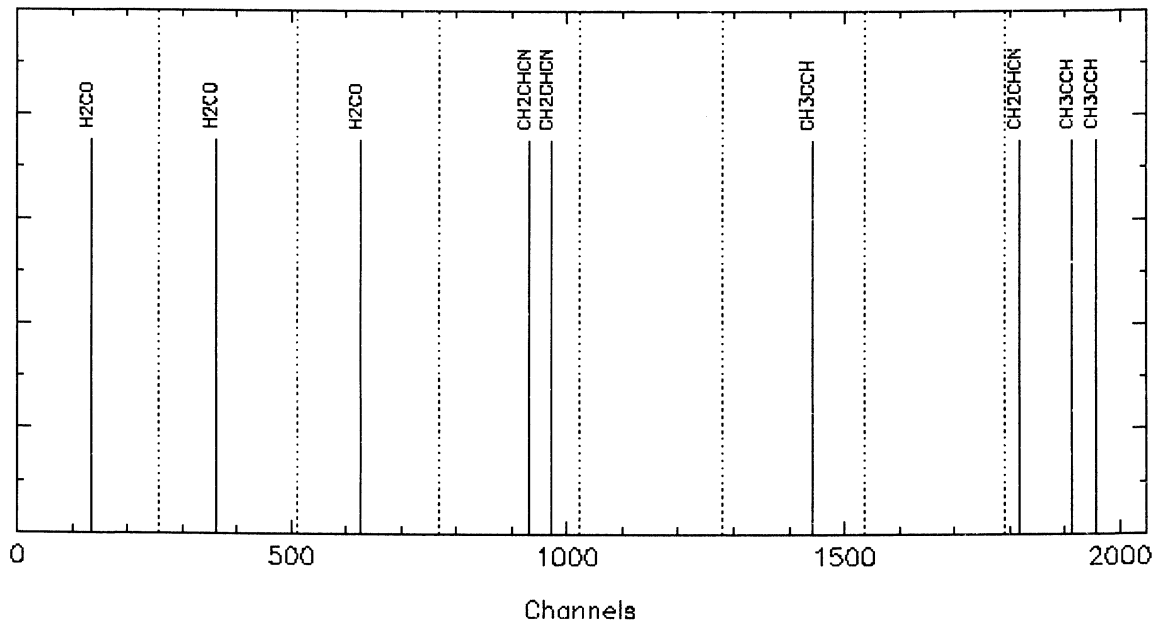
- High resolution: 0.02 - 0.05 km/s, or 4 kHz
  - Planetary winds
  - Cometary lines
  - Planetary satellites
  - Dark cloud core line profiles
  - Protostellar disks
  - Absorption lines
  - Zeeman probes of magnetic fields
- Special case higher resolution needs - not to be correlator drivers
  - Bistatic radar could require several hundred ~10Hz channels
  - SETI might benefit from 1 Hz resolution
- Largest channel widths
  - Bandwidth smearing - must be better than 24 Mhz
- Flexibility
  - Ability to place windows of appropriate resolution/bandwidth at specific points within the IF

# Other considerations

- Basebands - eight will allow bandwidths to conveniently match science goals, VLBA system.
- Channel number - 2mm Survey of Orion
  - 17000 potential lines over 40 Ghz, 12700 observed in Ori/KL
  - 1 line per 3 Mhz; current 1024 x 7.8 Mhz fails by 2x to give one channel per line.
  - More channels in wideband mode might be useful, if datarates were not increased.
- Dump times
  - 16 msec crosscorrelations
  - 1 msec autocorrelations



# BIMA Correlator example

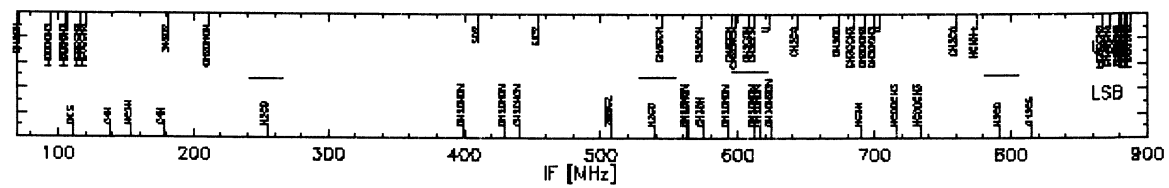



Obs. Freq. 218.86459 GHz
LO1: 220.28459 GHz

IF Freq. −150 MHz
LO2: 1270 MHz
VLSR: 0 km/s

Mode 4
Cross correlation

Corf1, Corf2, Corf3, Corf4 : 266.25366 528.75366 806.25 596.24634 MHz
Doppler shifted corfs : 266.25366 528.75366 806.25 596.24634 MHz
BW1, BW2, BW(3), BW(4): 25 25 25 25 MHz



# ALMA CORRELATOR SPECIFICATIONS

- 64 ANTENNAS
- 8 BASE BAND OUTPUTS PER ANTENNA
- 4 GSAMPLE/SEC PER BB, 4-BIT SAMPLES, 2-BITS CORRELATED
- MAXIMUM BANDWIDTH PER ANTENNA 16 GHz
- 1024 LEAD + 1024 LAG CORRELATORS PER BASELINE (WITH A CLOCK RATE OF 4 GHz)
- 32,768 LEAD + 32,768 LAG CORRELATORS PER BASELINE (WITH A CLOCK RATE OF 125 MHz)
- 1 MSEC ADJUSTABLE DELAY RANGE
- FULL POLARIZATION CAPABILITY (HH HV VH VV) PLUS AUTOCORRELATION
- DIGITAL FILTER FOR BANDWIDTHS LESS THAT 2 GHz
- MINIMUM ACCUMULATION TIMES, 16 MSEC CROSS, 1.0 MSEC AUTO
- 2 GBYTE/SEC TOTAL OUTPUT DATA RATE CAPACITY
- NO LIMIT ON SUB-ARRAYS
- ANALOG SUM
- PULSAR GATE

- PERFORMANCE EQUATUION

$$\text{SPECTRAL POINTS} = \frac{1024 \times F}{BB \times P}$$

F (BANDWIDTH FACTOR) = 1, 2, 4, ..., 32
BB (BASE BAND FACTOR) = 1, 2, 4, 8
P (POLARIZATION FACTOR) = 1, 2

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**Table 1. Examples of Correlator Modes**

| | Bandwidth | Corr. Products | $N_{chan} \times \Delta\nu$ | Total dv at 230 GHz | $\Delta$v at 230 GHz |
|---|---|---|---|---|---|
| A | 16 GHz (8 × 2 GHz) | XX | 1024 × 15.6 MHz | 20,900 km/s | 20 km/s |
| B | 8 GHz (4 × 2 GHz pairs) | XX,YY,XY,YX | 256 × 31.3 MHz | 10,400 km/s | 41 km/s |
| *or* | 8 GHz (4 × 2 GHz) | XX | 1024 × 7.8 MHz | 10,400 km/s | 10 km/s |
| C | 4 GHz (2 × 2 GHz pairs) | XX,YY,XY,YX | 256 × 15.6 MHz | 5,200 km/s | 20 km/s |
| *or* | 4 GHz (4 × 1 GHz pairs) | XX,YY,XY,YX | 512 × 7.8 MHz | 5,200 km/s | 10 km/s |
| D1 | 250 MHz (4 × 62.5 MHz pairs) | XX,YY,XY,YX | 8192 × 30.5 kHz | 330 km/s | 40 m/s |
| D2 | 125 MHz (2 × 62.5 MHz pairs) | XX,YY,XY,YX | 8192 × 15.3 kHz | 160 km/s | 20 m/s |
| D3 | 62.5 MHz (1 × 62.5 MHz) | XX | 32768 × 1.9 kHz | 82 km/s | 2.5 m/s |
| D4 | 32.8 kHz (1 × 32.8 kHz) | XX | 32768 × 1.0 Hz | 43 m/s | 0.1 cm/s |
| E | 1 GHz (4 × 250 MHz pairs) | XX,YY,XY,YX | 2048 × 0.5 MHz | 1,300 km/s | 0.6 km/s |
| *or* | 1 GHz (1 × 1 GHz pair) | XX,YY,XY,YX | 512 × 1.9 MHz | 1,300 km/s | 2.5 km/s |
| F | 4 GHz (2 × 2 GHz pairs) | XX,YY,XY,YX | 128 × 31.3 MHz | 5,200 km/s | 41 km/s |
| *and* | 4 GHz (2 × 2 GHz pairs) | XX,YY | 256 × 15.6 MHz | 5,200 km/s | 20 km/s |
| G | 6 GHz (3 × 2 GHz pairs) | XX,YY,XY,YX | 192 × 31.3 MHz | 7,800 km/s | 41 km/s |
| *and* | 500 MHz (1 × 500 MHz) | XX | 1024 × 0.5 MHz | 650 km/s | 0.6 km/s |
| H | 500 MHz (2 × 250 MHz) | YY | 2048 × 0.2 MHz | 650 km/s | 0.3 km/s |
| *and* | 250 MHz (1 × 250 MHz pair) | XX,YY | 1024 × 0.2 MHz | 330 km/s | 0.3 km/s |
| *and* | 62.5 MHz (1 × 62.5 MHz pair) | XX,YY | 4096 × 15 kHz | 82 km/s | 20 m/s |
| *and* | 1 MHz (1 × 1 MHz pair) | XX,YY,XY,YX | 2048 × 0.5 kHz | 1,300 m/s | 0.6 m/s |

Examples are described further in the text. Note that most examples are split into several lines in this table.

The *Bandwidth* column shows the total bandwidth covered, and how that bandwidth is divided among basebands or baseband pairs.

The *Corr. Products* column shows the polarization products produced by the correlator.

$N_{chan}$ is the number of channels; $\Delta\nu$ is the frequency resolution of each channel.

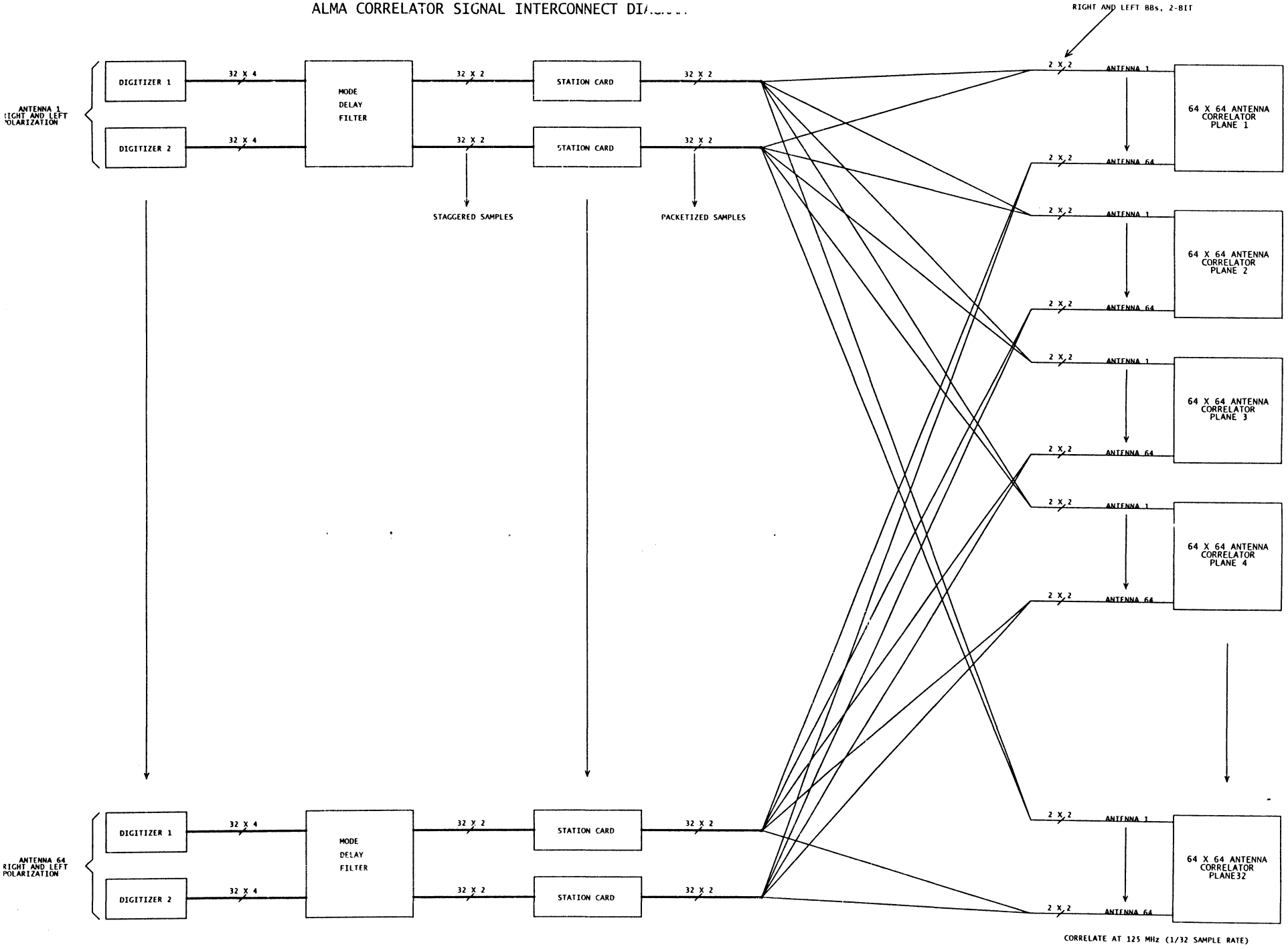
*Total dv at 230 GHz* is the total velocity coverage corresponding to the bandwidth (q.v.), assuming a line observed at 230 GHz.

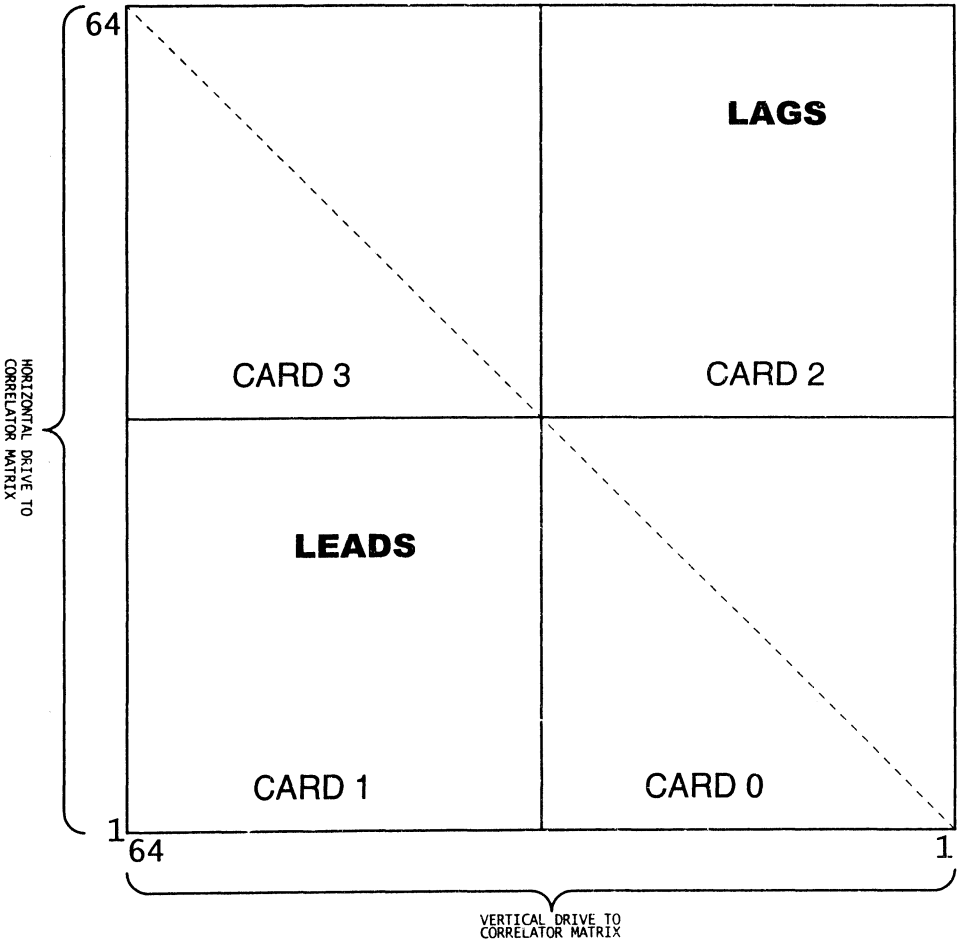
*$\Delta v$ at 230 GHz* is the velocity resolution corresponding to $\Delta\nu$ (q.v.), assuming a line observed at 230 GHz.

MMA CORRELATOR PERFORMANCE
(Selected Modes)

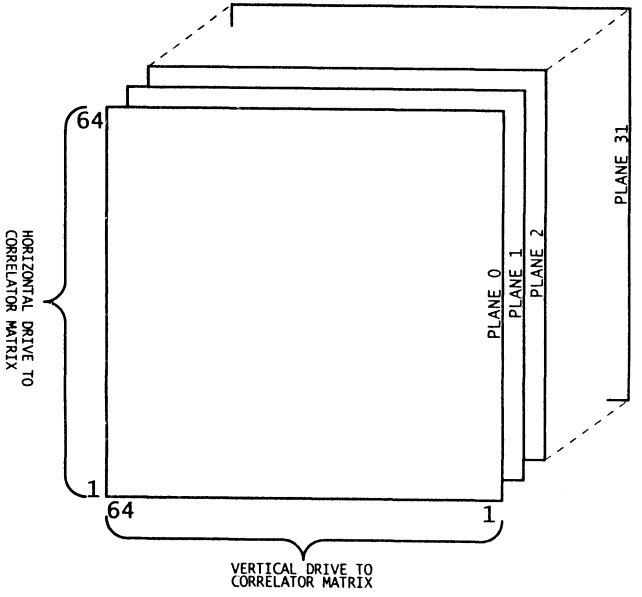
| # Samplers | Bandwidth/ Sampler | Cross-Polarization | Channels/ Product | At 230 GHz, in velocity space | |
|---|---|---|---|---|---|
| | | | | Total Range km/s | Resolution km/s |
| 8 | 2 GHz | yes | 64 | 9,391 | 40.8 |
| 8 | 2 GHz | no | 128 | 18,783 | 20.4 |
| 8 | 1 GHz | no | 256 | 9,391 | 5.1 |
| 8 | 500 MHz | yes | 2048 | 2,348 | 2.5 |
| 8 | 250 MHz | no | 1024 | 2,348 | 0.32 |
| 4 | 2 GHz | yes | 128 | 4,696 | 20.4 |
| 4 | 1 GHz | no | 512 | 4,696 | 2.5 |
| 4 | 500 MHz | yes | 512 | 1,174 | 1.3 |
| 4 | 250 MHz | no | 2048 | 1,174 | 0.16 |
| 2 | 2 GHz | yes | 256 | 2,348 | 10.2 |
| 2 | 1 GHz | no | 1024 | 2,348 | 1.3 |
| 2 | 500 MHz | yes | 1024 | 587 | 0.64 |
| 2 | 250 MHz | no | 4096 | 587 | 0.08 |
| 1 | 2 GHz | - | 1024 | 2,348 | 2.5 |
| 1 | 1 GHz | - | 2048 | 1,174 | 0.64 |
| 1 | 500 MHz | - | 4096 | 587 | 0.16 |
| 1 | 250 MHz | - | 8192 | 294 | 0.04 |

# ALMA CORRELATOR SIGNAL INTERCONNECT DI...

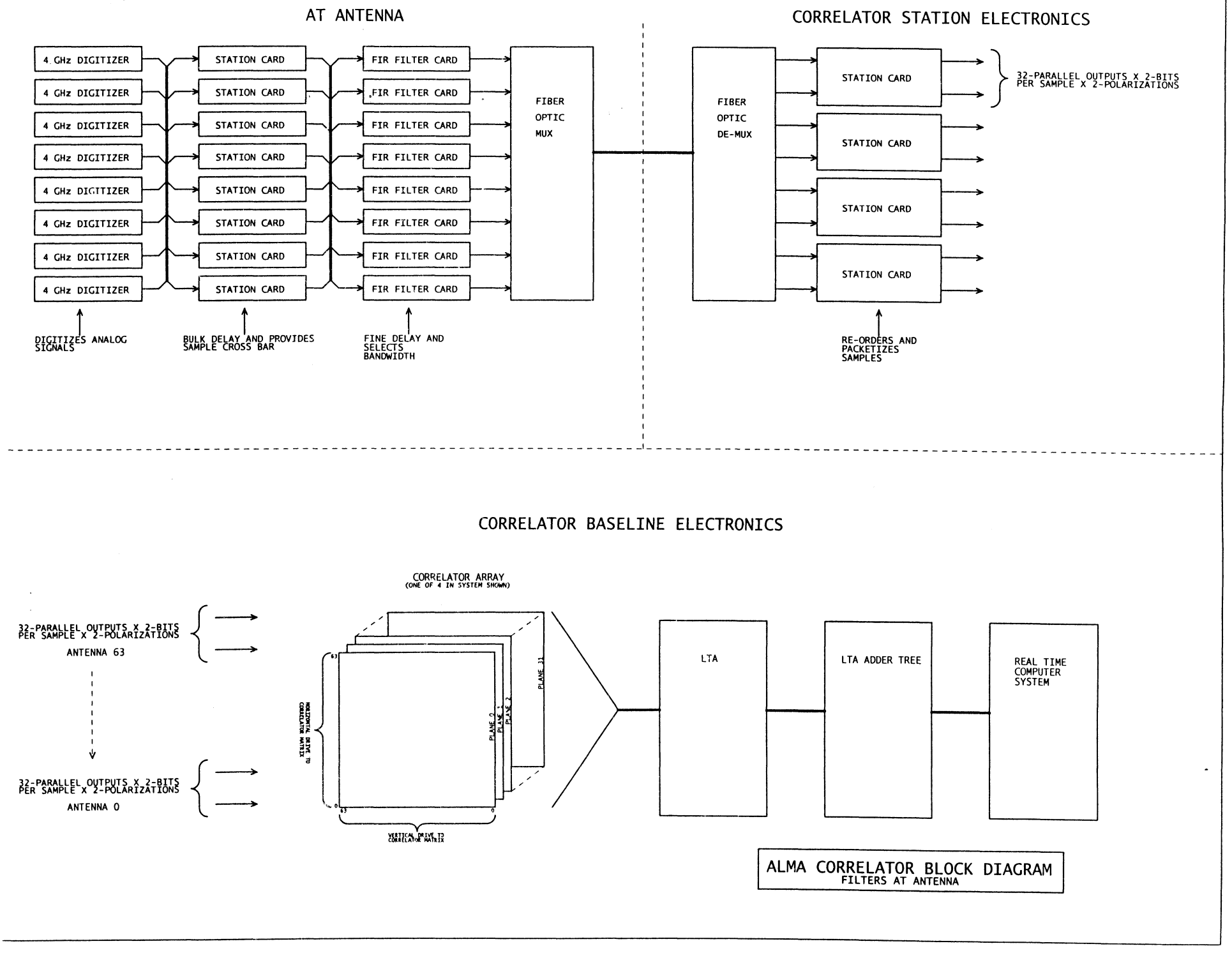





CORRELATOR PLANE




CORRELATOR ARRAY
(A TOTAL OF 4 ARE IN THE CORRELATOR)

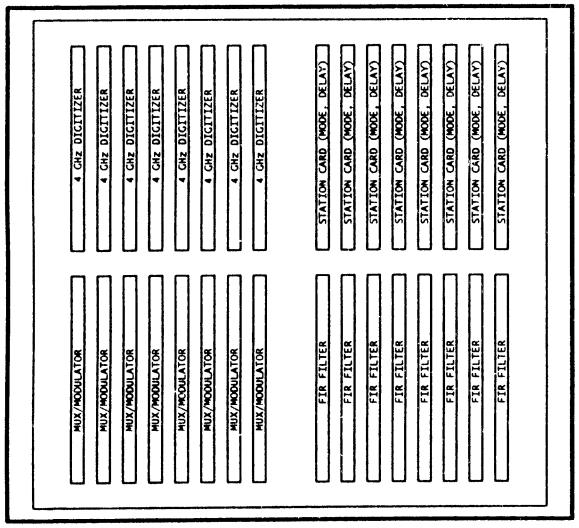



ALMA CORRELATOR BLOCK DIAGRAM
FILTERS AT ANTENNA

# FILTERS AT ANTENNA

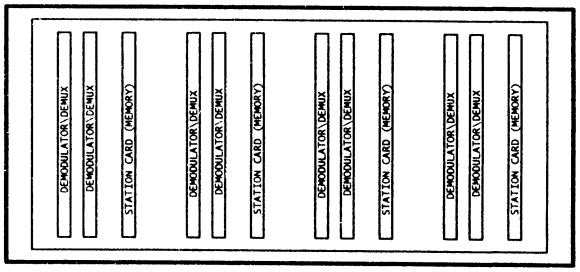
## ANTENNA ELECTRONICS BIN

1 REQD. PER ANTENNA




## CORRELATOR STATION ELECTRONICS BIN

64 REQUIRED IN 16 RACKS (AT 4 BINS PER RACK)

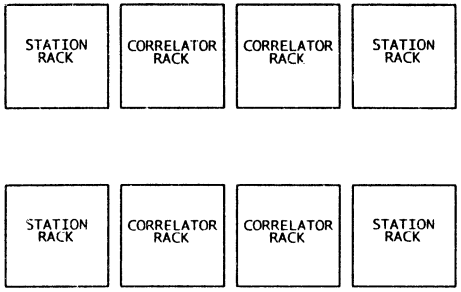



TWO BB OUTPUTS EACH FROM 4 ANTENNAS

## ONE CORRELATOR QUADRANT

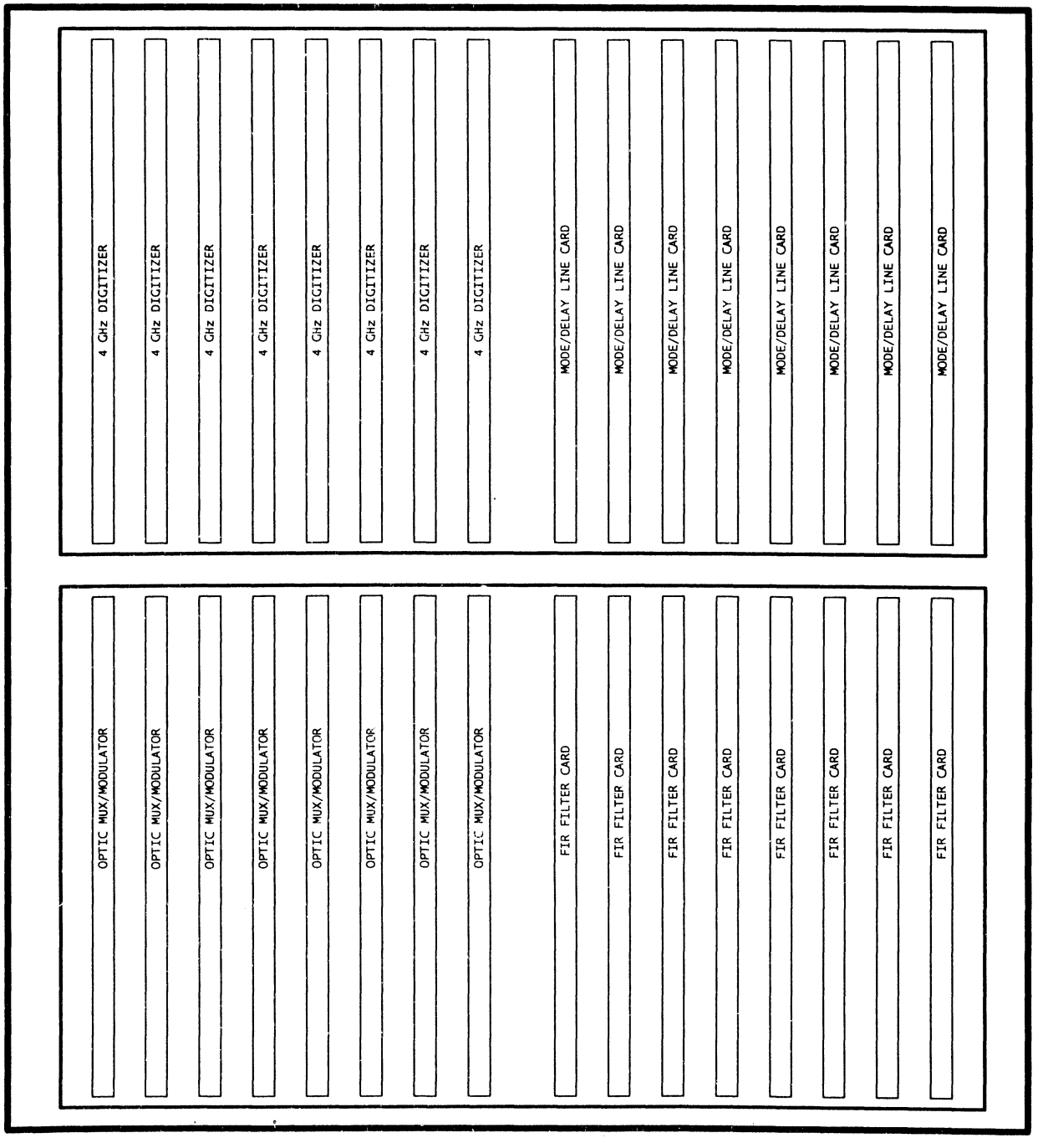
RACK FLOOR PLAN

32 RACKS IN FINAL SYSTEM



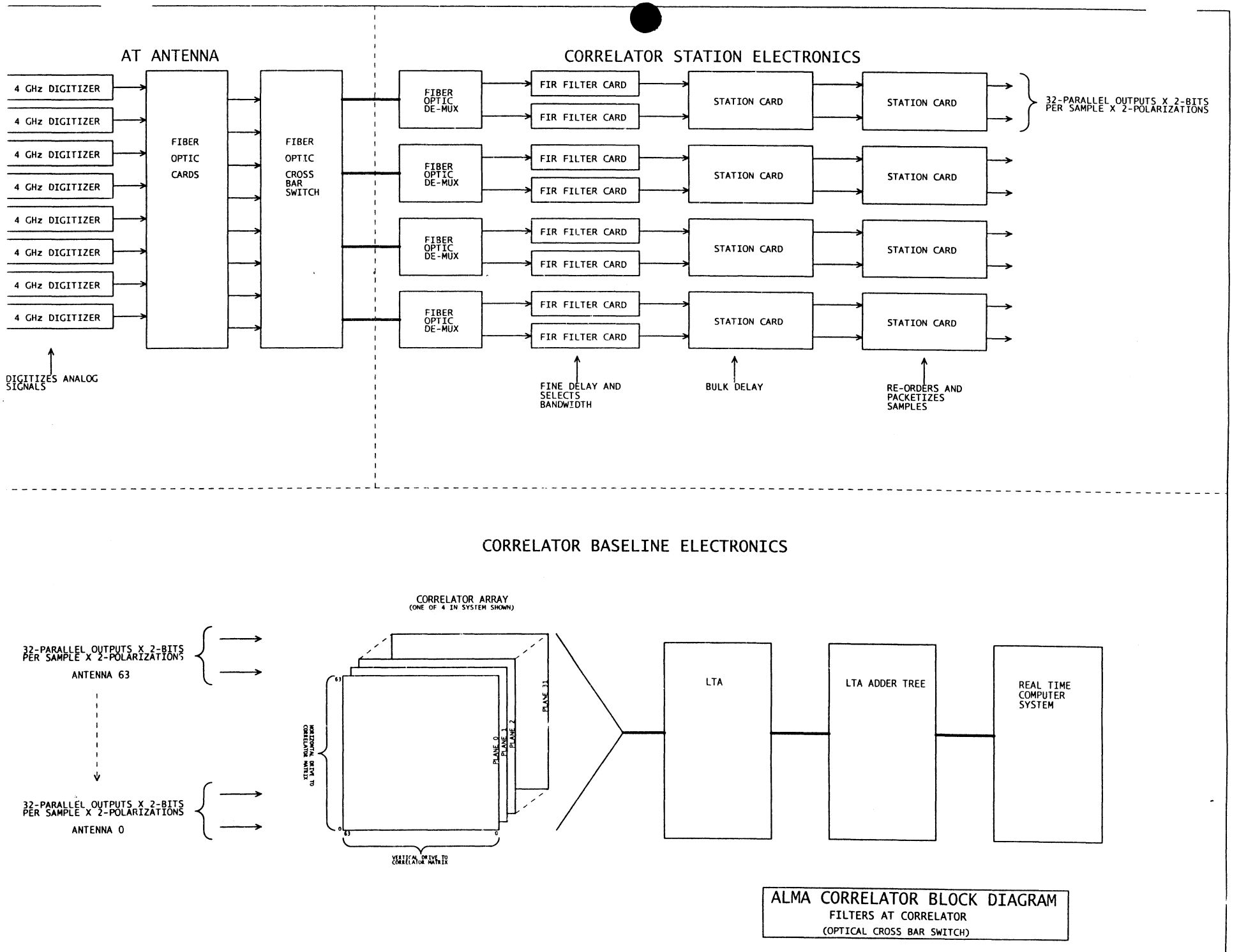

REQUIRES NO CONNECTION TO OTHER QUADRANTS

# ANTENNA ELECTRONICS BIN




DUAL 10.5 INCH BY SINGLE 19 INCH BIN
WITH A SINGLE 21 BY 19 INCH BACKPLANE

CARD SPACING = 1 INCH



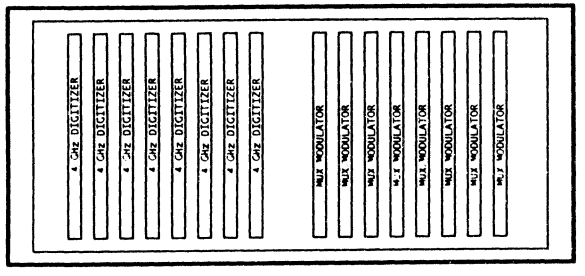

ALMA CORRELATOR BLOCK DIAGRAM
FILTERS AT CORRELATOR
(OPTICAL CROSS BAR SWITCH)

# FILTERS AT CORRELATOR

WITH OPTICAL CROSS BAR SWITCH

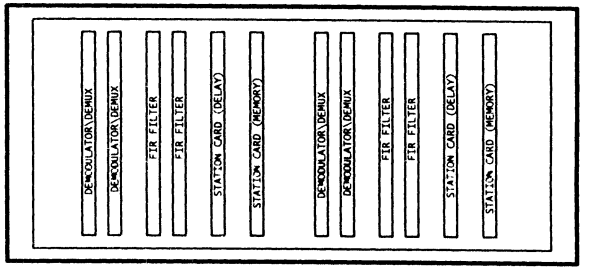
## ANTENNA ELECTRONICS BIN

1 REQD. PER ANTENNA




## CORRELATOR STATION ELECTRONICS BIN

128 REQUIRED IN 32 RACKS (AT 4 BINS PER RACK)

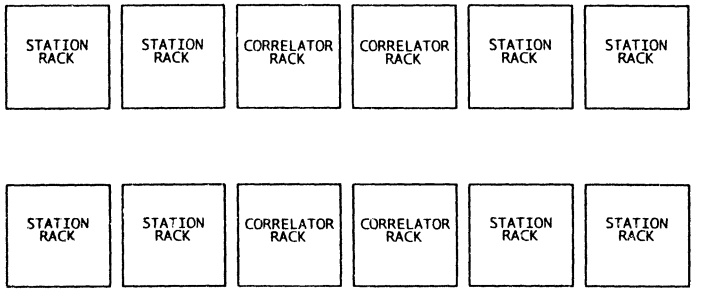



TWO BB OUTPUTS OF TWO ANTENNAS

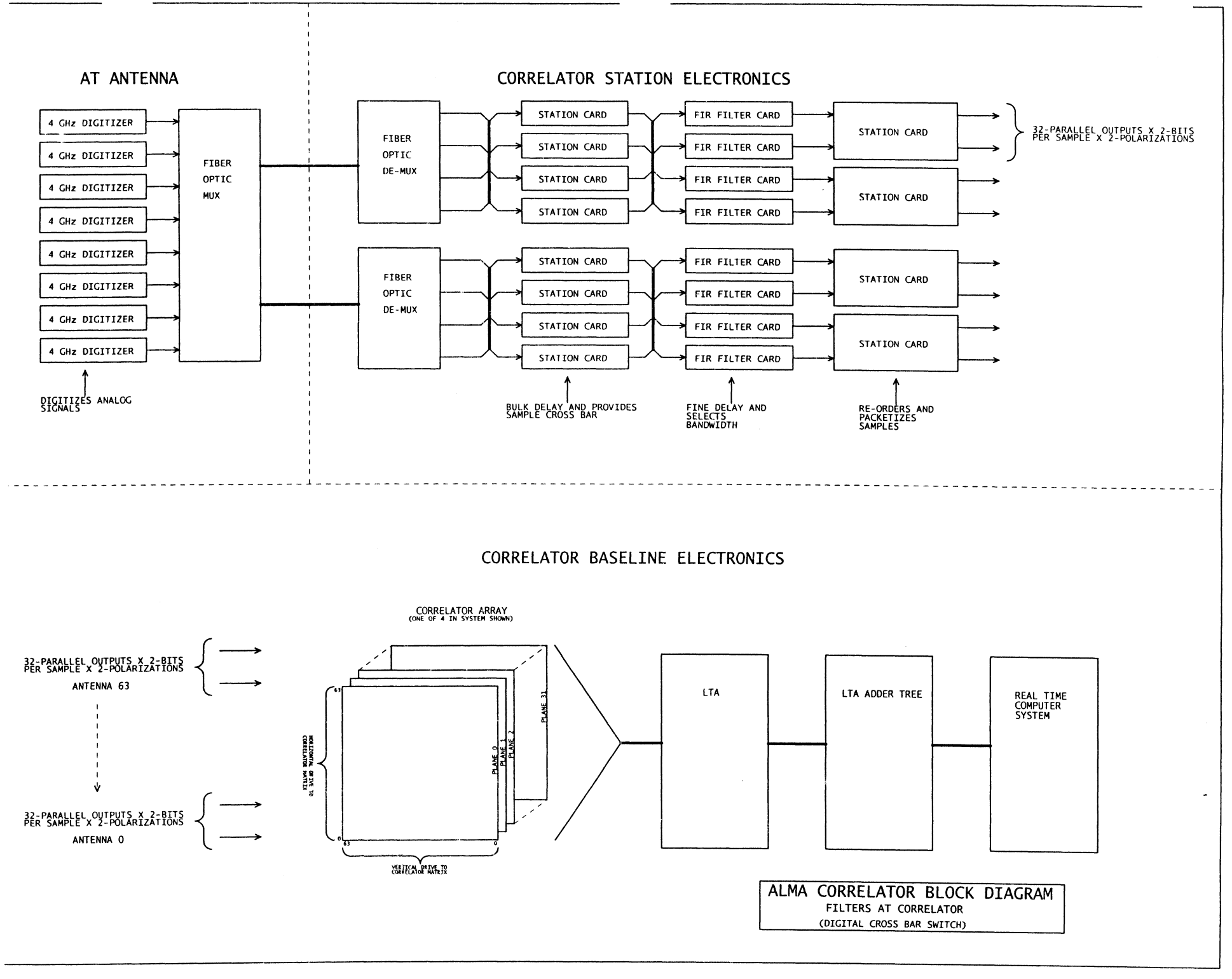
## ONE CORRELATOR QUADRANT

RACK FLOOR PLAN

48 RACKS IN FINAL SYSTEM




REQUIRES NO CONNECTION TO OTHER QUADRANTS

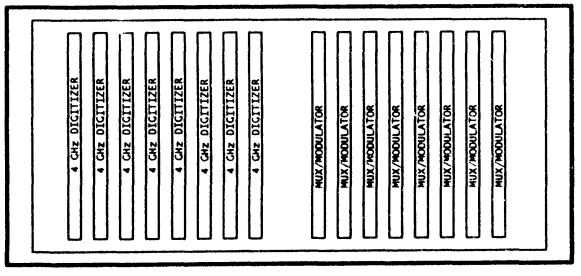

AT ANTENNA
CORRELATOR STATION ELECTRONICS
4 GHz DIGITIZER
FIBER OPTIC MUX
FIBER OPTIC DE-MUX
STATION CARD
FIR FILTER CARD
32-PARALLEL OUTPUTS X 2-BITS PER SAMPLE X 2-POLARIZATIONS
DIGITIZES ANALOG SIGNALS
BULK DELAY AND PROVIDES SAMPLE CROSS BAR
FINE DELAY AND SELECTS BANDWIDTH
RE-ORDERS AND PACKETIZES SAMPLES
CORRELATOR BASELINE ELECTRONICS
CORRELATOR ARRAY
(ONE OF 4 IN SYSTEM SHOWN)
32-PARALLEL OUTPUTS X 2-BITS PER SAMPLE X 2-POLARIZATIONS
ANTENNA 63
ANTENNA 0
HORIZONTAL DRIVE TO CORRELATOR MATRIX
VERTICAL DRIVE TO CORRELATOR MATRIX
PLANE 0
PLANE 1
PLANE 2
PLANE 31
LTA
LTA ADDER TREE
REAL TIME COMPUTER SYSTEM
ALMA CORRELATOR BLOCK DIAGRAM
FILTERS AT CORRELATOR
(DIGITAL CROSS BAR SWITCH)

# FILTERS AT CORRELATOR

WITH DIGITAL CROSS BAR SWITCH

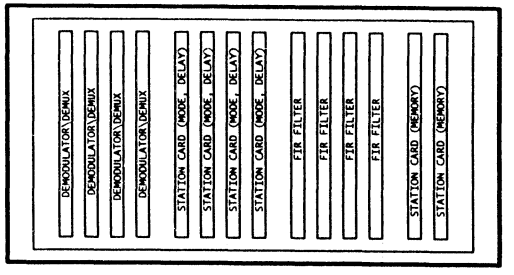
## ANTENNA ELECTRONICS BIN

1 REQD. PER ANTENNA




## CORRELATOR STATION ELECTRONICS BIN

128 REQUIRED IN 32 RACKS (AT 4 BINS PER RACK)

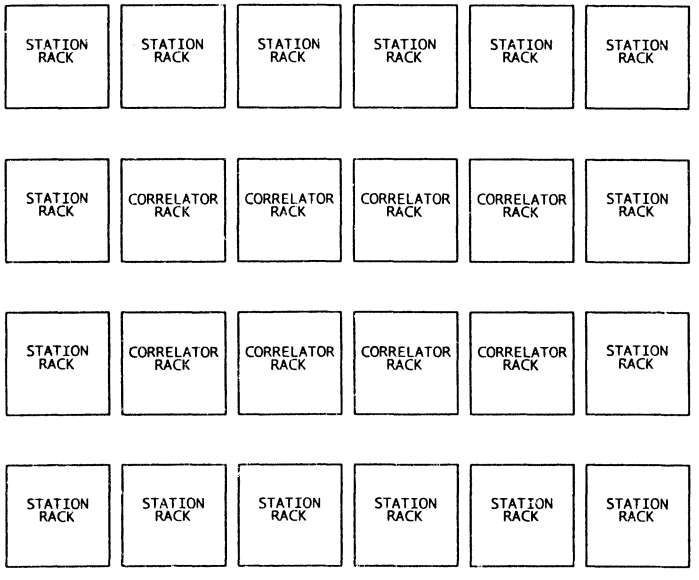



FOUR BB OUTPUTS OF ONE ANTENNA

## TWO CORRELATOR QUADRANTS

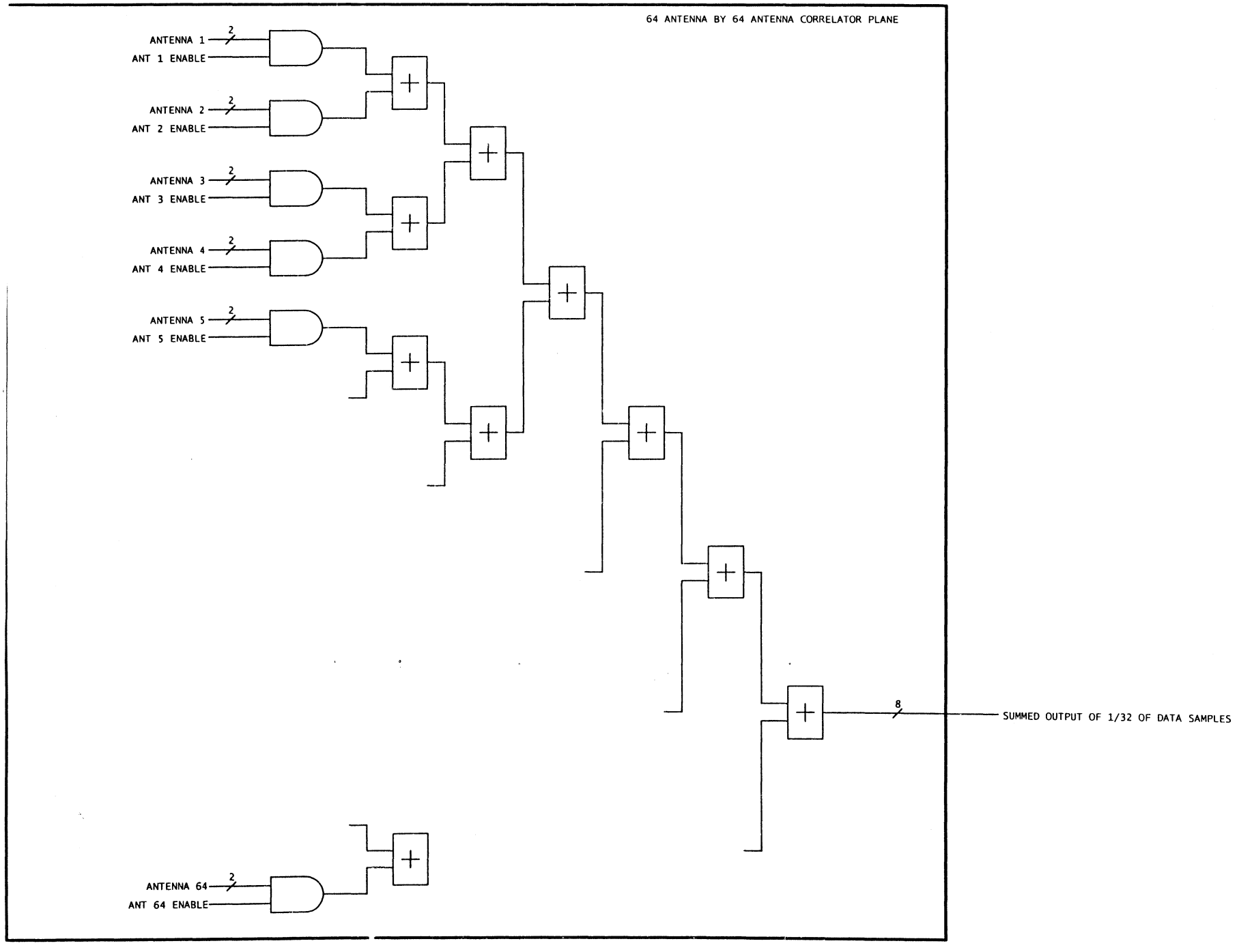
### RACK FLOOR PLAN

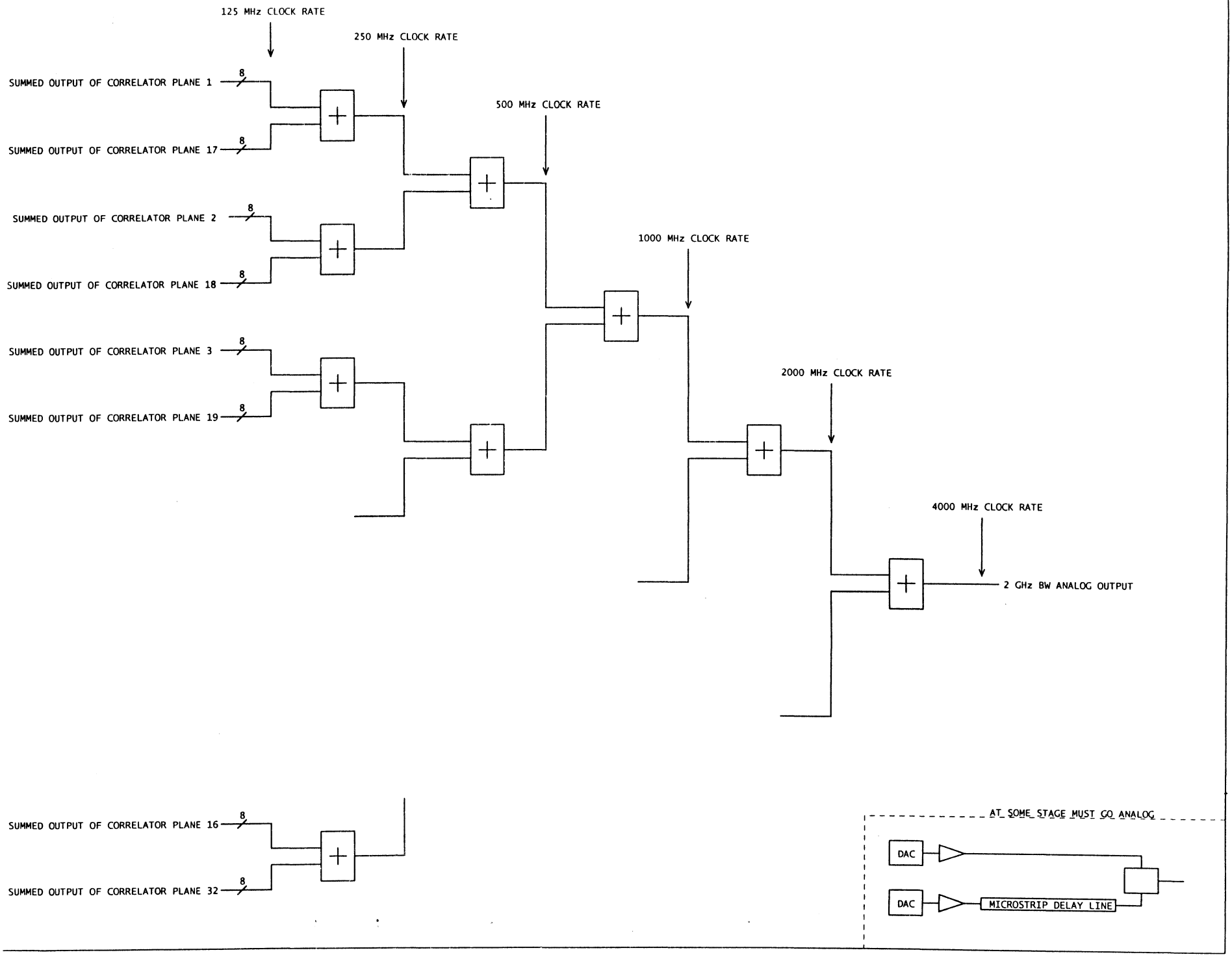
48 RACKS IN FINAL SYSTEM



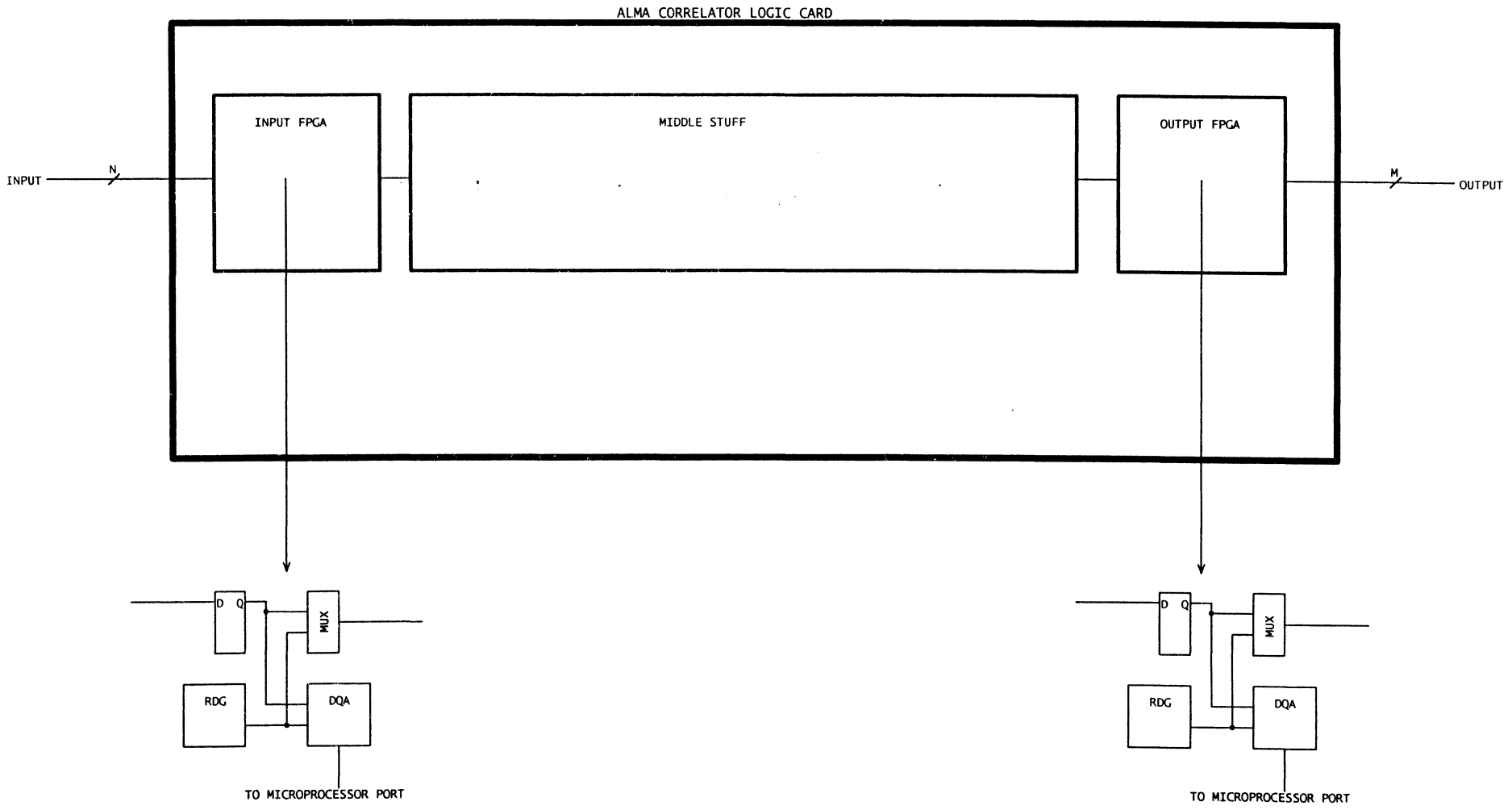

REQUIRES NO CONNECTION TO OTHER TWO QUADRANTS

(HAS PERFORMANCE PENALTY)

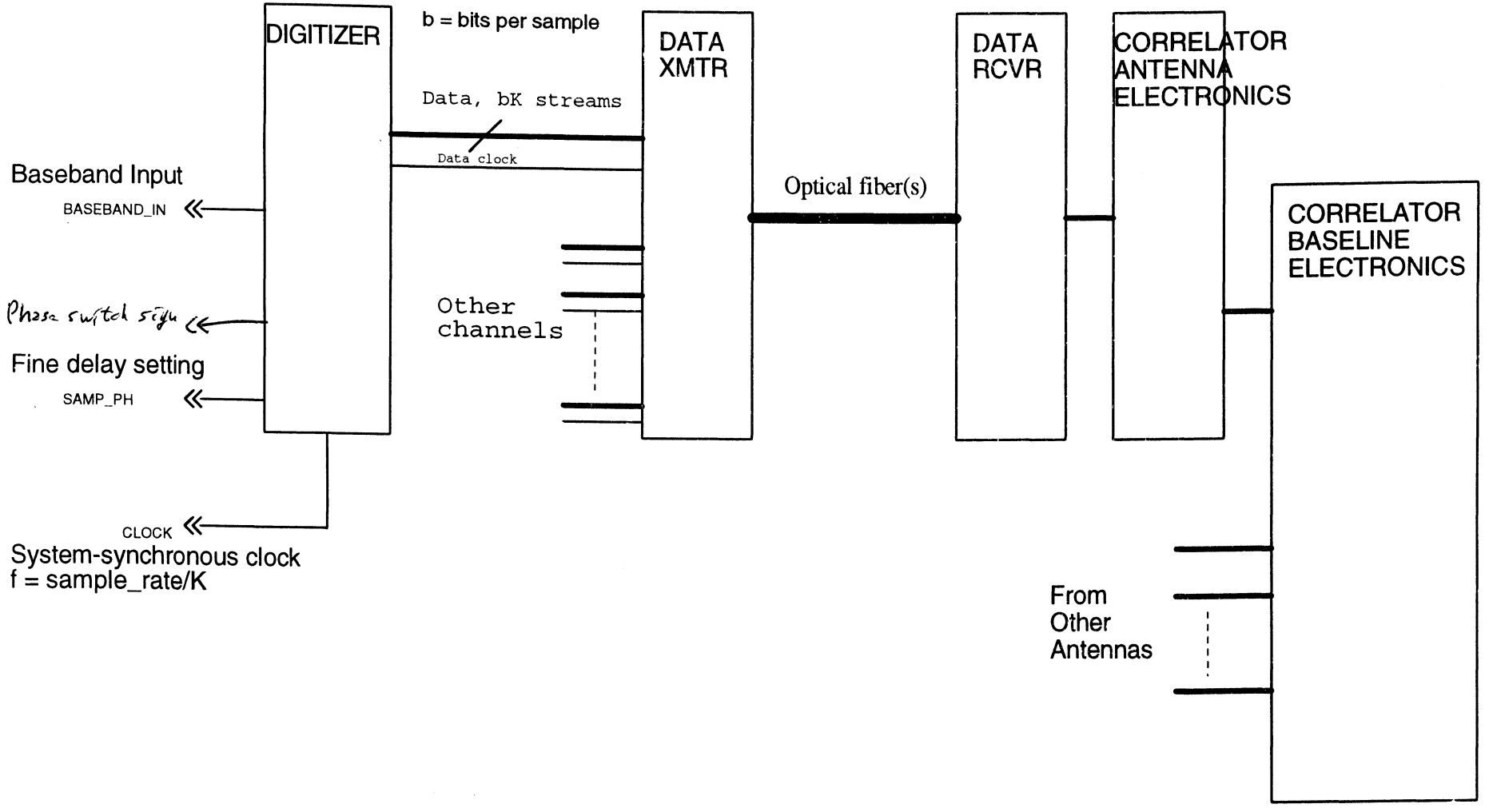

64 ANTENNA BY 64 ANTENNA CORRELATOR PLANE
ANTENNA 1
ANT 1 ENABLE
ANTENNA 2
ANT 2 ENABLE
ANTENNA 3
ANT 3 ENABLE
ANTENNA 4
ANT 4 ENABLE
ANTENNA 5
ANT 5 ENABLE
ANTENNA 64
ANT 64 ENABLE
2
8
SUMMED OUTPUT OF 1/32 OF DATA SAMPLES


125 MHz CLOCK RATE
250 MHz CLOCK RATE
500 MHz CLOCK RATE
1000 MHz CLOCK RATE
2000 MHz CLOCK RATE
4000 MHz CLOCK RATE
SUMMED OUTPUT OF CORRELATOR PLANE 1
SUMMED OUTPUT OF CORRELATOR PLANE 17
SUMMED OUTPUT OF CORRELATOR PLANE 2
SUMMED OUTPUT OF CORRELATOR PLANE 18
SUMMED OUTPUT OF CORRELATOR PLANE 3
SUMMED OUTPUT OF CORRELATOR PLANE 19
SUMMED OUTPUT OF CORRELATOR PLANE 16
SUMMED OUTPUT OF CORRELATOR PLANE 32
8
2 GHz BW ANALOG OUTPUT
AT SOME STAGE MUST GO ANALOG
DAC
DAC
MICROSTRIP DELAY LINE

# CORRELATOR SELF



# ALMA Digitizer -- System Context

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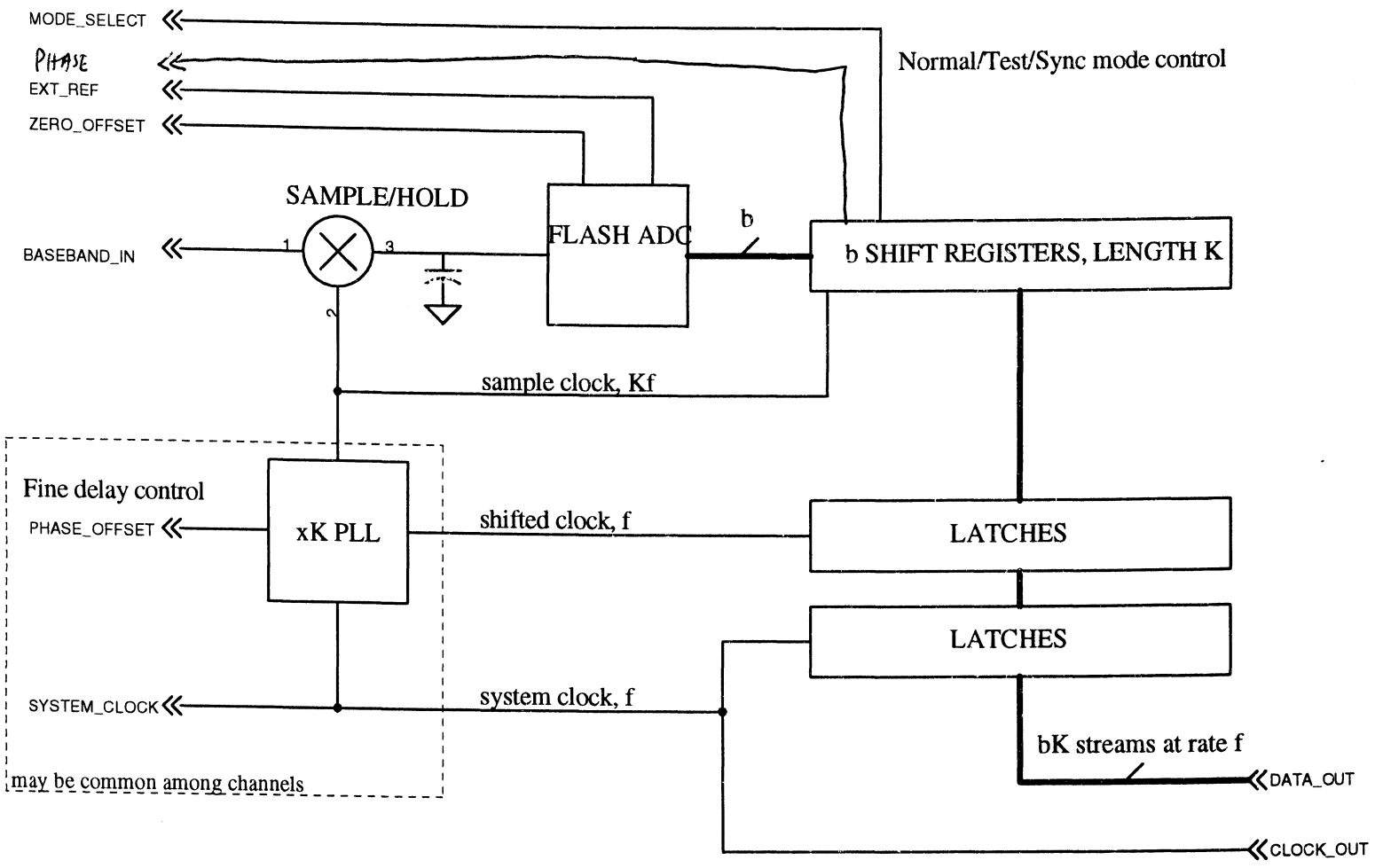
# Alma Digitizer -- Module Level Block Diagram



# ALMA DIGITIZER: MODULE LEVEL SPECIFICATIONS

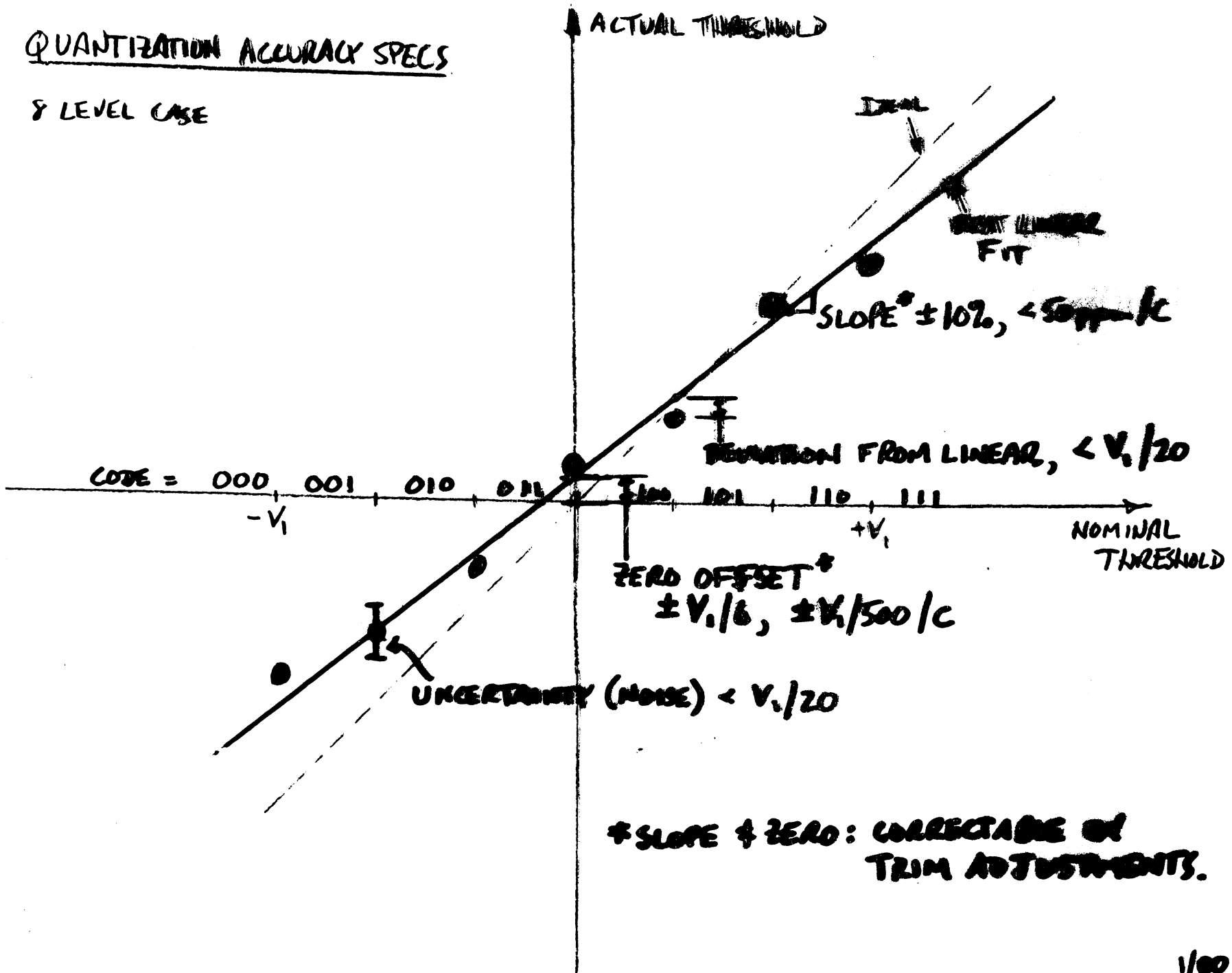
| | |
|---|---|
| o Input signal band | 2.0 to 4.0 GHz |
| o Sample rate | fs = 4.0 Gsamp/sec |
| o Aperture time | 50 psec max [-0.58dB @ 4 GHz] |
| o Sample time stability | 1 psec max rms jitter in 10s<br>1 psec/C max temperature coef. |
| o Quantization levels | 8 min, 16 preferred |
| o Quantization thresholds | Uniformly spaced, incl zero V (see separate sheet for accuracy) |
| o Systematic effects (incl clock feedthrough) | Included in accuracy, but avoid as much as possible |
| o Sample encoding | offset binary (no zero) |
| o Output demultiplexing factor | K = <TBD> (32?) |
| o Input clock | fclk = fs/K, constant phase |

Alternative: variable phase in addition to fixed phase, both at fs/K.

| | |
|---|---|
| o Sampling phase control | resolution <25 psec (36 deg at 4 GHz, 36/K deg at fclk)<br><br>accuracy <5 psec (7d) |

# QUANTIZATION ACCURACY SPECS

8 LEVEL CASE




*SLOPE & ZERO: CORRECTABLE BY TRIM ADJUSTMENTS.

1/00 LAB

# DELAY ERROR

$D = (B/c) \sin h \cos d$
$dD/dt = (B\ omega_e / c) \cos h \cos d$

| | |
|---|---|
| Maximum delay rate for B = 10 km: | 2.426e-9 (sec/sec) |
| Sample period @ 4 Gsamp/sec | 2.5e-10 sec |
| => minimum time per delay step | 0.1 sec |
| If fine delay setting uses PLL with 1 MHz bandwidth, settling time after step change will be about | 5e-6 sec |
| So delay will be wrong by 1 sample about of the time. | 5e-5 or .005% |

Conclusion: THIS SHOULD BE ACCEPTABLE.

# DESIGN CONSIDERATIONS AND OPEN QUESTIONS

- Sample or quantize first?
- Demulitplexing factor:

| | Clock | Stream/channel @ b=3 | Total streams @ b=3 |
|---|---|---|---|
| K=32 -> | 125 MHz | 96 | 768 |
| K=16 -> | 250 MHz | 48 | 384 |
| K=8 -> | 500 MHz | 24 | 192 |

- Common fine delay (sample phase) among channels, or separate?
- Is uniform threshold spacing acceptable? Do we need "tweaks" for thresholds or is it best to use on-chip precision divider?
- Should digitizer be bipolar internally, or use d.c. offset? (Will be a.c. coupled at baseband input.)
- Packaging:
  - How many digitizers per module?
  - Include digitizer with data transmitter?

JAN 1966: PROC IEEE 54:1, pp 2-19

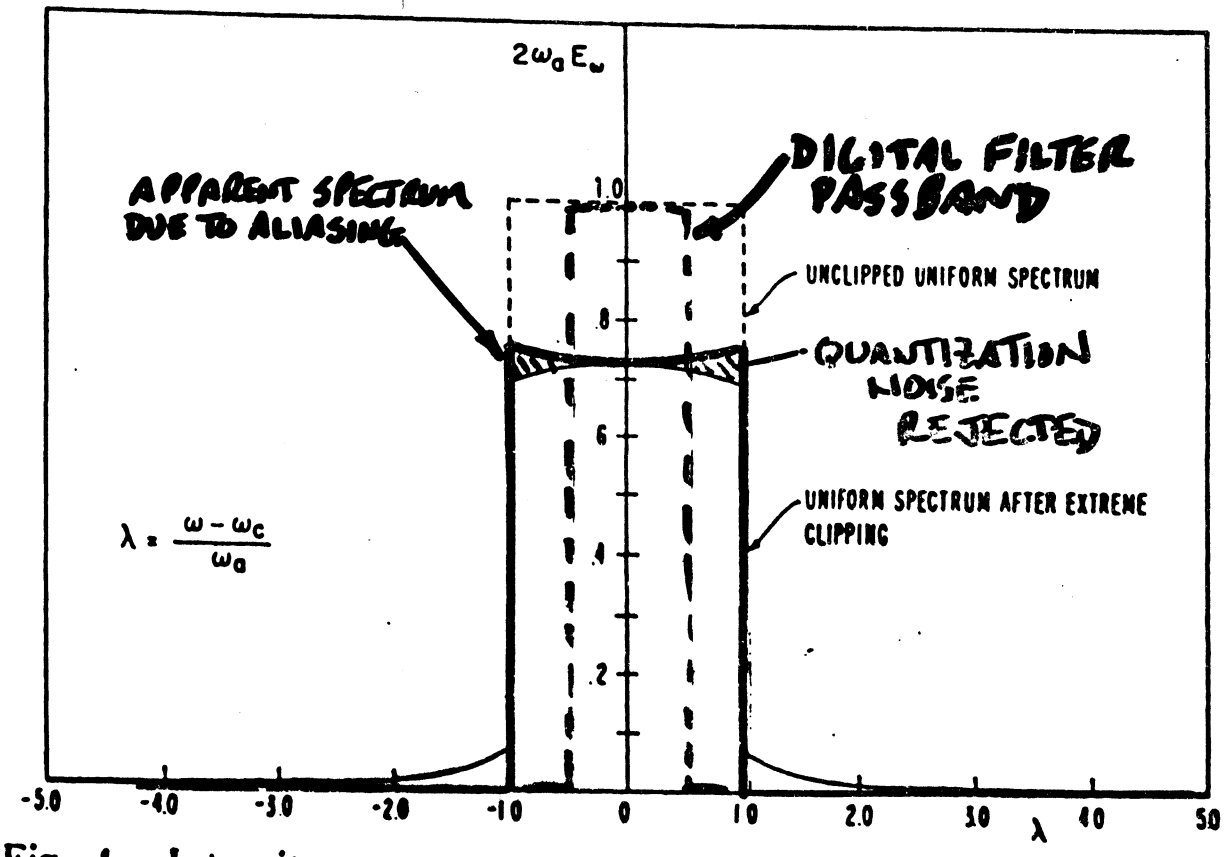
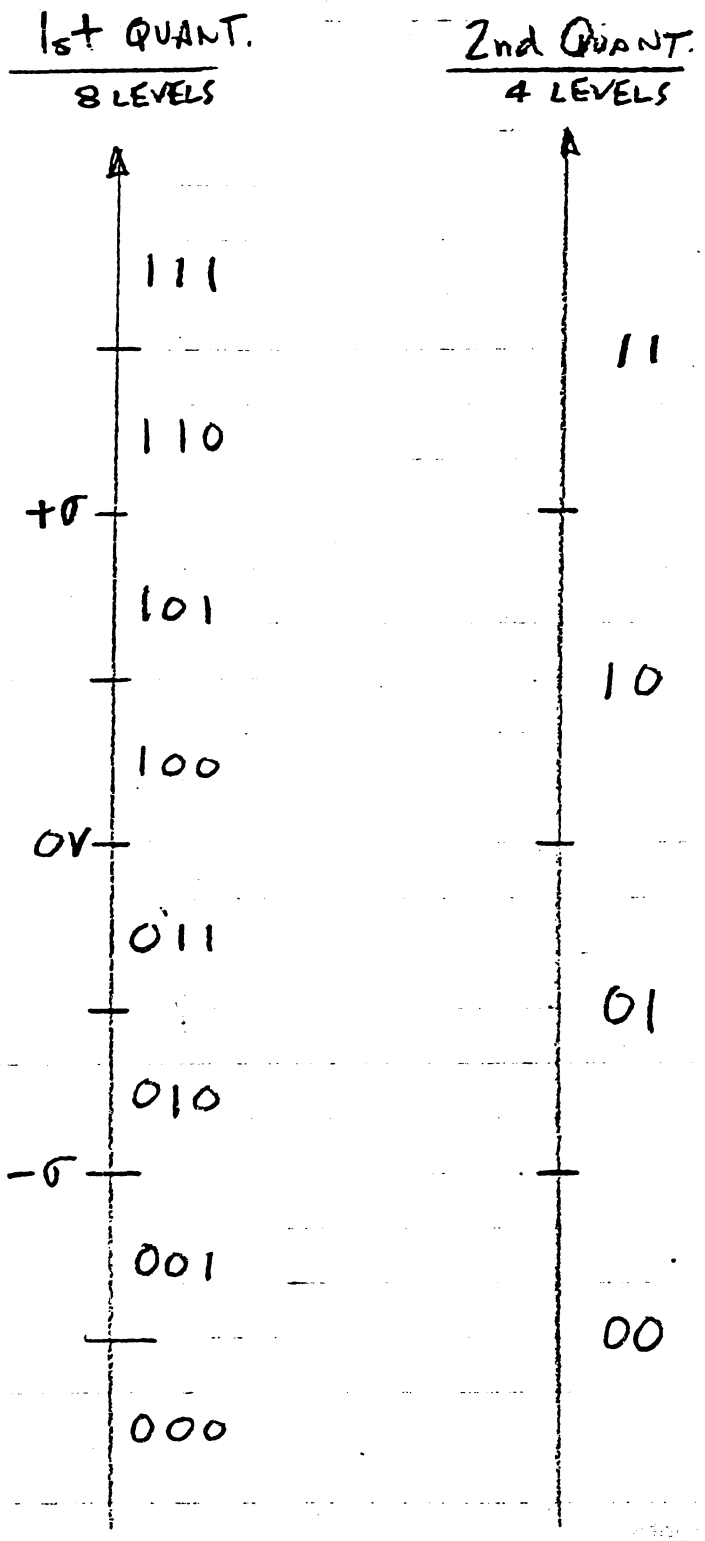



Fig. 4. Intensity spectrum of DINA (i.e., narrow-band normal noise) after extreme clipping, when the original spectrum is rectangular [Case (A)].




ALONE : 0.965 ALONE : 0.878

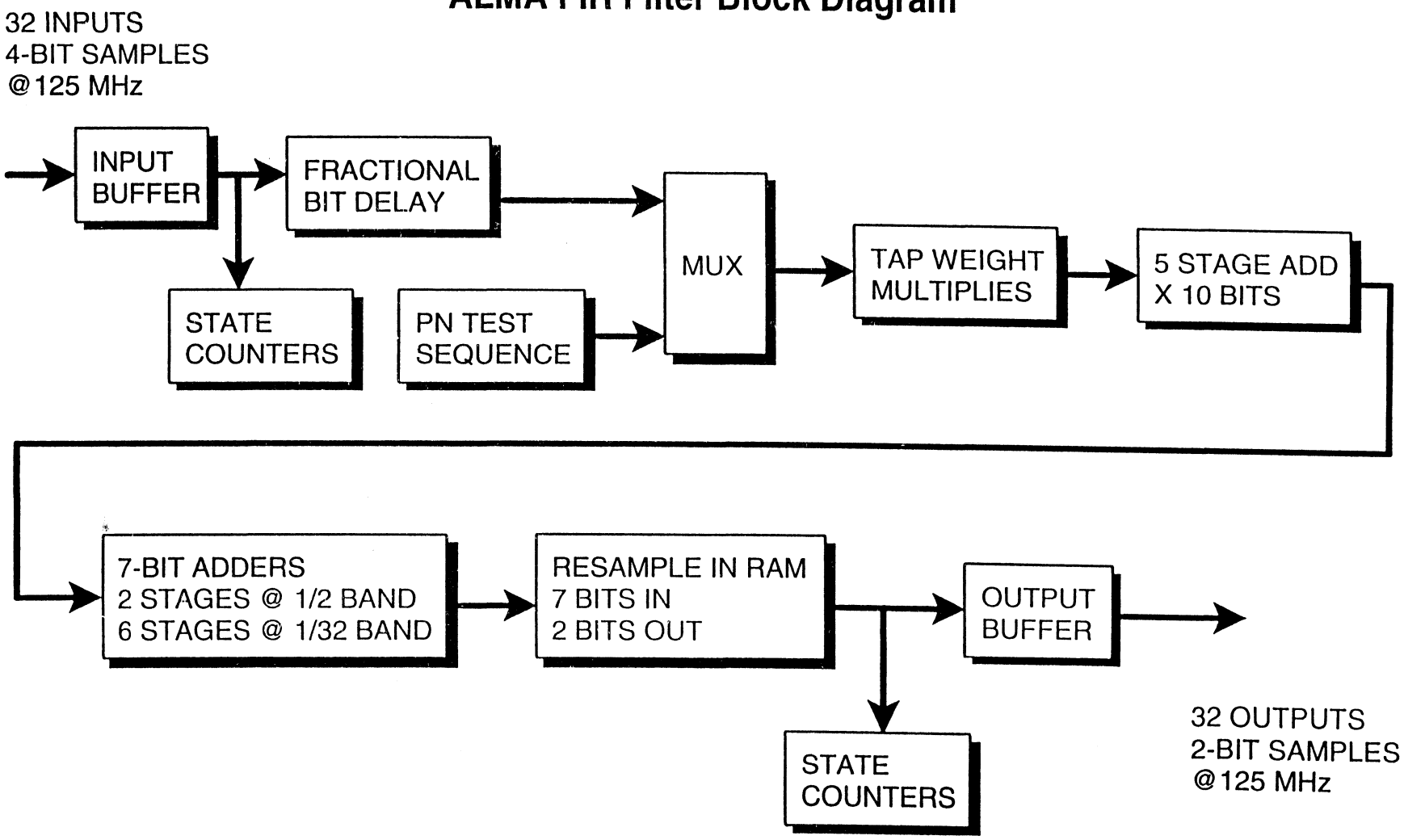
TOGETHER : 0.878

# ALMA CORRELATOR DIGITAL FILTER

- 4 GSAMPLE/SEC, 4-BIT QUANTIZATION INPUTS
- 128 TAPS AT 1/2 BANDWIDTH
- DOUBLE NUMBER OF TAPS FOR EACH FACTOR OF 2 REDUCTION IN OUTPUT BW (TO 32)
- 2048 TOTAL TAPS
- 10-BIT ARITHMETIC (7-BITS AT END OF ADDER TREE)
- RE-SAMPLE TO 2-BITS IN LOOK-UP TABLE RAM
- INPUT STATE COUNTERS
- OUTPUT STATE COUNTERS
- ESTIMATED TIME TO LOAD FPGA PERSONALITIES, 48 MSEC
- ESTIMATED TIME TO LOAD 2048 TAP WEIGHT TABLES, 20 MSEC

1-20-00
Weber

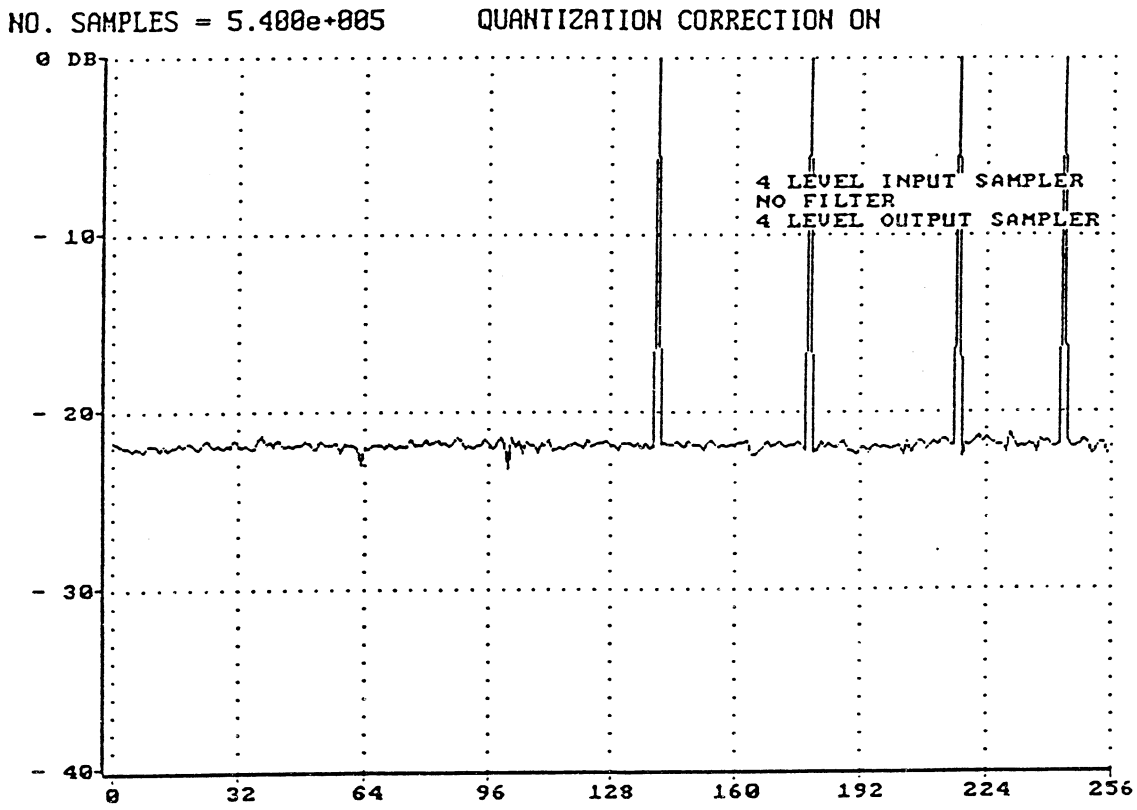
# ALMA FIR Filter Block Diagram



MEMO 248

# Simulated input signal

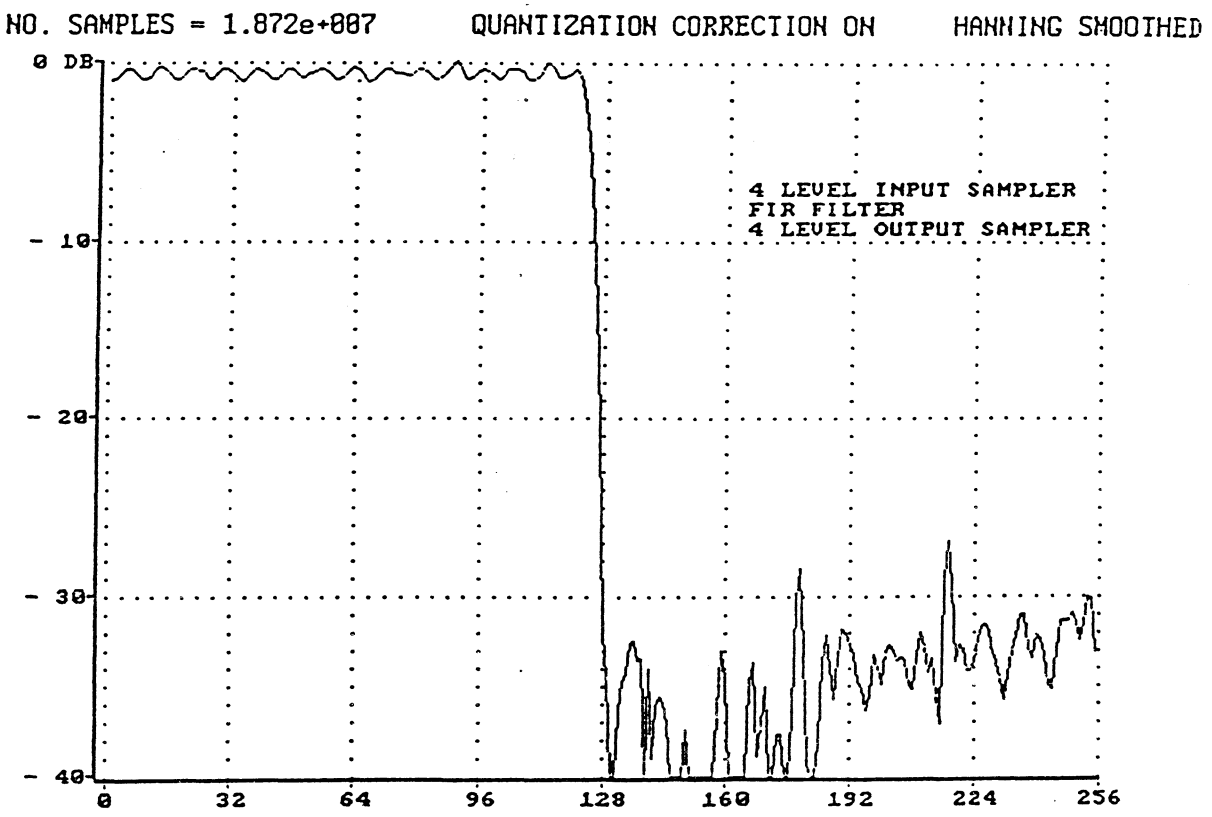
+22 dB spectral lines at
1.09, 1.40, 1.69, 1.19 GHz



MEMO 248

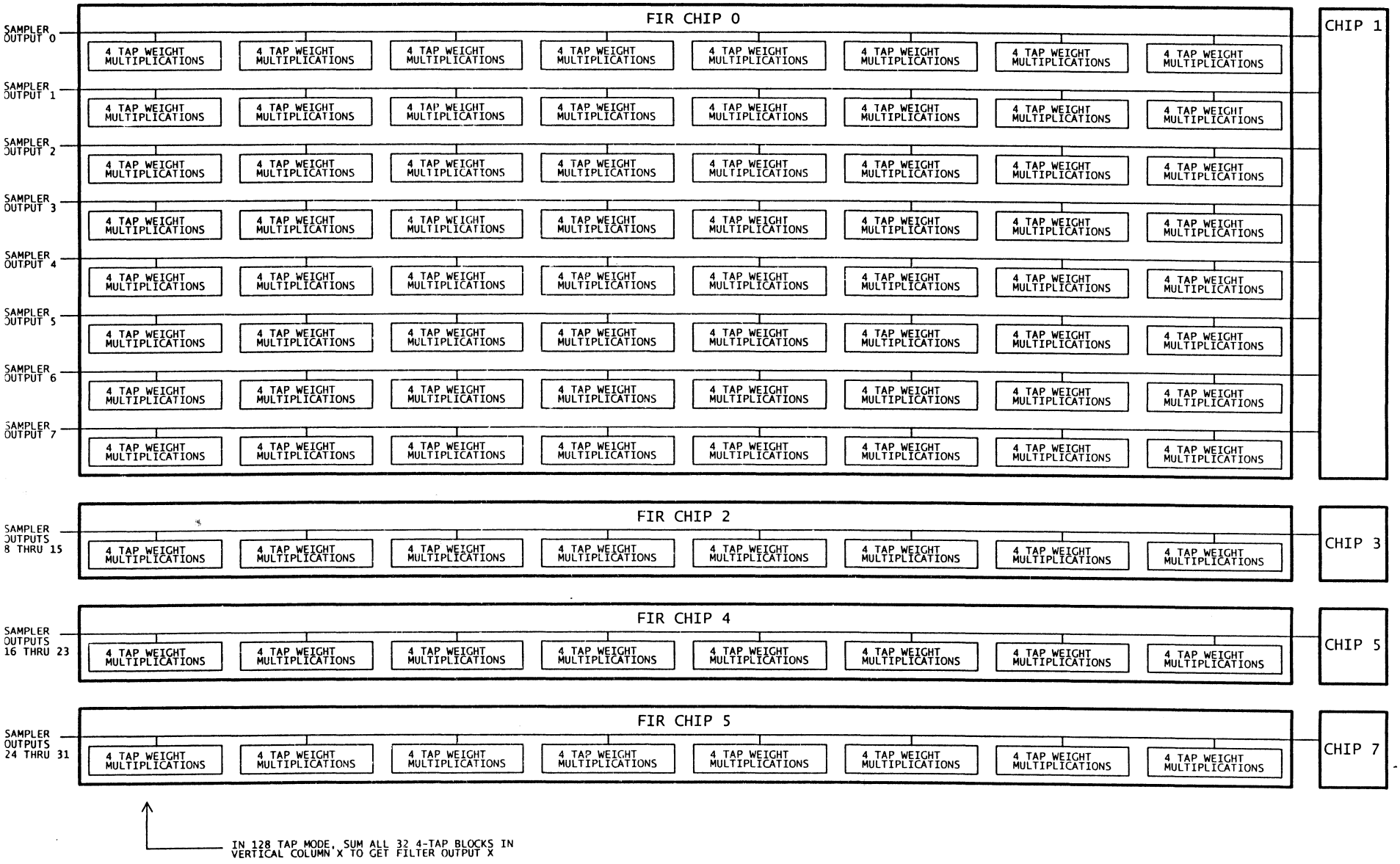
# Simulated Performance

## 1 GHz low pass filter

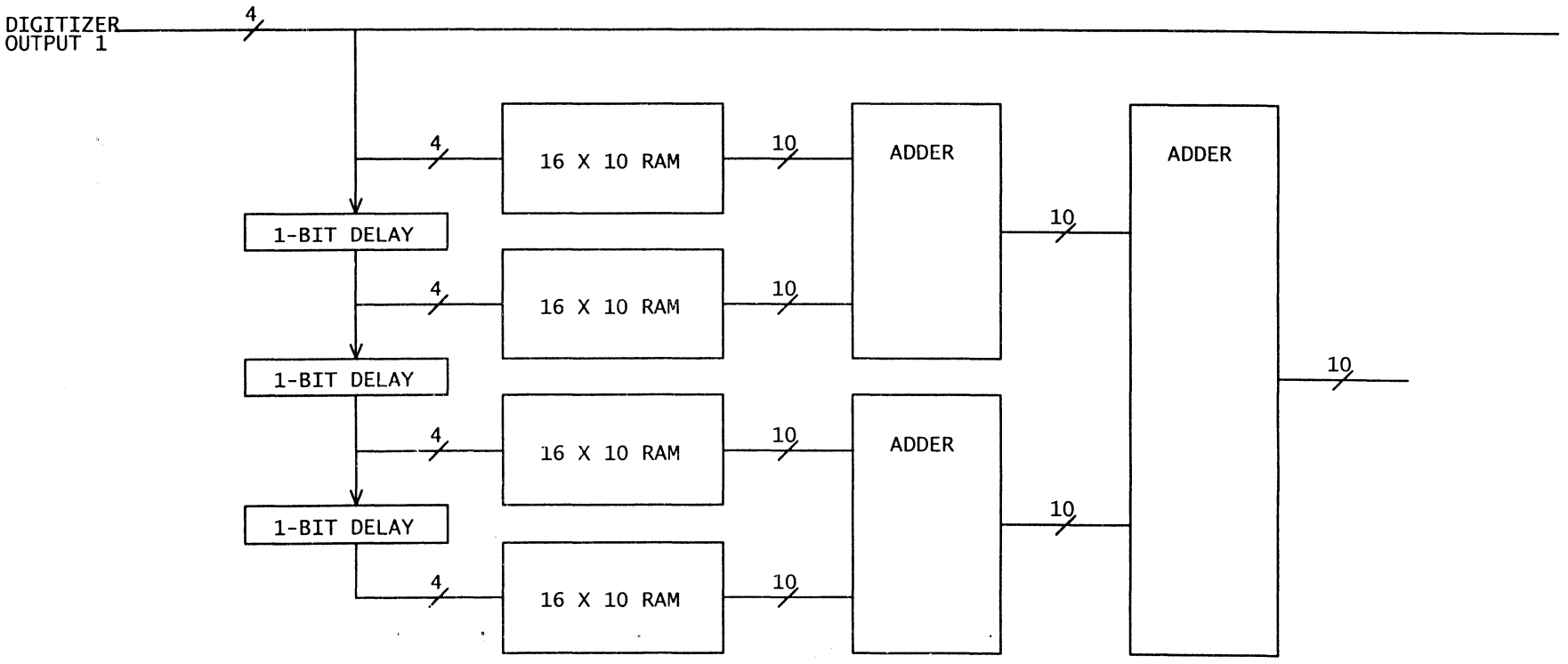


# FILTER CARD BLOCK DIAGRAM

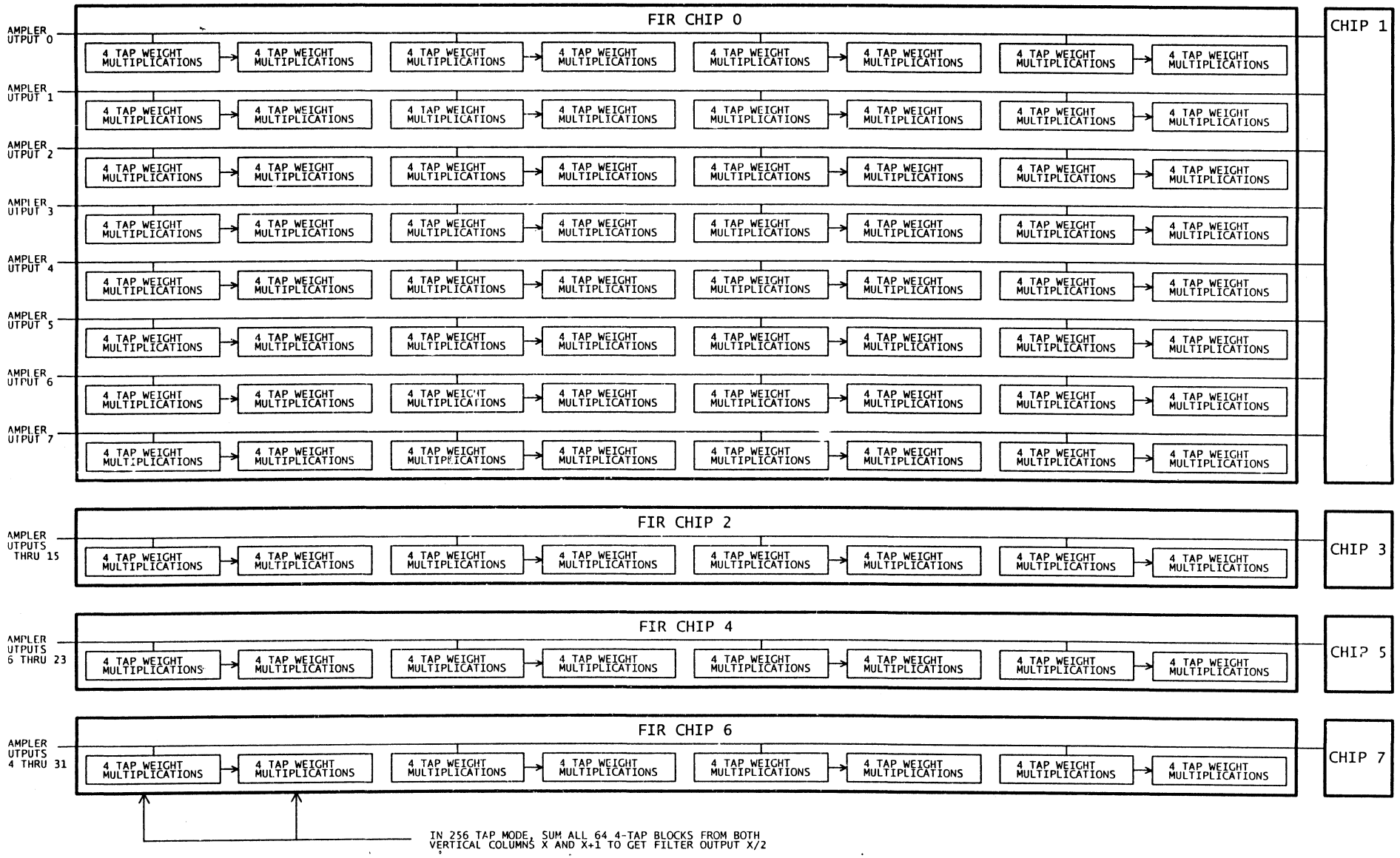
# FILTER CARD PROGRAMMED AS 1/2 BAND FILTER



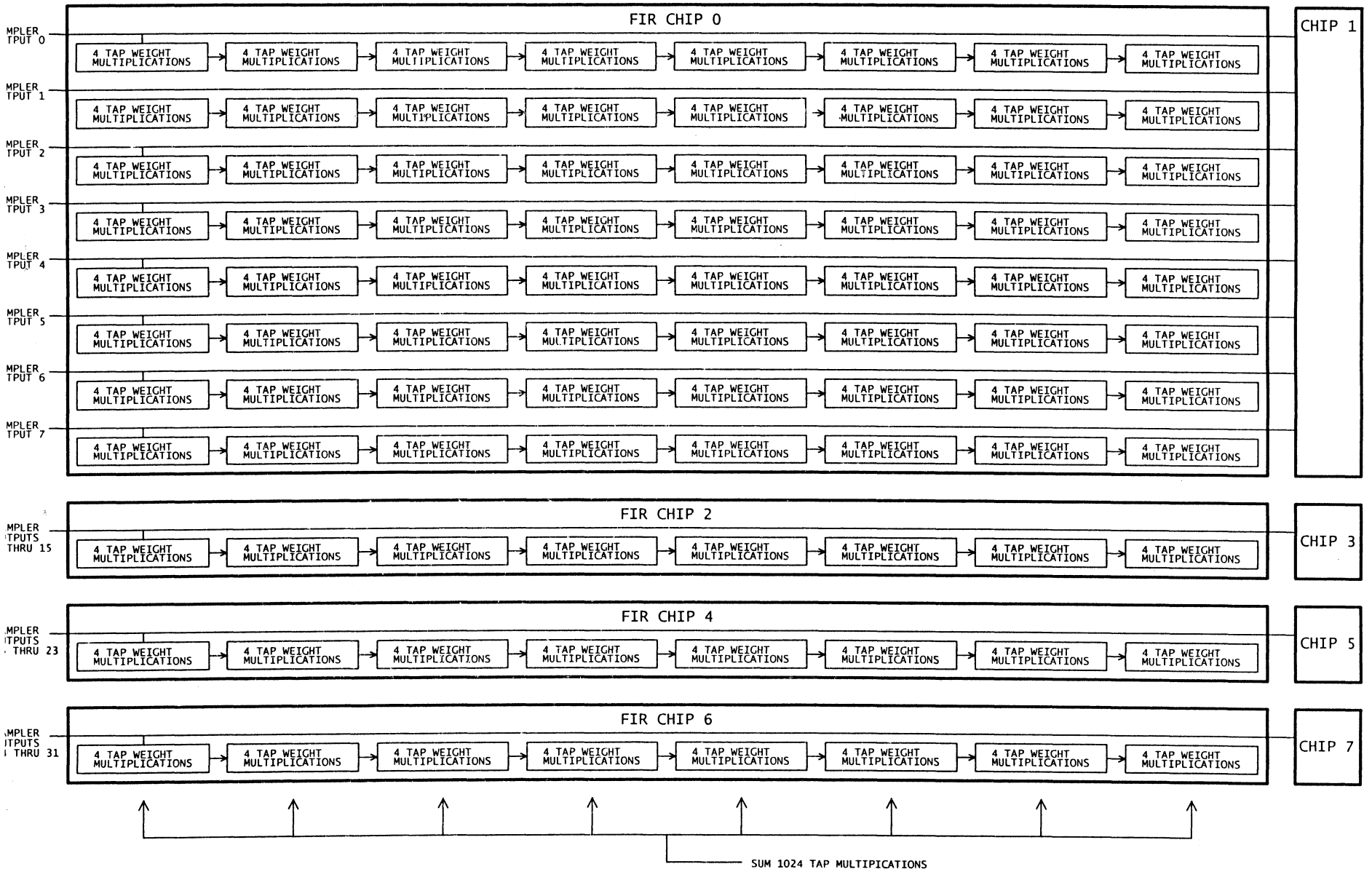
4 TAP MULTIPLIES FOR FIR OUTPUT 1



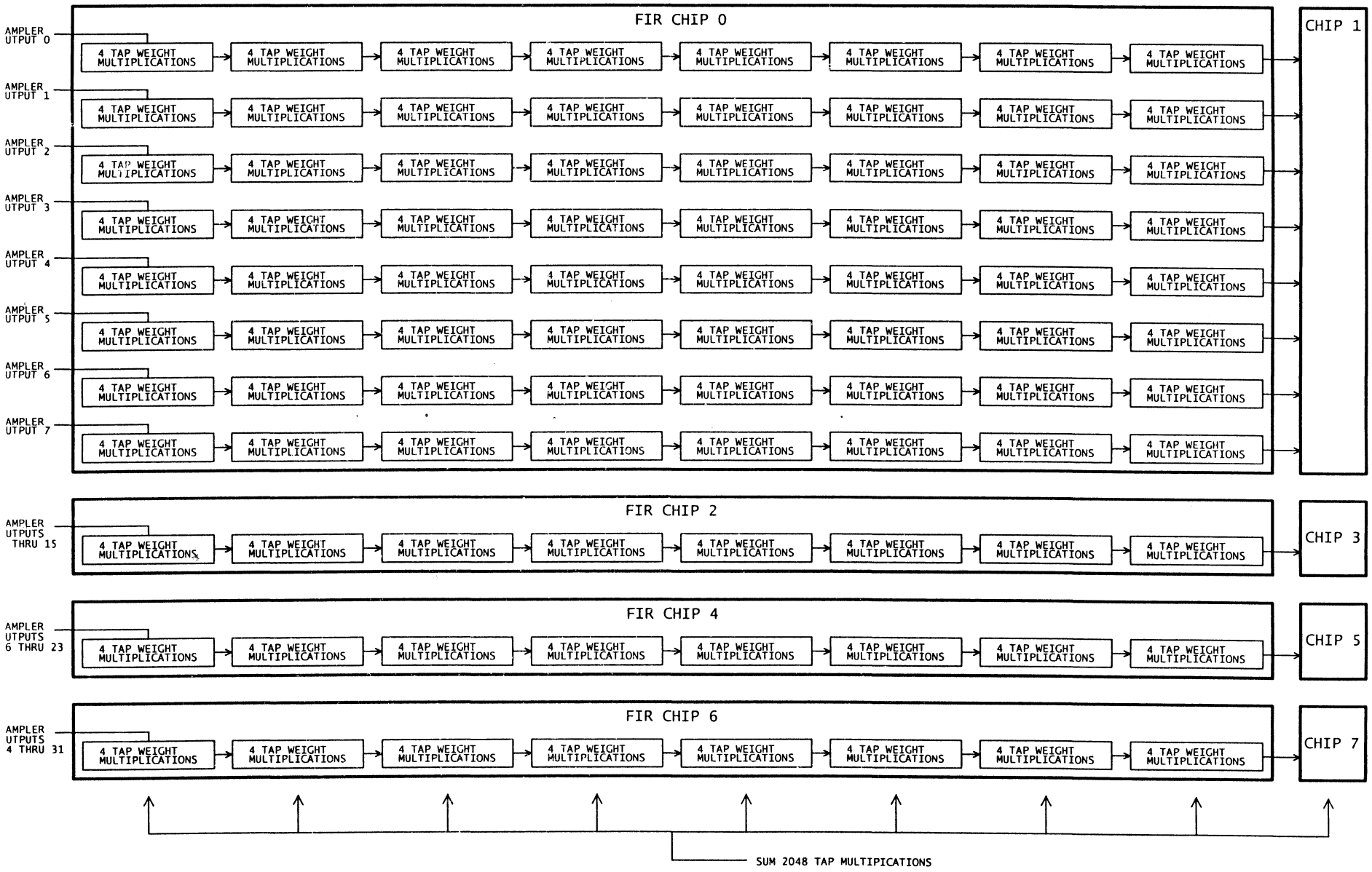
# FILTER CARD PROGRAMMED AS 1/4 BAND FILTER

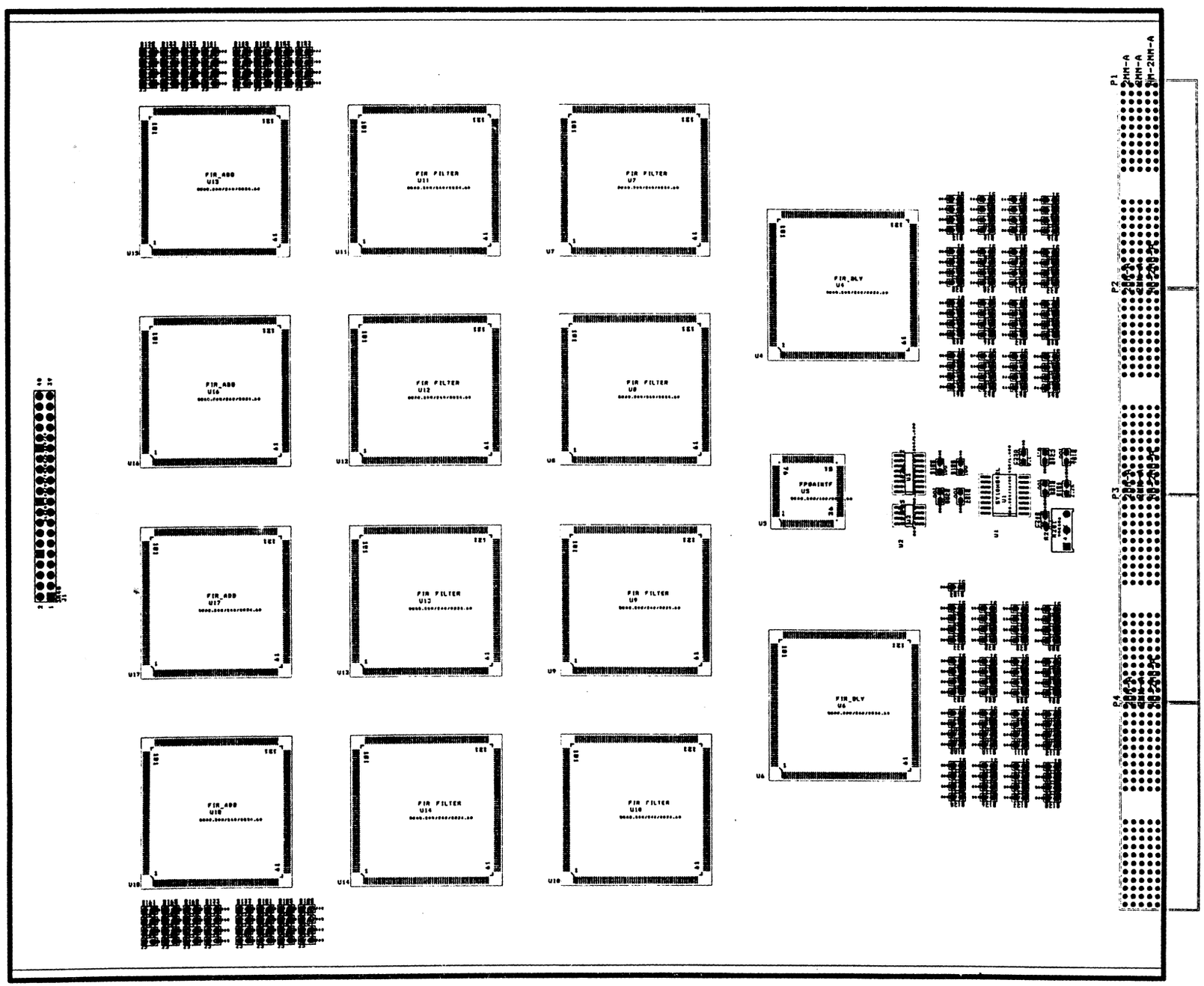


# FILTER CARD PROGRAMMED AS 1/16 BAND FILTER



# FILTER CARD PROGRAMMED AS 1/32 BAND FILTER




FIR_ADD
U13
FIR_ADD
U16
FIR_ADD
U17
FIR_ADD
U18
FIR FILTER
U11
FIR FILTER
U12
FIR FILTER
U12
FIR FILTER
U14
FIR FILTER
U7
FIR FILTER
U8
FIR FILTER
U9
FIR FILTER
U10
FIR_DLY
U4
FIR_DLY
U6
FPGAINTF
U5
P1
P2
P3
P4
J1

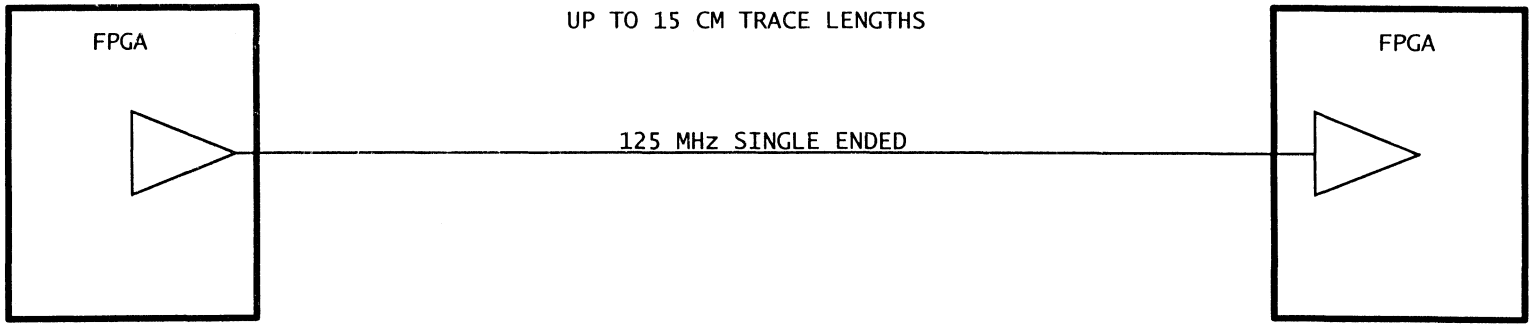
# ALMA CORRELATOR 125 MHz SIGNAL INTERFACES

- NUMBER OF RACK-TO-RACK INTERFACES OVER COAX OR TWIN-AX CABLES: 32,768
- NUMBER OF CARD-TO-CARD INTERFACES OVER BACKPLANES: 294,912
- NUMBER OF CHIP-TO-CHIP INTERFACES ON PRINTED CIRCUIT CARD RUNS: 2,500,000

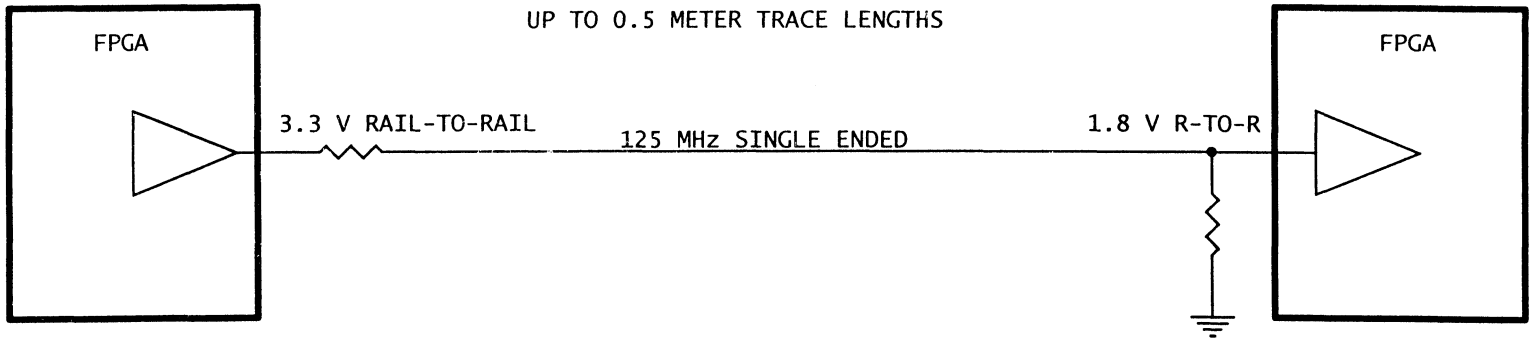
Webber

1-20-00

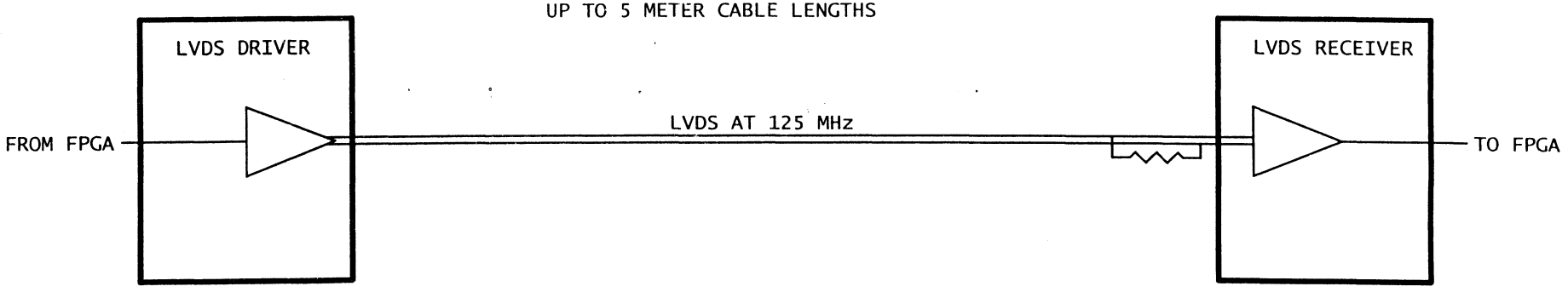
## CHIP TO CHIP CONNECTIONS ON A PRINTED CIRCUIT CARD



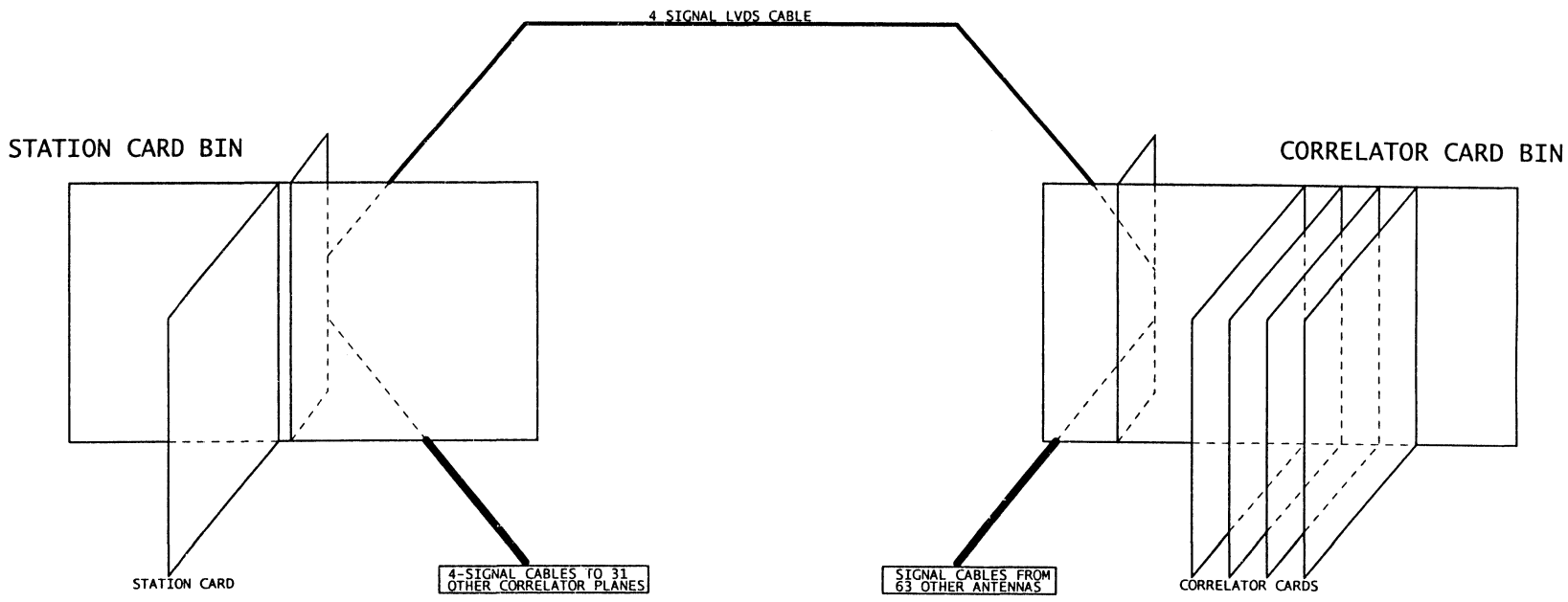

## CARD TO CARD CONNECTIONS OVER A BACKPLANE




## RACK TO RACK CONNECTIONS OVER CABLES



# RACK TO RACK DATA CABLING




128 SINGLE ENDED 125 MHz DATA INTERFACES FROM STATION CARD TO PADDLE BOARD

768 SINGLE ENDED 125 MHz DATA INTERFACES FROM PADDLE BOARD TO CORRELATOR CARDS VIA BACKPLANE

# Cost of Signal Cables in the ALMA Correlator

The prices below are based on a non-competitive cost estimate from Tensolite. Two basic cables were priced;

4-signal single ended cable 10 feet long (one wafer) $22.52
4-signal differential cable 10 feet long (two wafers) $37.70

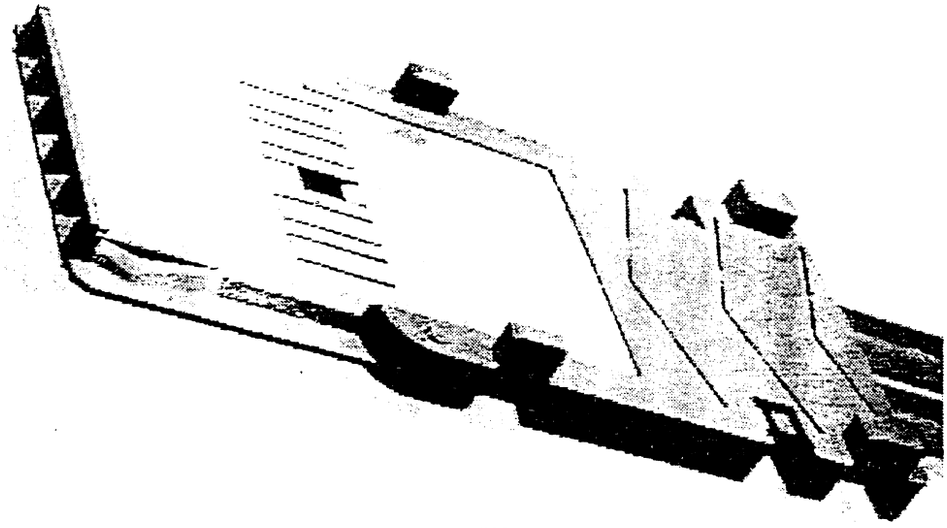
Both prices are for 1000 quantity purchases.

| data rate | transmission type | number of 4-signal cables required | total cost |
|---|---|---|---|
| 125 MHz | single ended | 8192 | $184K |
| 125 MHz | LVDS differential | 8192 | $309K |
| 250 MHz | LVDS differential | 4096 | $154K |
| 500 MHz | LVDS differential* | 2048 | $ 77K |

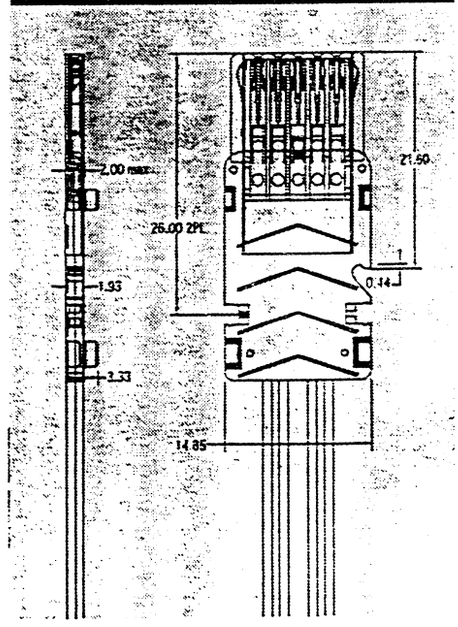
* using Altera driver/recivers

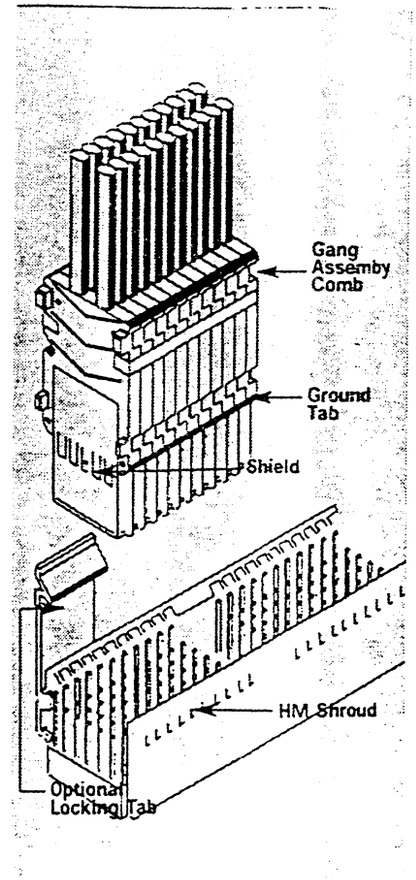
# 2MM HIGH-SPEED CABLE INTERCONNECT-TO-BACKPLANE SYSTEM

ISO 9001 CERTIFIED

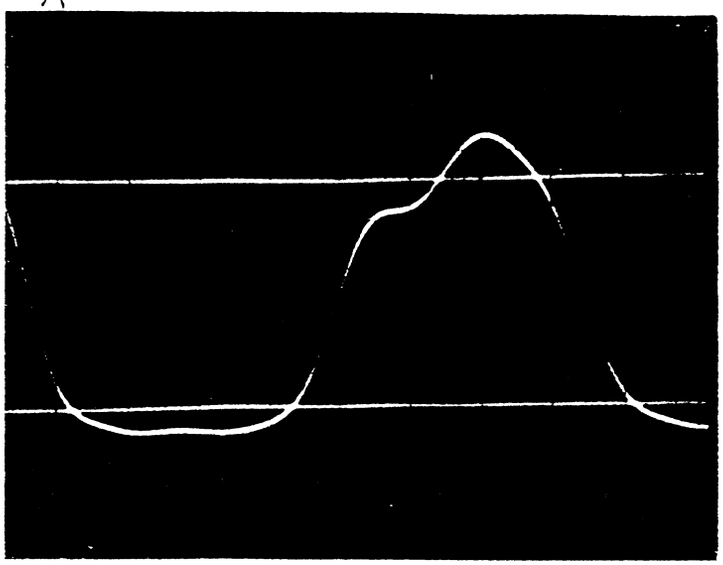


# HM



A



3.3V

0V

SLOW OBUFS

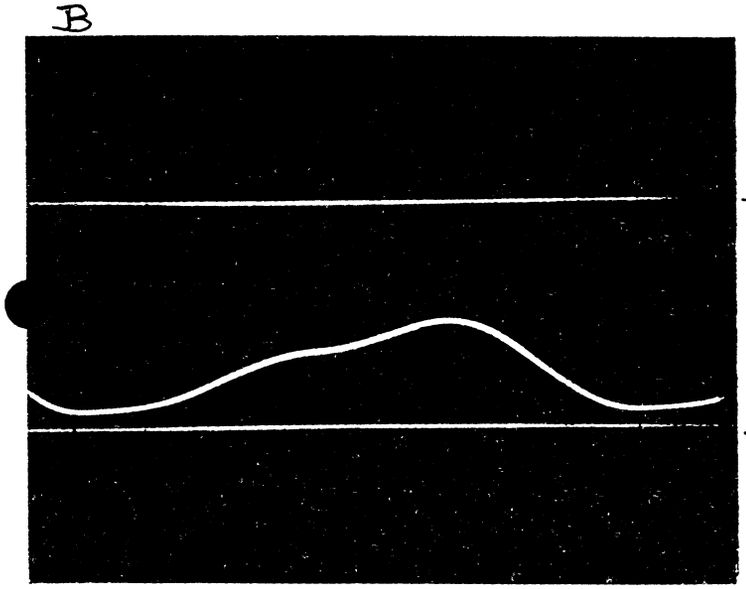
REFERENCE AT U22 OUTPUT

1 nsec/div

1 volt/div

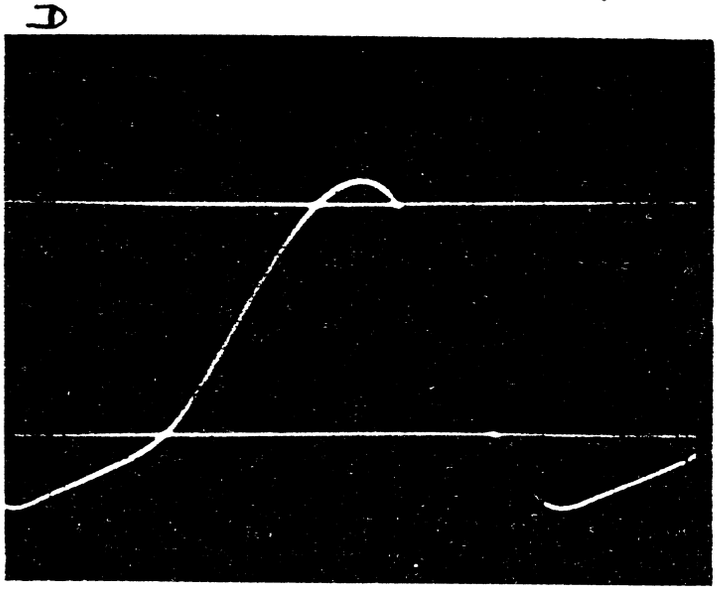
2 MA

B



16 MA

D

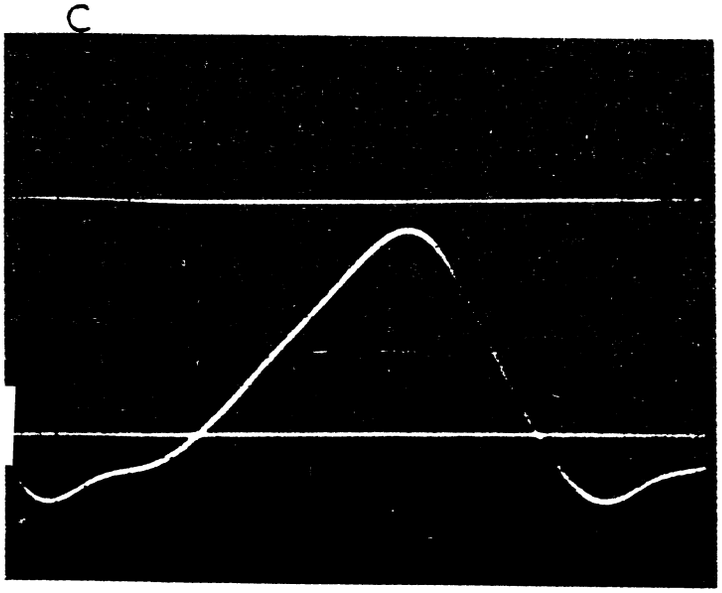


3.3V

0V

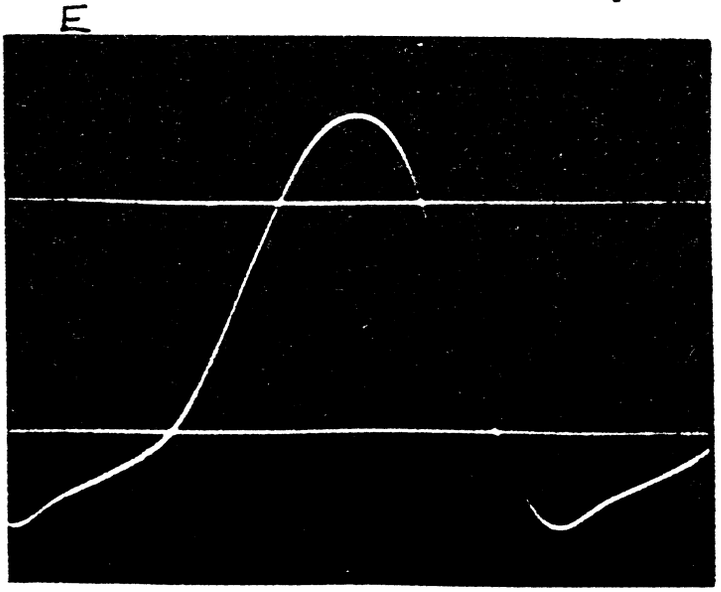
8 MA

C



24 MA

E



1 nsec / div

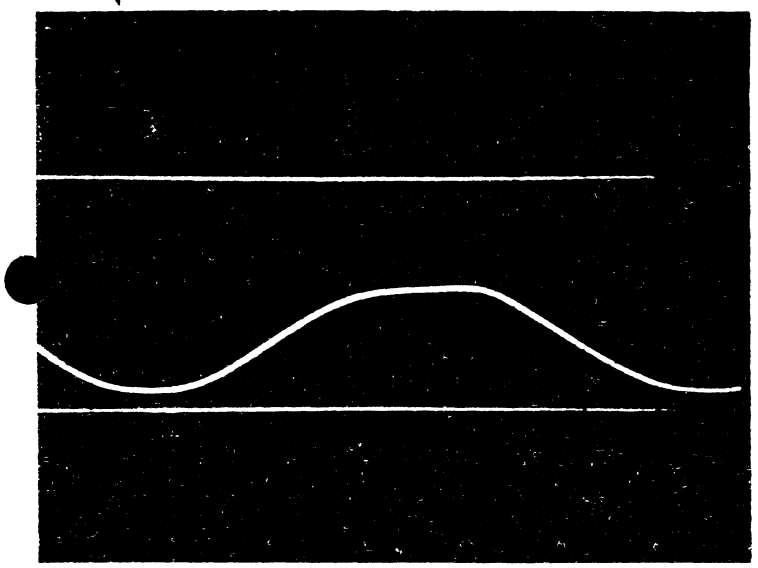
1 volt / div

RAILS = 0V → 3.3V

FAST
OBUFS

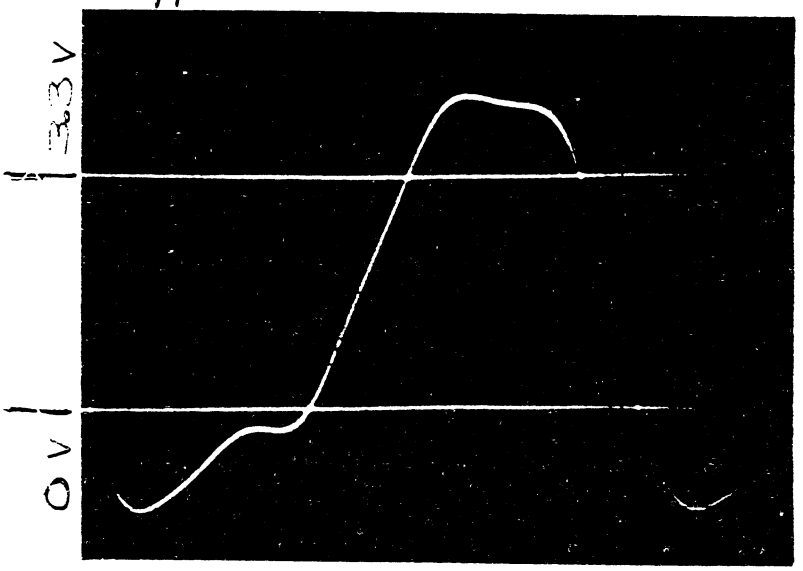
2 MA

F



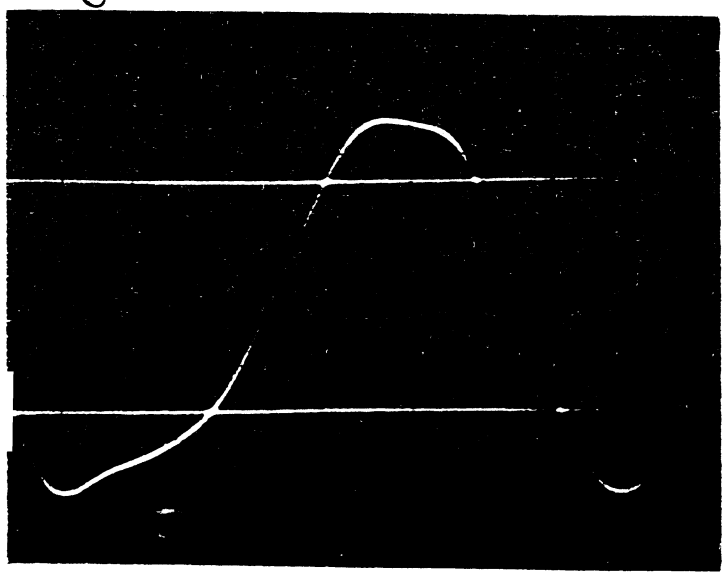
16 MA

H



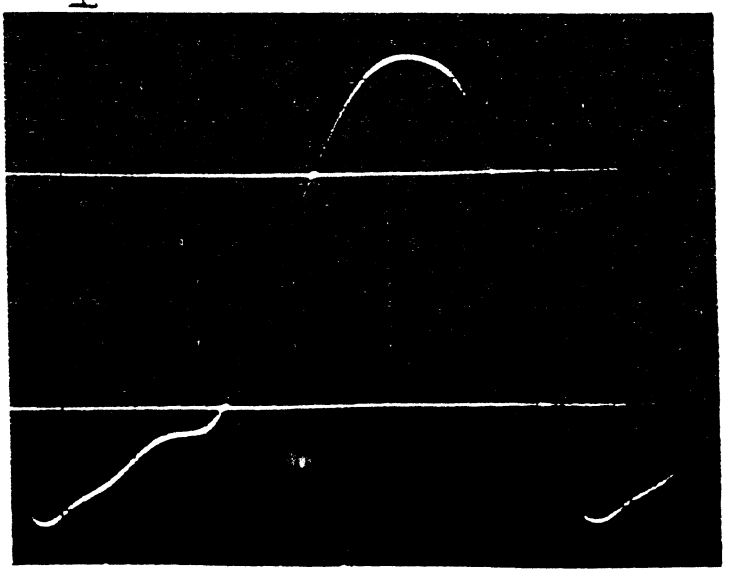

8 MA

G



24 MA

I



1 nsec/div

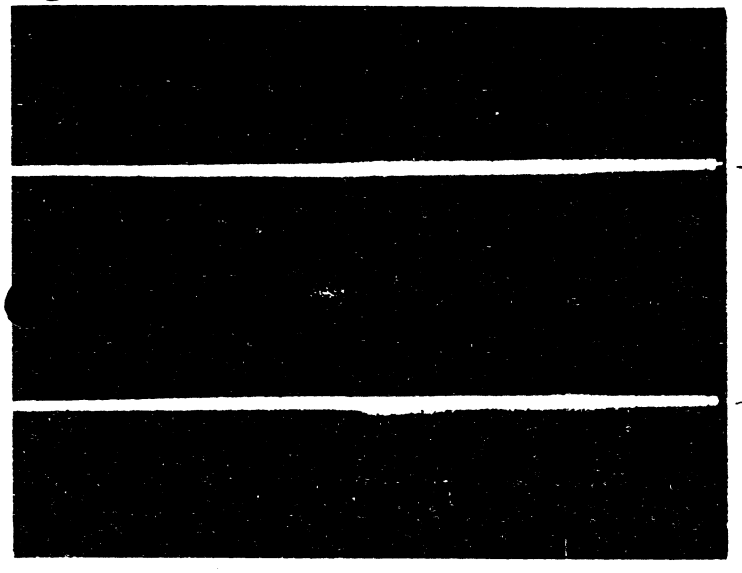
1 volt/div

RAILS = 0 V → 3.3V

SLOW
OBUFS ↓

2 MA ↓

B

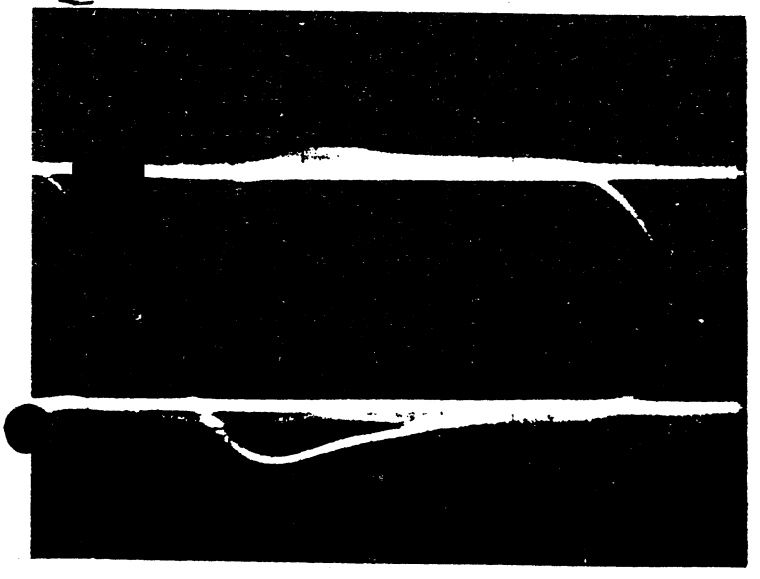


16 MA ↓

D

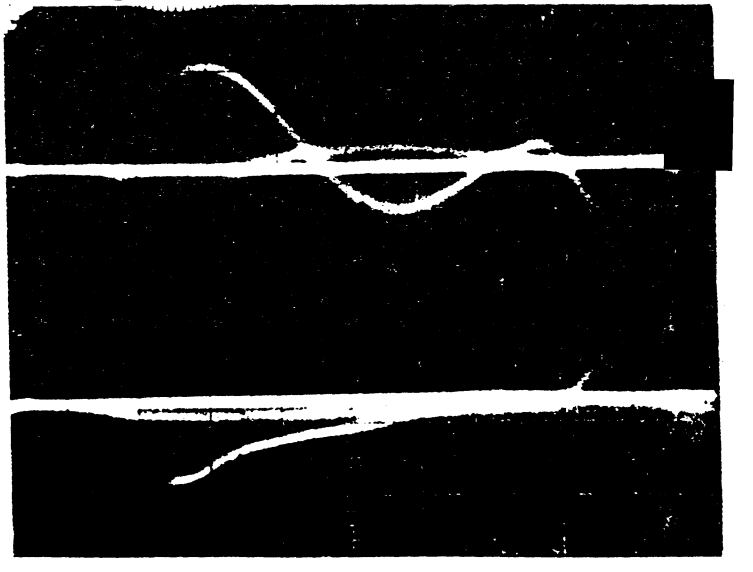
8 MA ↓

C



24 MA ↓

E



FAST
OBUFS

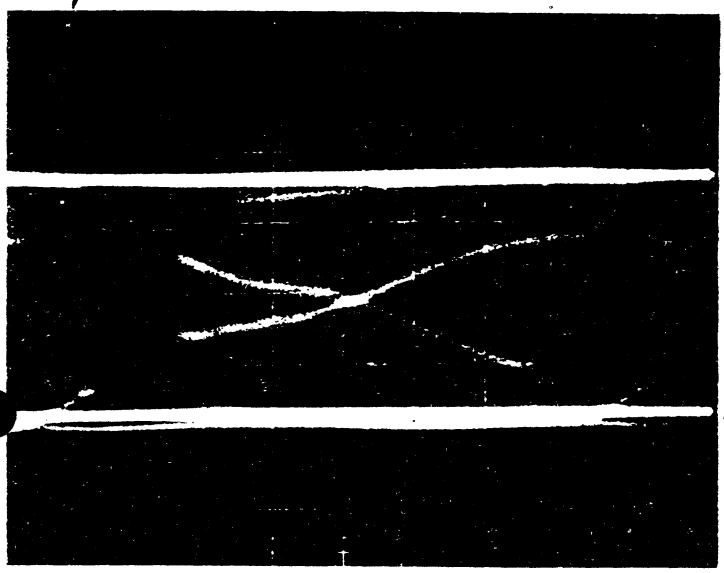
1 nsec/div

1 volt/div

RAILS = 0V → 3.3V

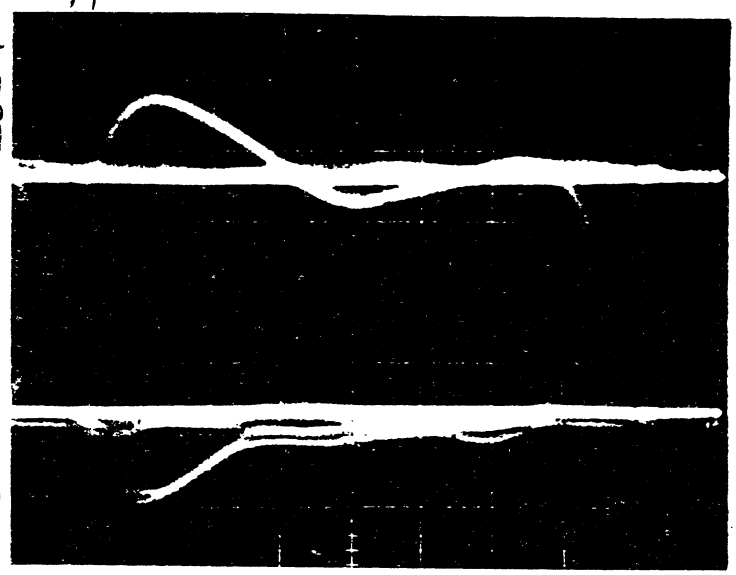
2 MA

F



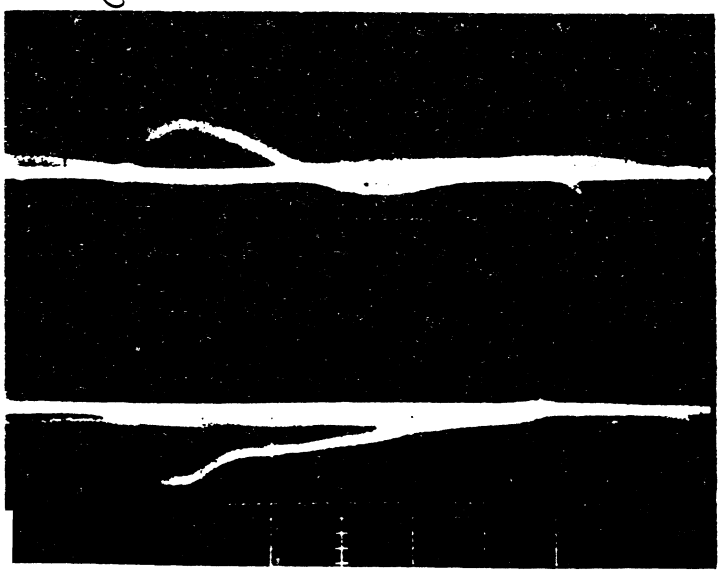
16 MA

H



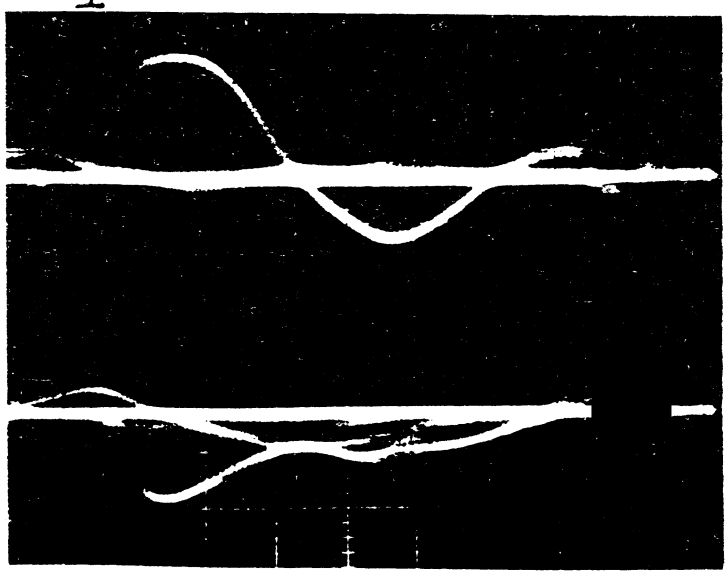

8 MA

G



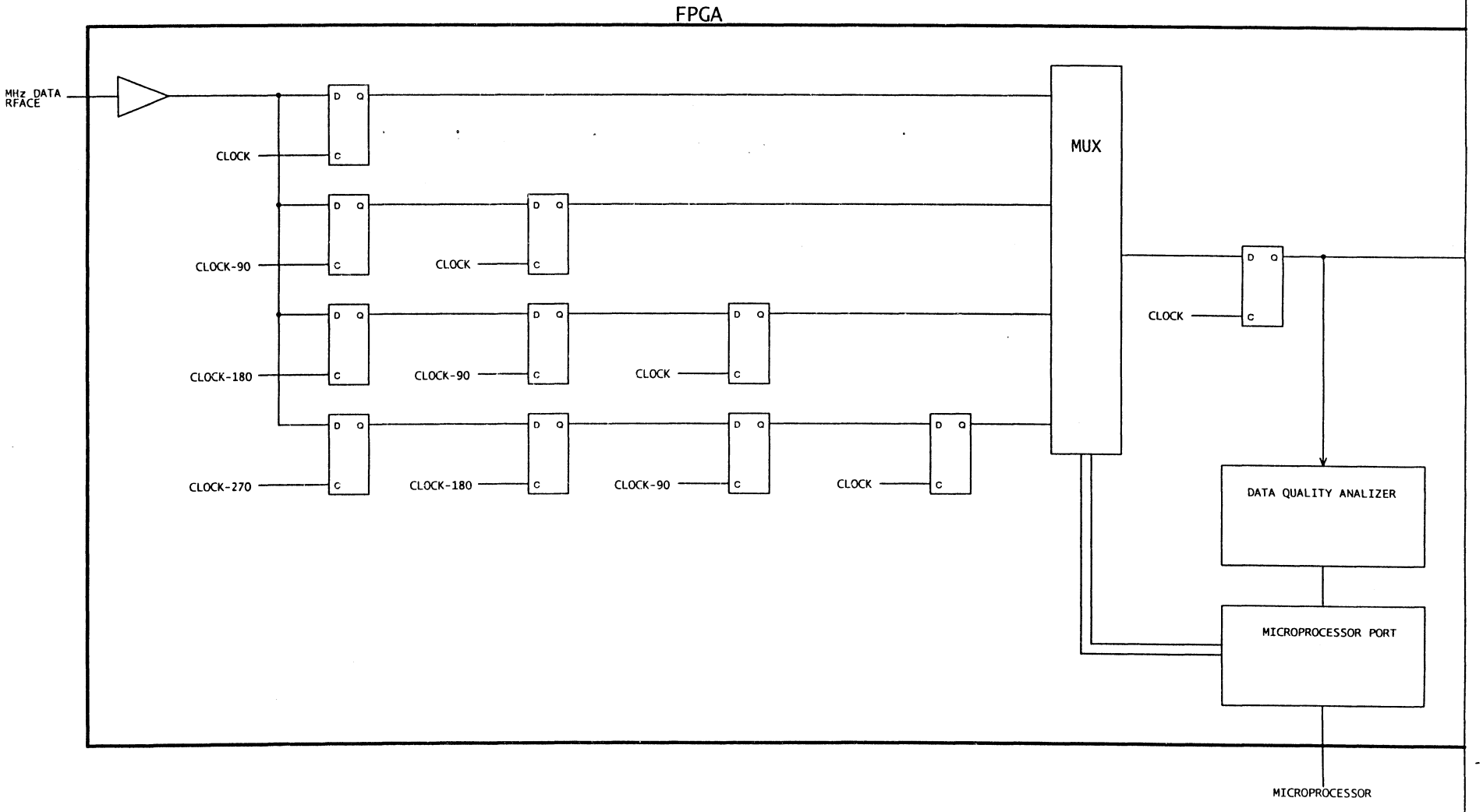
24 MA

I

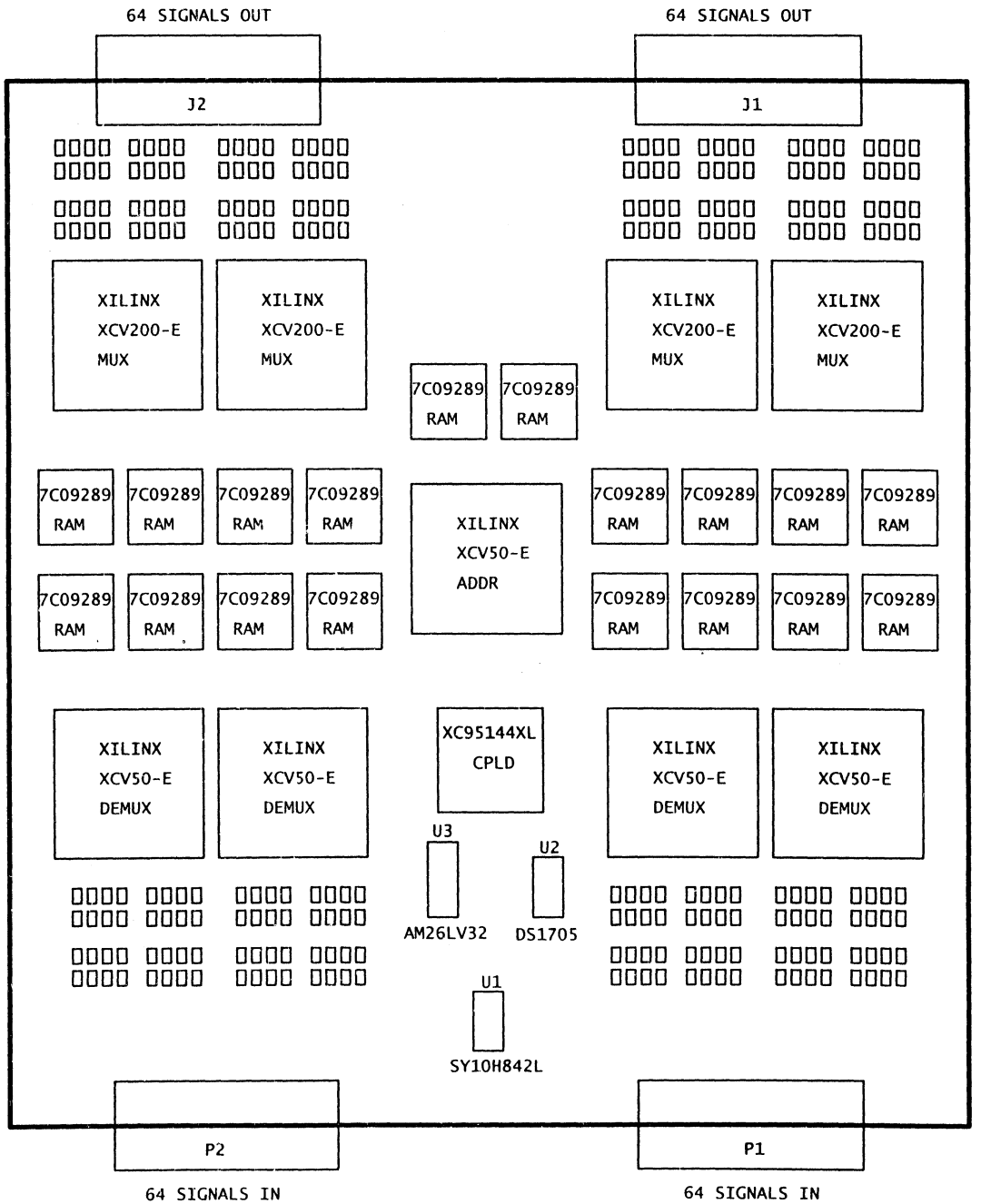


[illegible] CMOS/TTL TEST #2 [illegible]

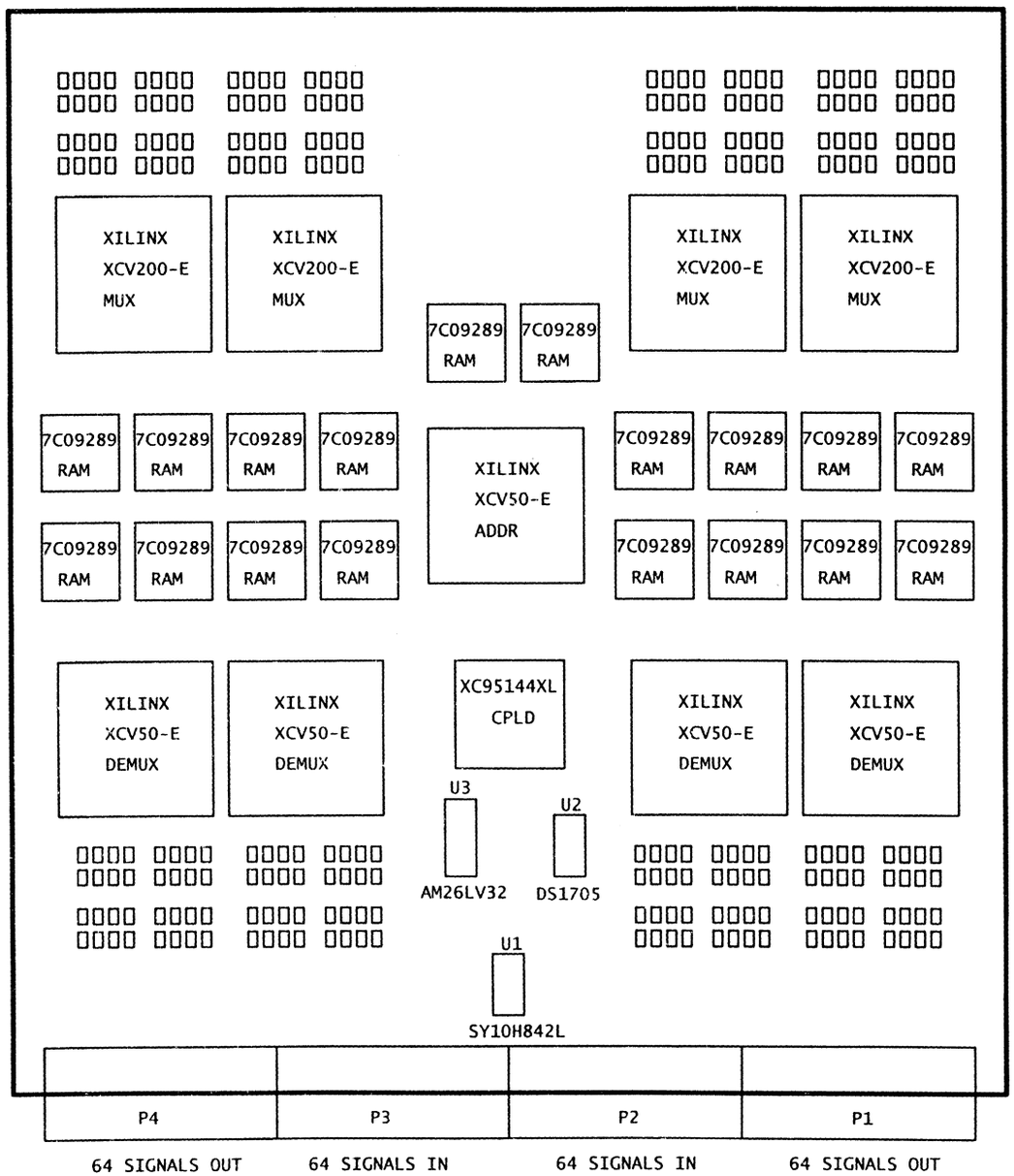
# QUADRATURE DATA CAPTURE



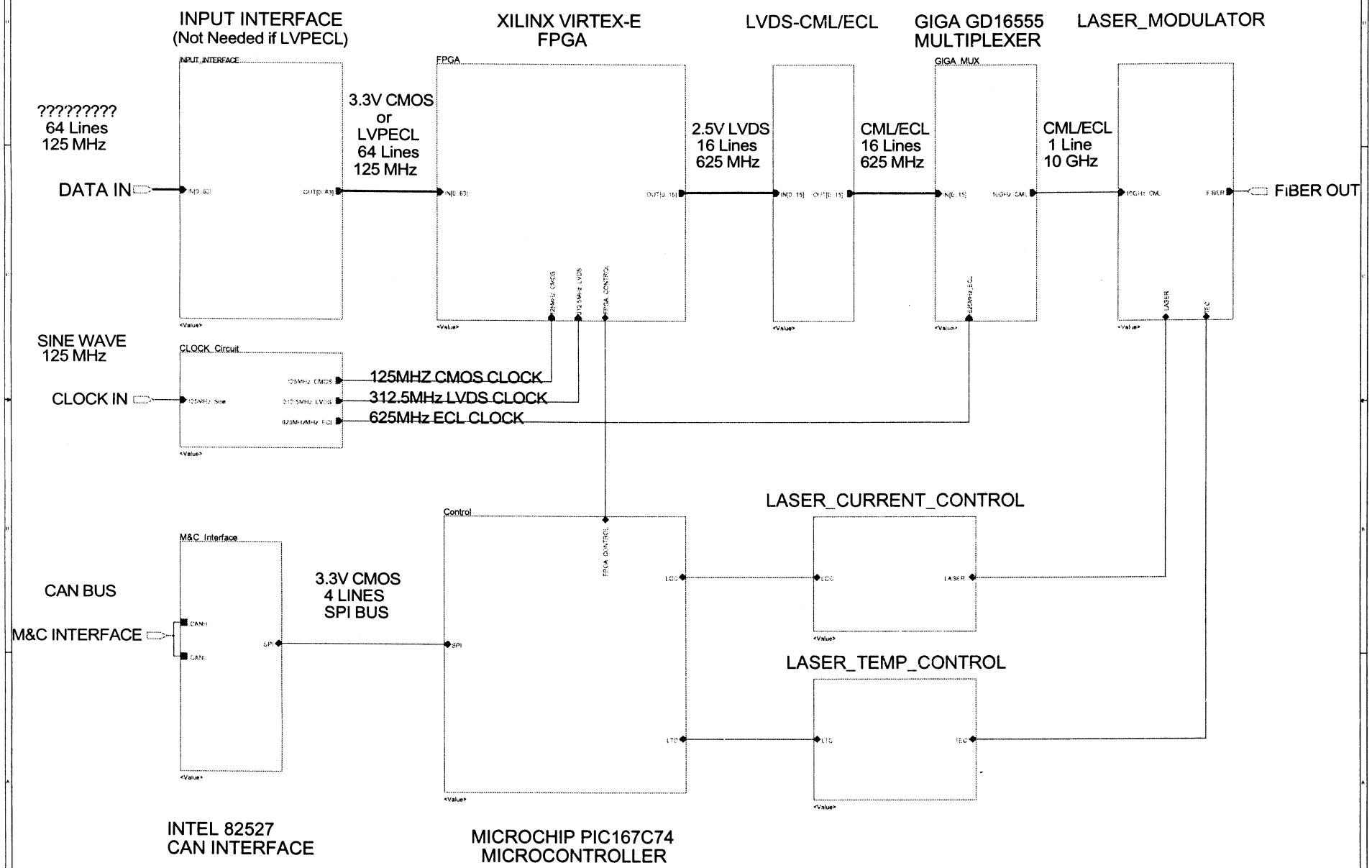
# STATION CARD



# STATION CARD



# FIBER OPTIC TRANSMITTER




1-20-00
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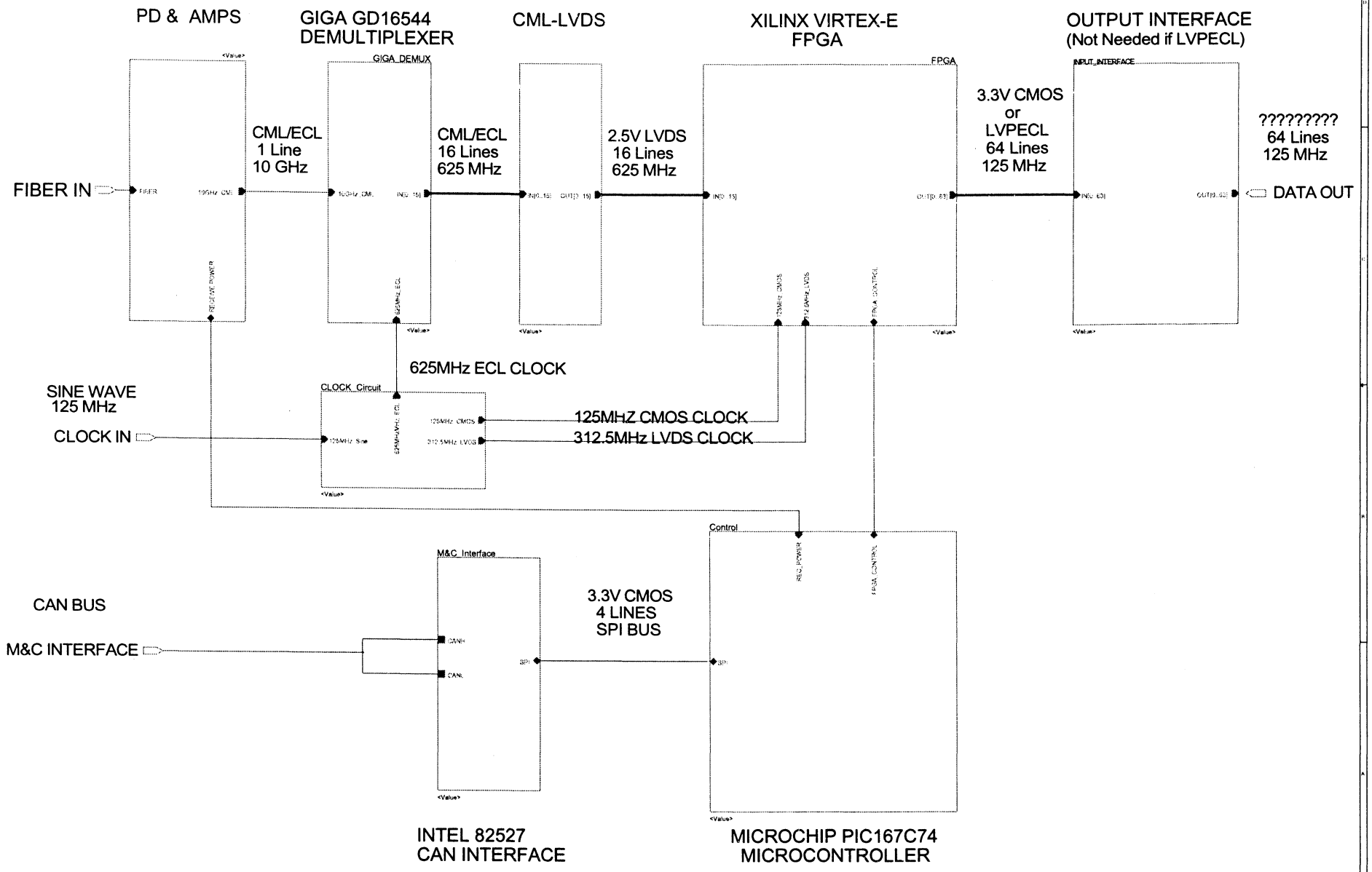
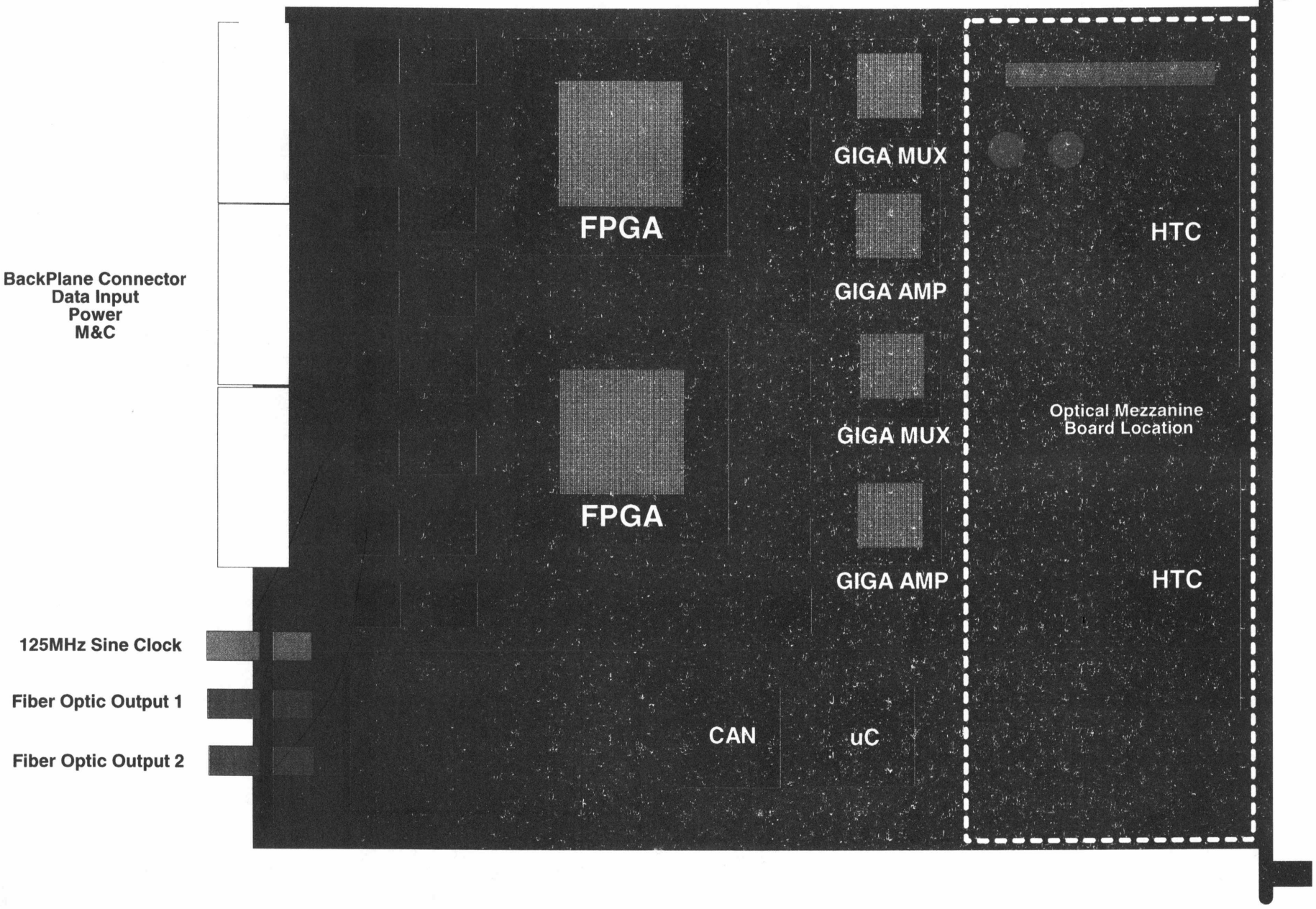
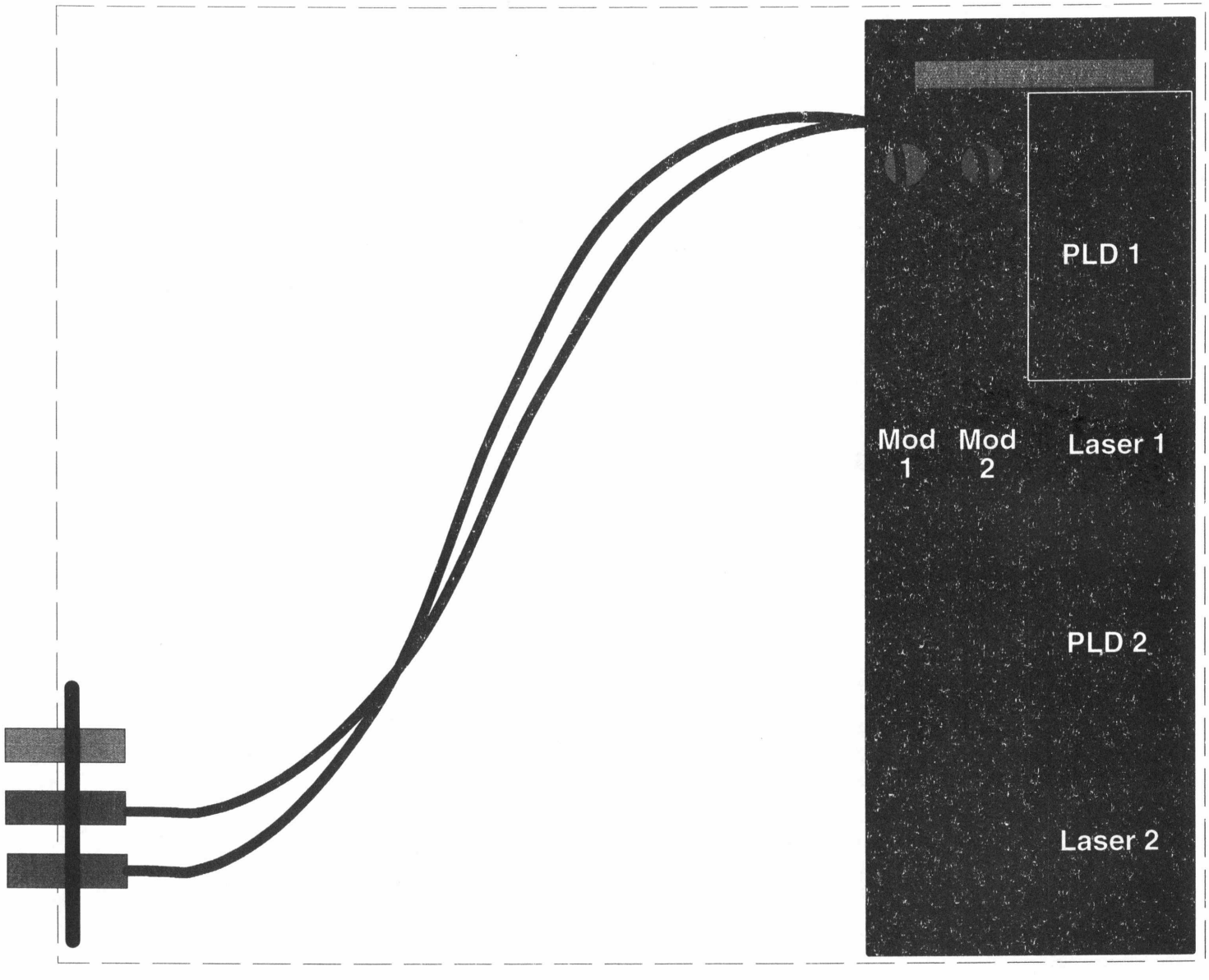
# FIBER OPTIC RECEIVER



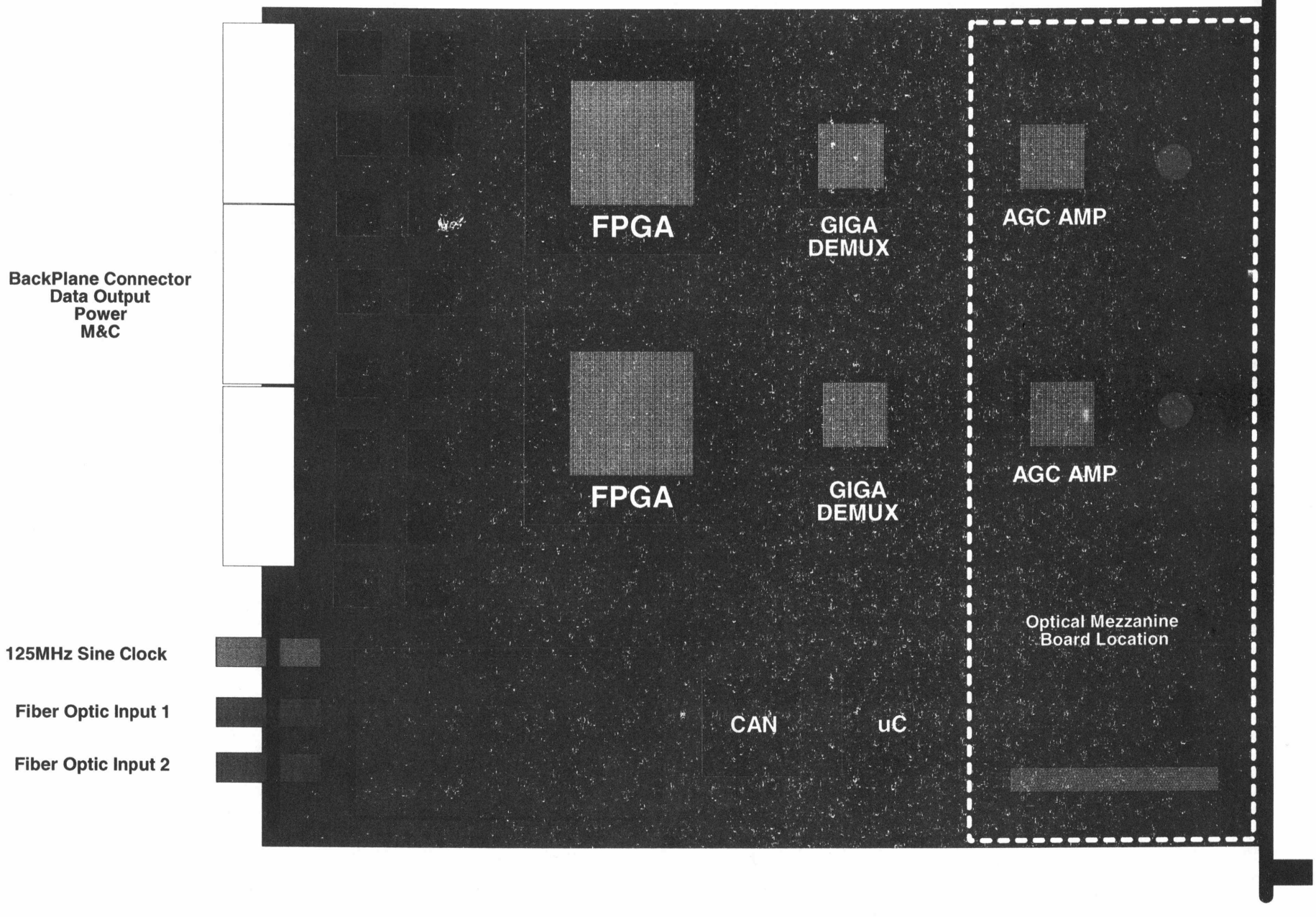
# Fiber Optic Transmitter Main Board



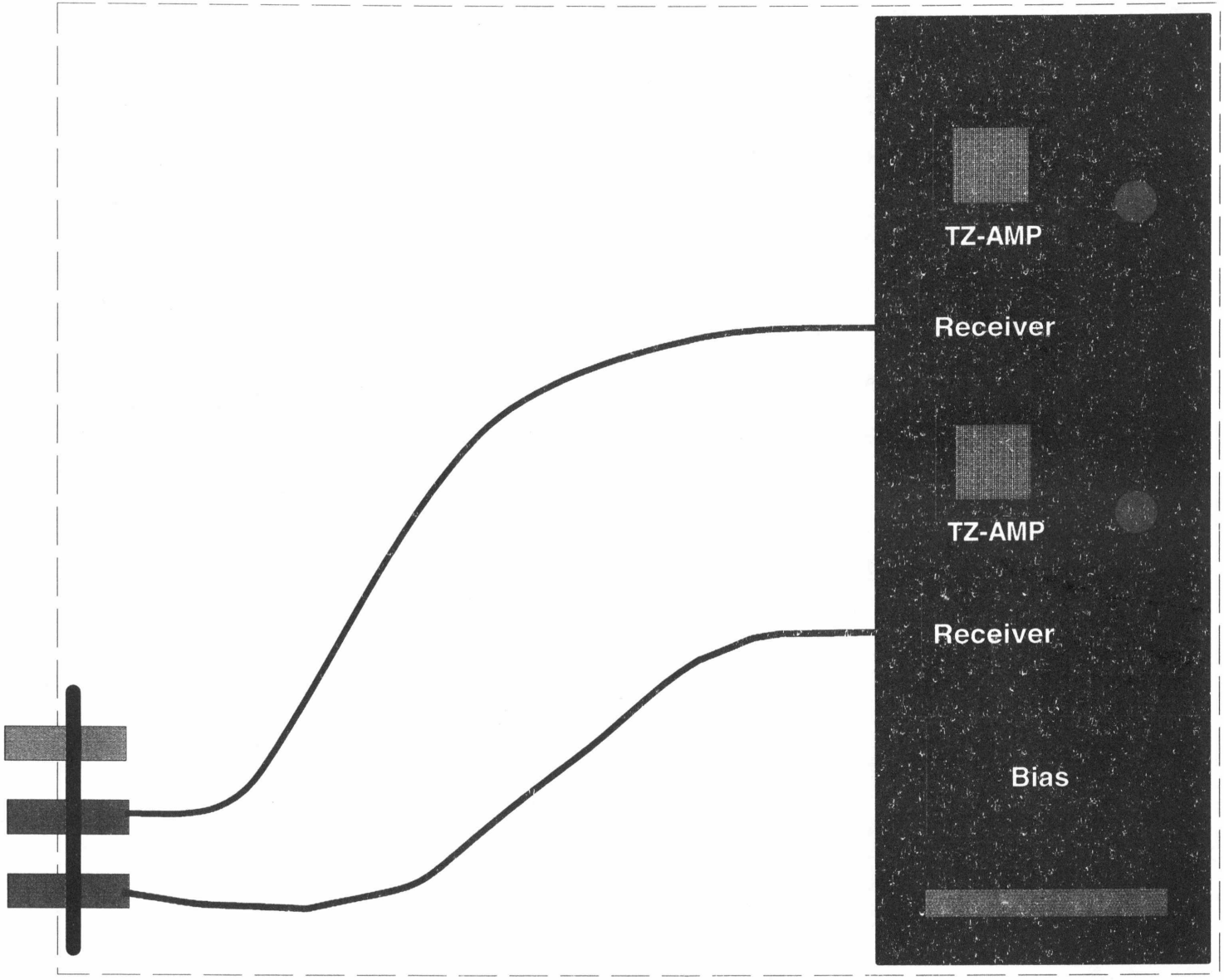
# Fiber Optical Transmitter Mezzanine Board



# F · Optic Receiver
# Main Board



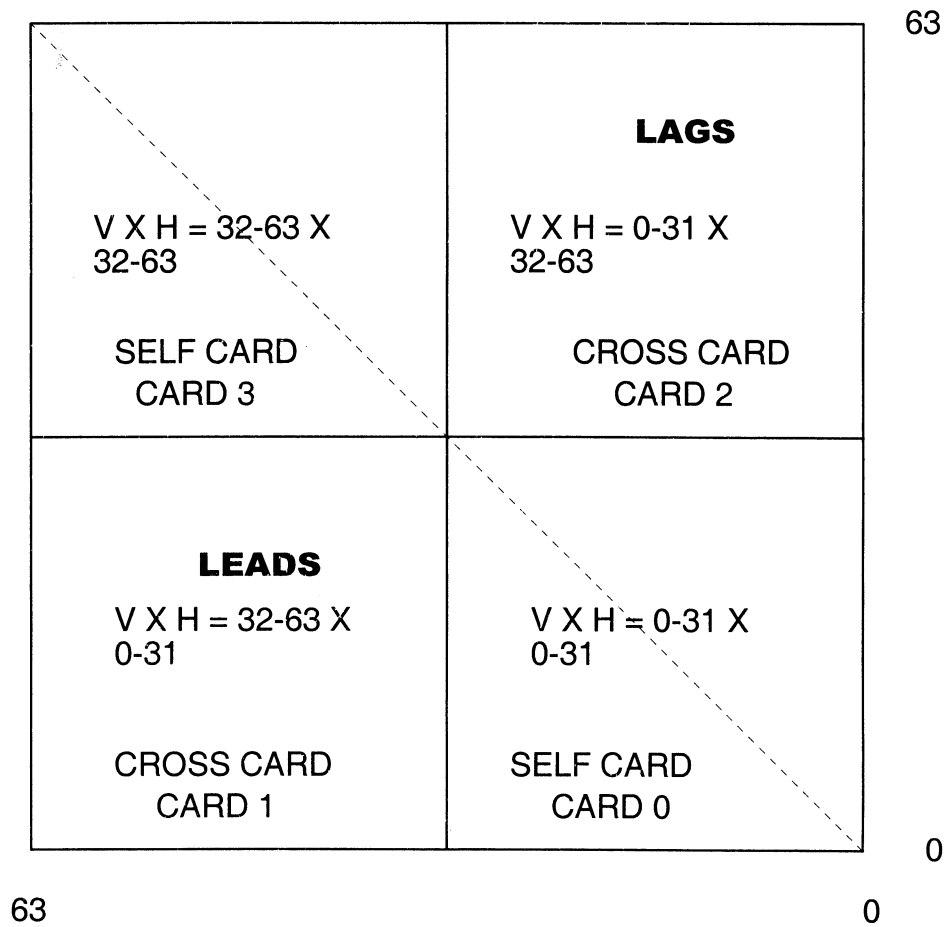
# Fiber Optic Receiver
# Mezzanine Optical Board



# CORRELATOR BOARD, RACK, AND CHIP

Joseph Greenberg

1-20-00
Webber

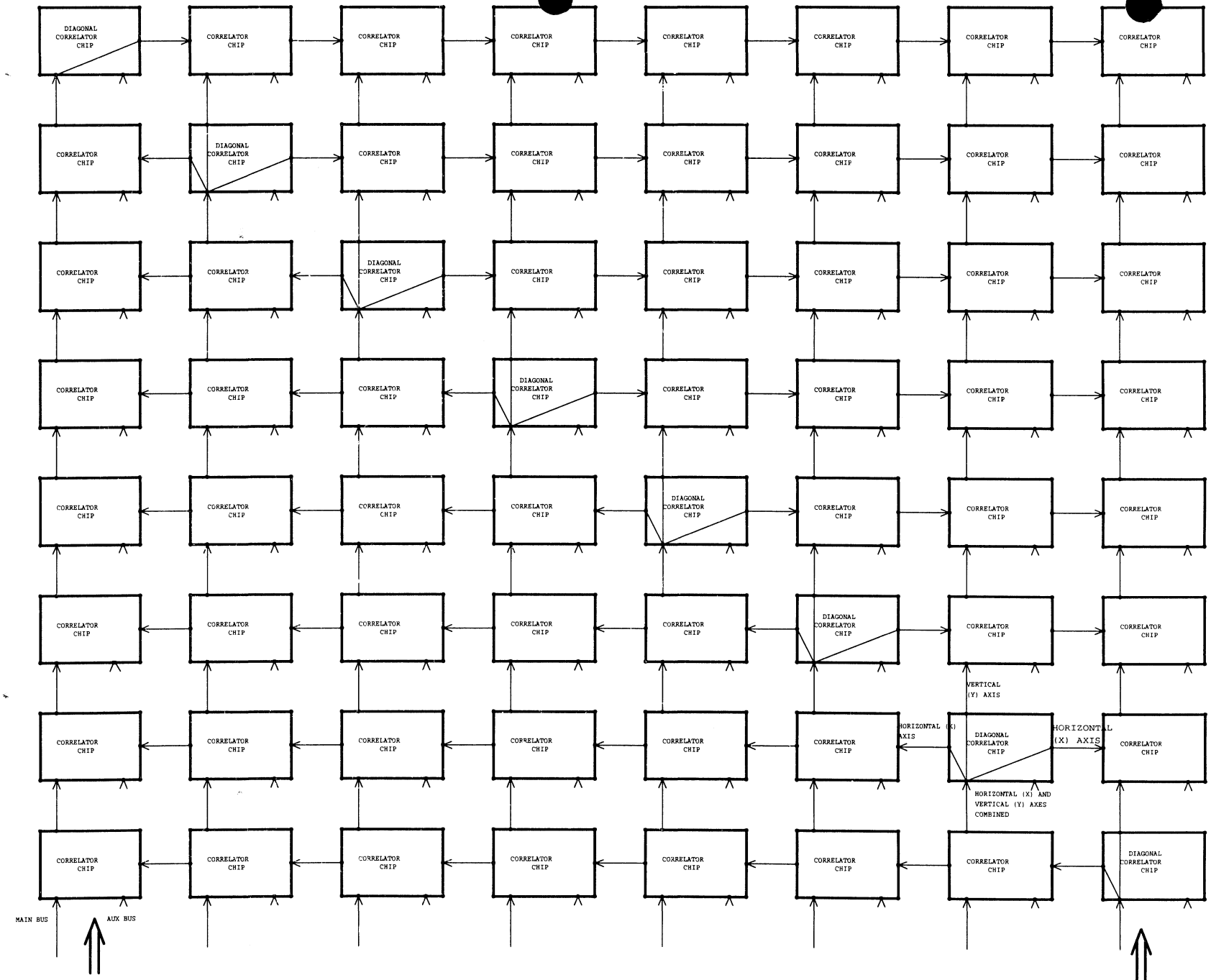



CROSS MULTIPLIER PLANE

(AUTO-CORRELATORS ON MATRIX DIAGONAL)

# SELF CARD

ALMA
CORRELATOR
CARD.



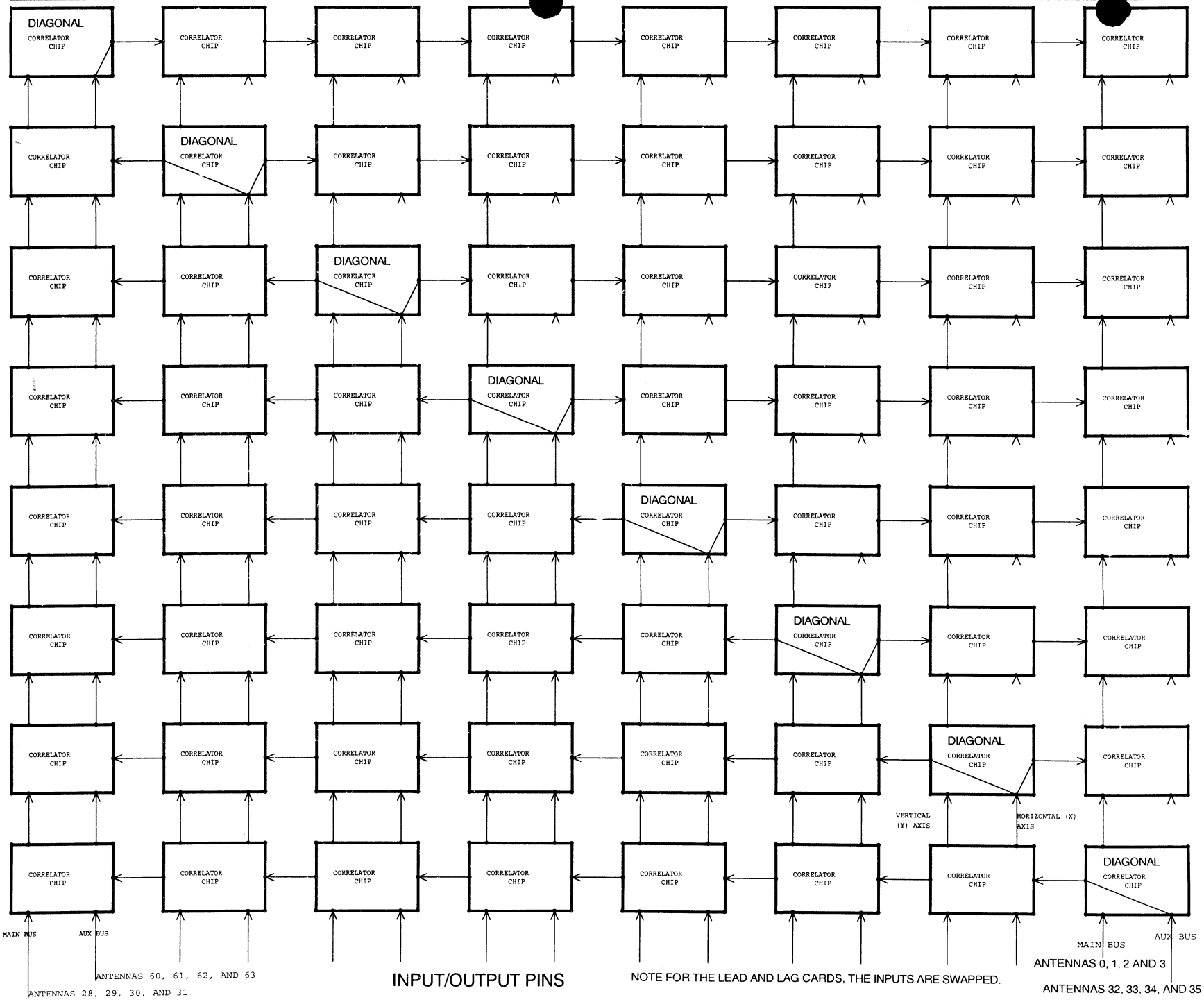

ANTENNAS 28, 29, 30, AND 31
OR
ANTENNAS 60, 61, 62, AND 63

INPUT/OUTPUT PINS

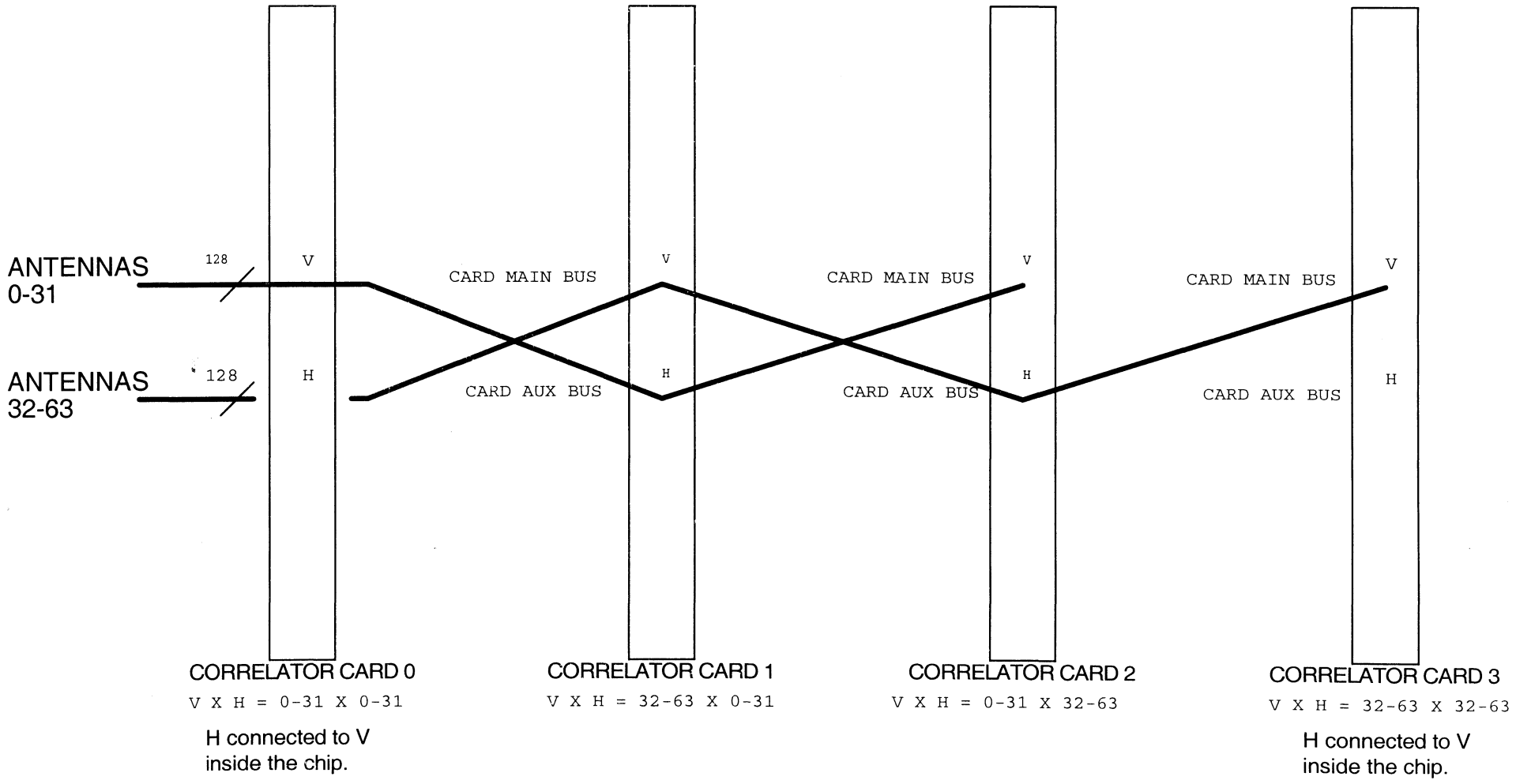
ANTENNAS 0, 1, 2 AND 3
OR
ANTENNAS 32, 33, 34, AND 35

# CROSS CARD

ALMA
CORRELATOR
CARD.



# SIGNAL DISTRIBUTION TO SET OF FOUR CORRELATOR CARDS

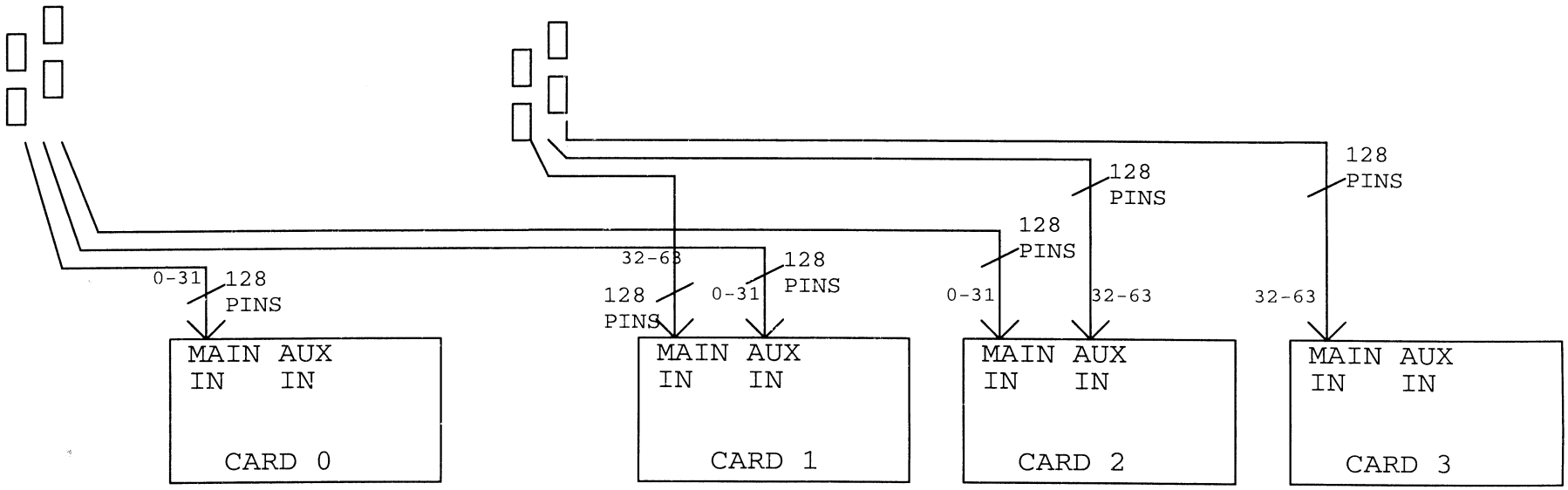


**BB PAIR 0**

ANT 0-31, 2 BB, 2 BITS, (128 BITS TOTAL), (32 CABLE WAFERS)

**BB PAIR 0**

ANT 32-63, 2 BB, 2 BITS, (128 BITS TOTAL), (32 CABLE WAFERS)

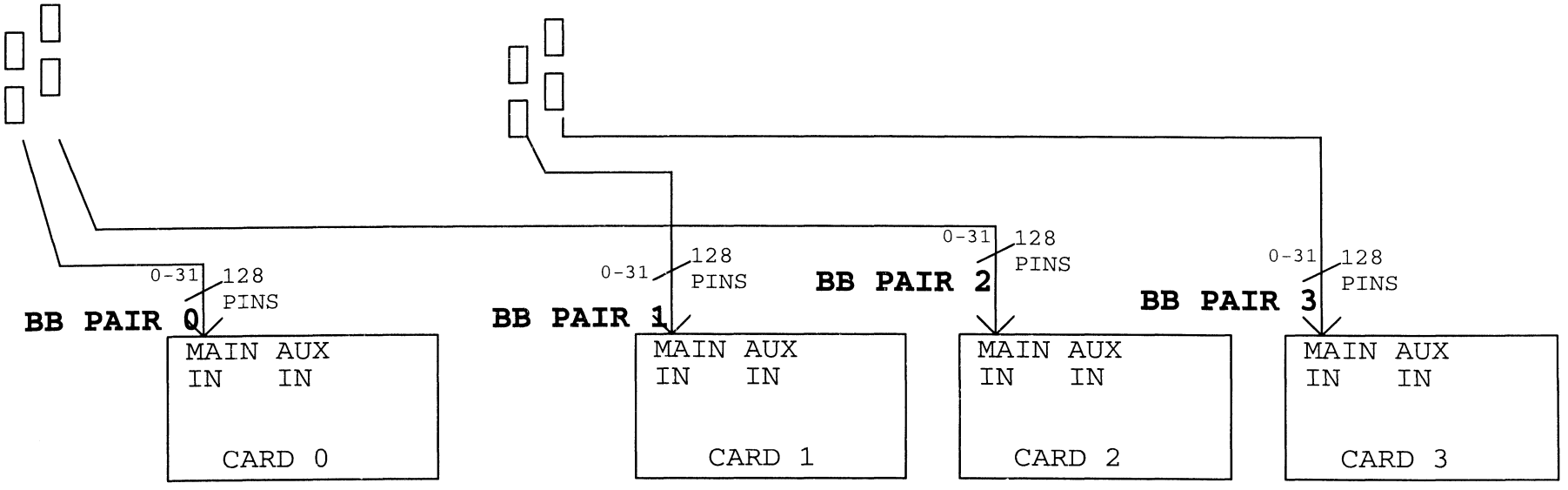



# CORRELATOR CARD INPUT SIGNAL DISTRIBUTION

**NORMAL (FULL SYSTEM)**

**BB PAIRS 0 AND 2**
ANT 0-31, 4 BB, 2 BITS, (256 BITS TOTAL), (64 CABLE WAFERS)

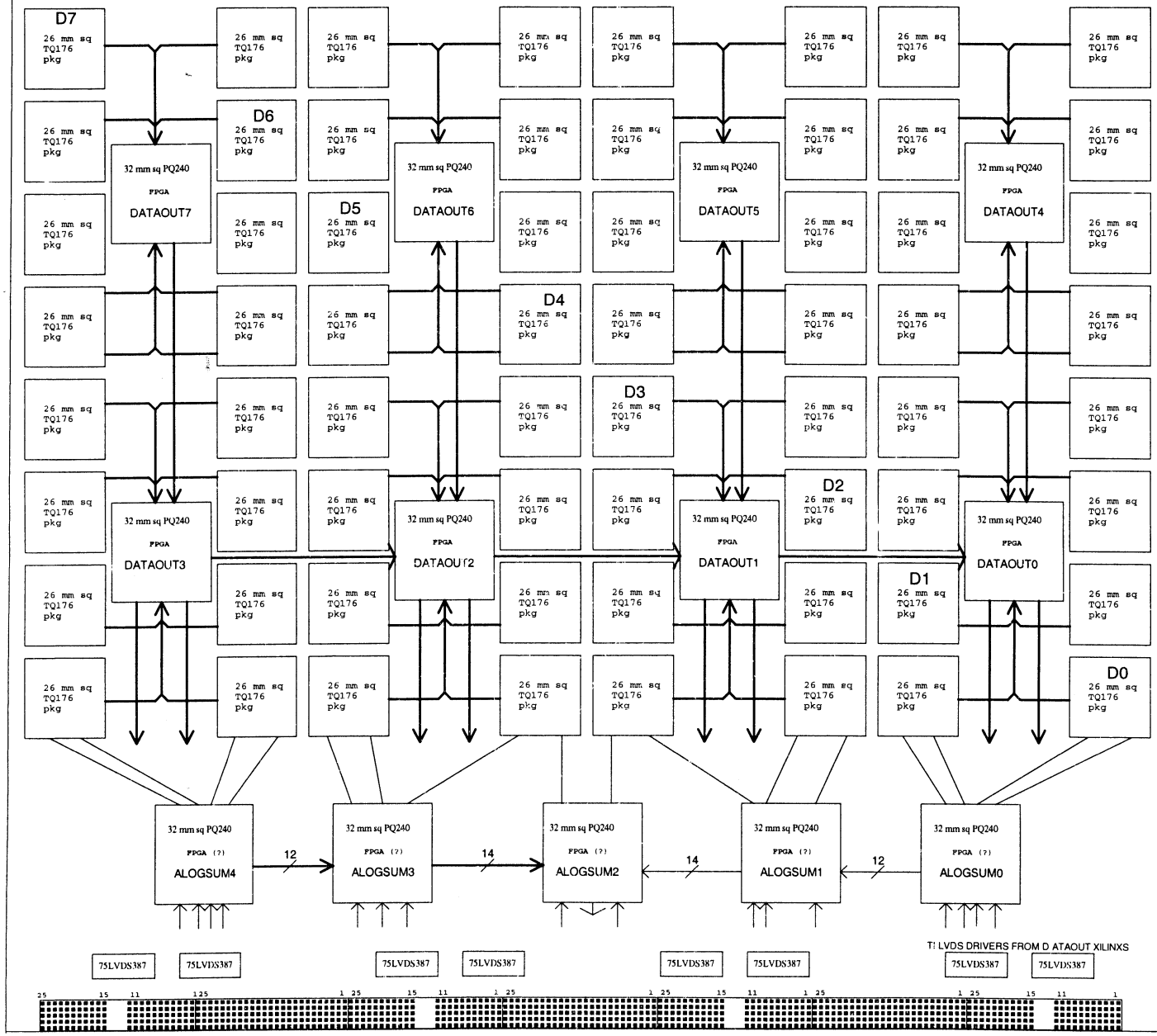
**BB PAIRS 1 AND 3**
ANT 0-31, 4 BB, 2 BITS, (256 BITS TOTAL), (64 CABLE WAFERS)




# CORRELATOR CARD INPUT SIGNAL DISTRIBUTION

**FIRST QUADRANT SPECIAL CONFIGURATION**

# CORRELATOR CARD LAYOUT



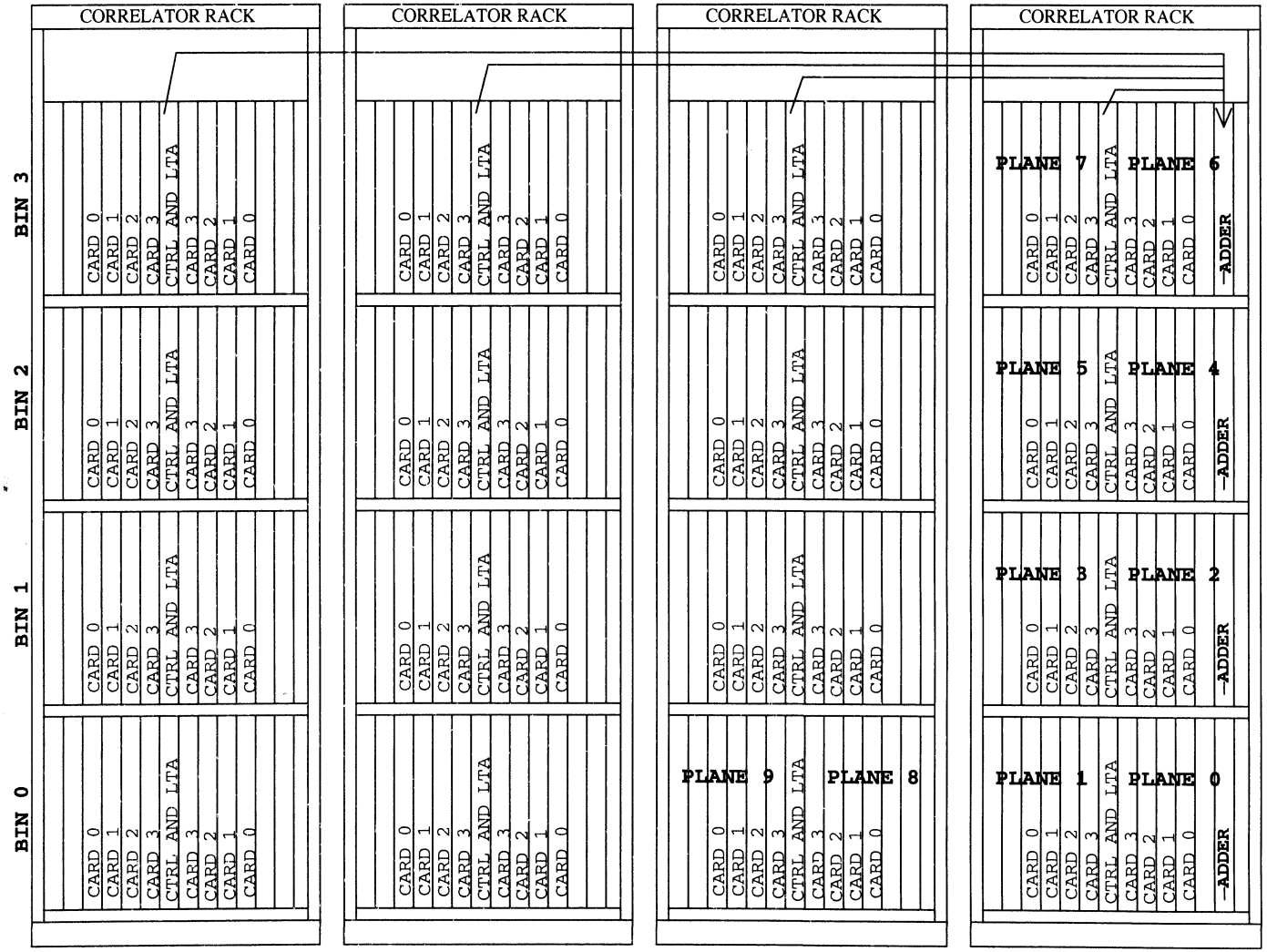

815 I/O PINS TOTAL

ASSUME 150 AMPS TOTAL, 1.5 AMPS PER PIN, 100 PINS FOR VOLTAGE AND 100 PINS FOR GROUND

815 - 200 = 615 PINS REMAINING
615 - 512 FOR ANT INPUT/OUTPUT
= 103 "FREE" PINS

9U (367 mm tall)
14.4 inches

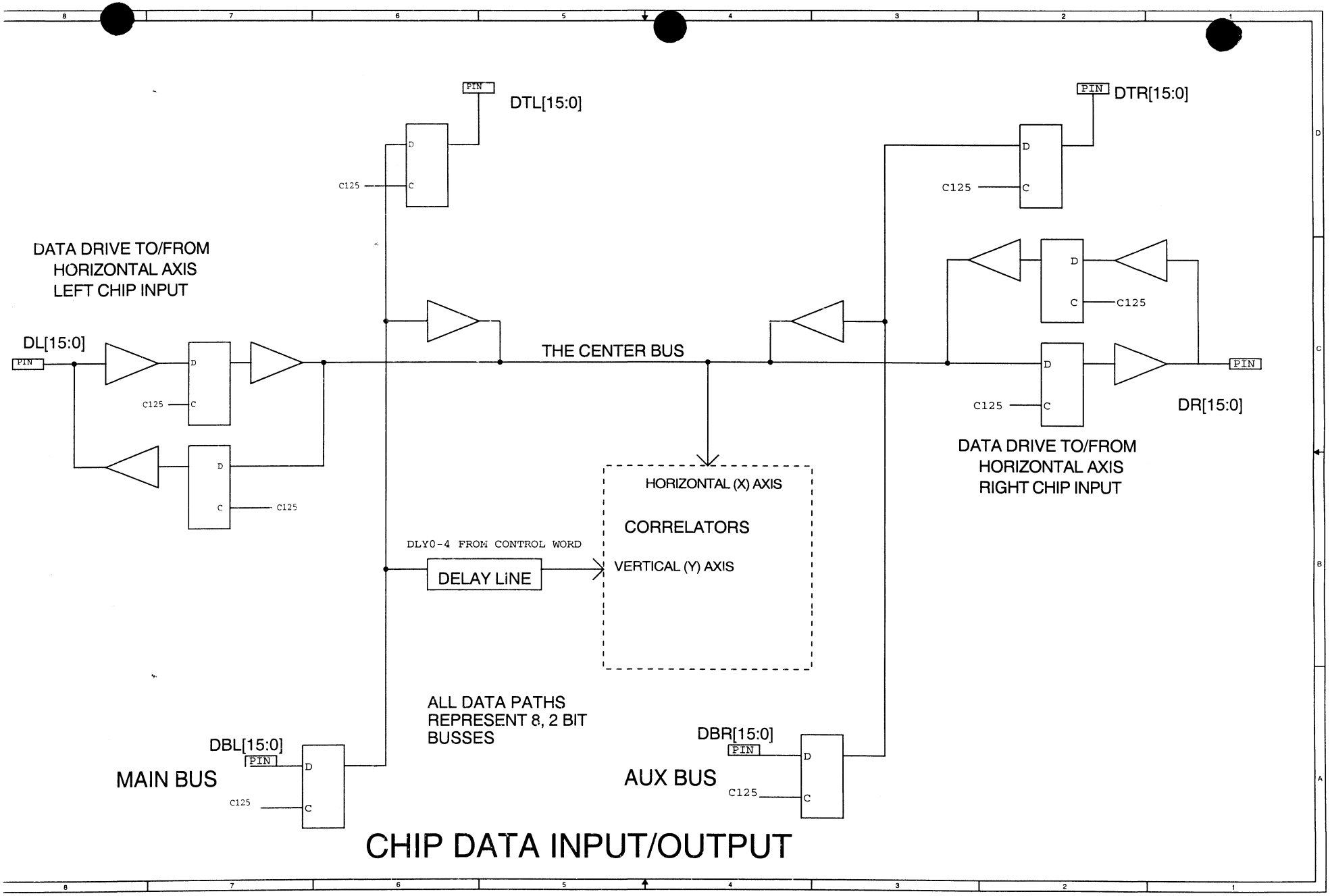
# ONE ARRAY




FRONT VIEW OF CORRELATOR RACK/BINS

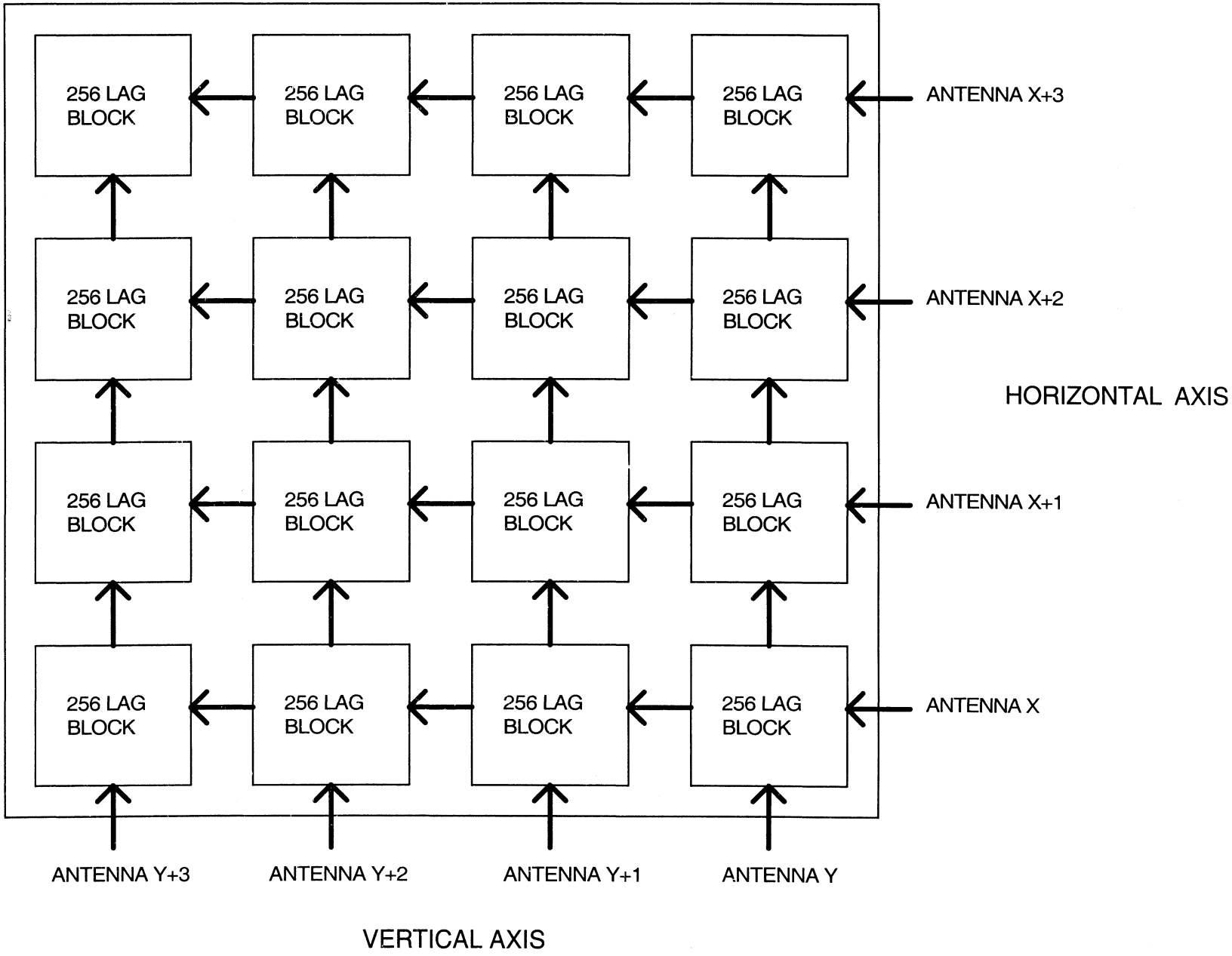
## ALMA Correlator Chip

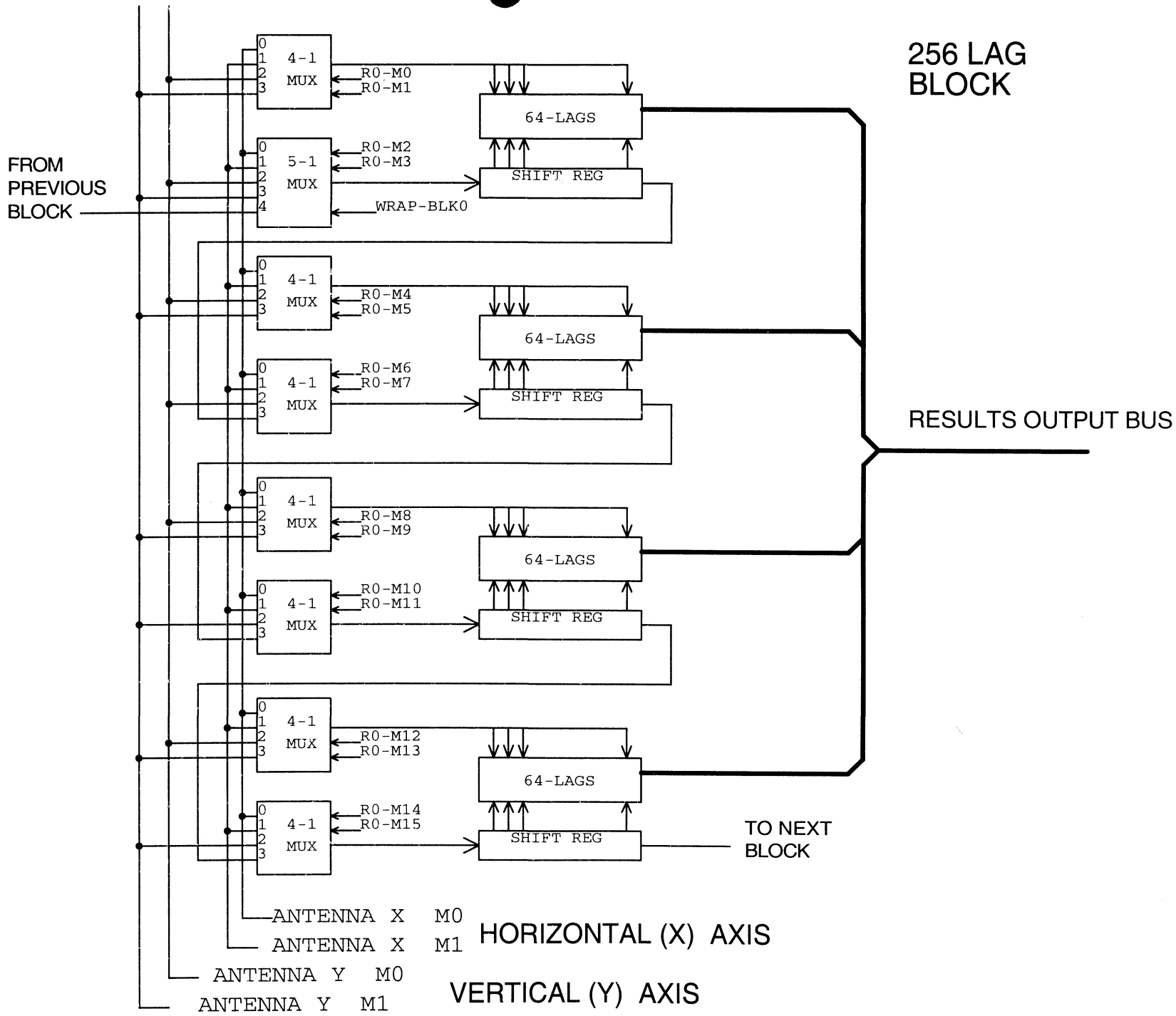
- 0.18 u CMOS technology
- 125 MHz System Clock
- 4096 or 8192 Lags
- 4 Antenna by 4 Antenna Array
- 240 Pin Quad Flat Pack Package
- 3.3 Volt I/O, 1.5 Volt core
- 2 bit, 4 level Multiplications
- 25 bit Accumulator
- 16 bit Secondary Result Storage
- Supports Oversampling
- Serial Program Word
- 64 chips/correlator card * 4 cards/plane * 32 planes * 4 Baseband pairs = 32,768 chips.
- Surface Mount Technology
- 2 Watts Power Dissipation for 8192 Lags



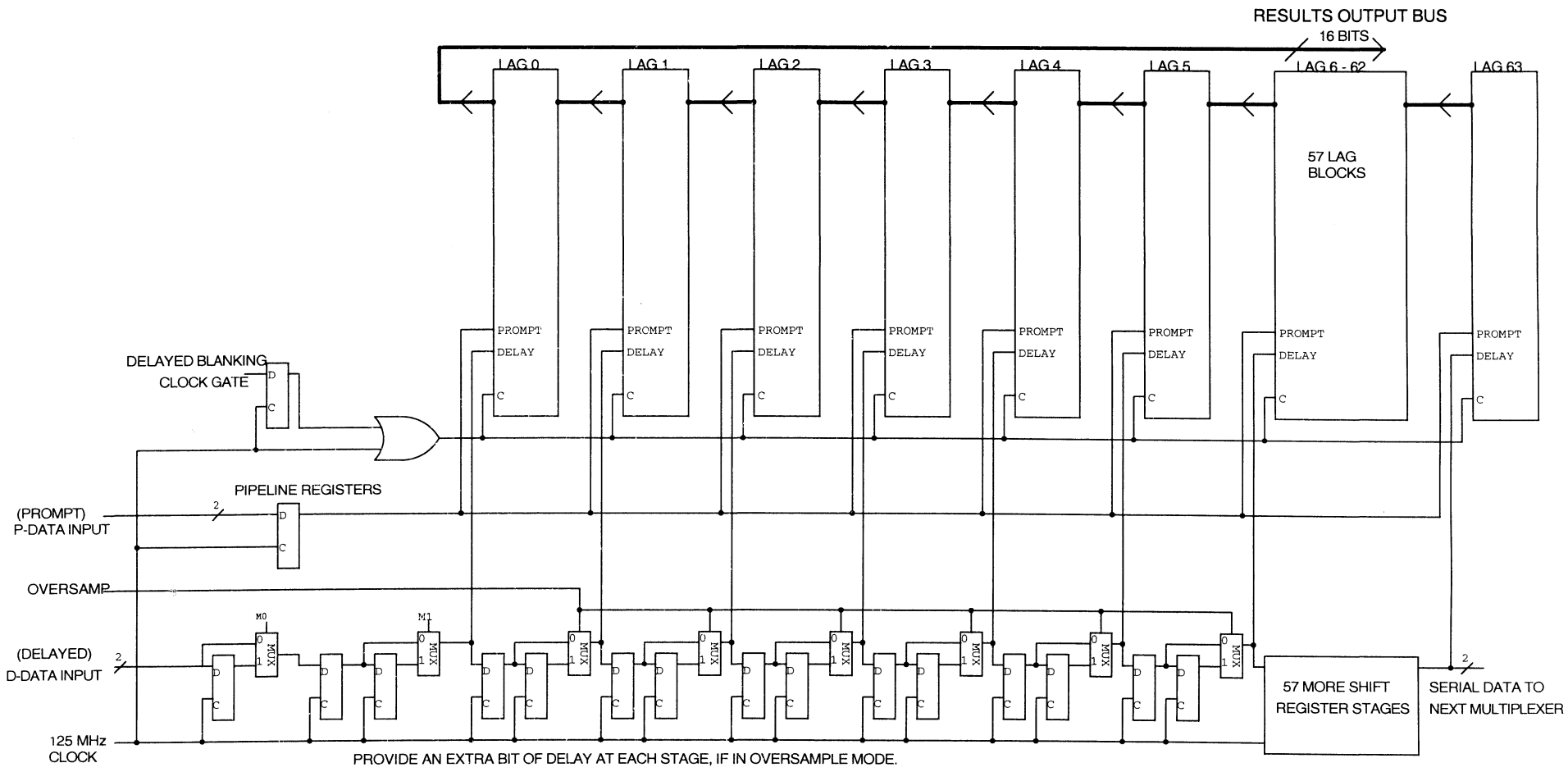

# CHIP DATA INPUT/OUTPUT

# SIXTEEN 256 LAG BLOCKS IN A SINGLE ALMA CORRELATOR CHIP

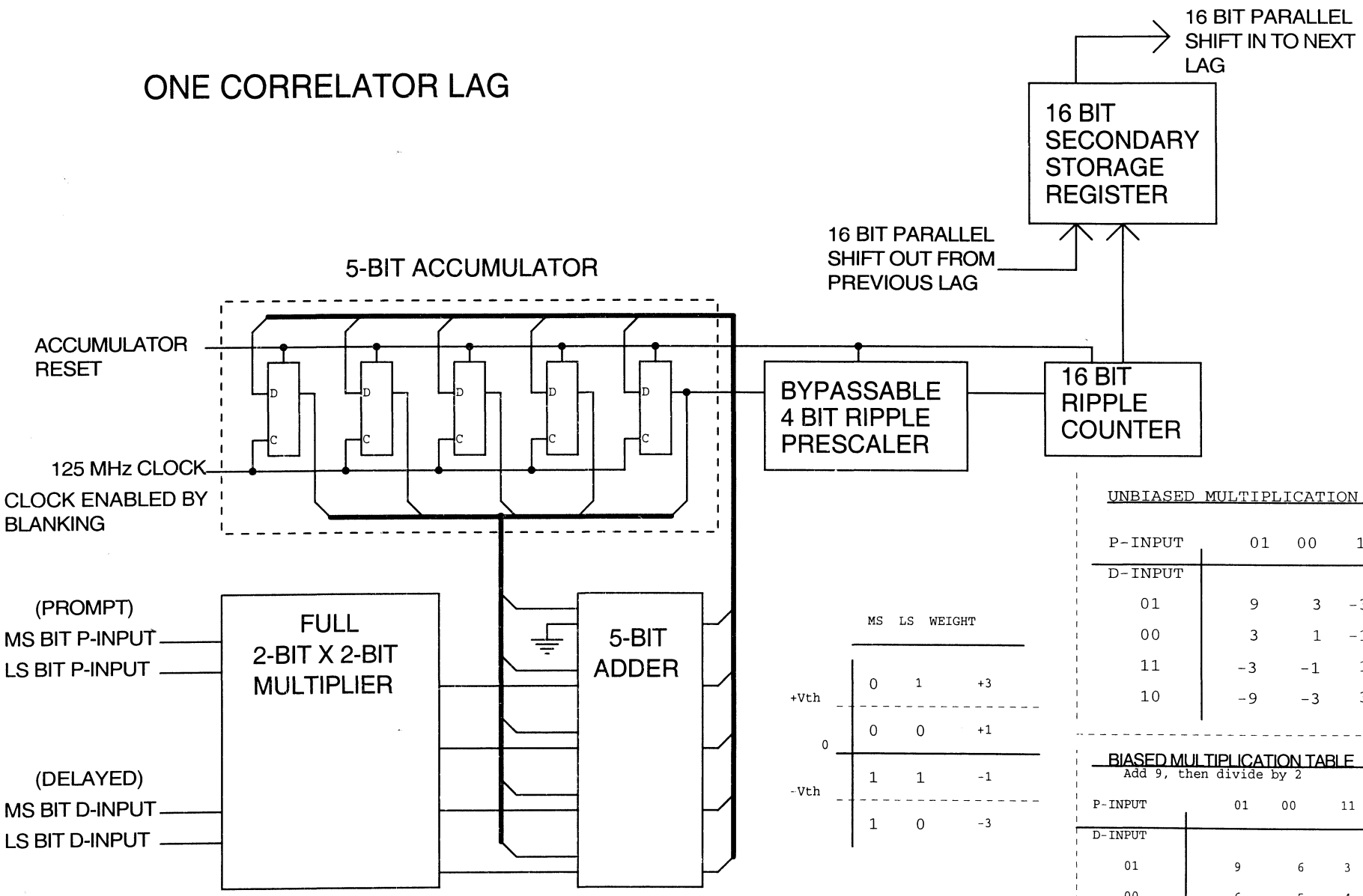



256 LAG BLOCK
FROM PREVIOUS BLOCK
4-1 MUX
5-1 MUX
R0-M0
R0-M1
R0-M2
R0-M3
WRAP-BLK0
R0-M4
R0-M5
R0-M6
R0-M7
R0-M8
R0-M9
R0-M10
R0-M11
R0-M12
R0-M13
R0-M14
R0-M15
64-LAGS
SHIFT REG
RESULTS OUTPUT BUS
TO NEXT BLOCK
ANTENNA X M0
ANTENNA X M1
HORIZONTAL (X) AXIS
ANTENNA Y M0
ANTENNA Y M1
VERTICAL (Y) AXIS

# 64-LAG CORRELATOR SUB-BLOCK



# ONE CORRELATOR LAG




| | MS | LS | WEIGHT |
|---|---|---|---|
| +Vth | 0 | 1 | +3 |
| | 0 | 0 | +1 |
| 0 | | | |
| | 1 | 1 | -1 |
| -Vth | 1 | 0 | -3 |

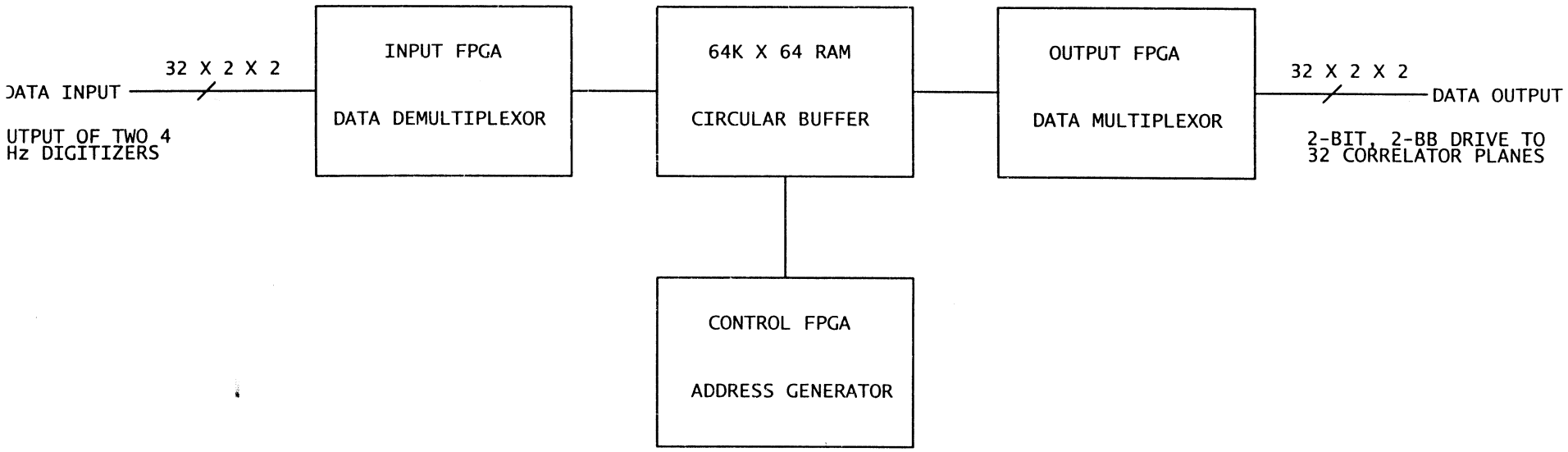
UNBIASED MULTIPLICATION TABLE

| P-INPUT / D-INPUT | 01 | 00 | 11 | 10 |
|---|---|---|---|---|
| 01 | 9 | 3 | -3 | -9 |
| 00 | 3 | 1 | -1 | -3 |
| 11 | -3 | -1 | 1 | 3 |
| 10 | -9 | -3 | 3 | 9 |

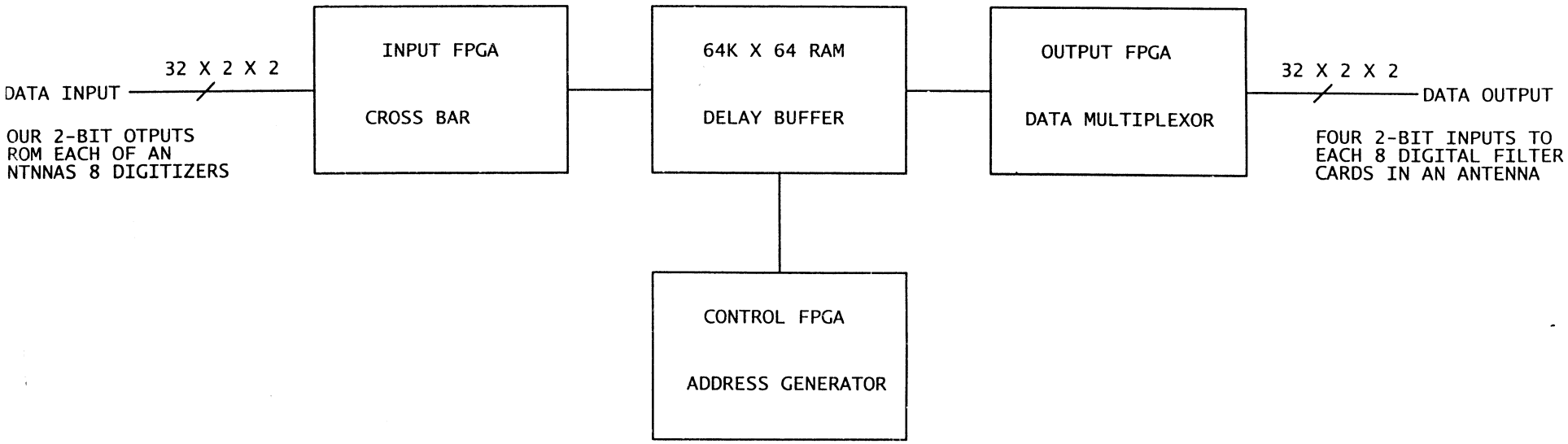
BIASED MULTIPLICATION TABLE
Add 9, then divide by 2

| P-INPUT / D-INPUT | 01 | 00 | 11 | 10 |
|---|---|---|---|---|
| 01 | 9 | 6 | 3 | 0 |
| 00 | 6 | 5 | 4 | 3 |
| 11 | 3 | 4 | 5 | 6 |
| 10 | 0 | 3 | 6 | 9 |

## STATION CARD BLOCK DIAGRAM (DATA PACKETIZER FUNCTION)




## STATION CARD BLOCK DIAGRAM (DELAY LINE/CROSS BAR FUNCTION)

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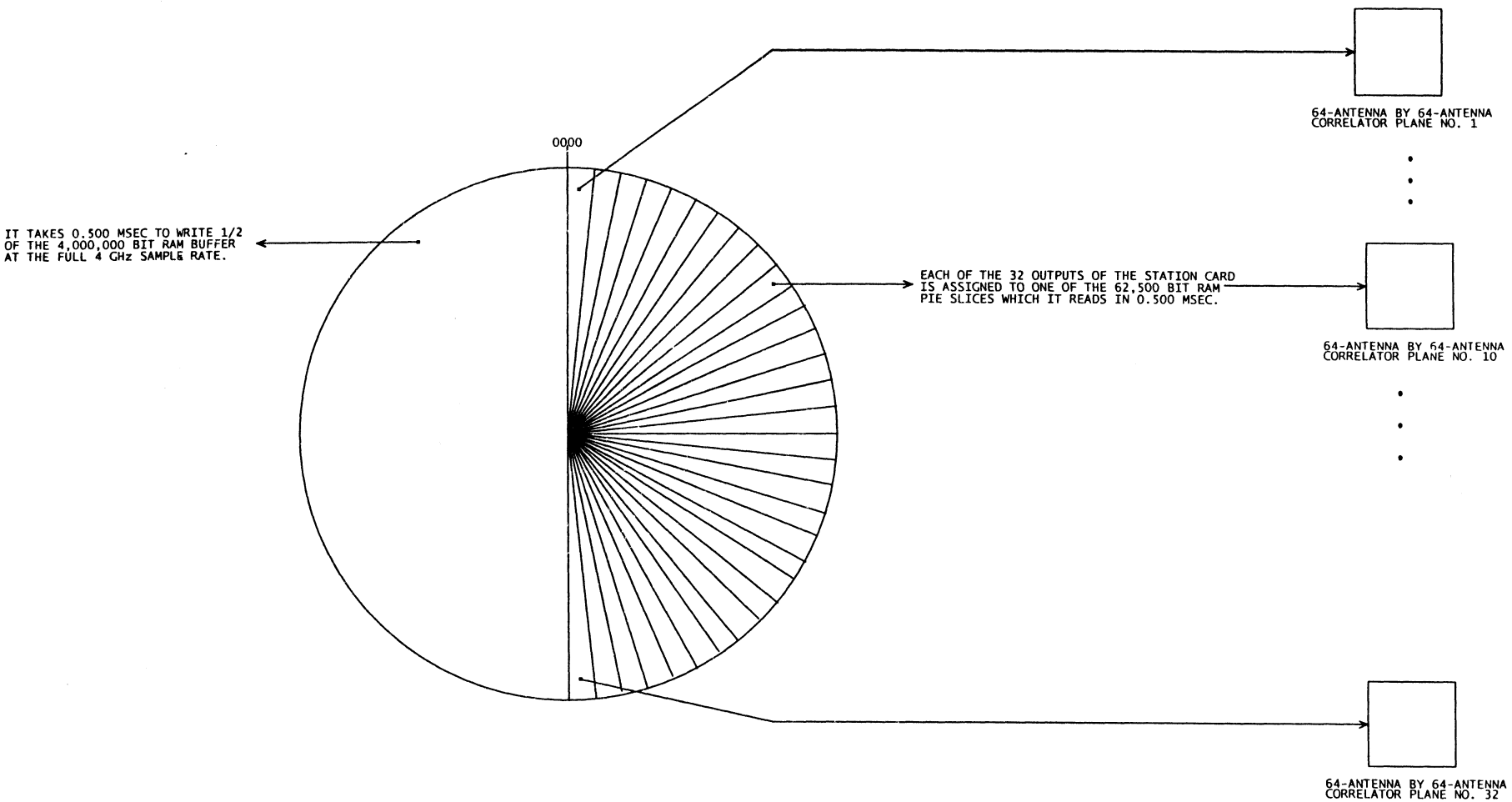
# STATION CARD MEMORY MAP

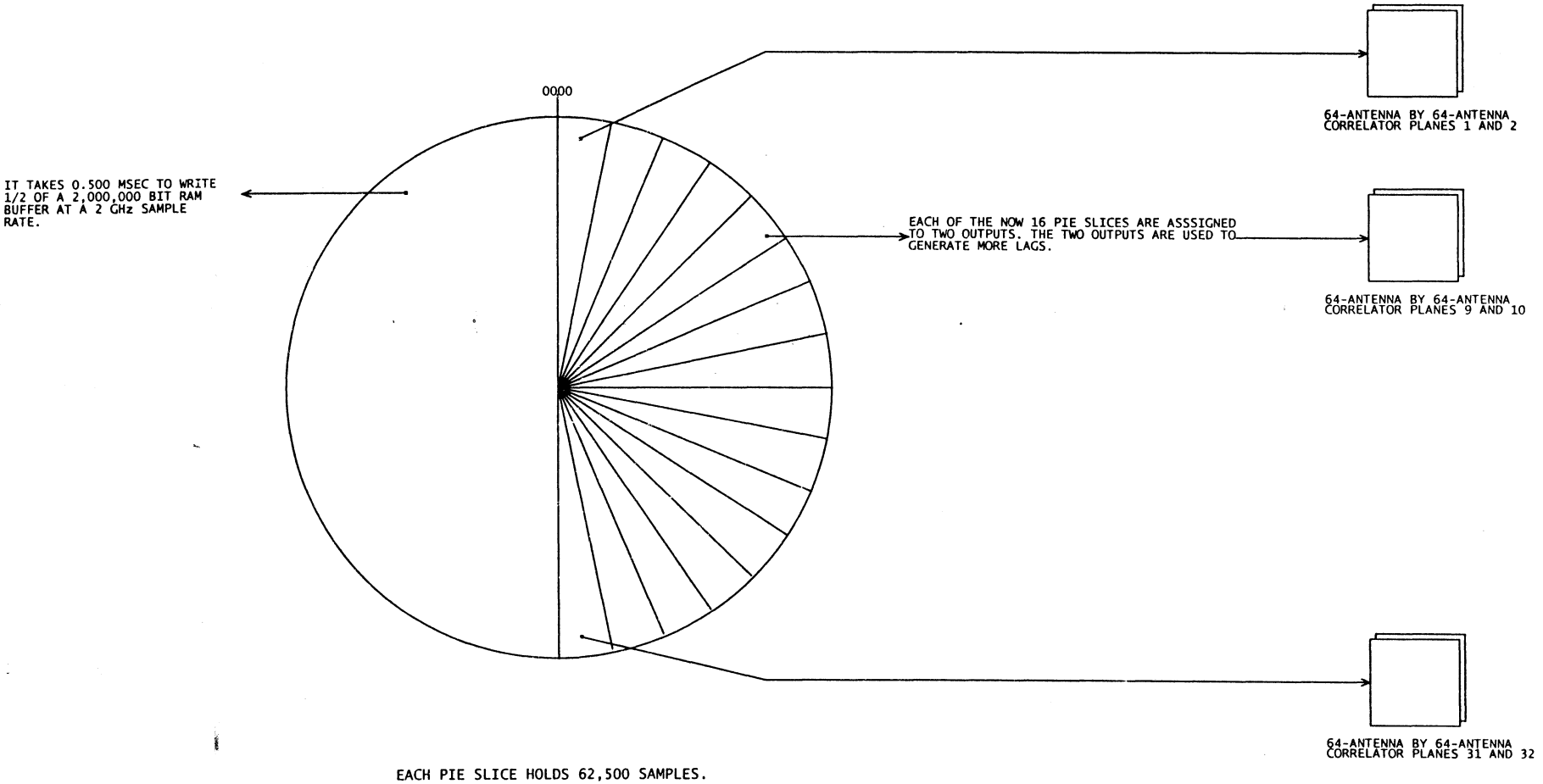
THE RAM BUFFER MAY BE THOUGHT OF AS A LARGE CIRCULAR BUFFER. ON THE INPUT SIDE, SAMPLES ARE WRITTEN INTO IT AT THE FULL 4 GHz SAMPLE RATE. ON THE OUTPUT SIDE, THE BUFFER IS DIVIDED INTO 32 "PIE SLICES" AND EACH OF THE 32 CARD OUTPUTS ARE ASSIGNED THE SAMPLES IN ONE OF THE PIE SLICES.




EACH PIE SLICE HOLDS 62,500 SAMPLES.

# STATION CARD MEMORY MAP

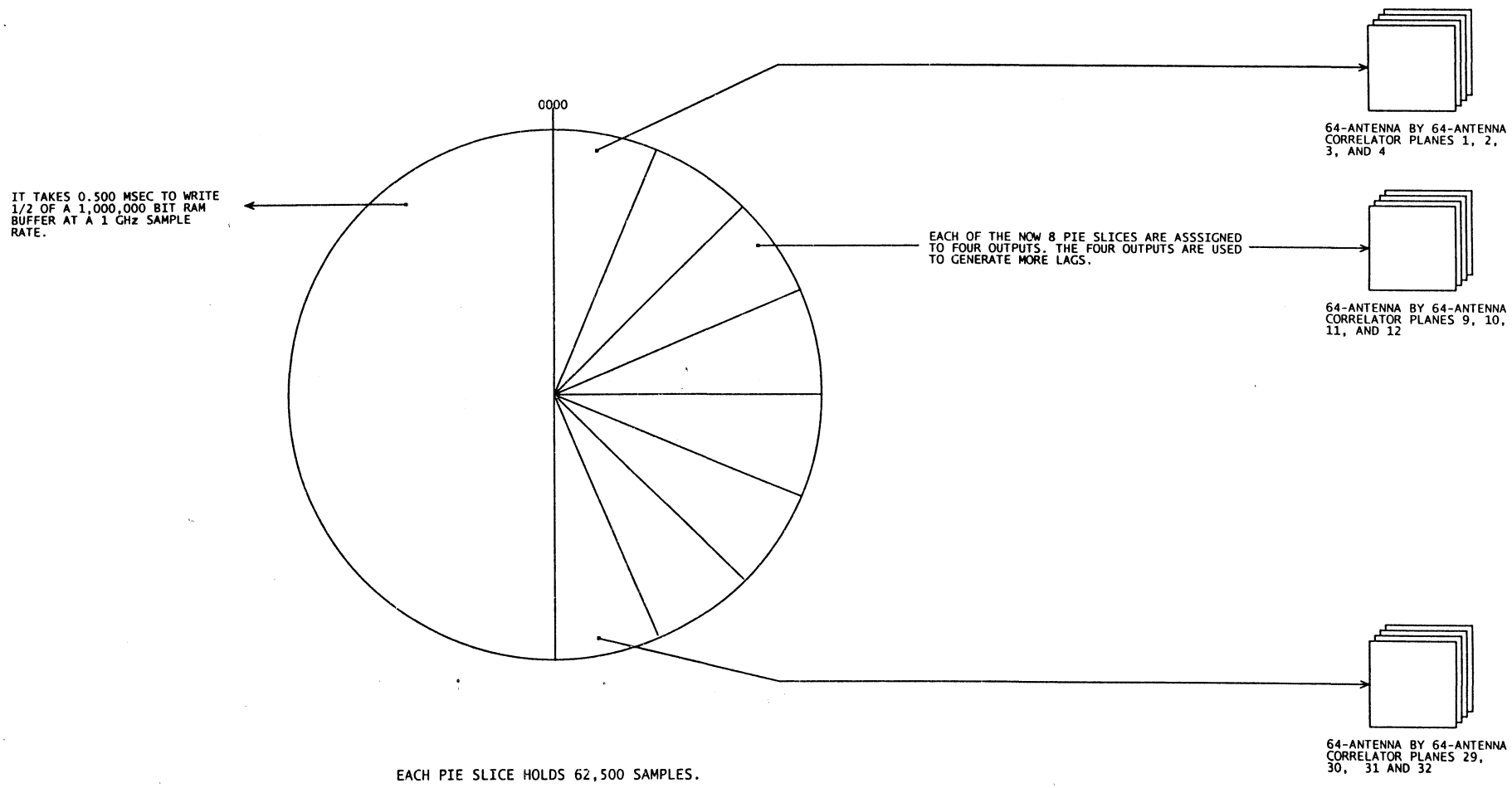
2 GHz SAMPLE RATE




EACH PIE SLICE HOLDS 62,500 SAMPLES.

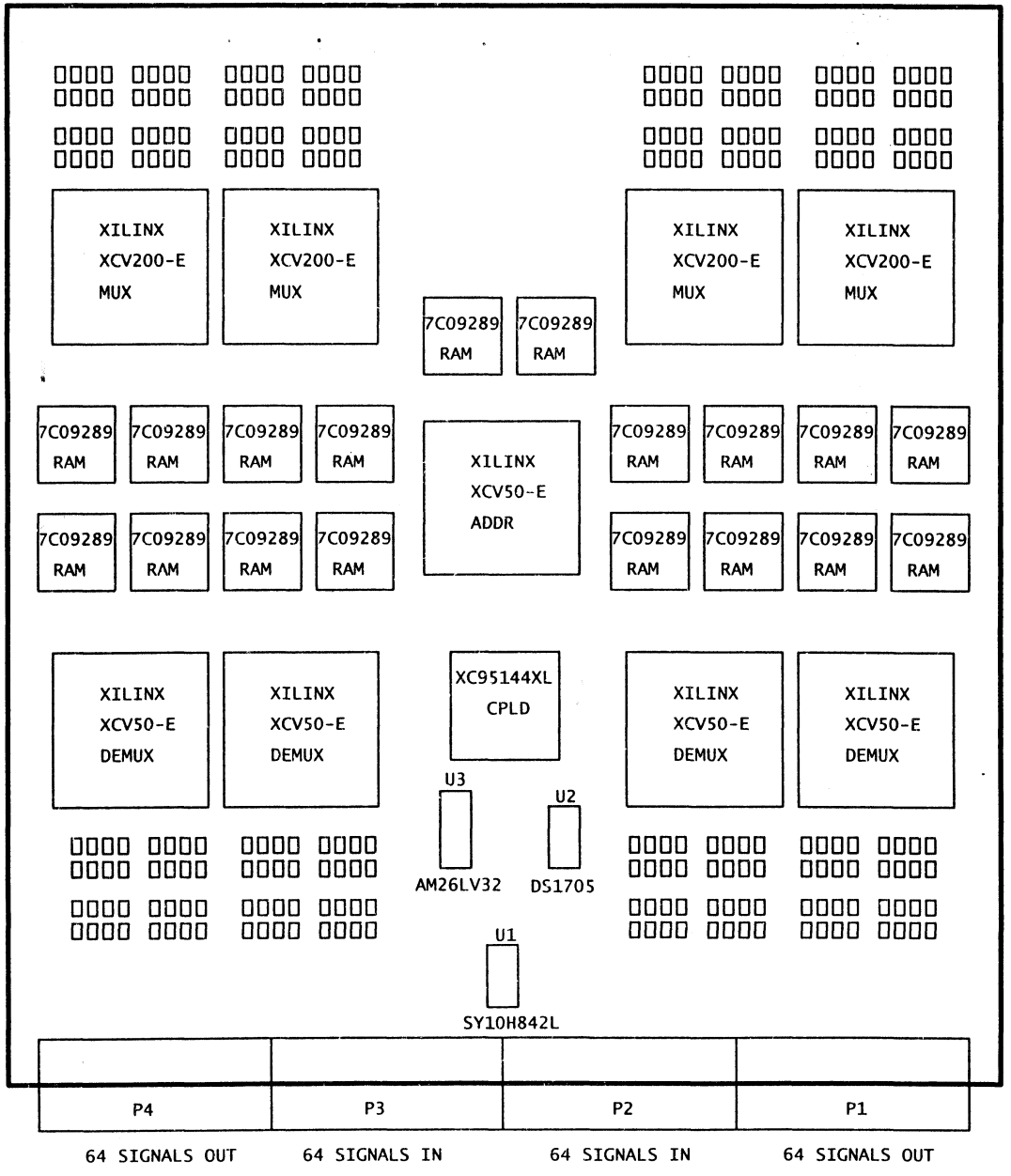
# STATION CARD MEMORY MAP

1 GHz SAMPLE RATE




EACH PIE SLICE HOLDS 62,500 SAMPLES.

# STATION CARD



# The ALMA Correlator Long Term Accumulator

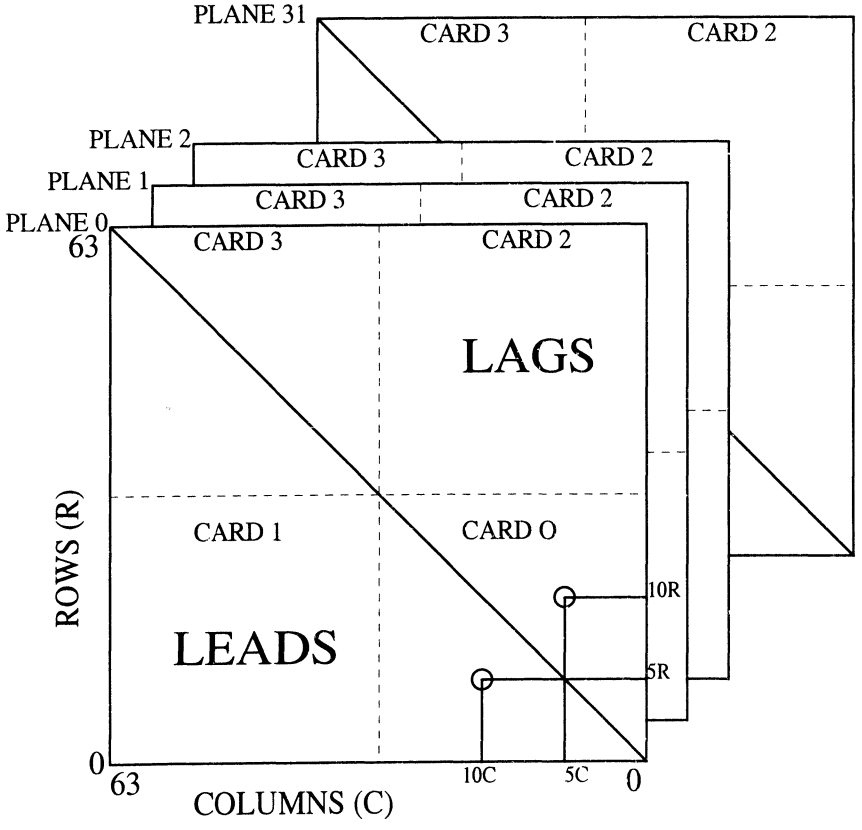
**Basic Requirement #1**

**LTA DESIGN CAPABLE OF HANDLING EITHER THE 4K OR 8K LAG CHIP**

## Provide accumulation for every correlator result:

ONE CORRELATOR ARRAY SHOWN

(128 CORRELATOR CARDS)




- ☐ 32 x 32 = 1024 INTERSECTIONS PER CORRELATOR CARD
- ☐ 512 RESULTS AT EACH INTERSECTION (8K CHIP)
- ☐ 512K RESULTS PER CARD
- ☐ 512 CARDS TOTAL IN SYSTEM
- ☐ ***256 MEG RESULTS TOTAL***

**NOTE:**

1 ALMA CORRELATOR CARD > 1 VLBA CORRELATOR

(512 K RESULTS) (420 K RESULTS)

(ONE CARD) (ONE SYSTEM)



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# The ALMA Correlator Long Term Accumulator (LTA)

## Basic Requirement # 2

Provide an ADDER TREE and INTERFACE (to VME) :

- Add accumulated results from individual LTA planes together (as required)
- Provide a simple parallel interface (custom) from the adder tree outputs to a bin in the VME rack
- Convert from the custom parallel interface to an off the shelf interface into the VME system

# The ALMA Correlator Long Term Accumulator

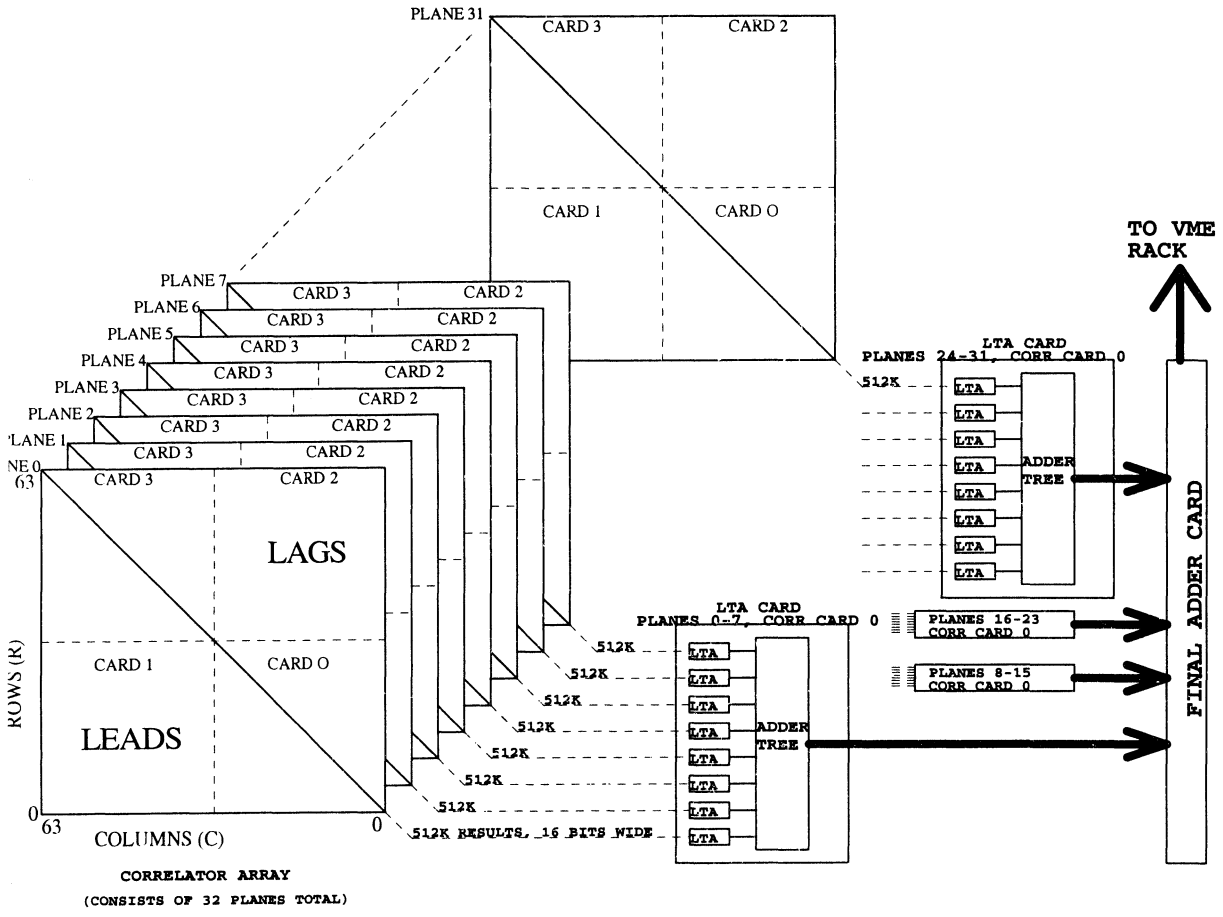
## ADDER TREE IMPLEMENTATION

FIRST STAGES ON LTA CARDS

FINAL ADDER CARD COMBINES FOUR LTA OUTPUTS

6 ADDER TREE MODES REQUIRED:

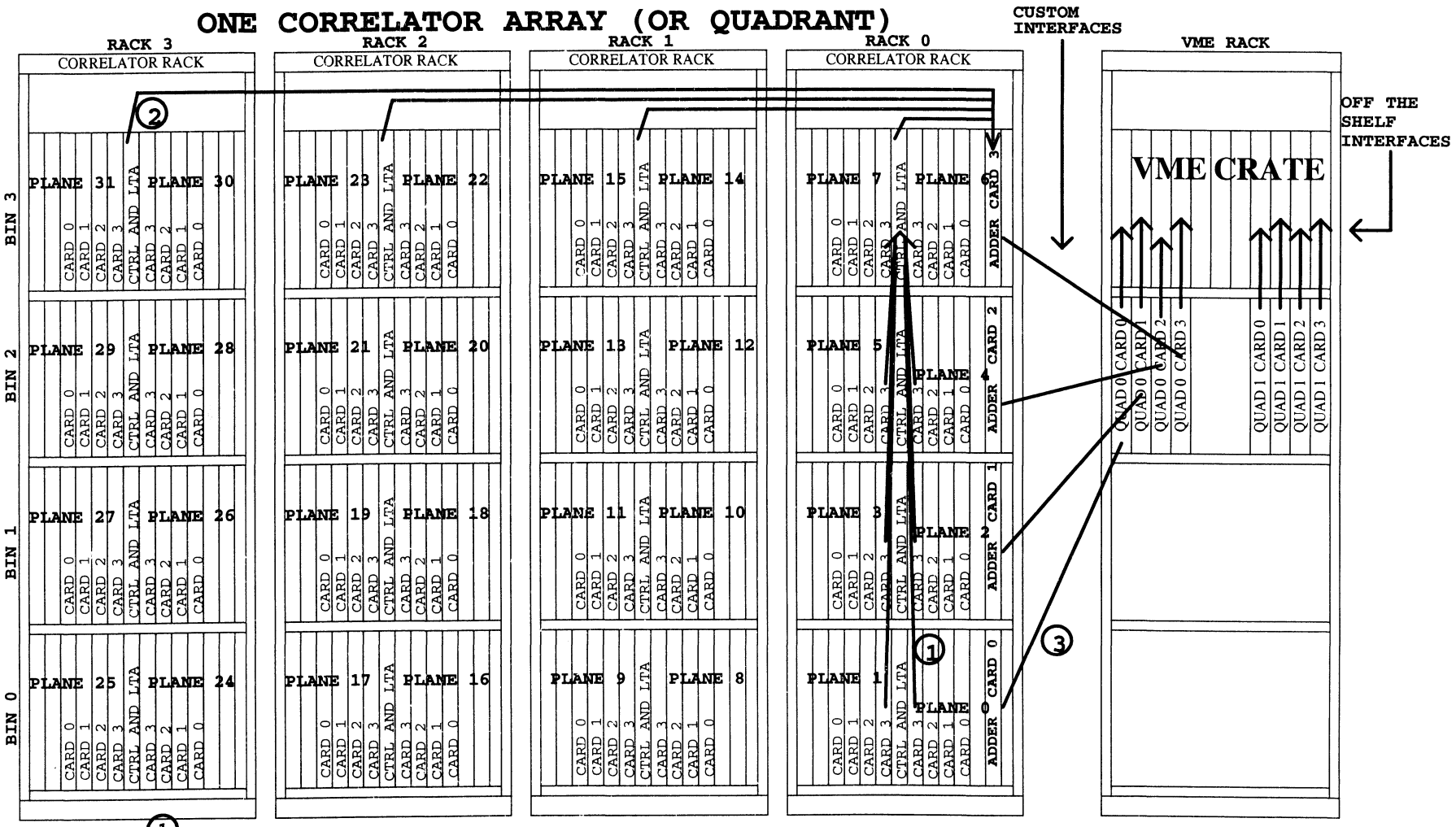
| ADDER TREE MODE | BW | NUMBER OF PLANES RQRD FOR 512 SPEC CHANS | TOTAL SPEC CHANS |
|---|---|---|---|
| 0 | 2 GHz | 32 PLANES | 512 |
| 1 | 1 GHz | 16 PLANES | 1024 |
| 2 | 500 MHz | 8 PLANES | 2048 |
| 3 | 250 MHz | 4 PLANES | 4096 |
| 4 | 125 MHz | 2 PLANES | 8192 |
| 5 | 62.5 MHz | 1 PLANE | 16384 |



# The ALMA Correlator Long Term Accumulator

## LTA System Overview

- One LTA card for each 8 correlator cards
  (512 correlator cards ---> 64 LTA cards)
- One FINAL ADDER card for each 4 LTA cards
  (64 LTA cards ----> 16 FINAL ADDER cards)
- One interface converter for each FINAL ADDER card (16 INTERFACE cards)




1 CORR TO LTA INTERFACE: 16 BITS MUXED OVER 8 BIT LVDS AT 125 MHz

2 LTA TO ADDER INTERFACE: 32 BITS MUXED OVER 16 BIT LVDS AT 125 MHz

3 ADDER TO VME INTERFACE: 32 BITS MUXED OVER 16 BIT LVDS AT 125 MHz

**The ALMA Correlator Long Term Accumulator (LTA)**

# Basic Specifications:

- Modes of operation (individual antenna basis)

  Auto Correlation Mode
  Only AUTO (self) products available

  Cross Correlation Mode
  All CROSS and AUTO products available

- Minimum accumulation time :

  16.0 msec for antennas in cross correlation mode

  1.0 msec for antennas in auto correlation mode

- Maximum accumulation time

  65 seconds for antennas in cross correlation mode
  (integer multiples of 16 msec: 65,536 1 msec intervals)
  (can support longer times if there is a need)

  8 msec for antennas in auto correlation mode
  (only 1, 2, 4 and 8 msec supported; for longer accumulation times, use cross correlation mode and only transfer auto products out of LTA)

## The ALMA Correlator Long Term Accumulator (LTA)

# Basic Specifications:

- Data Format

  LTA results are 32 bit unsigned integers (results from correlator cards are 16 bit unsigned integers)

- 2 GByte/sec total output data rate capacity

  Capable of transferring 512K 32 bit results every 16 msec on each of 16 output streams (128 MByte/sec per stream capacity)

  Corresponds to a full dump of all results in 2 GHz bandwidth mode (512 spectral channels produced)

- Independent control of correlation mode (cross or auto) and accumulation time for each of 64 antennas (in each quadrant)

- Start or stop accumulation (for each antenna) on 16 msec boundaries

- 16 bins provided for auto correlation mode results

  Allows VME system to transfer 1 msec results on 16 msec boundaries

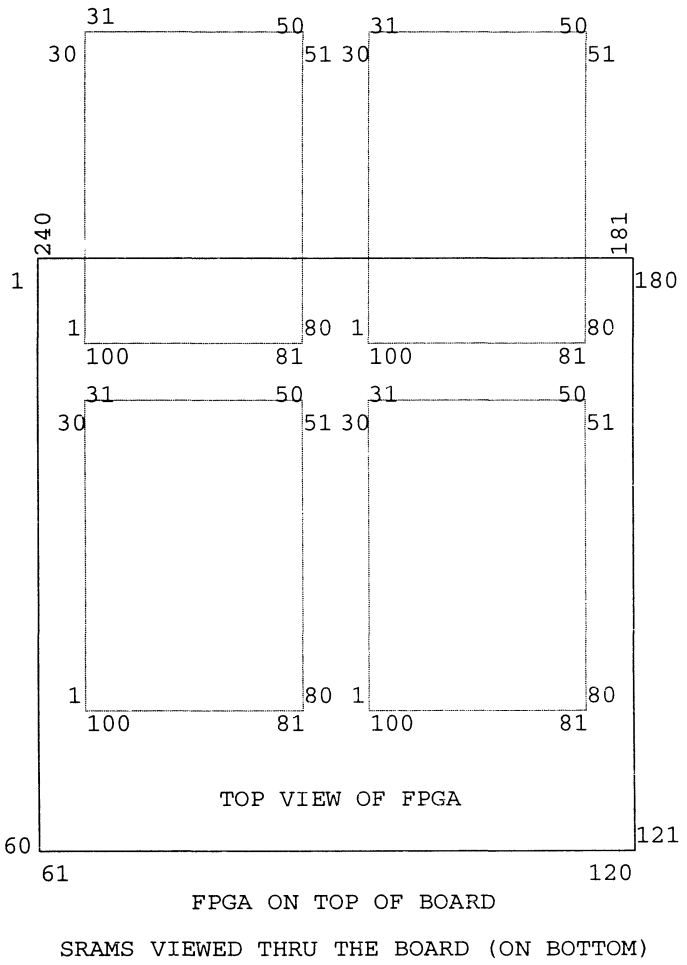
# The ALMA Correlator Long Term Accumulator (LTA)

Hardware Implementation

- Basic LTA Block

One FPGA chip, plus two or four SRAM chips

Handles the 512K results from a single correlator card:

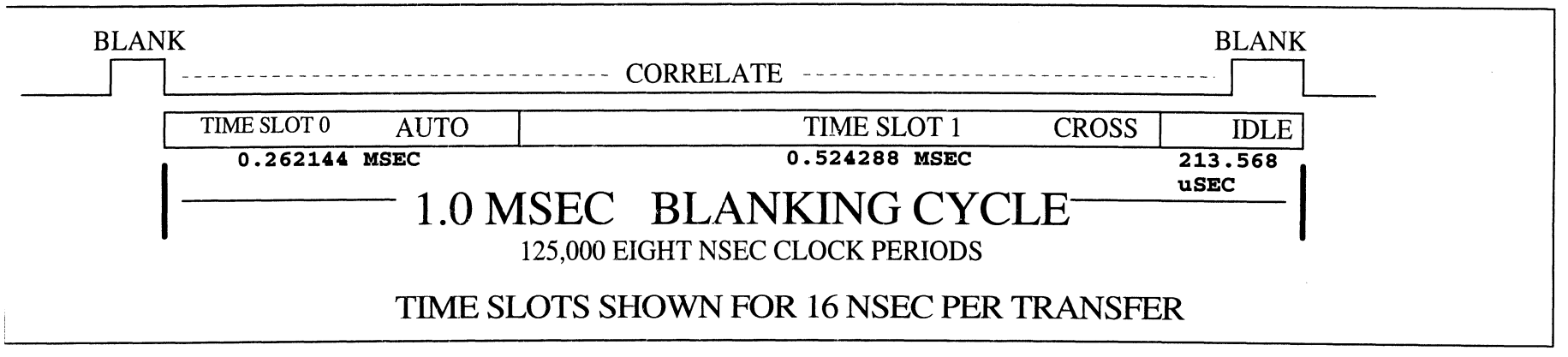



512K results, 4 bytes wide, double buffered = 32 MBits of ram
(Four 8 MBit SRAMs shown above)

The FPGA chip is approximately 1.5 inches square.

# The ALMA Correlator Long Term Accumulator

## Basic 1 msec cycle




**TIMESLOT 0:** 16,384 x 16 NSEC = 0.262144 MSEC

**TIMESLOT 1:** 32,768 x 16 NSEC = 0.524288 MSEC
(32,768 x 16 1 MSEC INTERVALS= 512K RESULTS TOTAL)

**TIMES SHOWN ARE THE MINIMUM POSSIBLE INTERVALS FOR EACH TIME SLOT; ACTUAL TIMESLOTS COULD BE LONGER DUE TO OVERHEAD IN THE CORRELATOR CHIP SHIFT OUT PROCESS**

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# The ALMA Correlator Computer Interface

## Correlator Results (High Data Rate Interface)

- LVDS interfaces from correlator racks to VME rack(s)
  (capable of full 128 MByte/sec rate out of LTA/Adder Tree)

  Total of 16 interfaces in full system (2 GByte/sec capacity)

- Front Panel Data Port (FPDP) Interface into VME bin

  Basic FPDP specifications:

  - 32 bit parallel interface
  - 40 MHz transfers (160 MByte/sec)
  - Cable length up to 5 meters

  Plan to limit cable length to 2 meters

  Plan to limit transfer rate to 25 MHz (100 MByte/sec max)
  (capacity of one result every 40 nsec, throttle back as required)

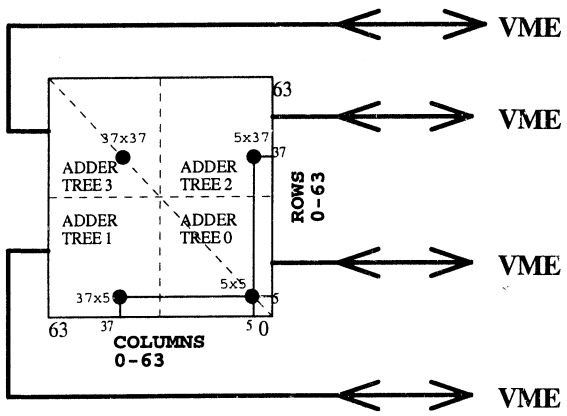
  Present plans suggest 80 nsec / result max utilization
  (50 MByte/sec)

Reasons for selecting FPDP:

- Ubiquitous
- Relatively simple
- 160 MByte/sec matches planned 128 MByte/sec output capacity of each stream

# THE ALMA CORRELATOR COMPUTER INTERFACE

(CORRELATOR RESULTS)




| ROW | | | | | | COLUMN | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | 0 | 5 | 4 | 3 | 2 | 1 | 0 |
| CARD MSB | | | | | | CARD LSB | | | | | |

**REQUEST PROTOCOL FOR EACH INTERFACE**

| BITS 15-10 | BITS 9-5 | BITS 4-0 |
|---|---|---|
| MASK NR (0-62) | ROW NR (0-31) | COLUMN NR (0-31) |

ONE OF 63 MASKS THAT SPECIFY WHICH PLANES ARE TO BE ADDED TOGETHER

- HOW MANY FPDP REQUIRED PER QUADRANT?

  MINIMUM:

  FOUR BI-DIRECTIONAL FPDP INTERFACES

  COULD CONSIDER:

  4 VME TO CORR FOR REQUESTS
  4 CORR TO VME FOR RESULTS

  OR

  4 VME TO CORR FOR REQUESTS
  8 CORR TO VME FOR RESULTS

- REQUEST PROTOCOL SUGGESTION:

  MAXIMUM REQUEST LIST IS 1024 REQUESTS (for 16 msec)

  2 BYTES PER REQUEST = 2048 BYTES IN 16 MSEC

  = 128 KBYTE/SEC

  MAY USE 5 Mbit/sec SYNCHRONOUS SERIAL INTERFACE INTERNALLY TO DISTRIBUTE THE REQUEST LIST TO THE LTA CARDS

# The ALMA Correlator Computer Interface

## Correlator Control (Low Data Rate Interface)

- Infineon (Siemens) C167 embedded processors

  All embedded code written in C (our goal anyway)

- CAN bus

  2000-6000 transactions per second (8 bytes each = 16-48 KByte/sec)
  64 Nodes max per bus

- Flash storage of FPGA images, C167 code etc.

  Large data blocks downloaded during "maintenance" time blocks

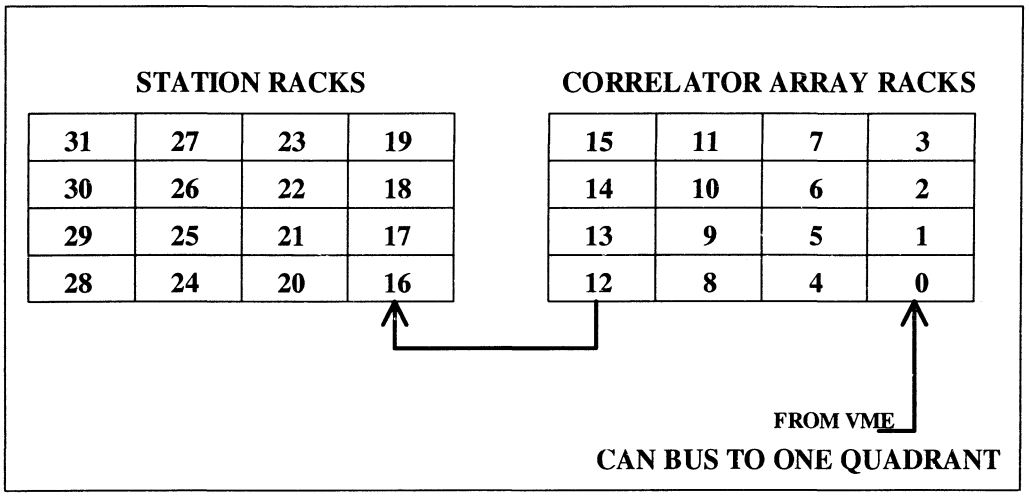
- No FPGA image changes as a function of mode

  This is the goal for at least all "normal" modes

- Local generation of mode based program words

# The ALMA Correlator Computer Interface

## Correlator Control (Low Data Rate Interface)




- LTA / Correlator Control Card "example"

| Parameter | | Corr | LTA |
|---|---|---|---|
| Correlation mode: | CROSS or AUTO | X | X |
| Accumulation time: | number of 1 msec multiples | | X |
| Over sample mode: | over sampled or not | X | |
| Polarization mode: | V, H, V+H or Full | X | |

All 16 cards require identical copies of the above parameters for each of 64 antennas -------- > CAN Broadcast mode?

Assume one CAN 8 byte transaction per antenna for the above parameters:

64 of the 2000 per second would then be required to totally re-configure the cards, if broadcast mode is viable, (1024 if not)

1-20-00

## SECOND ROUND OF BIDS

| Bidder | Design $ | Proto $ | Design $ + Proto $ | Part $ | Size sq mm |
|---|---|---|---|---|---|
| IMEC .18u 4K | $ 104,778 | $ 418,000 | $ 522,778 | $ 20 | 40 |
| IMEC .18u 8K | $ 104,778 | $ 418,000 | $ 522,778 | $ 38 | 75 |
| IMEC .25u 4K | $ 104,778 | $ 216,700 | $ 321,478 | $ 30 | 80 |
| Innotech .25u 4K | $ 108,300 | $ 178,000 | $ 286,300 | $ 45 | 121 |
| Innotech .18u 4K | $ 108,300 | $ 450,000 | $ 558,300 | $ 30 | 60 |
| Xentec | $ 148,000 | $ 237,000 | $ 385,000 | $ 29 | 108 |
| White Eagle | $ 476,000 | $ 432,750 | $ 908,750 | $ 70 | |
| Silicon Group | $ 550,000 | $ 393,525 | $ 943,525 | $ 48 | |
| Deep Submicron | $ 937,317 | $ 454,216 | $ 1,391,533 | $ 69 | 40 |
| Wyle/LSI/AI | $ 1,210,000 | $ 64,000 | $ 1,274,000 | $ 125 | 201 |

Unless otherwise indicated bids are for .25u 4K

## PROCESS OPTIONS FOR ALMA CORRELATOR ASIC

(based on conservative die size estimates)

| | 3lm 0.25um | 5lm 0.25um: | 4LM 0.18um: | 6LM 0.18um: | 3LM 0.35um: |
|---|---|---|---|---|---|
| Total NRE: | $177,600 | $222,000 | $421,800 | $510,600 | $103,600 |
| Total unit cost | $45.13 | $42.05 | $33.76 | $29.69 | $40.48 |
| number of units 39322 X die cost | $1,774,736.55 | $1,653,430.22 | $1,327,624.88 | $1,167,508.86 | $1,591,885.63 |
| total NRE + unit costs | $1,952,336.55 | $1,875,430.22 | $1,749,424.88 | $1,678,108.86 | $1,695,485.63 |
| Normalized to 0.25 3LM pricing | 100% | 96% | 100% | 107% | 112% |
| Total NRE at cost+20%: | $144,000 | $180,000 | $342,000 | $414,000 | $84,000 |