4-4-00

LTA Review

Half-msec buffering : non-contiguous / card, so
max. resolution <u>even</u> is 1msec - even for pulsars

Add custom → FPDP to Project Book

Operational scenario samples

Pulsar modes? (1) Analog sum
(2) Blanking + binning - implies only 1 sub-array
Don't have a pulsar gate in the chip — OK w/ only 1 sub-array
Will have an NCO on each correlator FPGA - OK for slow pulsars